A Dead -Time Compensation Circuit for Voltage Source Inverters

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***Abstract*—** Dead-time, which is required to prevent short circuit of the dc bus voltage of a voltage source inverter, causes distortion in the output voltage of the inverter. In this paper, the effects of dead-time are discussed, and a dead-time compensation circuit is proposed. The compensation circuit modifies the width of gate pulses based on the direction of load current. The circuit is described in detail, and is validated on a single-phase voltage source inverter. Experimental results, demonstrating both the effect of dead-time and also its compensation, are presented.

***Index Terms*—** Dead-time, dead-time compensation, pulse width modulation (PWM), voltage source inverter (VSI)

I. INTRODUCTION

NOWADAYS PWM inverters are widely used in applications such as motor drives, uninterruptible power supplies (UPS) and active power filters. The non-ideal nature of the switching devices in the inverter demands a short delay to be introduced between the gating signals of the top and bottom devices in an inverter leg to prevent the short circuit of DC link. This is called *dead time*. During dead-time, both the transistors (active devices) in an inverter leg are in off condition. Either the top diode or bottom diode conducts, depending on the direction of load current. Hence there could be an error in the output voltage depending on the direction of load current, as will be discussed in section II. Though the error in voltage is only for a short duration, the effects of this could be considerable when carrier frequency is high. Dead-time results in a change in fundamental voltage, and also causes low frequency distortion as will be seen in section II.

Consequently, in motor drives, there could be pulsating torque due to the low frequency distortion. Further, the steady torque itself could be different if there is a significant change in the fundamental voltage due to the dead-time. In active filters or harmonic compensators, the amplitude of lower-order harmonic voltages/currents could be significantly different owing to dead-time.

Dead-time effects have been studied and certain compensation methods have been proposed [1]-[5]. The compensation methods fall into two categories, namely compensation based on averaging theory [1] and compensation based on pulse by pulse correction [2]. The former method considers the averaged effect of dead-time [1]. The latter method increase or decrease the width of every pulse, as required, to compensate for the effect of dead-time [2]. The compensation circuit proposed in this paper is based on the latter method.

The compensation principle is discussed in section III. In section IV, the compensation circuit is described in detail. Test setup and experimental results are presented in sections V and VI, respectively. The conclusions are given in section VII.

II. DEAD TIME EFFECT

Fig.1 shows one leg of a voltage source inverter. Here the two devices are switched complementarily. The load current is I_A. Load current leaving the pole or mid-point of the inverter leg, (as shown in Fig.1) is considered positive, while current entering into the pole is considered negative. The output voltage V_{AO} is the voltage at the pole (mid-point) A, measured with respect to the dc bus mid-point O. The inverter is switched using unipolar sine-triangle PWM [6]. The modulating signals of the two leg are equal in amplitude and are phase-shifted by 180°. These are compared against a common triangular carrier. This paper considers different carrier frequencies to demonstrate the effect of dead time and its compensation.

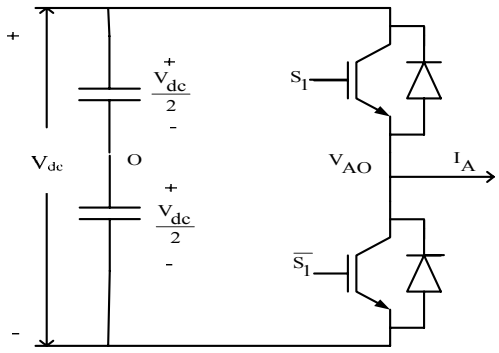


Fig.1. One leg of a voltage source inverter.

Fig.2 shows the timing diagram of a voltage source inverter to analyze the effect of dead time for positive direction of load current. Here S and $\bar{S}$ are the ideal gate signals to be applied to the top and bottom devices over a carrier cycle. The rising edges of the both signals S and $\bar{S}$ are delayed by the required dead-time T_d. These gating signals with the dead-time incorporated are indicated as S_1 and $\overline{S_1}$, respectively. The output voltage during dead-time is decided by the direction (polarity) of load current. For positive load current, the bottom diode of the inverter leg conducts, and hence the output voltage is negative. The output voltages corresponding to the ideal gate signals and signals with dead-time are shown by dotted and solid lines, respectively. As seen from Fig.2, there

is a negative error in the output voltage during the dead-time whenever signal S has a rising edge. This is indicated by the hatched area in Fig.2. The hatched area or the error volt-second is given by (1). On the other hand, there is no error whenever the signal S has a falling edge.

$$\Delta A = V_{dc} * T_d \qquad (1)$$

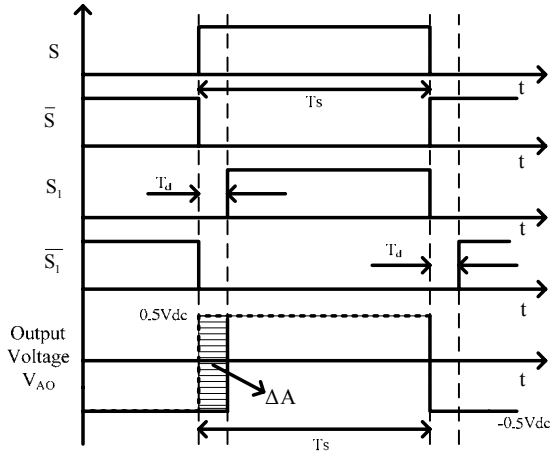


Fig.2. Timing diagram of voltage source inverter to analyze the dead time effect for positive load current.

Similarly, Fig.3 shows the effect of dead time on the output pole voltage for the negative direction of load current. As seen from Fig.3, there is a positive error in the output voltage during the dead-time whenever signal S has a falling edge. This is indicated by the hatched area in the Fig.3. The hatched area or the error volt-second is same as in (1), but the polarity is different now. However there is no error when the signal S has a rising edge.

Fig.4. Illustrates the relationship between the load current and the error voltage. The error voltage V_ε is defined as the difference between the actual pole voltage (with dead-time) to the ideal pole voltage (without dead-time). The error voltage pulses are of width T_d. The pulses are positive if the load current is negative, and vice versa, as shown in Fig.4. Though the error voltage pulses are narrow, their effect could be considerable if the carrier frequency is higher as mentioned in section I. The number of pulses depends on the switching frequency and the fundamental frequency. The pulse number (n_p) is given by the expression.

$$\mathrm{n_p} = \frac{f_c}{f} \qquad (2)$$

Where f_c is the carrier frequency and f is the fundamental frequency.

The error voltage can be averaged over every carrier cycle. The averaged error voltage is a square wave of height 'h' as shown in Fig.4 (b). Since the carrier frequency is much higher than the fundamental frequency, it is reasonable to assume that the square wave contains the fundamental and lower harmonic components of the error voltage. The height 'h' of the square

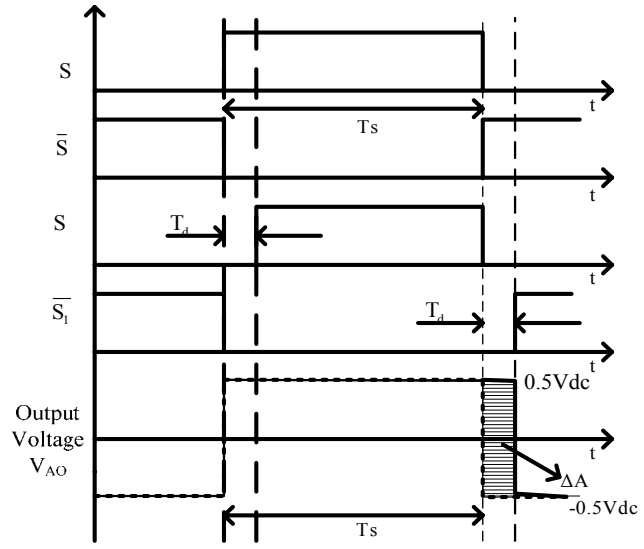


Fig.3.Timing diagram of voltage source inverter to analyze the dead time effect for negative load current.

is given by (3).

$$h = \frac{n_p}{2}(\mathrm{T_d} * V_{dc})(\frac{1}{2f}) = f_c * \mathrm{T_d} * Vdc \qquad (3)$$

The amplitude of kth harmonic of the square wave is given by (4).

$$V_k = 4\ h/\pi k = 4f_c * \mathrm{T_d} * \frac{V_{dc}}{\pi k} \qquad k = 1,3,5 \ldots\ldots \qquad (4)$$

Let $\mathrm{V_a}$ be the fundamental component of the ideal output voltage. The fundamental component $V_{\varepsilon 1}$ of the error voltage is in phase opposition with load current. The fundamental component $\mathrm{V_{a1}}$ of the actual output is now given by the phasor sum of $\mathrm{V_a}$ and $V_{\varepsilon 1}$ as shown in Fig.5. As seen from (4), V_k is proportional to the product of f_c and $\mathrm{T_d}$. If this product is high, the effect of dead-time is significant.

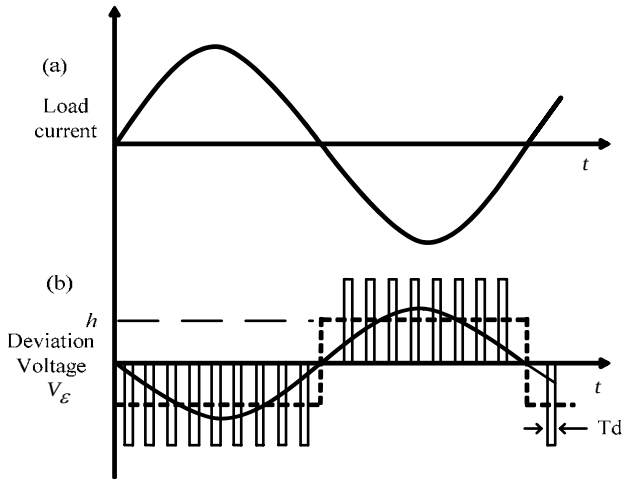


Fig.4. (a) Load current and (b) error voltage due to dead-time.

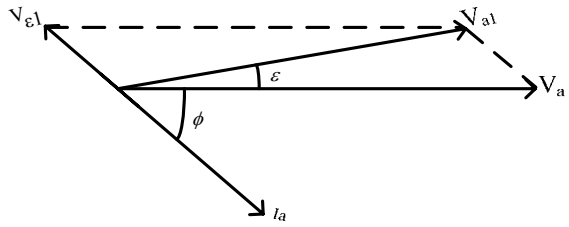


Fig.5. Effect of dead time on fundamental voltage.

III. COMPENSATION PRINCIPLE

The compensation principle here is based on the pulse by pulse correction of the gate signal as mentioned in section I. When the load current is positive, the width of the output voltage reduces by the dead-time duration T_d as brought out in Fig.2. Now, the effect of dead time could be compensated for, if this pulse width could be increased by T_d. Fig.5 illustrates how this can be done. The signals S, $\bar{S}$, and $\overline{S_1}$ in Fig.2 are reproduced in Fig.5. Delaying the falling edge of S_1 by T_d and the rising edge of $\overline{S_1}$ by T_d results in S_{1c} and $\overline{S_{1c}}$, respectively. If the signals S_{1c} and $\overline{S_{1c}}$ are used to switch top and bottom devices, then the width of output voltage will be equal to its ideal width. Now, compared to the ideal case, the actual pole voltage has the same average value, but is only delayed in time by T_d.

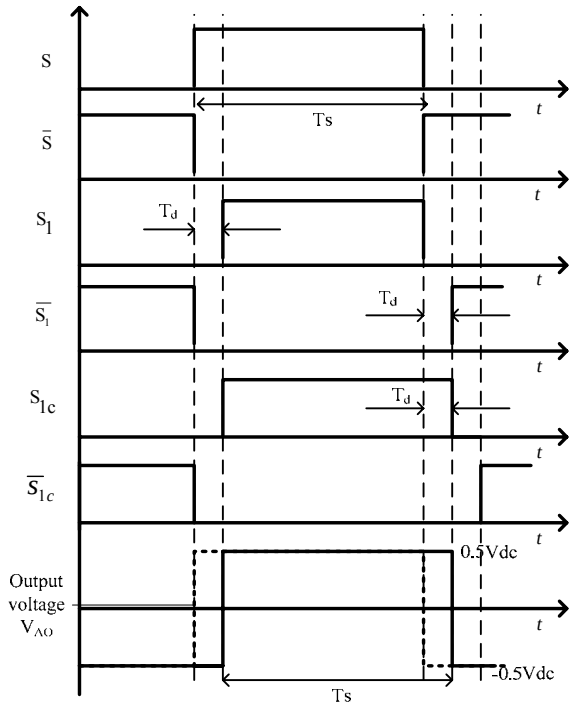


Fig.5. Dead time compensation for positive direction of load current.

Similarly, if the load current is negative, then the width of the output voltage increases by T_d as shown by Fig.3. This can be compensated for by decreasing this width by T_d. This is achieved by delaying the rising edge of S_1 and the falling edge of $\overline{S_1}$ by T_d to obtain S_{1c} and $\overline{S_{1c}}$, respectively, as illustrate in Fig.6. Such compensation assumes that the average value of the output voltage equals the average of the ideal output voltage. Once again, the output voltage is simply delayed in time by T_d

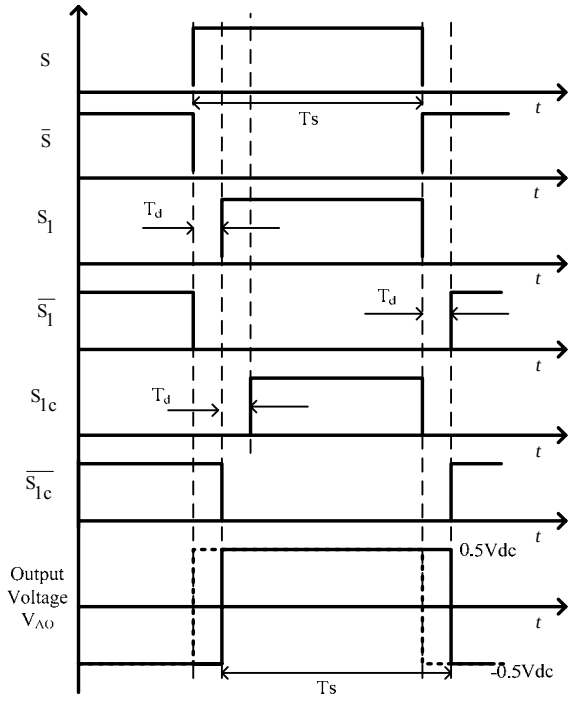


Fig.6. Dead time compensation for negative direction of load current.

IV. COMPENSATION CIRCUIT

Based on the discussion in the previous section, to compensate for the effect of dead-time, the falling edge of S_1 and the rising edge of $\overline{S_1}$ need to be delayed by T_d if the load current is positive. Similarly, the rising edge of S_1 and the falling edge of $\overline{S_1}$ delayed by T_d for negative load current. This is done by the compensation circuit shown in Fig.7. The signals S_1 and $\overline{S_1}$ and the load current are inputs to the circuit. The polarity of the load current is determined by the comparator circuit. Depending on the polarity of current, the edges of S_1 and $\overline{S_1}$ are delayed by T_d as mentioned earlier.

The gating signal S_1 and $\overline{S_1}$ are fed to a NOR gate, the output of which is ANDed with polarity of load current. The result is ORed with the S_1. This signal and its compliment are passed through identical delay circuits, whose delay is equal to the dead-time T_d, to obtain the gating signal S_{1c} and $\overline{S_{1c}}$. These signals are used to drive the top and bottom devices in the inverter leg.

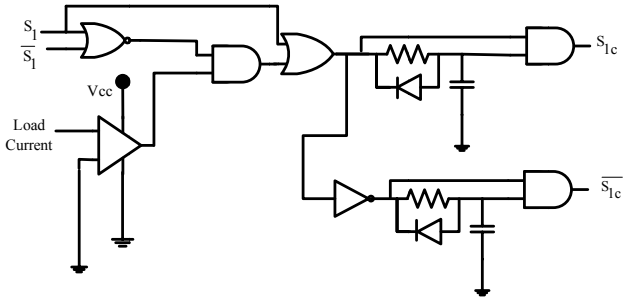


Fig.7. Proposed Dead-time compensation circuit.

V. TEST SETUP

The proposed dead-time compensation circuit is incorporated into a single-phase H-bridge inverter, shown in Fig.8. The MOSFETs used are IRFP250N. Unipolar sinusoidal pulse width modulation method is adopted with a switching frequency of 15kHz or 25kHz. The sinusoidal pulse width modulation signals are generated using analog circuits.

The inverter is loaded with R-L load of resistance 33Ωand inductance 40 H. The dc bus voltage is 60V, the modulation index is 0.8, and the frequency of modulation is 50Hz.

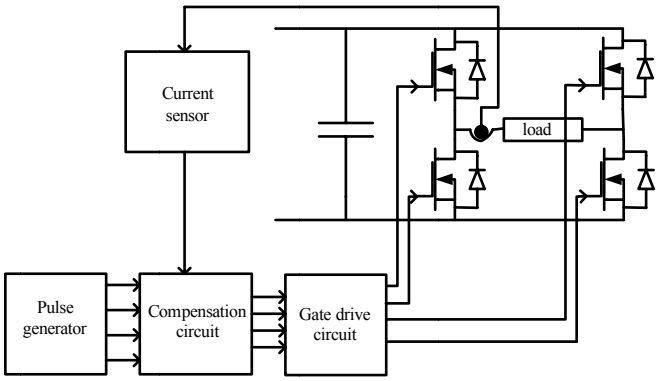


Fig.8 Block diagram of test setup.

VI. EXPERIMENTAL RESULTS

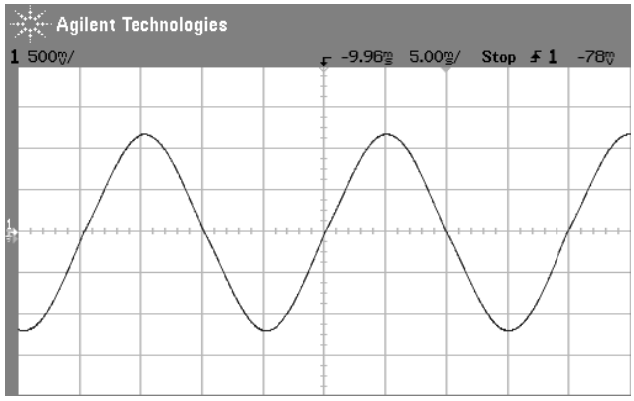
The effect of dead-time and its compensation by the proposed circuit are studied experimentally in this section. The study considers different values of dead-time, namely 1.5µs, 5µs and 10µs. A dead-time of 1.5µs is what is actually used in the inverter. The two higher values of T_d are chosen to experimentally validate the effect of dead-time, studied theoretically in section II. Also, carrier frequencies of 15kHz and 25kHz are considered as mentioned earlier.

As discussed earlier, the effect of dead-time depends on the ratio defined in (5), where is period of carrier wave.

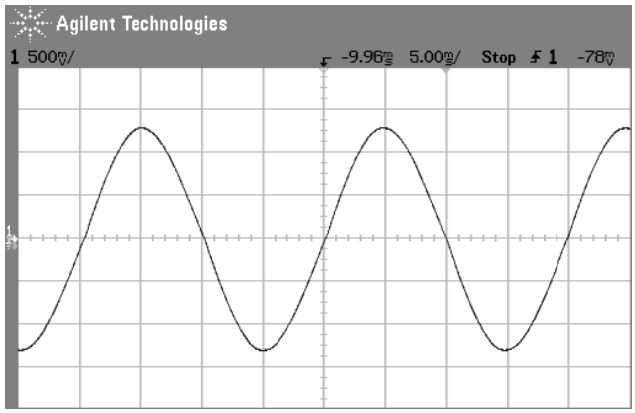
— (5)

Fig.9 to Fig.14 present the measured load current waveforms for progressively increasing values of *k* . The part (a) of each of these figures shows the load current without dead-time compensation, while the part (b) shows the improved current waveform with dead-time compensation.

For the dc bus voltage, modulation index and load conditions specified in section V, the peak value of the load current is estimated to be 1.36A, ignoring device drops and the effect of dead-time.



(a)

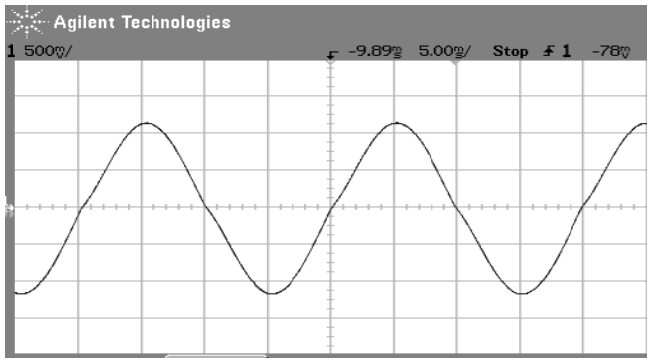


(b)

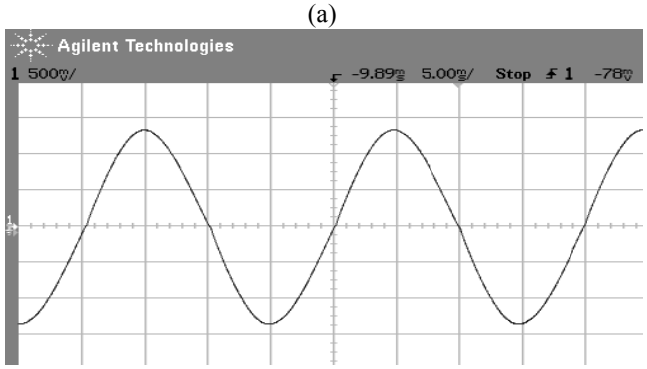
Fig.9. Load current for =1.5µs, =66.67µs (i.e. =0.0225), (a) without dead time compensation and (b) with dead time compensation (scale Y-axis 0.5A/div, X- axis 5ms/div).

Fig.9 presents the load currents for =0.0225 (i.e. =1.5µs, =66.67µs), without and with dead-time compensation, From Fig.9a we observe that, without compensation, the amplitude of the load current is less than the expected value. With compensation, there is an improvement in the load current amplitude as brought out by Fig.9b.

From Fig.10a, Fig.11a, Fig.12a, Fig.13a and Fig.14a we can observe the reduction in amplitude and increase in distortion of the load current with increase in the value of *k*. Fig.10b and Fig.11b, shows the load current for *k* =0.0375 and 0.075. Here the dead-time effect is completely eliminated. For , while the amplitude of current increases and the distortion reduces significantly due to dead-time compensation, the dead-time effect is not totally eliminated, as seen from Fig.12 to Fig.14. Further, for high values of *k*, dead-time compensation results in pulse dropping close to the peak of modulation of signal and distortion, as seen from Fig.12b,Fig.13b and Fig.14b.

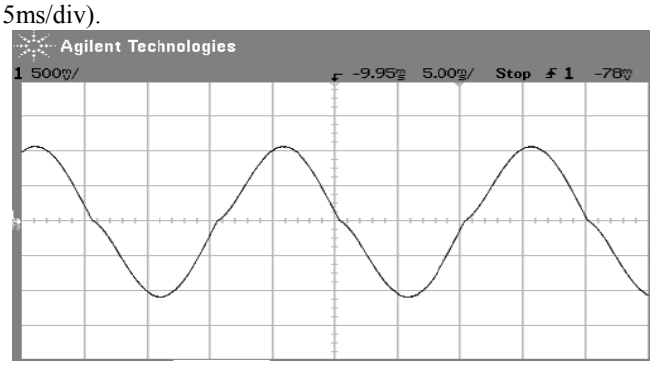


(a)

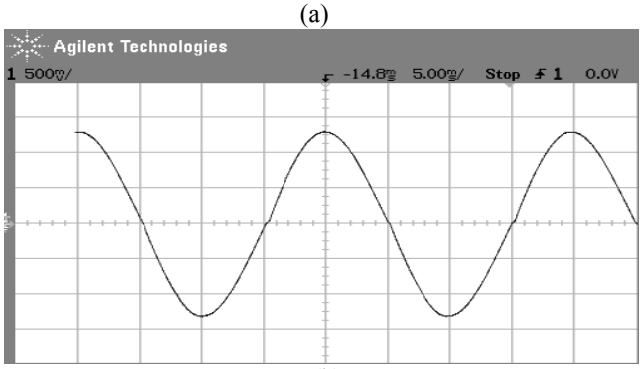


(b)

Fig.10. Load current for =1.5µs, =40µs (i.e. =0.0375),(a) without dead time compensation (b)with dead time compensation (scale Y-axis 0.5A/div, X-axis 5ms/div).

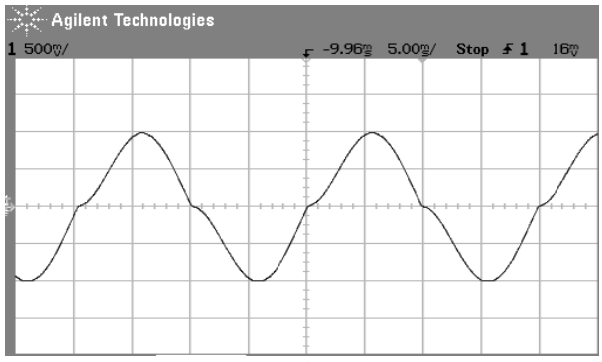


(a)

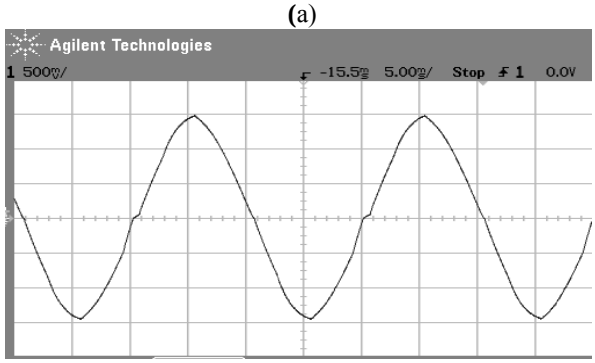


(b)

Fig.11. Load current for =5µs, =66.67µs (i.e. =0.075),(a) without dead time compensation (b)with dead time compensation (scale Y-axis 0.5A/div, X-axis 5ms/div).

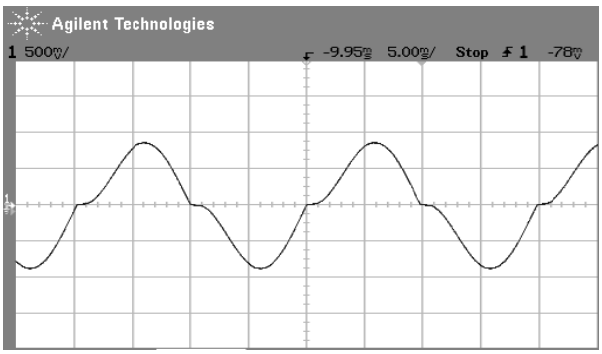


(a)

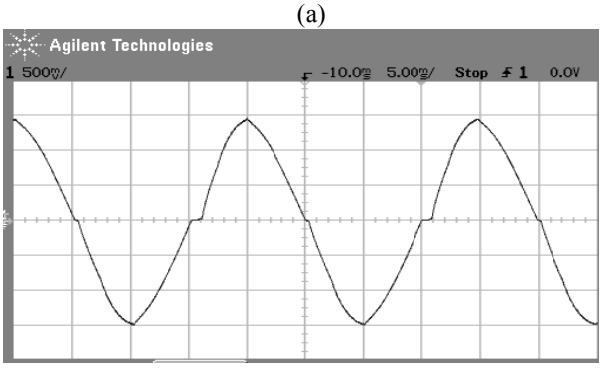


(b)

Fig.12.Load current for =5µs, =40µs (i.e. =0.125), (a) without dead time compensation (b)with dead time compensation (scale Y-axis 0.5A/div, X-axis 5ms/div).

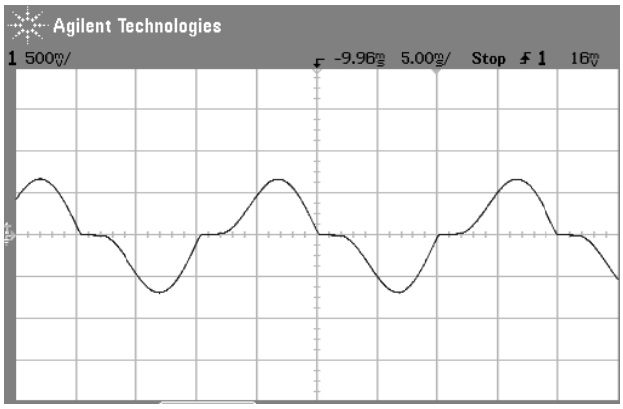


(a)

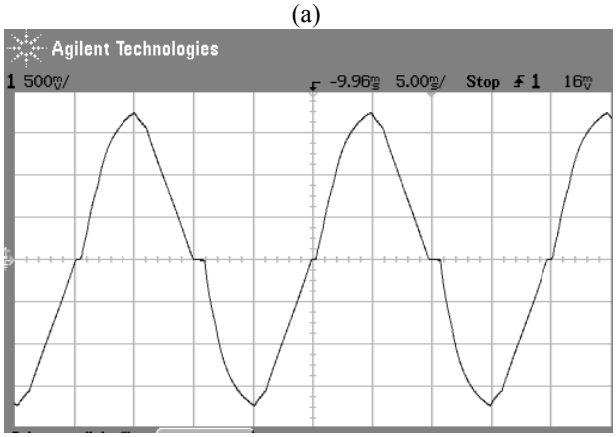


(b)

Fig.13. Load current for =10µs, =66.67µs (i.e. =0.15),(a) without dead time compensation and (b)with dead time compensation (scale Y-axis 0.5A/div, X-axis 5ms/div).



(a)



(b)

Fig.14. Load current for =10µs, =40µs (i.e. =0.25),(a) without dead time compensation circuit (b)with dead time compensation circuit (scale Y-axis 0.5A/div, X-axis 5ms/div).

Thus, the compensation circuit is effective in compensating the effects of dead-time for $k < 0.1$, as will be the case in most practical inverters.

VII. Conclusion

A dead time compensation circuit is proposed to avoid the effects of dead-time in the voltage source inverter. It is experimentally verified on a single phase H-bridge inverter. The experimental results demonstrate the effectiveness of compensation for 1, where k is the ratio of dead-time to carrier period. For a typical dead-time of 1µs, this compensation circuit is effective upto a carrier frequency of 100 kHz. The compensation circuit presented is simple, and can be easily incorporated into the protection and dead-time circuit of any inverter.

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