HARDWARE DEAD TIME COMPENSATION FOR VSI BASED ELECTRICAL DRIVES

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ABSTRACT

A full hardware modulator board for space vector modulation which allows the dead time effects compensation is presented in this paper. It consists of a fully integrated digital set-up implemented on a programmable logic device. It is based on an adequate modification of the switching sequence generation on the base of the phase stator current signs and of the power modules status. In the paper, a detailed description of the modulator set-up will be provided together with some experimental results.

1. INTRODUCTION

Pulse width modulated voltage source inverter (VSI) for three phase loads are widely used for feeding induction motors. The control strategies adopted for such systems are commonly divided in two categories: in the former, a direct control on the load currents is performed, while, in the latter, the load currents are indirectly controlled by means of the average load voltage. This paper is focussed on the effects of the non-ideal power switching elements of the VSI controlled by means of PWM techniques [1]. As a matter of fact, between the modulation controller and the gates of the power modules, a "dead time" circuit has to be introduced in order to avoid the shoot-trough of the DC link. In this time interval, both power switches of a bridge leg are turned off. The following effect is a load dependent magnitude and phase error in the output voltage. This implies a difference between the reference space vector of the feeding voltage, imposed by the control strategy, and the one actually imposed by the inverter to the motor. The phenomenon occurs when in a leg of the inverter the current is not flowing in the device which is turned off. By increasing the pulse frequencies, the switching dead time takes a remarkable part of the whole modulation period and, thus, it distorts the average load voltage more and more seriously. The main effects can be classified as follows:

- distorted amplitude of voltages and currents, as well as the mean value of the torque developed by the motor, which become all dependent on the dead time effect;
- low order voltage and current harmonics which causes torque ripple;
- deterioration of drive performances especially in open loop and direct torque control strategies.

Several solution are proposed in the literature [2]-[5] but most of them needs additional costs, due to the strong hardware and/or software requirements, which sometimes cannot be accepted, especially if an open-loop low cost system has to be designed.

In this paper, a low cost digital space vector modulator is proposed. It consists of a simple SVM modulator with an additional stage introduced just before the inverter power module gates dead time circuit. On the basis of the stator current signs and on the power modules status, this additional unit generates an additional blank time on the modulation signals which compensate the effect of the following dead time circuit. All the system is fully integrated inside a low cost programmable logic device.

2. PRINCIPLES OF THE COMPENSATION STRATEGY

The commonly used three-phase PWM inverter with an induction motor as load is shown in fig. 1. It allows for generating only seven space vectors of the output voltage. Space vector modulation consists in generating a switching sequence over a modulation period T_s, in such a way as to get a mean space vector **v** of the voltage feeding the motor just equal to the reference one **v***, generated by the adopted control strategy. In the most general case, the switching sequence to impose in a space vector modulation is:

$\mathbf{v}_i$	for the time	$\alpha_i T_s$
$\mathbf{v}_{i+1}$	for the time	$\alpha_j T_s$
$\mathbf{v}_0$	for the time	$\alpha_0 T_s$

with:

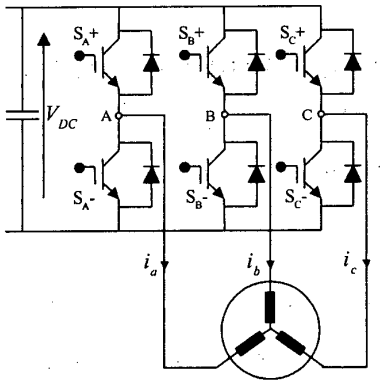

Fig.1 - Three phase voltage source inverter.

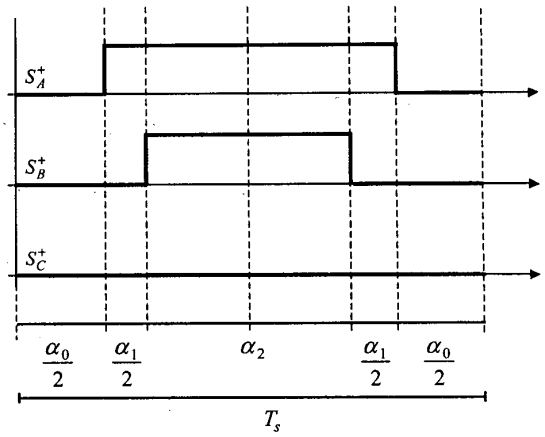

Fig. 2 - Symmetric Space Vector Modulation signals.

$$\alpha_i = \sqrt{3}\frac{|\mathbf{v}^*|}{V_{DC}}\sin\left(\frac{\pi}{3}-\beta\right)$$

$$\alpha_j = \sqrt{3}\frac{|\mathbf{v}^*|}{V_{DC}}\sin(\beta)$$

$$\alpha_0 = 1-\alpha_i-\alpha_j$$

and where $\mathbf{v}_i$ and $\mathbf{v}_{i+1}$ are the voltage space vectors adjacent in the complex plane to $\mathbf{v}^*$, β is the argument of $\mathbf{v}^*$ with respect to $\mathbf{v}_i$, V_{DC} is the DC bus voltage, and $\mathbf{v}_0$ the null vector. The mean voltage space vector resulting over a modulation period is:

$$\mathbf{v}^* = \alpha_i \mathbf{v}_i + \alpha_j \mathbf{v}_j \qquad (1)$$

Generally, as long as (1) is satisfied, for the resulting voltage space vector it makes no difference the order by which the different vectors $\mathbf{v}_i$ and $\mathbf{v}_{i+1}$ are combined. But, as regards the switching losses, harmonic distortion and dead time effect, the combination sequence can be very important [6]. In particular, the symmetric sequence has been chosen and adopted in this paper. It consists in generating a symmetric signal within the sampling period T_s for each switch of the inverter. In fig.2 the gate signal sequence is shown, for the three upper switches of the VSI, when the reference voltage space vector belongs to the first sector. The sequence is:

$\mathbf{v}_0 \Rightarrow \mathbf{v}_1 \Rightarrow \mathbf{v}_2 \Rightarrow \mathbf{v}_1 \Rightarrow \mathbf{v}_0$

for the times:

$$\frac{\alpha_0}{2}T_s \Rightarrow \frac{\alpha_1}{2}T_s \Rightarrow \alpha_2 T_s \Rightarrow \frac{\alpha_1}{2}T_s \Rightarrow \frac{\alpha_0}{2}T_s$$

In even sectors, the sequence ($\mathbf{v}_i$, $\mathbf{v}_{i+1}$) has to be swapped in order to keep the symmetry of the signals.

Unfortunately, switching devices do not have ideal behaviour. In particular, the turn-off operation is not instantaneous, and a finite time delay t_d, generally known as dead time, has to be imposed between the turn-off command of a switching device and the corresponding turn-on command of the other switching device in the same leg. If the current is not flowing in the device which is turned off, the space vector of the supply voltage does not change instantaneously, but with a time delay just equal to t_d. Thus, the effective switching sequence can result different from the imposed one. As example, in fig.3 the dead time effect is shown when the phase current sign in the first leg of the inverter is positive, that it when it flows from the inverter to the motor. In particular, it can be noticed that the dead time effect occurs on the rising edge of the signal. When $i_a < 0$, the dead time effect occurs on the falling edge of the signal. It has to underline that the blank time circuit always impose the delay on the switch-on end, but the actual effect on the output voltage depends on the stator current sign. Starting

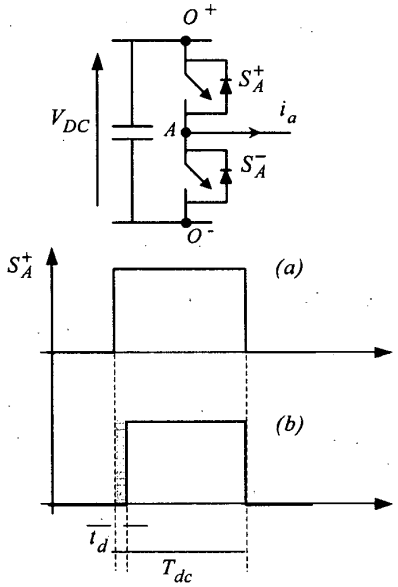

Fig.3 - Dead time effect on the modulation signals when $i_a > 0$: *(a)* original signals, *(b)* switch output voltages.

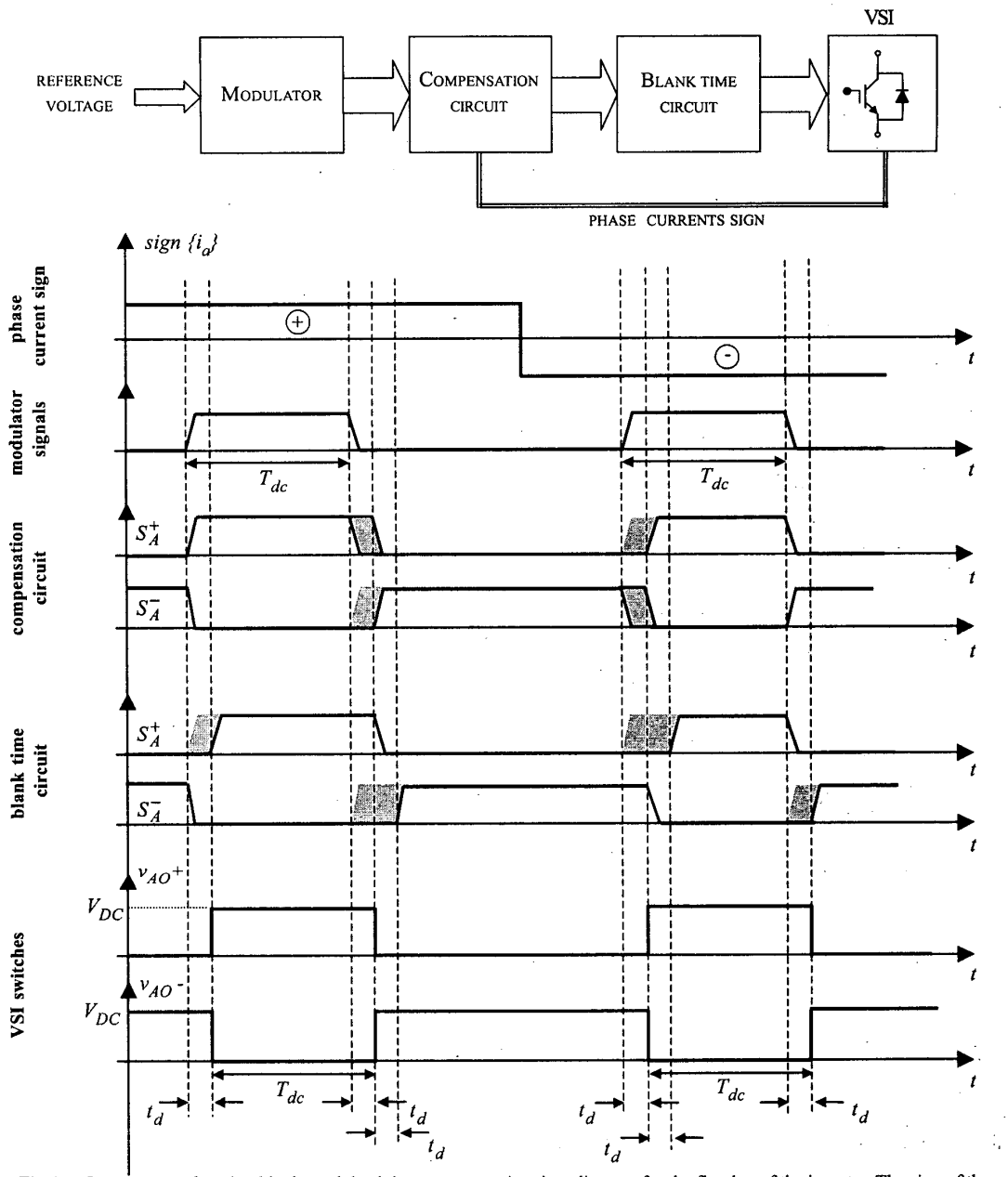

Fig 4 - Compensator function blocks and dead time compensation time diagram for the first leg of the inverter. The sign of the current is considered positive when it flows from the inverter to the motor.

from these considerations, an additional circuit can be inserted just after the switching sequence generation circuit. In fig. 4, the proposed modulator function blocks and the time diagram of all the signals are shown. Starting from the reference value of the voltage, the modulator unit generates a signal with a duty cycle time of T_{dc}. Following, the "*compensation circuit*" unit increases or decrease the signal of the time t_d, depending on the phase stator current sign, in such a way to compensate the blank time effect. In particular, if $i_a > 0$, the new duty cycle time will be $T_{dc} + t_d$, if $i_a < 0$, the new duty cycle time will be $T_{dc} - t_d$. The new signals are after processed from the "*blank time circuit*" unit which adds the dalay time t_d to the switch-on sides of the signals. The output signals are now sent to the driver circuits of the inverter power modules, which generate a voltage duty cycle equal to the original one T_{dc}.

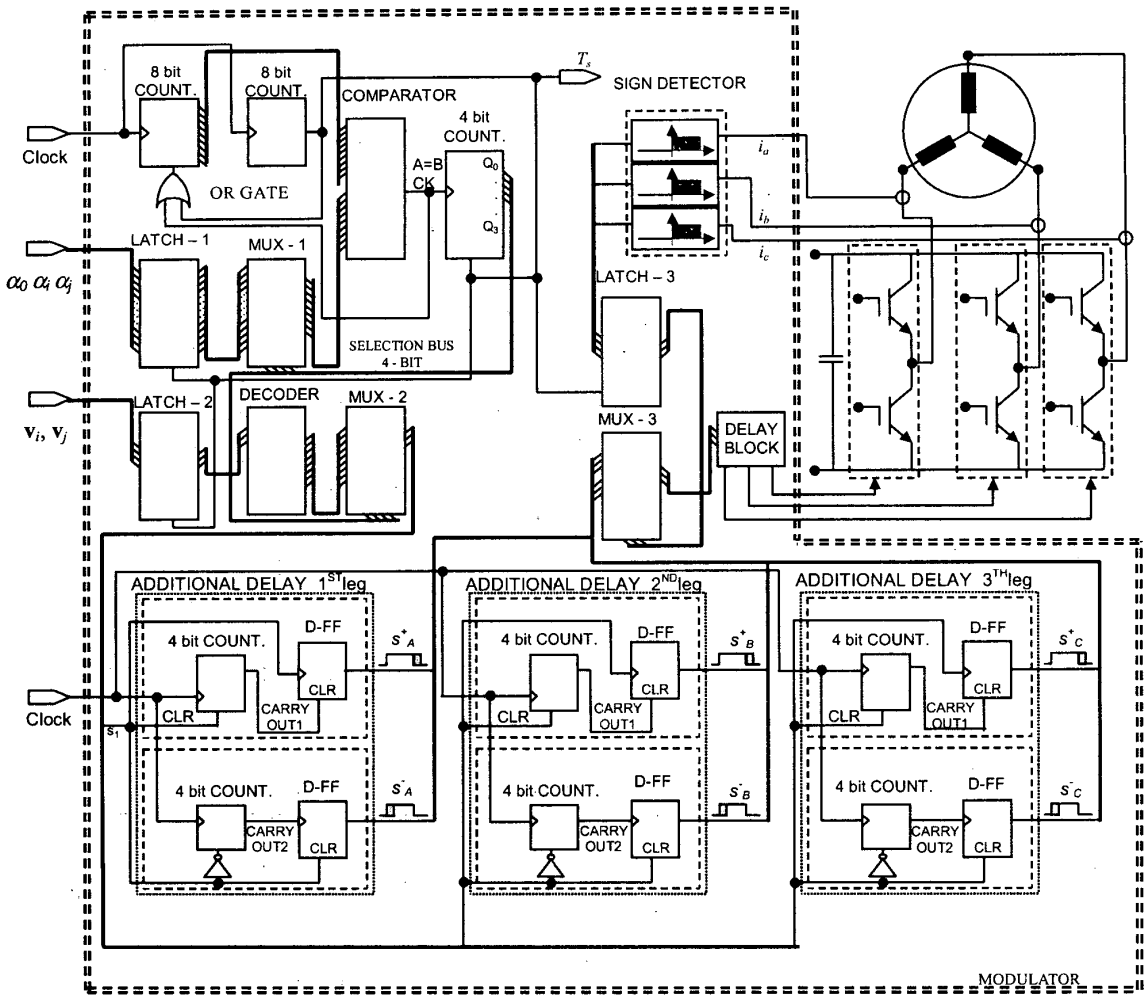

Fig 5 - Circuit of the space vector modulator with dead time compensation.

3. MODULATOR HARDWARE DESIGN

A version of the modulator suitable for voltage control of VSI, which accept as inputs the switching pattern referred to the voltage space vector to be imposed, is shown in fig. 5. A quartz oscillator and a programmable frequency divisor have been used as time base. Three 8-bit digital ports are used for the time delays α_i, α_j and α_o, while 3 bits are used for the voltage sector selection. An interrupt signal generator is also included to eventually synchronize an external control unit. The switching pattern signal temporisation is achieved by means of two 8-bit counters, a multiplexer and a comparator. After this stage, the compensation is performed by means of three circuits mounted at the modulator output which increase or decrease of a programmable number of clock pulses the original duty cycle width depending on the 3 bits of the current sign detector. All the circuit has been implemented by means of a programmable logic devices. In particular, a MAX7000® device by Altera has been used. It is an high-performance CMOS EPROM-based PLD built on multiple array matrix

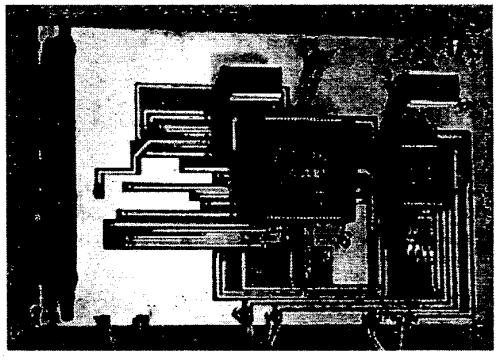

Fig. 6 - Prototype of the proposed SVM modulator.

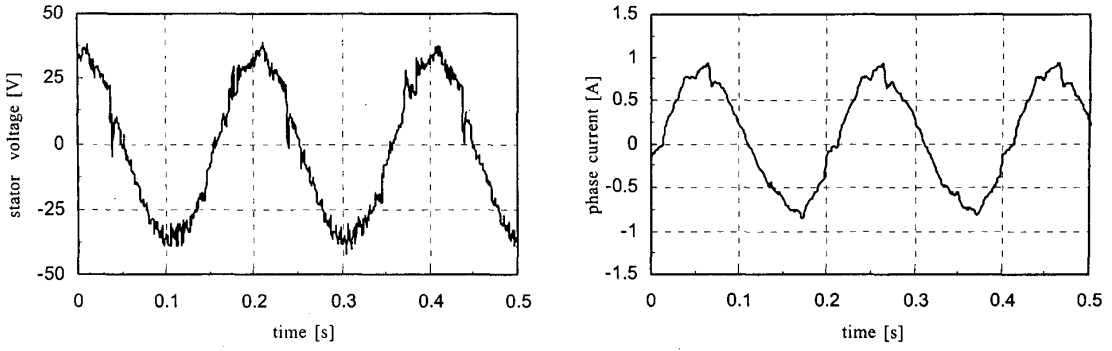

Fig.7 - Experimental results achieved by modulating with the proposed compensation system: stator voltage and phase current for the motor of tab. I when a 30 V, 5Hz voltage space vector is imposed as reference one.

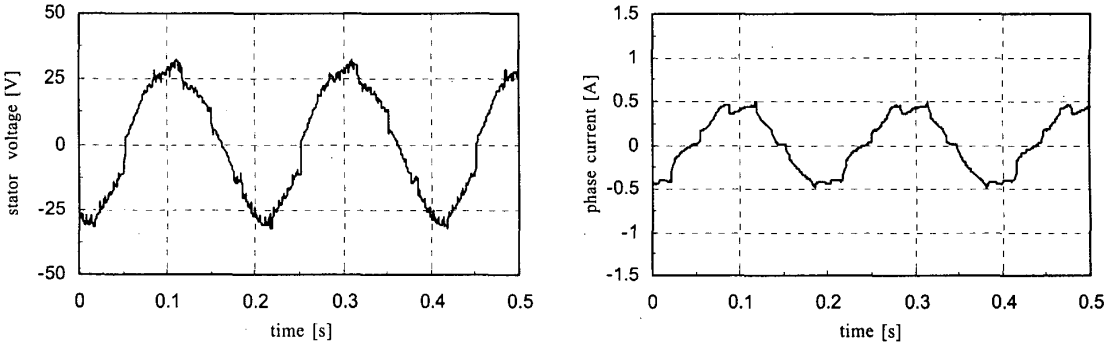

Fig.8 - Experimental results achieved by modulating without compensation: stator voltage and phase current for the motor of tab. I when a 30 V, 5Hz voltage space vector is imposed as reference one.

(MAX) architecture. The final circuit is shown in fig. 6.

4. EXPERIMENT RESULTS

The proposed hardware dead time compensator has been used as a part of a *V/f* ac drive with a 750W induction motor, whose parameters are shown in tab. I. Phase currents and voltages have been monitored by means of Hall-effect sensors. In particular, for what concerns the voltages, a low pass filter has been adopted in order to eliminate the modulation high order harmonics and to monitor only the low region of the voltage spectrum, which is the part more affected by dead time. The computation of the magnitude and the phase of the reference voltage has been performed by means of a DSP based digital system. A 32 bit I/O interface has been adopted to connect the control unit with the proposed modulator.

All the experiments have been focussed on the low speed region of the drive, where the space vector modulation is strongly influenced by the dead time distortion. The first test has been performed by setting the phase peak voltage to 30V and the frequency to 5Hz. The results concerning one phase voltage and current are shown in figs 7 and 8. It can be seen that a remarkable reduction of the drop voltage is achieved by compensating the switching signals with the proposed hardware modulator. In order to verify the limits of the adopted compensator, a lower frequency experiment has been performed. In particular, a peak voltage of 18V and a frequency of 3Hz have been imposed. The results, shown in figs 8 and 9, confirm that with the compensation almost all the drop voltage, which occurs without compensation, is eliminated. By decreasing more the voltage frequency and peak, the motor fed with no compensated modulation completely stops, while, with compensation, it keeps on running without the need of an additional boost voltage.

Table I - Parameters of the tested motor.

power rating	750	[W]	rated voltage	380	[V]
rated velocity	1395	[rpm]	pole pairs	2	
stator resistance	18.2	[Ω]	rotor resistance referred to stator	10.3	[Ω]
air gap inductance	689	[mH]	stator inductance	17.0	[mH]
rotor inductance referred to stator	11.4	[mH]	total inertia	0.0018	[kgm^2]

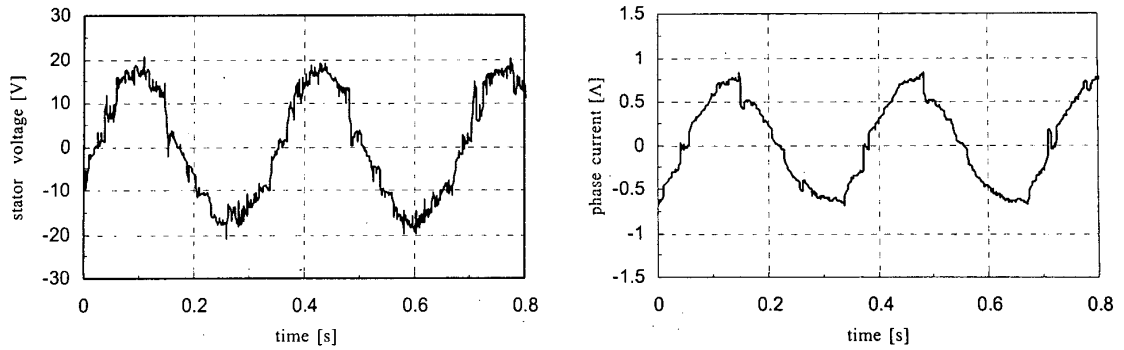

Fig.9 - Modulation with the proposed compensation system: stator voltage and phase current for the motor of tab. I when a 18 V, 3Hz voltage space vector is imposed as reference one.

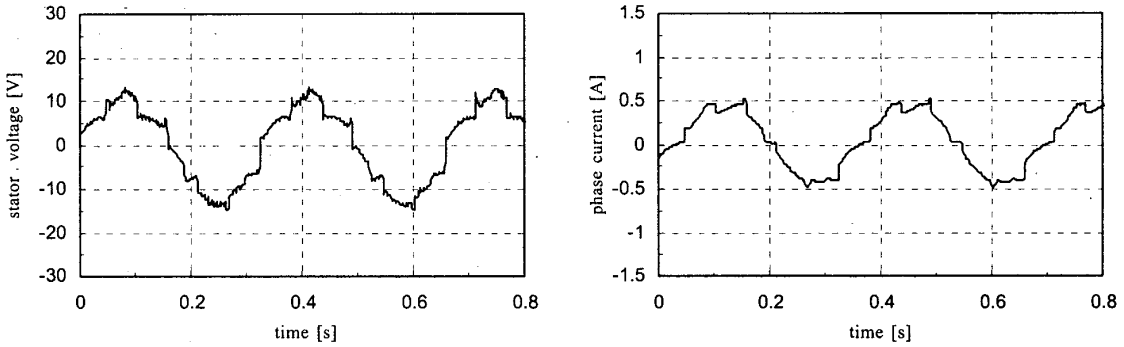

Fig.10 - Modulation without compensation: stator voltage and phase current for the motor of tab. I when a 18 V, 3Hz voltage space vector is imposed as reference one.

CONCLUSION

A simple full hardware architecture dead time compensator for voltage source inverter has been described in this paper. It consists on an additional modulation circuits which adds or remove the dead time amplitude from the modulation signals duty cycle, depending on the phase currents sign. A detailed description of the adopted layout and circuit has been also provided. The dead time compensator has been finally tested on a ac drive with an open loop *V/f* control, in such a way as to better remark the dead time effect on the voltage output waveforms. In particular, the low speed region has been investigated. All the results confirms that the proposed compensator drastically reduce the dead time voltage drop and considerably increases the overall drive performances.

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