# A New Approach of Dead-Time Compensation for PWM Voltage Inverters

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***Abstract*—It is essential to insert a switching delay time in sinusoidal pulsewidth modulation (PWM) voltage-fed inverters to prevent a short circuit in the dc link. This causes well known dead-time effect which is detrimental to the performance of the output voltages. Many compensation schemes were proposed to overcome the drawbacks. In this paper, based on a systematic approach, a new approach to *accurately* compensate the dead-time effect is presented. The system analysis and compensation synthesis are straightforward without averaging the output voltage deviation. The model of the PWM voltage inverter with time delay circuit leads us to a systematic approach of compensation. The simulation responses and experimental results show the validity of the analysis and verify the effectiveness of the proposed compensation method.**

***Index Terms*—Dead-time compensation, PWM voltage inverters, systematic approach.**

## I. Introduction

In RECENT years, the techniques developed for voltage-fed PWM inverters have gained wide attention in induction motor drives. The recently developed switching devices in the PWM inverter such as IGBT, MOSFET, and others have very fast switching frequency above tens of kilohertz. It is natural to insert a switching delay time to avoid the conduction overlap of the switching devices. This results in dead-time effect which causes serious output voltage distortions and torque pulsations. Remarkable efforts have been made to correct for dead-time errors [1]–[8].

In the literature, the relationship between distortion and carrier frequency was pointed out in [1]. The dead-time effect was evaluated by averaging the voltage deviation over a half cycle of the inverter [2]. Two compensation schemes of modification of the reference wave and logical combination of PWM signals were proposed. The PWM strategy in [3] presented a distorted voltage compensation method to eliminate zero current clamping. More recently, a pulse-based technique has been proposed by Leggate and Kerkman for dead-time compensation without significant magnitude and phase errors in the output voltage of the inverter [4]. The method is independent of operating frequency, carrier frequencies and load, but it requires double sampling per carrier period. Muñoz and Lipo developed a dead-time compensation technique based on an instantaneous back calculation of current phase angle [5]. A method for both dead time and zero current crossing effect compensation was also proposed by Ben-Brahim [6].

In this paper, a new method based on a systematic approach is proposed to *accurately* compensate the dead-time effect for PWM voltage inverters. The system analysis and compensation synthesis are straightforward without averaging the output voltage deviation. The simulation responses and experimental results are also presented to show the validity of the analysis proposed in the paper.

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## II. Dead-Time Effect and Modeling

### A. Dead-Time Effect

The schematic diagram of a three-phase sinusoidal PWM (SPWM) inverter is sketched in Fig. 1. The carrier signal $v_c(t)$ and voltage command $v_i(t)$ compare each other to generate an SPWM signal which is the input to an inserted switching time delay circuit. The control signals $v_{g1}$ and $v_{g2}$ are applied to the gates of IGBTs $T_1$ and $T_2$, respectively. Both IGBTs can not conduct simultaneously to prevent a short circuit in the dc link. The phase voltage $v_a$ is applied to an induction motor (IM). The antiparallel diodes $D_1$ and $D_2$ are employed as freewheeling diodes for the inductive load of the induction motor. The dc-link voltage of the inverter is denoted by $V_{\rm dc} = 2E$.

The key waveforms of the PWM inverter in Fig. 1 are shown in Fig. 2 for phase current $i_a > 0$ and $i_a < 0$. The signal $v_2$ is obtained from SPWM signal $v_1$ by a logic inverter. The delay time $T_d$ is prespecified between the positive-going edges of gating signal $v_{g1}$ $(v_{g2})$ and SPWM signal $v_1$ $(v_2)$, respectively. Let us now consider the case where the inductive phase current $i_a > 0$. $T_1$ turns on when gating signal $v_{g1}(t)$ goes high, and causes phase voltage $v_a(t)$ to be $E$. When $v_{g1}(t)$ goes zero, $T_1$ turns off, causing the freewheeling diode $D_2$ to be turned on by the positive phase current $i_a$. The phase voltage $v_a(t)$ thereby becomes to be $-E$. The similar illustration can be applied for the case where $i_a < 0$. $T_2$ turns on when $v_{g2}(t)$ goes high, and thus $v_a(t) = -E$. When $v_{g2}(t)$ goes zero, $T_2$ turns off. Inductive current $i_a$ turns on the freewheeling diode $D_1$, and thus $v_a(t) = E$. The states of power transistors, diodes and phase voltage $v_a(t)$ are summarized in Tables I and II for time intervals ①, ②, ③, ④with $i_a > 0$ and $i_a < 0$, respectively.

### B. Dead-Time Modeling

To proceed, let us define an error signal $e(t)$ between voltage command $v_i(t)$ and carrier signal $v_c(t)$ by

$$e(t) = v_i(t) - v_c(t). \tag{1}$$

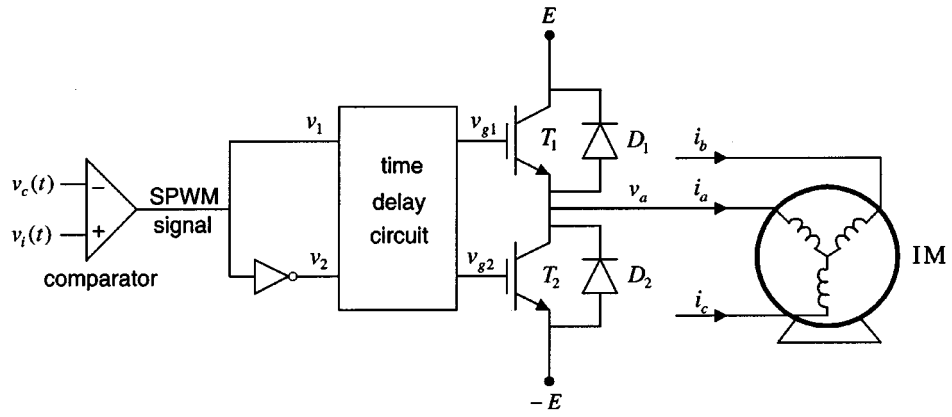


Fig. 1. A PWM inverter with time-delay circuit.

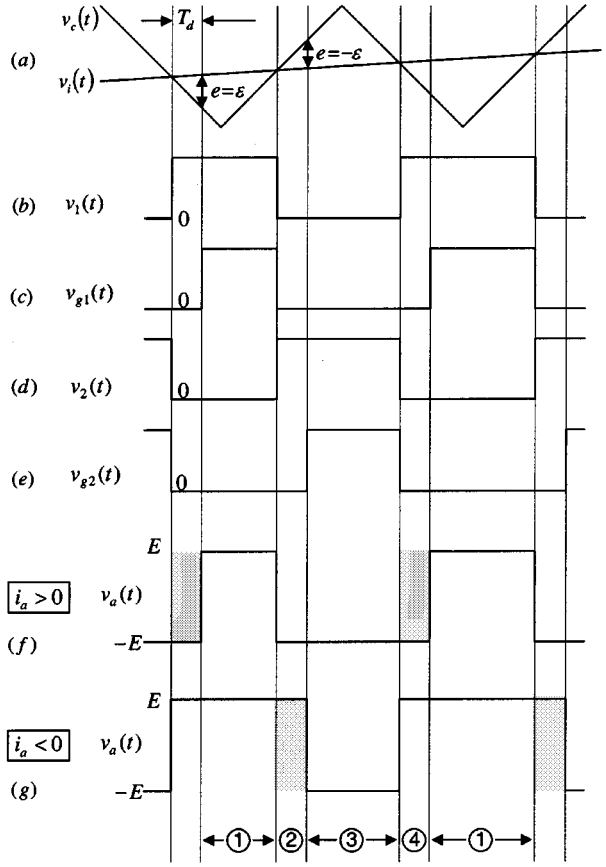


Fig. 2. PWM control signals $v_{g1}(t)$ and $v_{g2}(t)$, and phase voltage $v_a(t)$.

TABLE I
STATES OF POWER TRANSISTORS, DIODES AND PHASE VOLTAGE $v_a(t)$ FOR $i_a > 0$

| | $T_1$ | $D_1$ | $T_2$ | $D_2$ | $v_a(t)$ |
|---|---|---|---|---|---|
| ① | on | off | off | off | $E$ |
| ② | off | off | off | on | $-E$ |
| ③ | off | off | on | on | $-E$ |
| ④ | off | off | off | on | $-E$ |

TABLE II
STATES OF POWER TRANSISTORS, DIODES AND PHASE VOLTAGE $v_a(t)$ FOR $i_a < 0$

| | $T_1$ | $D_1$ | $T_2$ | $D_2$ | $v_a(t)$ |
|---|---|---|---|---|---|
| ① | on | on | off | off | $E$ |
| ② | off | on | off | off | $E$ |
| ③ | off | off | on | off | $-E$ |
| ④ | off | on | off | off | $E$ |

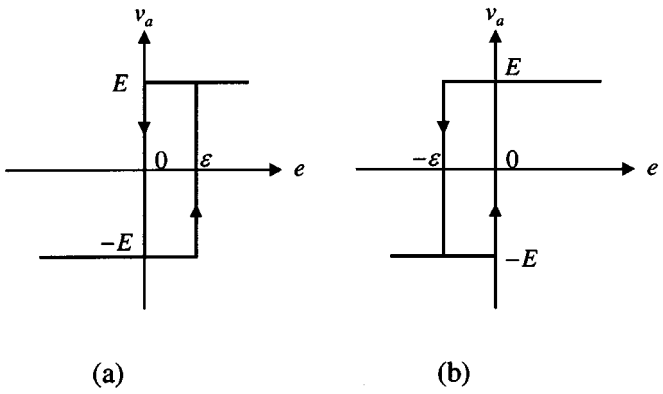


Fig. 3. Relationship between phase voltage $v_a(t)$ and error signal $e(t)$ for (a) $i_a > 0$; (b) $i_a < 0$.

Based on this definition, it is seen from Fig. 2(a), (f) and (g) that the relationship between the phase voltage $v_a(t)$ and error signal $e(t)$ is illustrated in Fig. 3 for $i_a > 0$ and $i_a < 0$. The voltage deviation $\varepsilon$ depends on the delay time $T_d$ and the slope of the triangular waveform of the carrier signal $v_c(t)$. Assume that the command signal $v_i(t)$ is slowly varying compared to the high frequency carrier signal $v_c(t)$. The ratio $-\varepsilon/T_d$ is equal to the down-slope $-2V_c/(T_c/2)$ of the triangular carrier signal $v_c(t)$, and thus we have

$$\varepsilon = T_d \frac{2V_c}{T_c/2} = 4f_c T_d V_c \tag{2}$$

where $V_c, T_c$, and $f_c$ denote the amplitude (one half of the peak-to-peak voltage), period and frequency of the carrier signal $v_c(t)$, respectively.

It is interesting to note that there exists a hysteresis nonlinearity between the signals $v_a(t)$ and $e(t)$ in Fig. 3. With the help of the definition (1), Fig. 3 leads to the block diagram of Fig. 4 for a PWM inverter with time delay circuit as shown in Fig. 1.

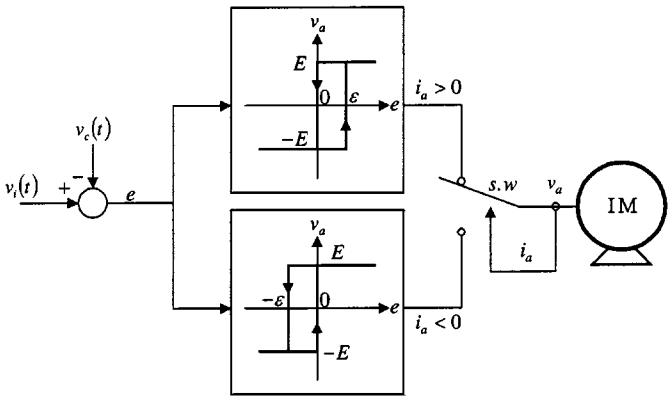


Fig. 4. Block diagram for a PWM inverter with time-delay circuit.

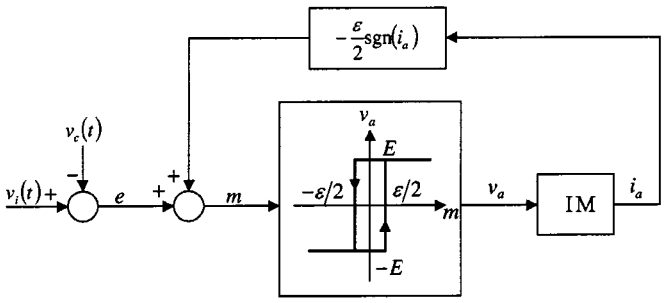


Fig. 5. Equivalent block diagram for Fig. 4.

From a system point of view, Fig. 4 can be further equivalently simplified to Fig. 5 where the sign function $\mathrm{sgn}(i_a)$ is defined as $+1$ for $i_a > 0$ and $-1$ for $i_a < 0$. This simplification follows directly from the fact that

$$\begin{aligned} i_a > 0: \quad & m = e - \frac{\varepsilon}{2} \Rightarrow \left(e = 0, \text{then } m = -\frac{\varepsilon}{2}\right) \quad \text{and} \\ & \left(e = \varepsilon, \text{then } m = \frac{\varepsilon}{2}\right) \\ i_a < 0: \quad & m = e + \frac{\varepsilon}{2} \Rightarrow \left(e = -\varepsilon, \text{then } m = -\frac{\varepsilon}{2}\right) \quad \text{and} \\ & \left(e = 0, \text{then } m = \frac{\varepsilon}{2}\right). \end{aligned} \tag{3}$$

Hence, the hysteresis related $m$ to $v_a$ in Fig. 5 is shifted right for $i_a > 0$ and left for $i_a < 0$ by a quantity $\varepsilon/2$ to give rise to the hysteresis related $e$ and $v_a$ shown in Fig. 4. This verifies the equivalence between Figs. 4 and 5.

## III. Proposed Method of Compensation

Based on Fig. 5, the model describing the dead-time effect, we will propose a compensation method via a systematic approach in this section.

It is seen that the block diagram for an idealized PWM inverter with no time delay circuit in Fig. 1 is depicted in Fig. 6. The transfer characteristic from input $\hat{e}$ to output $v_a$ is an ideal relay which is a memoryless type nonlinearity. It is clear that Fig. 6 can be easily obtained by setting $\varepsilon = 0$ in Fig. 4 or $T_d = 0$ in Fig. 2(a).

As stated above, our objective is to transform the block diagram in Fig. 5 into that in Fig. 6 by a proper compensation.

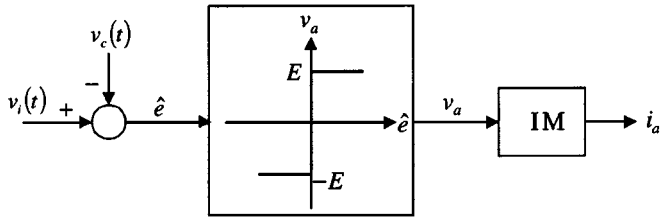


Fig. 6. Block diagram for an idealized PWM inverter.

To this end, the effect due to the upper block $-(\varepsilon/2)\mathrm{sgn}(i_a)$ in Fig. 5 must be first canceled by a feedback block $g(i_a) = (\varepsilon/2)\mathrm{sgn}(i_a)$ as shown in Fig. 7. Then, a feedforward hysteresis compensation block $f(\hat{e})$ is added to compensate the hysteresis transfer characteristic from $m$ to $v_a$ to obtain an ideal relay characteristic. The resulting PWM inverter with compensation blocks $g(i_a)$ and $f(\hat{e})$ is shown schematically in Fig. 7. The transfer characteristic from $v_i$ to $i_a$ of compensated system in Fig. 7 is equivalent to that in Fig. 6. It has an inherent phase lag if the feedforward compensation $f(\hat{e})$ is neglected.

We are now ready to practically implement the dead-time compensation for a PWM inverter with time delay circuit in Fig. 1. In this regard, it follows from Fig. 7 that

$$e = [v_i(t) - f(\hat{e}) + g(i_a)] - v_c(t) \tag{4}$$

where $\hat{e} = v_i - v_c$ and nonlinear functions $f(\hat{e})$ and $g(i_a)$ are shown in Fig. 7. It is interesting to note that the signal $v_i(t)$ in (1) is replaced by $v_i(t) - f(\hat{e}) + g(i_a)$. Based on this observation, the dead-time compensation for the PWM inverter in Fig. 1 is shown schematically in Fig. 8. The system analysis and compensation synthesis are straightforward without averaging output voltage deviation.

## IV. Simulation Responses

In this section, the simulations are carried out to verify the proposed compensation method. The results are also compared with those with no dead-time compensation and those with average voltage compensation method [2], [6].

The simulations are performed by Simulink on Matlab [9]. The system block diagram for PWM inverters with time delay circuit is shown in Fig. 5 with the model of induction motors depicted in Fig. 9, [10] where $\omega_m = 120 f_e/P$ (rpm) denotes the mechanical rotation speed in the steady state, related to the electrical frequency $f_e$ and the number of poles $P$. Here the subscript $dq$ is used for a vector in the plane of the $d$-$q$ axis. The transformations between the phase vector and $d$-$q$ vector are given by

$$v_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \text{ and}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_d \\ I_q \end{bmatrix}. \tag{5}$$

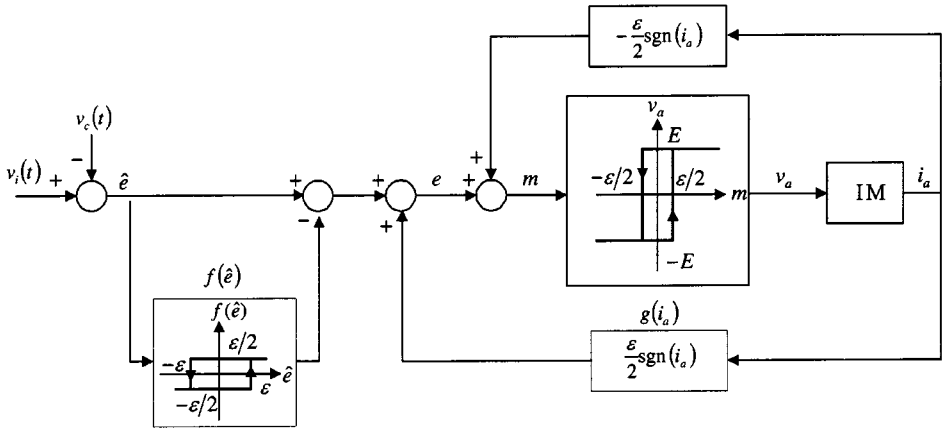


Fig. 7. Proposed method for dead-time compensation.

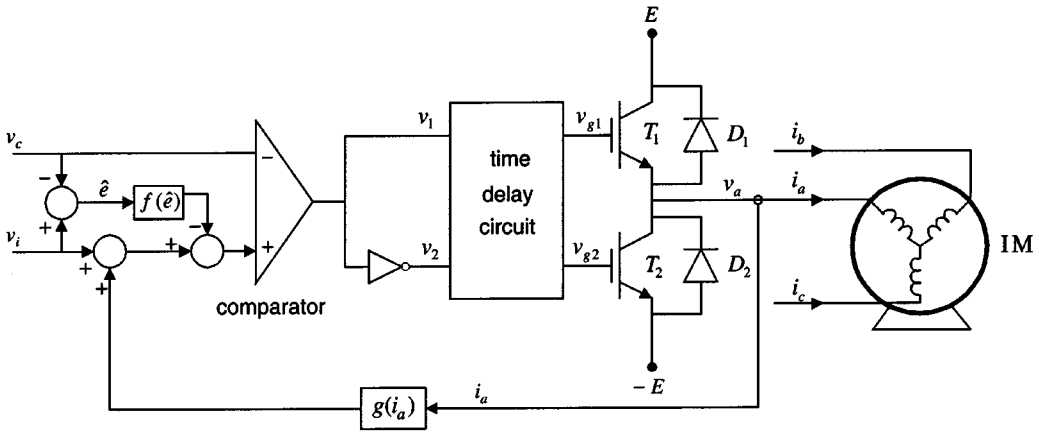


Fig. 8. PWM inverter with proposed compensation method.

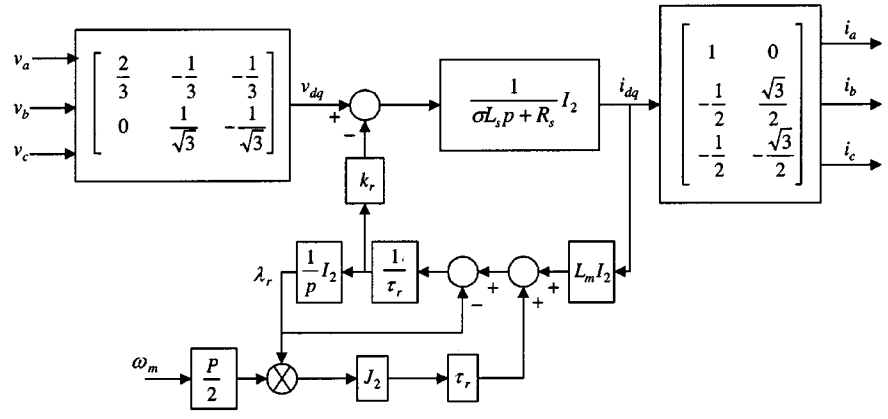


Fig. 9. Simulation model for induction motors with no load.

The parameters of the induction motor are listed in Table III. The rotor time constant is $\tau_r = L_r/R_r = 54.8$ ms and rotor coupling factor is $k_r = L_m/L_r = 0.925$. $\lambda_r$ is the rotor flux linkage vector in the plane of the $d$-$q$ axis and $\sigma = 1 - L_m^2/L_sL_r = 0.144$ is the leakage factor of the motor. Time derivative operator is denoted by $p = d/dt$, $I_2$ is the $2 \times 2$ identity matrix and $J_2$ is the $2 \times 2$ skew–symmetric matrix of the form

$$J_2 = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \tag{6}$$

TABLE III
INDUCTION MOTOR PARAMETERS.

| | | | |
|---|---|---|---|
| Stator Resistance $R_s$ | 3.41 [Ω] | Stator Inductance $L_s$ | 0.1868 [H] |
| Rotor Resistance $R_r$ | 3.41 [Ω] | Mutual Inductance $L_m$ | 0.1728 [H] |
| Number of Poles $P$ | 4 | Rotor Inductance $L_r$ | 0.1868 [H] |

The dc-link voltage is $V_{\mathrm{dc}} = 2E = 135$ V and the carrier signal frequency is $f_c = 1800$ Hz with amplitude $V_c = 15$

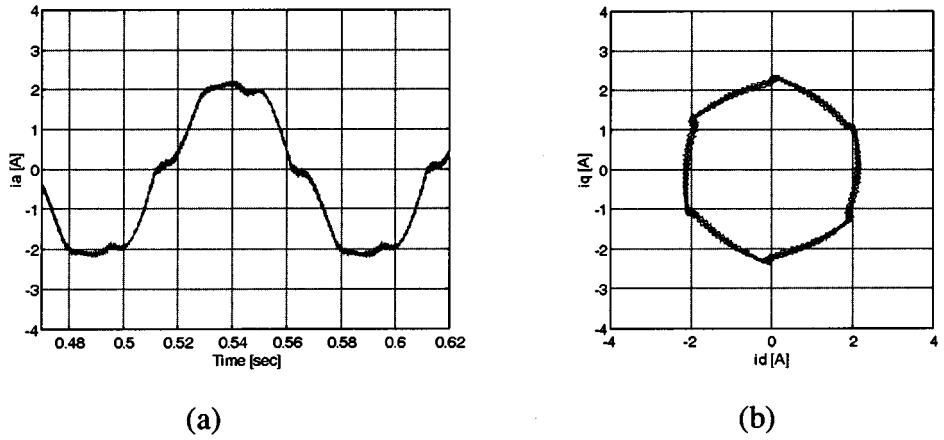


Fig. 10. (a) Steady-state phase current waveform $i_a(t)$ obtained with no dead-time compensation. (b) The $x$-$y$ plot of $i_d$ and $i_q$.

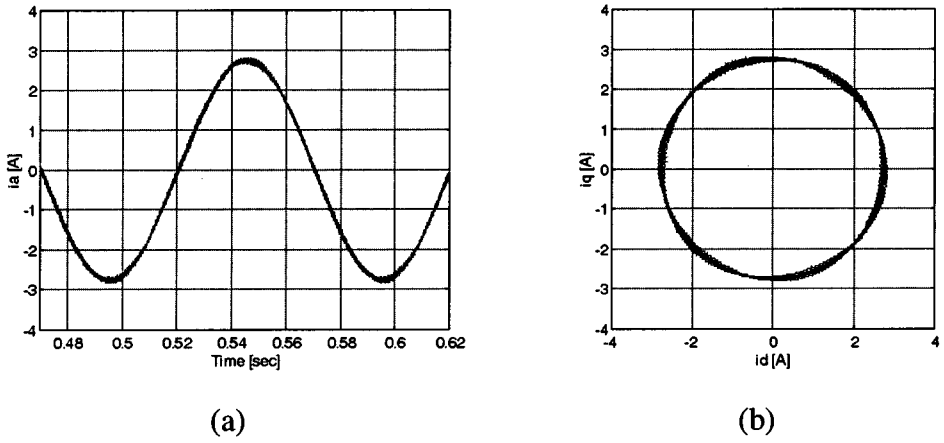


Fig. 11. (a) Steady-state phase current waveform $i_a(t)$ obtained with proposed compensation method. (b) The $x$-$y$ plot of $i_d$ and $i_q$.

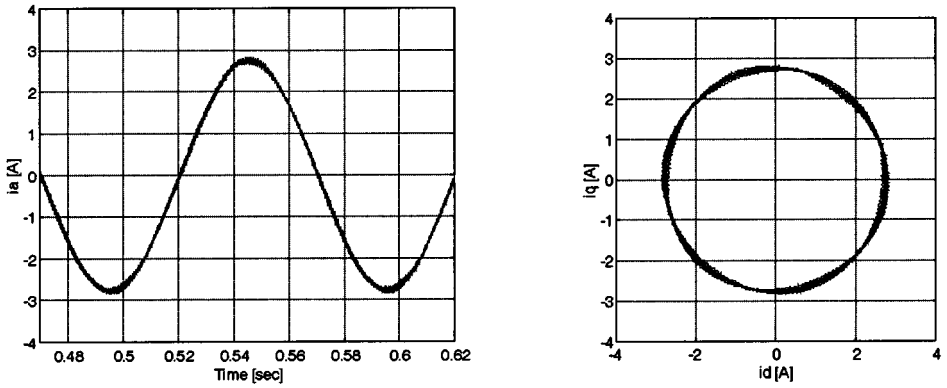


Fig. 12. Steady-state current waveforms obtained with the average voltage compensation method.

V. The frequency of the sinusoidal command voltage $v_i(t)$ is $f_e = 10$ Hz with amplitude 7.5 V. The dead time of the PWM inverter is $T_d = 40\,\mu$s. The mechanical rotation speed at no load is given by $\omega_m = 120 f_e/P = 300$ rpm in Fig. 9 and voltage deviation is $\varepsilon = 4 f_c T_d V_c = 4.32$ V.

By computer simulation, the steady-state phase current waveform $i_a(t)$ obtained with no dead-time compensation is shown in Fig. 10. The current is significantly distorted and zero current clamping phenomenon is apparent. In Fig. 11, the simulation result with proposed compensation method is presented in the steady state. The phase current maintains sinusoidal waveform which shows the perfect distortion voltage compensation. Both $i_d$ and $i_q$ are stator currents of $i_{dq} = [i_d \; i_q]^T$.

For comparison, the simulation results of the average voltage compensation method proposed in [2], [6] are also illustrated in Fig. 12. It is seen from [6] that if the PWM gain $k_{\rm PWM} = V_{\rm dc}/2V_c$ where $V_{\rm dc} = 2E$ is also taken into account, then the compensation average deviation voltage added to the voltage command is given by $(\Delta V/k_{\rm PWM})\mathrm{sgn}(i_a)$. Since the average deviation voltage is given by $\Delta V = V_{\rm dc} T_d/T_c$, we have $(\Delta V/k_{\rm PWM})\mathrm{sgn}(i_a) = 2 f_c T_d V_c \,\mathrm{sgn}(i_a) = \varepsilon/2\,\mathrm{sgn}(i_a) = g(i_a)$. The last equality but one follows directly from (2). It

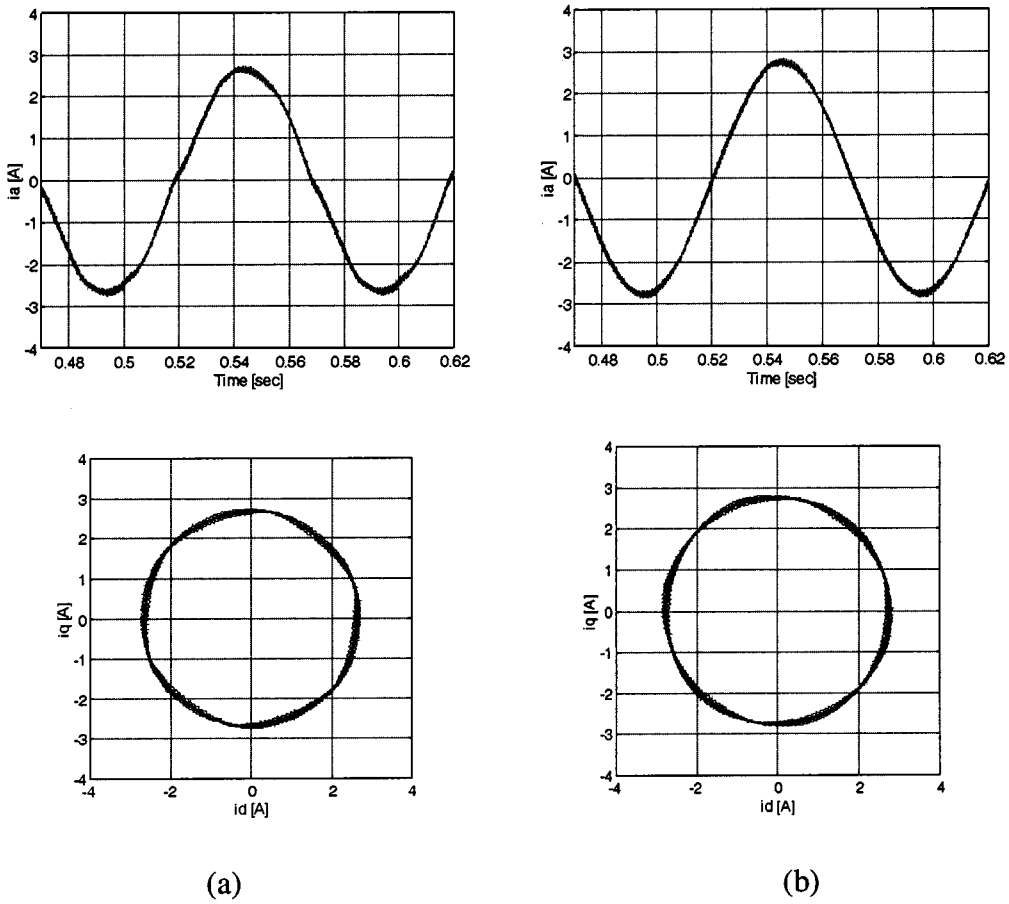


Fig. 13. (a) No dead-time compensation. (b) Proposed compensation method for switching frequency $f_c = 1800$ Hz and delay time $T_d = 10\ \mu$s.

is interesting to note that the average voltage compensation method only provides the feedback phase current compensation $g(i_a)$ in Fig. 7. However, no feedforward hysteresis compensation $f(\hat{e})$ is provided. Hence it is seen directly from Fig. 7 that the compensated system proposed by the average voltage compensation method [2], [6] exhibits a nonlinear hysteresis. It is not an ideal relay characteristic for an idealized PWM voltage inverters as shown in Fig. 6. As a result, the average voltage compensation method has an inherent phase lag from a system point of view, which is determined by the hysteresis width of $\varepsilon$.

The simulation results in Figs. 10–12 are illustrated for $f_c = 1800$ Hz and $T_d = 40\ \mu$s. For $f_c = 1800$ Hz and lower delay time $T_d = 10\ \mu$s, the results are shown in Fig. 13. In addition, for much higher switching frequency $f_c = 3000$ Hz and $T_d = 40\ \mu$s, the results are shown in Fig. 14.

## V. Experimental Results

Experimental results are also presented to show the validity of the proposed compensation method. The parameters of the induction motor are listed in the Table III. The dc-link voltage, dead time of the PWM inverter, carrier signal and sinusoidal command are given in the previous section so that voltage deviation $\varepsilon = 4f_cT_dV_c = 4.32$ V. Hence the feedback phase current compensation is given by $g(i_a) = (\varepsilon/2)\mathrm{sgn}(i_a) = 2.16\,\mathrm{sgn}(i_a)$ and the feedforward hysteresis compensation $f(\hat{e})$ is shown in Fig. 15. The overall system is shown schematically in Fig. 8. In the experiment, the induction motor is operated at a constant mechanical rotation speed $\omega_m = 120f_e/P = 300$ rpm in the steady state.

If no dead-time compensation is applied for the voltage inverter, the waveform in Fig. 16(a) shows that phase current $i_a(t)$ is distorted when the magnitude of the current is nearly zero. Fig. 16(b) displays the current waveform using the proposed dead-time compensation method operation at $f_e = 10$ Hz with no load. The distortion of the current waveform is greatly diminished. This demonstrates the validity of the proposed strategy.

## VI. Conclusion

In this paper, a new approach of dead-time compensation for PWM voltage inverters is presented. The inverter with time delay circuit is modeled by a block diagram which makes the dead-time compensation become clear. It consists of a feedback phase current cbompensation and a feedforward hysteresis compensation. The system analysis and compensation synthesis are straightforward without averaging the output voltage deviation over a half cycle of the inverter. Computer simulations and experimental results validate the usefulness of the proposed compensation method to eliminate the dead-time effect for PWM voltage inverter with time delay circuit.

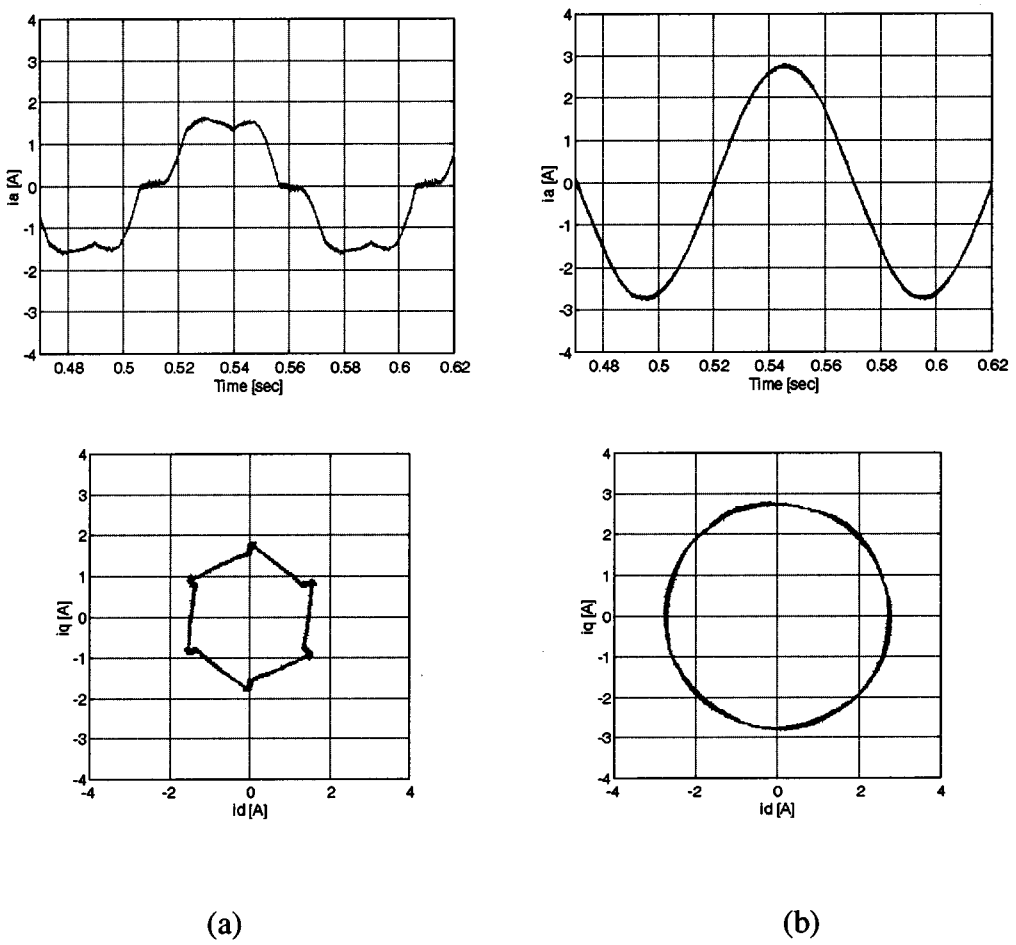


Fig. 14. (a) No dead-time compensation. (b) Proposed compensation method for switching frequency $f_c = 3000$ Hz and delay time $T_d = 40\,\mu$s.

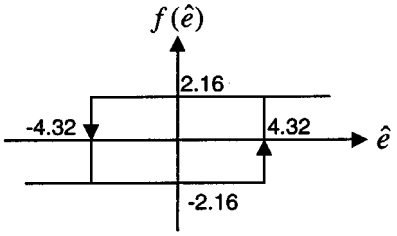


Fig. 15. Feedforward hysterisis compensation $f(\hat{e})$.

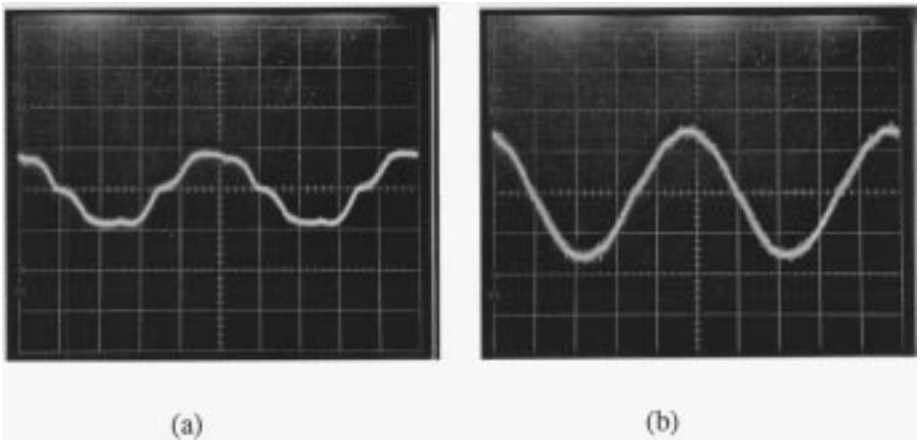


Fig. 16. Steady-state phase current waveform $i_a(t)$. (a) No dead-time compensation. (b) Proposed method (horizontal 20 ms/div, vertical 2 A/div).

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