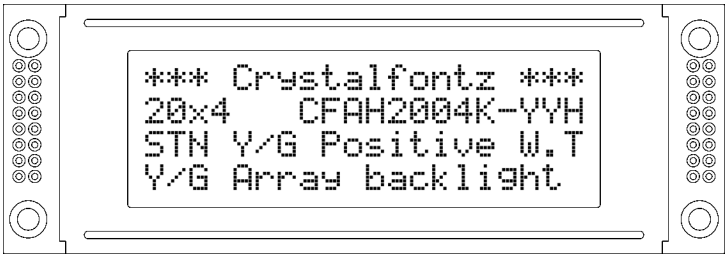
Crystalfontz America, Incorporated

CHARACTER LCD MODULE SPECIFICATIONS



Crystalfontz Model Number	**CFAH2004K-YYH-JP#**
Hardware Version	**v0.0 December 2005**
Data Sheet Version	**v0.0a January 2006**
Product Pages	www.crystalfontz.com/products/2004K

Customer Name	
Customer Part Number	

Crystalfontz America, Incorporated
12412 East Saltese Avenue
Spokane Valley, WA 99216-0357

Phone: (888) 206-9720
Fax: (509) 892-1203
Email: techinfo@crystalfontz.com
URL: www.crystalfontz.com

REVISION HISTORY

HARDWARE	
2005/12/01	Current hardware version: **v0.0** New module.

DATA SHEET	
2005/12/01	Data Sheet version: v0.0 New Data Sheet.
2006/01/01	Current Data Sheet version: **v0.0a** Changes since last released version (v0.0): Added "Luminous Intensity" specification (Pg. 12). Minor formatting and rewording changes to improve readability.

CONTENTS

LIST OF FIGURES

FEATURES

- 20x4 LCD has a large display area in a compact 116 mm x 40 mm package (4.57" x 1.57"). CFAH2004K-YYH-JP# is only 2 millimeters higher than our 20x2 LCD CFAH2002A.
- 8-bit or 4-bit parallel interface.
- Industry standard HD47780 compatible controller.
- RoHS compliant (indicated by "#" at the end of the part number).
- Yellow-green array LED backlit with STN yellow-green, positive transflective mode LCD (displays dark characters on yellow-green background).
- Wide temperature operation: -20 °C to +70°C.
- Sunlight readable.

MODULE CLASSIFICATION INFORMATION

C F A H 2 0 0 4 K - Y Y H - J P #
❶ ❷ ❸ ❹ ❺ ❻ ❼ ❽ ❾ ❿

❶	Brand	Crystalfontz America, Inc.
❷	Display Type	H – Character
❸	Number of Characters (horizontally)	20
❹	Number of Lines (vertically)	04
❺	Model Identifier	K
❻	Backlight Type & Color	Y – LED, yellow-green
❼	Fluid Type, Image (positive or negative), & LCD Glass Color	Y – STN, positive, yellow-green
❽	Polarizer Film Type, Temperature Range (normal or wide), & View Angle (o 'clock)	H – Transflective, WT, 6:00
❾	CGROM Font	JP – Japanese and English
❿	RoHS Status	# – RoHS Compliant

ORDERING INFORMATION

PART NUMBER	FLUID	LCD GLASS COLOR	IMAGE	POLARIZER FILM	BACKLIGHTS
CFAH2004K-YYH-JP#	STN	yellow-green	positive	transflective	yellow-green array LEDs

Also see Backlight Characteristics (By Module Part Number) (Pg. 12).

SYSTEM BLOCK DIAGRAM

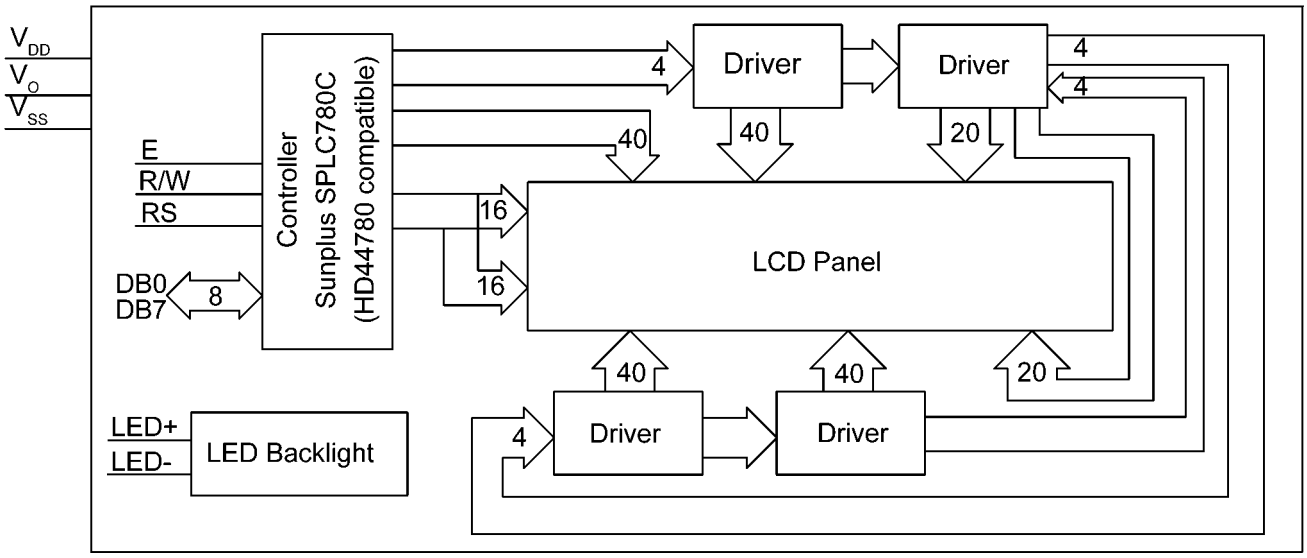


Figure 1. System Block Diagram

PHYSICAL CHARACTERISTICS

ITEM	SIZE (mm)
Module Dimensions	116 (W) x 40 (H) x 15.0 (D)
Viewing Area	76 (W) x 25.2 (H)
Active Area	70.4 (W) x 20.8 (H)
Character Size	2.95 (W) x 4.75 (H)
Character Pitch	3.55 (W) x 5.35 (H)
Dot Size	.55 (W) x .55 (H)
Dot Pitch	.60 (W) x .60 (H)
Depth	15.0
Weight	68 grams (typical)

TEMPERATURE RANGE

CRITERIA	SPECIFICATION
Operating Temperature Range	-20°C minimum to +70°C maximum
Storage Temperature Range	-30°C minimum to +80°C maximum

OPTICAL CHARACTERISTICS

Viewing Direction	6 o'clock

ITEM	SYMBOL	CONDITION	MINIMUM	TYPICAL	MAXIMUM
View Angle	(V)θ	CR>2	-20°		35°
Contrast Ratio	(H)φ	CR>2	-30°		30°
LCD Response Time	T rise			250 ms	
	T fall			250 ms	

CONDITIONS FOR DEFINITIONS IN FIGURES 2 AND 3

- Operating Voltage: V_{OP}
- Viewing Angle (θ, φ): 0°, 0°
- Frame Frequency: 64 Hz
- Driving Waveform: 1/N Duty, 1/a Bias

DEFINITION OF OPERATION VOLTAGE (V_{OP})

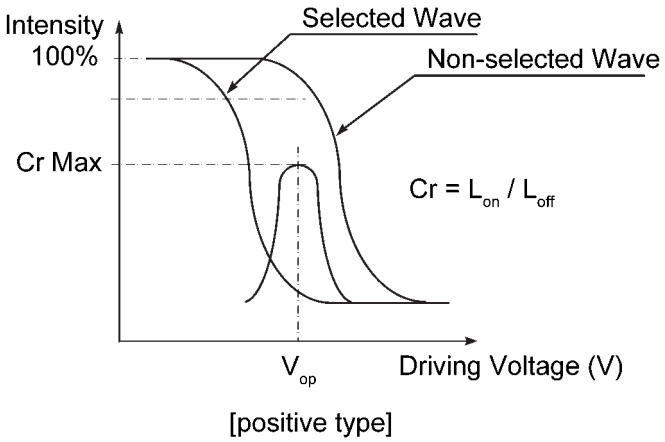


Figure 2. Definition of Operation Voltage (V_{OP})

DEFINITION OF RESPONSE TIME (TR, TF)

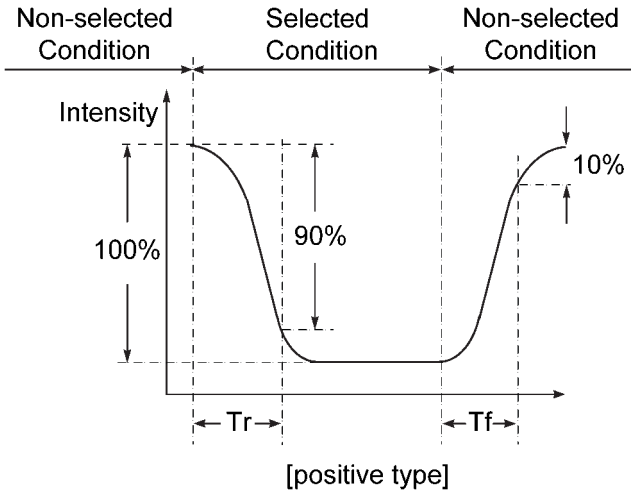


Figure 3. Definition of Response Time (Tr, Tf)

DEFINITION OF VIEWING ANGLE (CR>2)

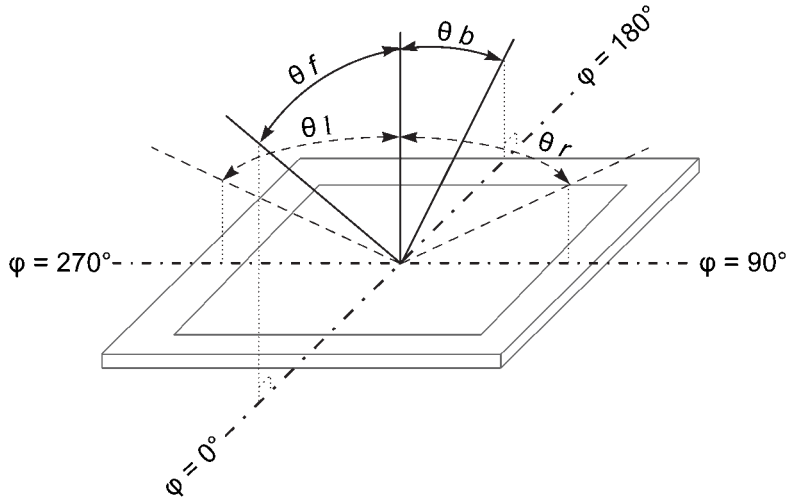


Figure 4. Definition of Viewing Angle

ELECTRICAL SPECIFICATIONS

DRIVING METHOD	SPECIFICATION
Duty	1/16
Bias	1/5

CHARACTERISTIC	SYMBOL	ABSOLUTE MAXIMUM RATINGS
Operating Voltage	V_{DD}	-0.3v to +7.0v
Driver Supply Voltage	V_{LCD}	$V_{LCD} = V_{DD}$ -12v to $V_{LCD} = V_{DD}$ + 0.3v or V_O = -7v to V_O = +5.3v (for VDD = +5v)
Input Voltage Range	V_{IN}	-0.3v to V_{DD} + 0.3v

LCD SUPPLY VOLTAGE		MINIMUM	TYPICAL	MAXIMUM
Supply voltage for driving LCD (V_{DD} - V_O)	T_A = 0ºC			+4.8v
	T_A = +25ºC		+4.5v	
	T_A = +50ºC	+4.2v		

CURRENT CONSUMPTION	MINIMUM	TYPICAL	MAXIMUM
Supply current (I_{DD}) V_{DD} = +5v		+1.2 mA	

DC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	TEST CONDITION
Input High Voltage	V_{IH1}	+2.2v		V_{DD}	Pins: E, RS, R/W, DB0 - DB7
Input Low Voltage	V_{IL1}	-0.3v		-0.6v	
Input High Current	I_{IH}	-2.0 µA		+2.0 µA	Pins: RS, R/W, DB0 - DB7 V_{DD} = +5.0v
Input Low Current	I_{IL}	-20 µA	-50 µA	-100 µA	
Output High Voltage	V_{OH1}	+2.4v		V_{DD}	I_{OH} = - 0.1 mA Pins: DB0 - DB7
Output Low Voltage	V_{OL1}			+0.4v	I_{OL} = 0.1 mA Pins: DB0 - DB7

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard anti-static precautions as you would for any other PCB such as expansion cards or motherboards. For more information, read CARE AND HANDLING PRECAUTIONS (Pg. 18).

TYPICAL V_O CONNECTIONS

Adjust V_O to +1v (V_{LCD} = +4v) as an initial setting. When the module is operational, readjust V_O for optimal display appearance.

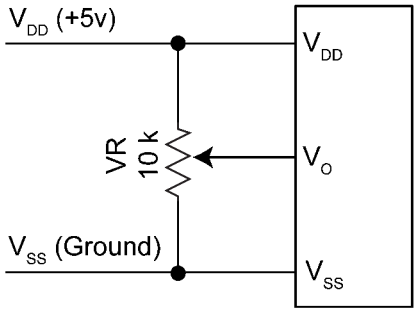


Figure 5. V_O Connections for Normal Temperature Operation

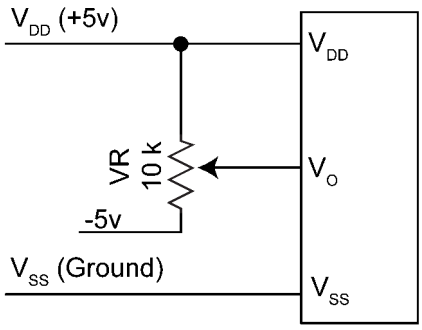


Figure 6. V_O Connections for Wide Temperature Operation

BACKLIGHTS

The CFAH2004K-YYH-JP# uses LED backlights. LED backlights are easy to use properly but they are also easily damaged by abuse.

> **NOTE**
> Do not connect +5v to the backlight terminals. This will ruin the backlight.

LEDs are “current” devices. The important thing to an LED is the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor will work well in most applications and is much less complex than a current source.

You need to know what the forward voltage of the LEDs will be so you can calculate a current limiting resister (R_{LIMIT}). The forward voltage will vary slightly from display to display.

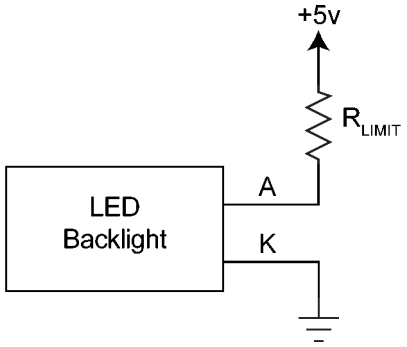


Figure 7. Typical LED Backlight Connections

The general equation to calculate R_{LIMIT} is:

$$R_{LIMIT}\ (\text{minimum}) = \frac{V_{DD}\ (\text{supply voltage}) - V_{LED}\ (\text{LED forward voltage})}{I_{LED}\ (\text{maximum LED current})}$$

The specific R_{LIMIT} calculation for the CFAH2004K-YYH-JP# at V_{DD} = +5v is:

$$R_{LIMIT} = \frac{5v - 4.2v}{0.180\ A\ (maximum)} = 5\Omega\ (minimum)$$

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

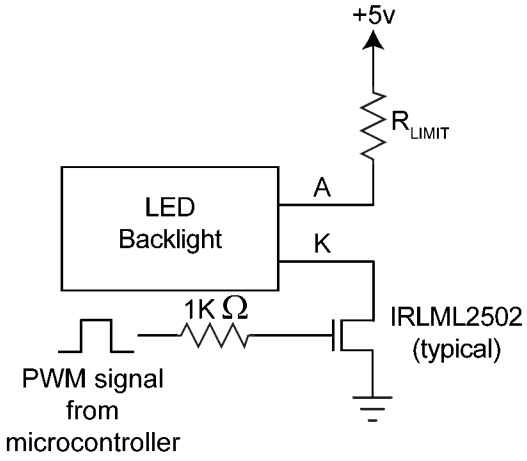


Figure 8. Typical LED Backlight Connections for PWM Dimming

BACKLIGHT CHARACTERISTICS (BY MODULE PART NUMBER)

CFAH2004K-YYH-JP# ***Dark characters on yellow-green background***			
PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**
Current (I_{LED})		180 mA	
Forward Voltage (V_{LED})	+4.0v	+4.2v	+4.4v
Reverse Voltage			+5v
Luminous Intensity (IV) I_{LED} = 190 mA		34 cd/m^2	
Wavelength (λ p) I_{LED} = 190 mA		568 nm	

RELIABILITY

ITEM	SPECIFICATION
LCD portion (excluding Backlight)	50,000 to 100,000 hours (typical)
Yellow-green LED Backlights	50,000 to 100,000 hours (typical)

INTERFACE PIN FUNCTIONS

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
1	V_{SS}	+0v	–	Ground
2	V_{DD}	+5.0v	–	Supply voltage for logic
3	V_O	variable	–	Supply voltage for driving LCD V_O = +1v typical at V_{DD} = +5v which gives a V_{LCD} = (V_{DD} - V_O) = +4v
4	RS	H/L	I	Register selection input H: data register (for read and write) L: instruction code (for write)
5	R/W	H/L	I	Read/write selection input H: read (MPU←module) L: write (MPU→module)
6	E	H,H→L	I	Read/write enable signal H: write data is latched on the falling edge H→L: read data is enabled by a high level
7	DB0	H/L	I/O	Data bit 0
8	DB1	H/L	I/O	Data bit 1
9	DB2	H/L	I/O	Data bit 2
10	DB3	H/L	I/O	Data bit 3
11	DB4	H/L	I/O	Data bit 4
12	DB5	H/L	I/O	Data bit 5
13	DB6	H/L	I/O	Data bit 6
14	DB7	H/L	I/O	Data bit 7
15	LED+ (A)	–	–	Supply voltage for LED “A” or “anode” or “+” of LED backlight
16	LED- (K)	–	–	Supply voltage for LED “K” or “cathode” or “-” of LED backlight

SPLC780C CONTROLLER INTERFACE INFORMATION

The CFAH2004K-YYH-JP# uses a Sunplus SPLC780C controller. The CFAH2004K-YYH-JP# is compatible with the industry standard Hitachi HD44780 controller. Software written for modules that use the HD44780 should work without modification for the CFAH2004K-YYH-JP#.

For your reference, we included the SPLC780C controller data sheet as an appendix to this CFAH2004K-YYH-JP# data sheet. Links to some of the most useful sections of the SPLC780C data sheet are:

- Instruction description (see 5. Functional Description in Appendix B, page 6).
- Instruction table (see 5.3 Instruction Table in Appendix B, page 8.)
- Initializing the module (see 5.7 Reset Function in Appendix B, page 11).
- Timing Characteristics (see 6. Electrical Specifications in Appendix B, page 21).

DISPLAY POSITION DDRAM ADDRESS

The following table shows the relationship between the controller's addresses and the corresponding character location on the CFAH2004K-YYH-JP#.

ROW	COLUMN																			
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**
0	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0xA	0xB	0xC	0xD	0xE	0xF	0x10	0x11	0x12	0x13
1	0x40	0x41	0x42	0x43	0x44	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E	0x4F	0x50	0x51	0x52	0x53
2	0x14	0x15	0x16	0x17	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
3	0x54	0x55	0x56	0x57	0x58	0x58	0x5A	0x5B	0x5C	0x5D	0x5E	0x5F	0x60	0x61	0x62	0x63	0x64	0x65	0x66	0x67

CHARACTER GENERATOR ROM (CGROM)

To find the code for a given character, add the two numbers that are shown in bold for its row and column. For example, the lowercase "h" is in the column labeled "96_{10}" and in the row labeled "8_{10}". So you would add 96 + 8 to get 104. When you send a byte with the value of 104 to the display, then a lowercase "h" will be shown. Additional character sets are available. Minimum order may be required. (See APPENDIX B: SUNPLUS SPLC780C CONTROLLER DATA SHEET (Pg. 26).)

Figure 9. Character Generator ROM (CGROM)

MODULE OUTLINE DRAWING

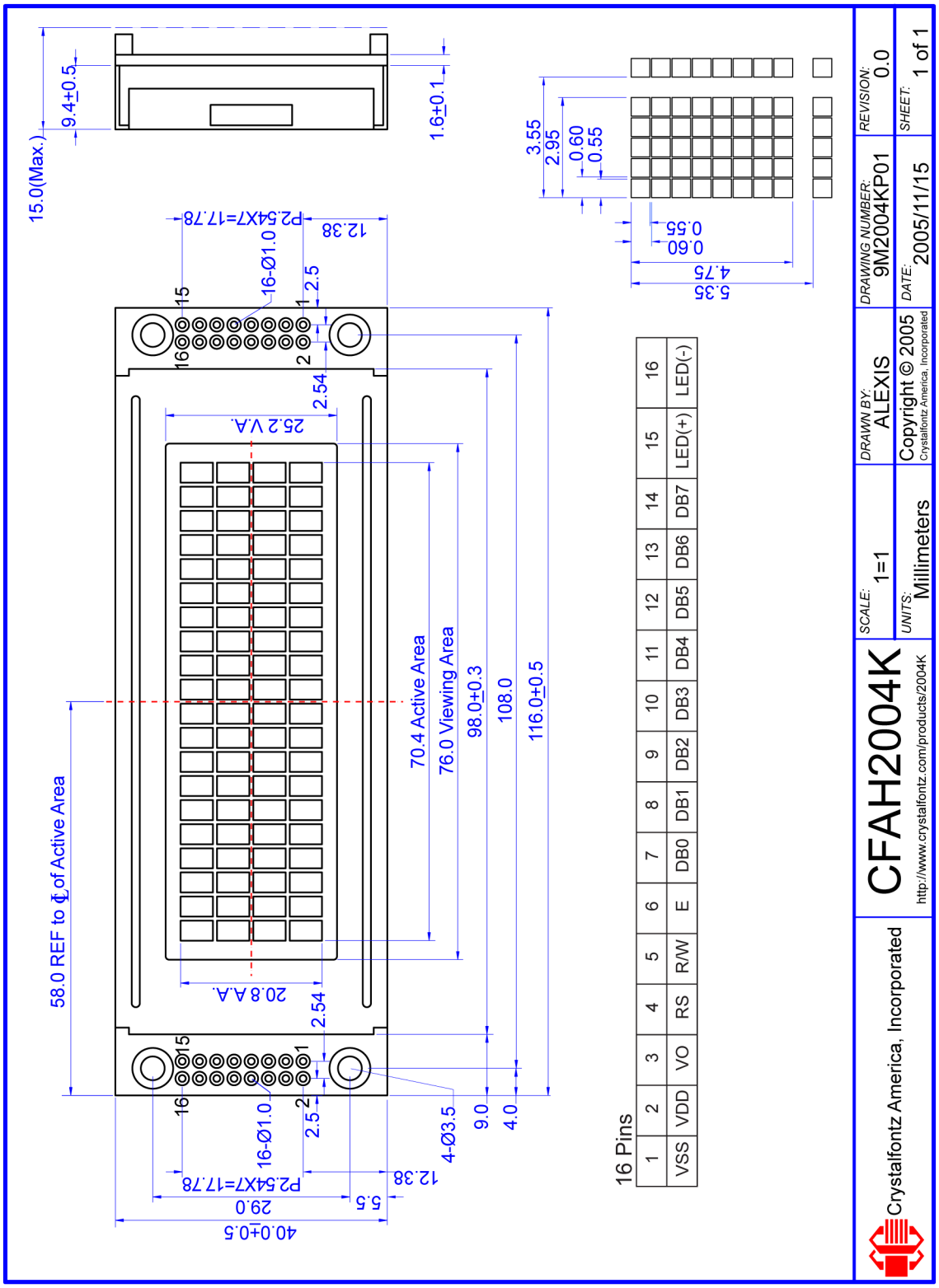


Figure 10. CFAH2004K Module Outline Drawing

CARE AND HANDLING PRECAUTIONS

For optimum operation of the CFAH2004K-YYH-JP# and to prolong its life, please follow the precautions described below.

ELECTROSTATIC DISCHARGE (ESD)

Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- To protect the polarizer from damage, the CFAH2004K-YYH-JP# ships with a protective film over the LCD glass. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- Place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the CFAH2004K-YYH-JP#, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the CFAH2004K-YYH-JP#.
- Do not modify the tab of the metal holder or make connections to it.
- Solder only to the I/O terminals. Use care when removing solder—it is possible to damage the PCB.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the CFAH2004K-YYH-JP# to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the CFAH2004K-YYH-JP#.
- Do not place weight or pressure on the CFAH2004K-YYH-JP#.

IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful to not get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not eat the LCD panel.

CLEANING

- To clean the front of the LCD, a standard household glass cleaner works well. Gently wipe with a nonabrasive soft cloth.
- The exposed surface of the LCD “glass” is actually the front polarizer laminated to the glass. The polarizer is made out of a fairly soft plastic and is easily scratched or damaged. The polarizer will eventually become hazy if you do not take great care when cleaning it. Long contact with moisture (from condensation or cleaning) may permanently spot or stain the polarizer.

OPERATION

- Your circuit should be designed to protect the CFAH2004K-YYH-JP# from ESD and power supply transients.
- Observe the operating temperature limitations: a minimum of -20°C to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

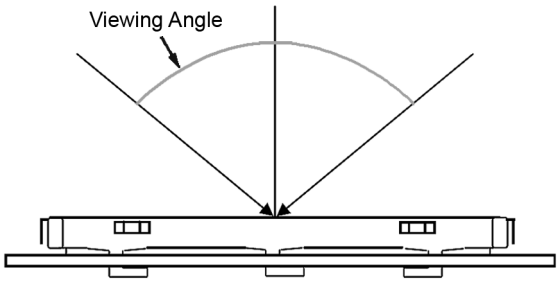
STORAGE

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: a minimum of -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the CFAH2004K-YYH-JP#s while they are in storage.

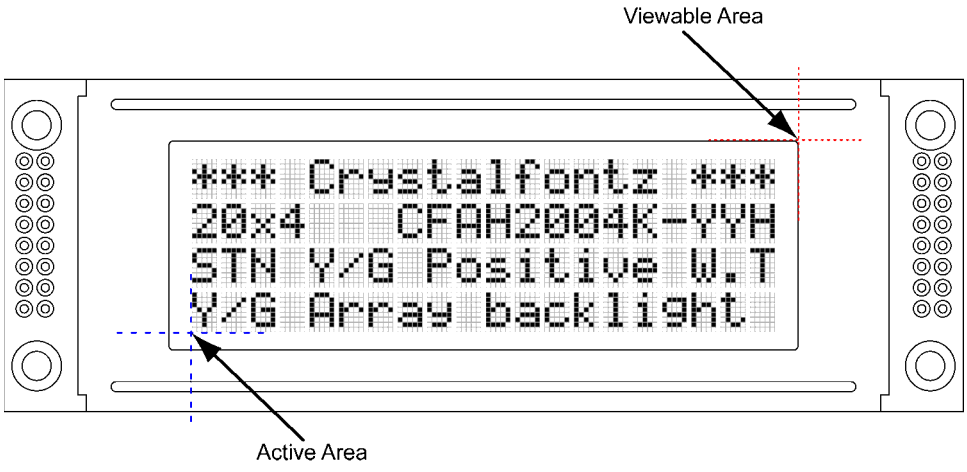
APPENDIX A: QUALITY ASSURANCE STANDARDS

INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH
- For visual inspection of active display area
  - Source lighting: two 20 Watt or one 40 Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewable angle: inspect at 45° angle of vertical line right and left, top and bottom



DEFINITION OF ACTIVE AREA AND VIEWABLE AREA



ACCEPTANCE SAMPLING

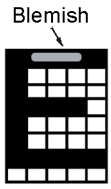
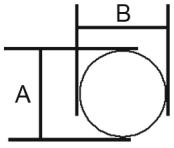
DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

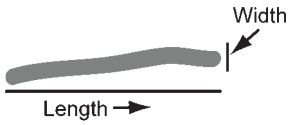
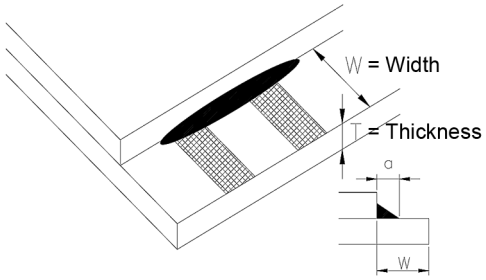
DEFECTS CLASSIFICATION

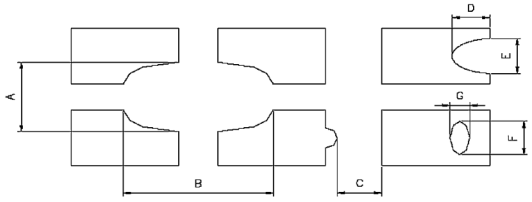
Defects are defined as:

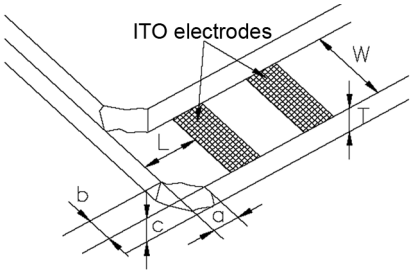
- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

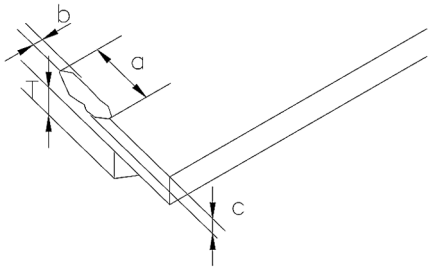
ACCEPTANCE STANDARDS

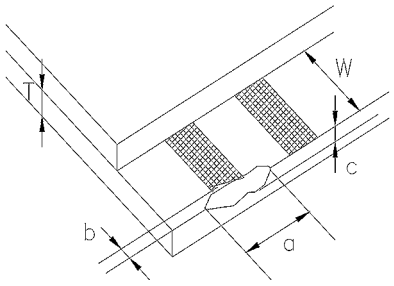
#	DEFECT TYPE	CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications. (See Inspection Conditions (Pg. 20).			Major
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major
4	Blemishes or foreign matter on display segments		*Defect Size (mm)*	*Acceptable Qty*	Minor
			≤0.3	3	
			≤2 defects within 10 mm of each other		
5	Other blemishes or foreign matter outside of display segments	Defect size = (A + B)/2 	*Defect Size (mm)*	*Acceptable Qty*	Minor
			≤0.15	Ignore	
			0.15 to 0.20	3	
			0.20 to 0.25	2	
			0.25 to 0.30	1	

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th colspan="3">CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Dark lines or scratches in display area
 
</td><td>Defect Width (mm)</td><td>Defect Length (mm)</td><td>Acceptable Qty</td><td rowspan="6">Minor</td></tr>
<tr><td>≤0.03</td><td>≤3.0</td><td>3</td></tr>
<tr><td>0.03 to 0.05</td><td>≤2.0</td><td>2</td></tr>
<tr><td>0.05 to 0.08</td><td>≤2.0</td><td>1</td></tr>
<tr><td>0.08 to 0.10</td><td>≤3.0</td><td>0</td></tr>
<tr><td>≥0.10</td><td>>3.0</td><td>0</td></tr>
<tr><td rowspan="5">7</td><td rowspan="5">Bubbles between polarizer film and glass</td><td colspan="2">Defect Size (mm)</td><td>Acceptable Qty</td><td rowspan="5">Minor</td></tr>
<tr><td colspan="2">≤0.20</td><td>Ignore</td></tr>
<tr><td colspan="2">0.20 to 0.40</td><td>3</td></tr>
<tr><td colspan="2">0.40 to 0.60</td><td>2</td></tr>
<tr><td colspan="2">≥0.60</td><td>0</td></tr>
<tr><td>8</td><td>Glass rest defect</td><td colspan="3"> 

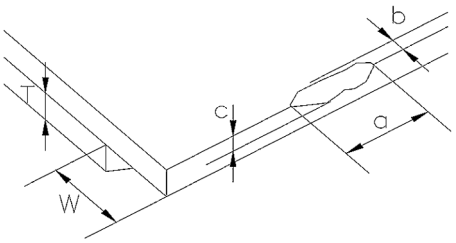
a≤1/4W</td><td>Minor</td></tr>
<tr><td rowspan="6">9</td><td rowspan="6">Display pattern defect</td><td colspan="3"> 
</td><td rowspan="6">Minor</td></tr>
<tr><td>Dot Size (mm)</td><td colspan="2">Acceptable Qty</td></tr>
<tr><td>((A+B)/2)≤0.2</td><td colspan="2" rowspan="4">≤3 total defects
≤2 pinholes per digit</td></tr>
<tr><td>C>0</td></tr>
<tr><td>((D+E)/2)≤0.25</td></tr>
<tr><td>((F+G)/2)≤0.25</td></tr>
</table>

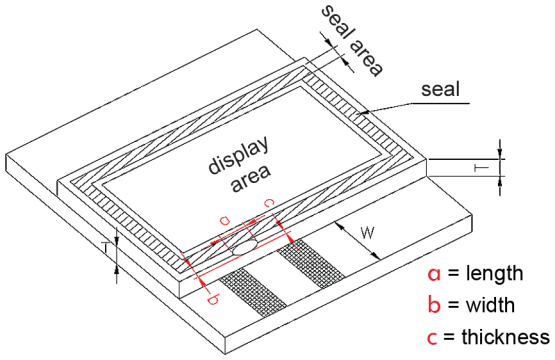
<table>
<tr><th>#</th><th>DEFECT TYPE</th><th>CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td>10</td><td>Chip in corner</td><td> 

<table>
<tr><th>a</th><th>b</th><th>c</th><th>Acceptable Qty</th></tr>
<tr><td><4 mm</td><td>≤W</td><td>c≤T</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>11</td><td>Chip on “non-contact” edge of LCD</td><td> 

<table>
<tr><th>a</th><th>b</th><th>c</th><th>Acceptable Qty</th></tr>
<tr><td>≤3 mm</td><td>≤1 mm</td><td>≤T</td><td>Ignore</td></tr>
<tr><td>≤4 mm</td><td>≤1.5 mm</td><td>≤T</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>12</td><td>Chip on “contact” edge of LCD, on the active side</td><td> 

<table>
<tr><th>a</th><th>b</th><th>c</th><th>Acceptable Qty</th></tr>
<tr><td>≤2 mm</td><td>≤W/4</td><td>≤T</td><td>Ignore</td></tr>
<tr><td>≤3 mm</td><td>≤W/4</td><td>≤T</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
</table>

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th>CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td>13</td><td>Chip on “contact” edge of LCD, on the inactive side</td><td> 

<table>
<tr><th>a</th><th>b</th><th>c</th><th>Acceptable Qty</th></tr>
<tr><td>≤3 mm</td><td>≤1 mm</td><td>≤T</td><td>Ignore</td></tr>
<tr><td>≤4 mm</td><td>≤1.5 mm</td><td>≤T</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>14</td><td>Chip in seal area</td><td> 

<table>
<tr><th>a</th><th>b</th><th>c</th><th>Acceptable Qty</th></tr>
<tr><td><3 mm</td><td>≤1.5 mm</td><td>≤1/2 T</td><td>3</td></tr>
<tr><td colspan="4">Unacceptable if c>50% of glass thickness or if the seal area is damaged.</td></tr>
</table></td><td>Minor
Major</td></tr>
<tr><td>15</td><td>Backlight defects</td><td>1. Light fails or flickers. (Major)
2. Color and luminance do not correspond to specifications. (Major)
3. Exceeds standards for display’s blemishes or foreign matter (see test 5, Pg. 21), and dark lines or scratches (see test 6, Pg. 22). (Minor)</td><td>See list</td></tr>
<tr><td>16</td><td>COB defects</td><td>1. Pinholes >0.2 mm.
2. Seal surface has pinholes through to the IC.
3. More than 3 locations of sealant beyond 2 mm of the sealed areas.</td><td>Minor</td></tr>
<tr><td>17</td><td>PCB defects</td><td>1. Oxidation or contamination on connectors.*
2. Wrong parts, missing parts, or parts not in specification.*
3. Jumpers set incorrectly. (Minor)
4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. (Minor)
*Minor if display functions correctly. Major if the display fails.</td><td>See list</td></tr>
</table>

#	DEFECT TYPE	CRITERIA	MAJOR / MINOR
18	Soldering defects	1. Unmelted solder paste. 2. Cold solder joints, missing solder connections, or oxidation.* 3. Solder bridges causing short circuits.* 4. Residue or solder balls. 5. Solder flux is black or brown. *Minor if display functions correctly. Major if the display fails.	Minor

APPENDIX B: SUNPLUS SPLC780C CONTROLLER DATA SHEET

The complete *Sunplus SPLC780C 16COM/40SEG Controller/Driver Data Sheet* (47 pages) follows.

DATA SHEET

凌陽科技
SUNPLUS

SPLC780C

16COM/40SEG Controller/Driver

JUL. 09, 2002

Version 1.1

Table of Contents

PAGE

16COM/40SEG CONTROLLER/DRIVER

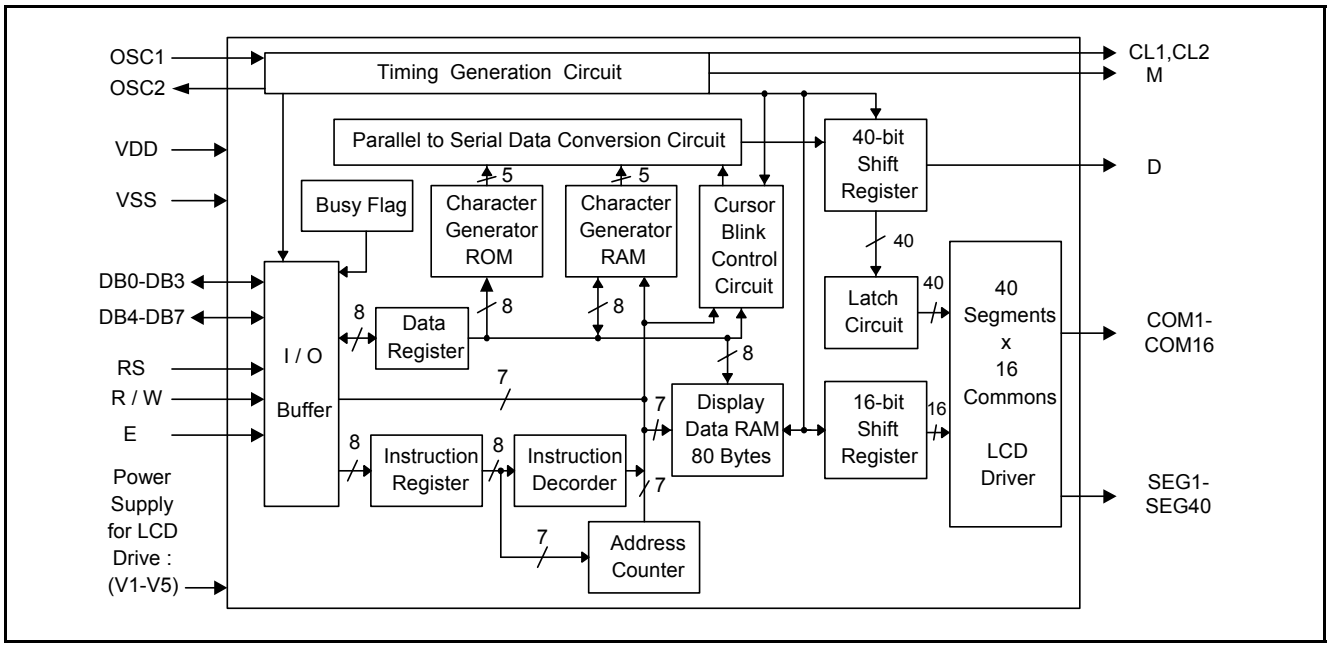
1. GENERAL DESCRIPTION

The SPLC780C, a dot-matrix LCD controller and driver from SUNPLUS, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC780C provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC780C is able to display up to two 8-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- 4-bit or 8-bit MPU interfaces
- Direct driver for LCD: 16 COMs x 40 SEGs
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Low Power Consumption
- Package form: 80 QFP or bare chip available

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	33	I	Power input
VSS	23	I	Ground
OSC1 OSC2	24 25	-	Both OSC1 and OSC2 are connected to resistor for internal oscillator circuit. For external clock operation, the clock is input to OSC1.
V1 - V5	26 - 30	I	Supply voltage for LCD driving.
E	38	I	A start signal for reading or writing data.
RW	37	I	A signal for selecting read or write actions. 1: Read, 0: Write.
RS	36	I	A signal for selecting registers. 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag - Address Counter (for read).
DB0 - DB3	39 - 42	I/O	Low 4-bit data
DB4 - DB7	43 - 46	I/O	High 4-bit data
CL1	31	O	Clock to latch serial data D.
CL2	32	O	Clock to shift serial data D.
M	34	O	Switch signal to convert LCD waveform to AC.
D	35	O	Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.
SEG1 - SEG22 SEG23 - SEG40	22 - 1 80 - 63	O	Segment signals for LCD.
COM1 - COM16	47 - 62	O	Common signals for LCD.

5. FUNCTIONAL DESCRIPTIONS

5.1. Oscillator

SPLC780C oscillator supports not only the internal oscillator operation, but also the external clock operation.

5.2. Control and Display Instructions

Control and display instructions are described in details as follows:

5.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.

5.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

5.2.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I / D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

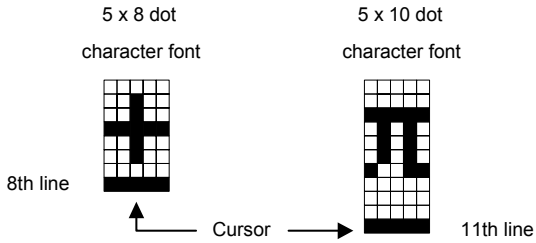
5.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

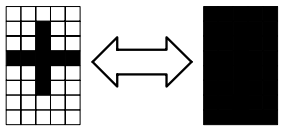
B = 1: Blinks on, B= 0: Blinks off



5.2.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



Blink display alternately

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

5.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Data transferred with 8-bit length (DB7 - 0).

DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring.

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

It cannot display two lines with 5 x 10 dots character font.

5.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets Character Generator RAM Address (aaaaaa)2 to the Address Counter.

Character Generator RAM data can be read or written after this setting.

5.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets Display Data RAM Address $(aaaaaaa)_2$ to the Address Counter.

Display data RAM can be read or written after this setting.

In one-line display (N = 0),

$(aaaaaaa)_2$: $(00)_{16}$ - $(4F)_{16}$.

In two-line display (N = 1),

$(aaaaaaa)_2$: $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_2$: $(40)_{16}$ - $(67)_{16}$ for the second line.

5.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter $(aaaaaaa)_2$ is read.

5.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

5.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM.

To read data correctly, do the following:

1). The address of the Character Generator RAM or Display Data RAM or shift the cursor instruction.

2). The " Read " instruction.

5.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	38μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	38μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	38μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	38μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	38μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in counter	38μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	38μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	38μs

Note: "-": don't care

5.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780C starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY_	Only shift the cursor's position to the left (Y).
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY_	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	OMPANY_	Write " N ". The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPAMY_	Shift the display and the cursor's position to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	OMPANY_	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	COMPAMY_	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	:
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME_	Both the display and the cursor return to the original position (address 0).

5.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780C starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font.
4	0 0 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appears.
5	0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
6	1 0 0 1 0 1 1 0 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.

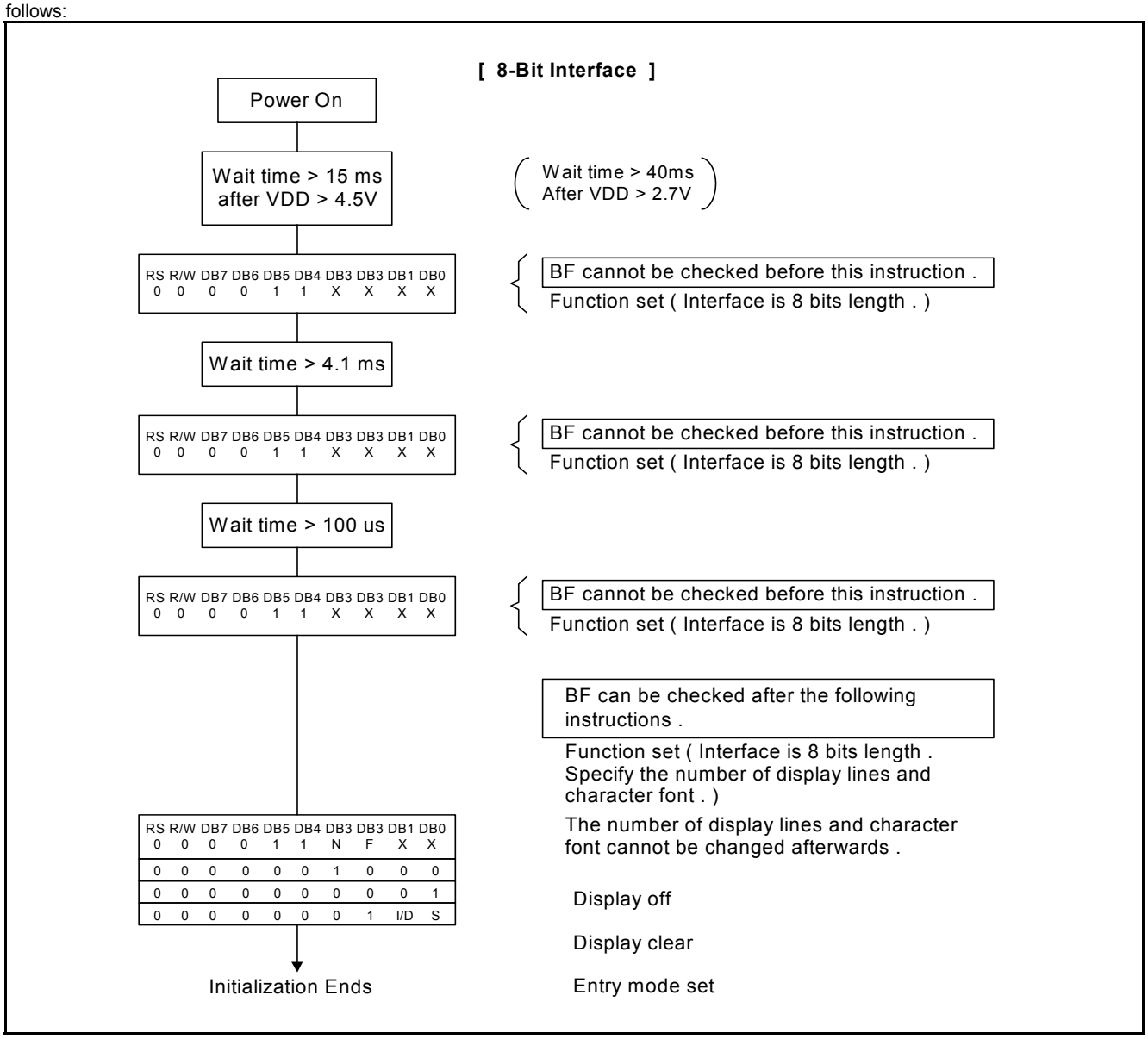
5.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780C starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 8 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	:
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T ". The cursor is incremented by one and shifted to the right.
10	:	:	:
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.

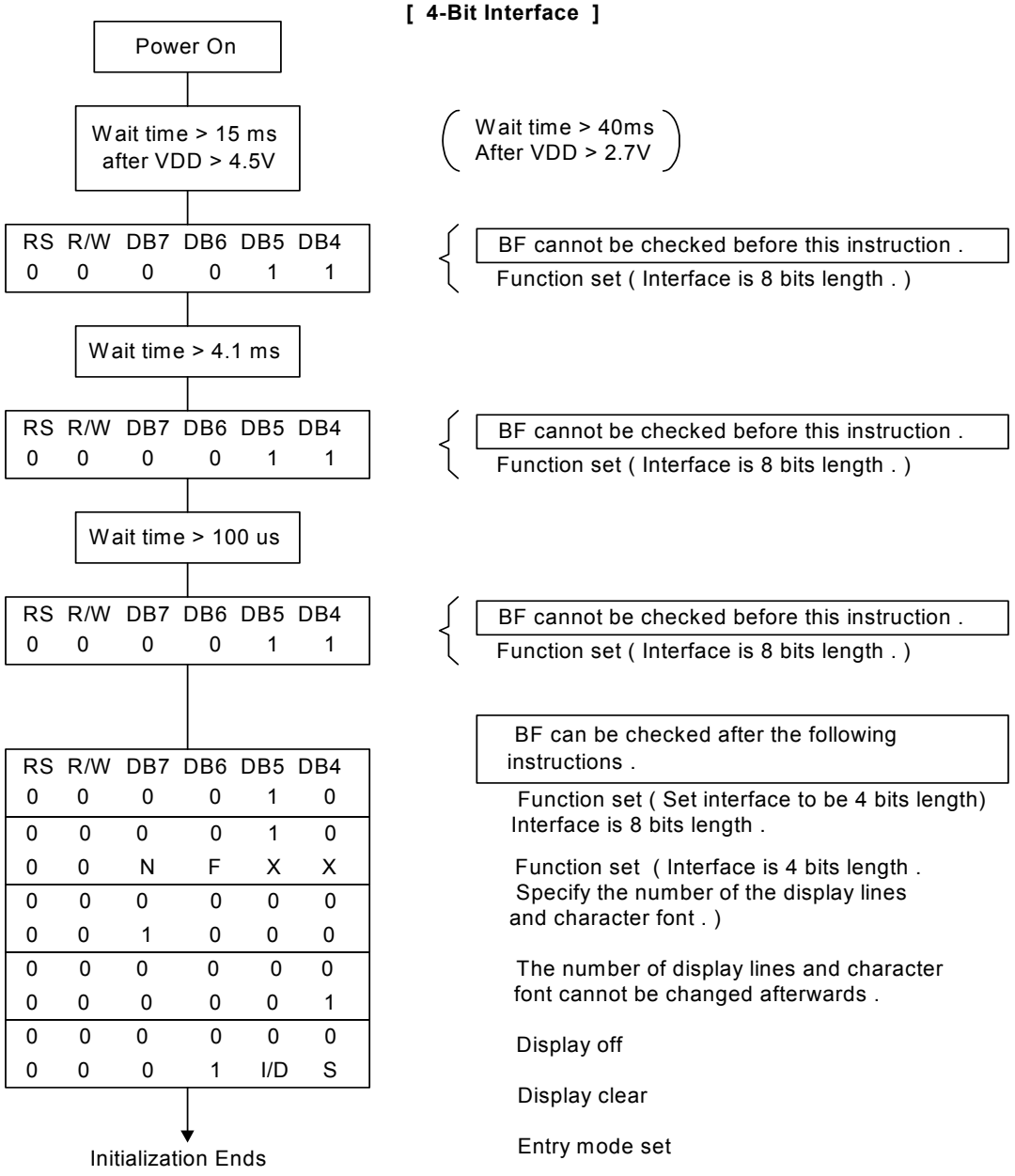
No.	Instruction	Display	Operation
12	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	:	:	:
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

5.7. Reset Function

At power on, SPLC780C starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows:

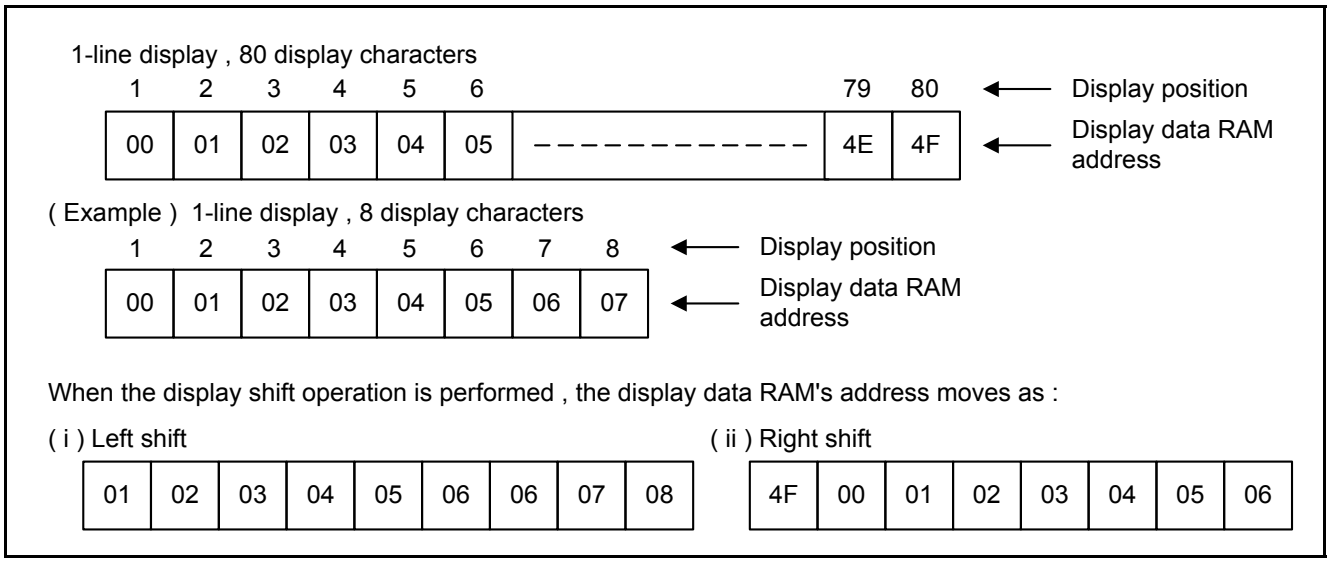


[4-Bit Interface]



5.8. Display Data RAM (DD RAM)

The 80-bit DD RAM is normally used for storing display data. Those DD RAM not used for display data can be used as general data RAM. Its address is configured in the Address Counter. The relationships between Display Data RAM Address and LCD's position are depicted as follows.



5.9. Timing Generation Circuit

The timing generating circuit is able to generate timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are generated independently.

5.10. LCD Driver Circuit

Total of 16 commons and 40 segments signal drivers are valid in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals output drive-waveforms and the others still output unselected waveforms.

5.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dots or 5 x 10 dots character patterns. It also can generate 192's 5 x 8 dots character patterns and 64's 5 x 10 dots character patterns.

5.12. Character Generator RAM (CG RAM)

Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns or 5 x 10 dots for 4-character patterns.

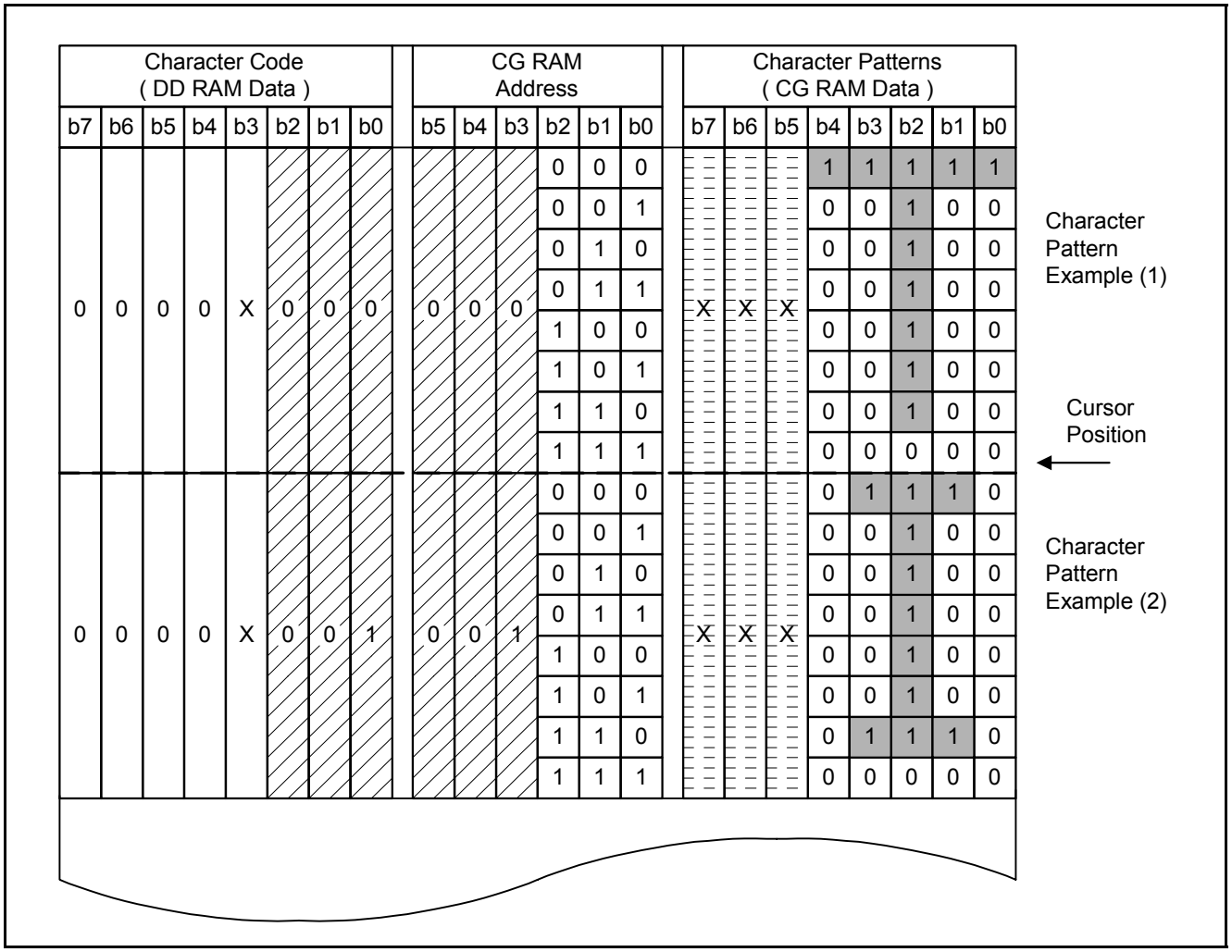
The following diagram shows the SPLC780C character patterns:

Correspondence between Character Codes and Character Patterns.

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

The relationships between Character Generator RAM Addresses, Character Generator RAM Data (character patterns), and Character Codes are depicted as follows:

5.12.1. 5 x 8 dot character patterns



Note1: It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 " : No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

5.12.2. 5 X 10 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)								
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	X	0	0	X	0	0	0	0	0	0	-	-	-	1	0	0	0	1	
										0	0	0	1	-	-	-	1	0	0	0	1	
										0	0	1	0	-	-	-	1	0	0	0	1	
										0	0	1	1	-	-	-	1	0	0	0	1	
										0	1	0	0	-	-	-	1	0	0	0	1	
										0	1	0	1	X	X	X	1	0	0	0	1	Character Pattern Example (1)
										0	1	1	0	-	-	-	1	0	0	0	1	
										0	1	1	1	-	-	-	1	0	0	0	1	
										1	0	0	0	-	-	-	1	0	0	0	1	
										1	0	0	1	-	-	-	1	1	1	1	1	Cursor Position
										1	0	1	0	-	-	-	0	0	0	0	0	←
										1	0	1	1	-	-	-	-	-	-	-	-	
										1	1	0	0	-	-	-	-	-	-	-	-	
										1	1	0	1	X	X	X	X	X	X	X	X	
										1	1	1	0	-	-	-	-	-	-	-	-	
										1	1	1	1	-	-	-	-	-	-	-	-	

Note1: ▨ It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

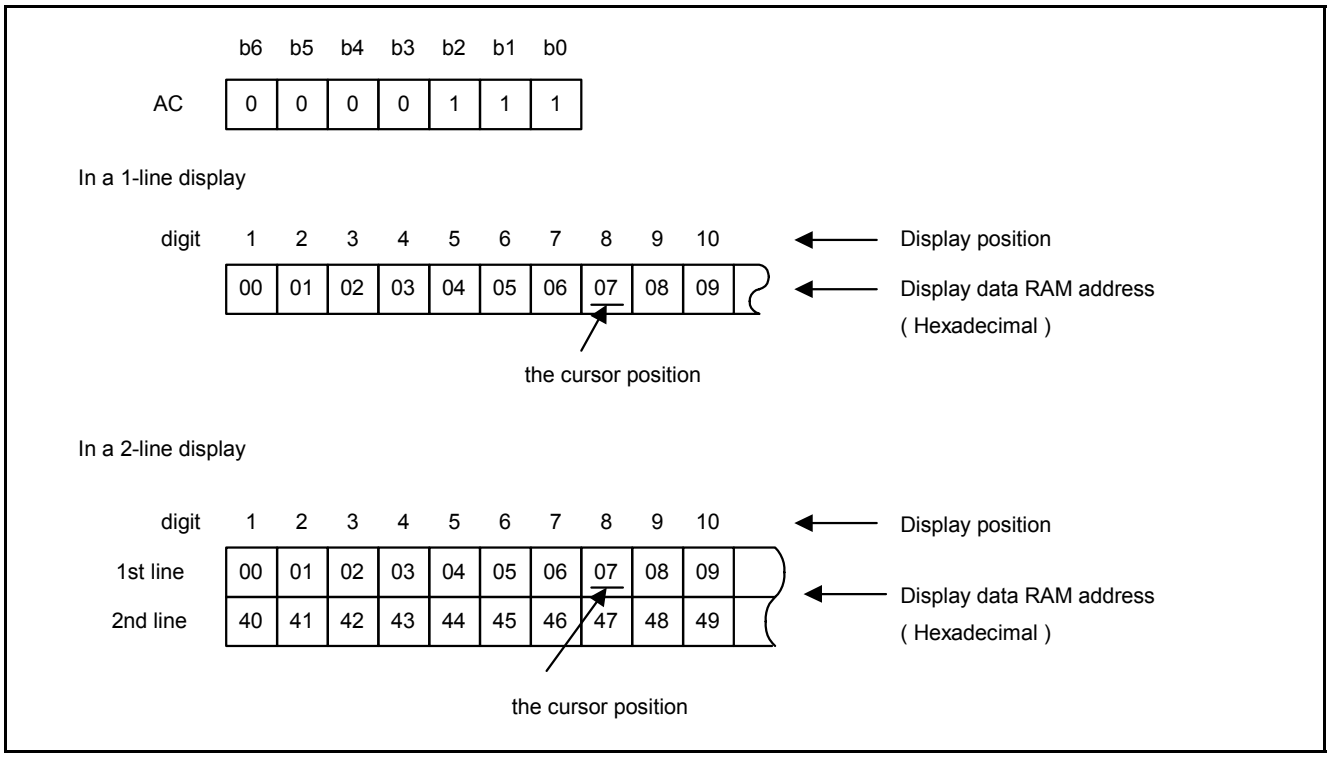
Note4: " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16,and (09) 16 can display " U " character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

5.13. Cursor/Blink Control Circuit

This circuit generates the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the Display Data RAM Address defined in the Address Counter. When the Address Counter is (07) 16, the cursor position is shown as belows:



5.14. Interfacing to MPU

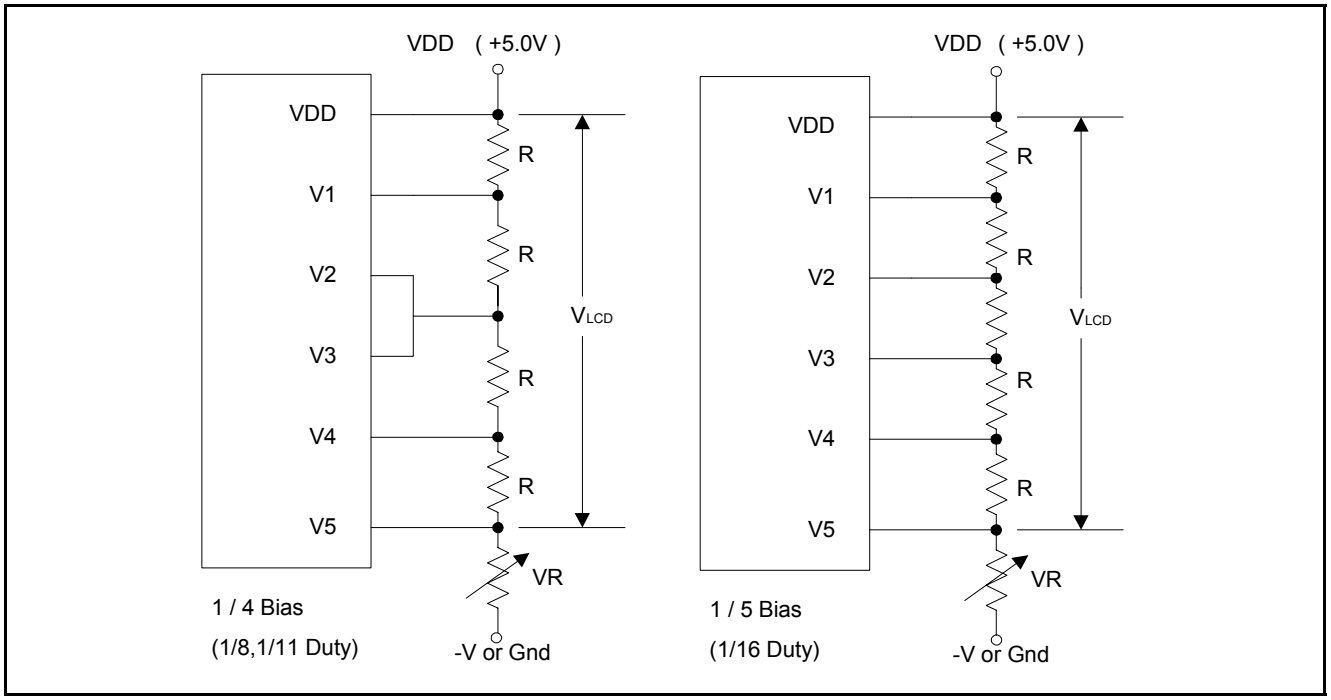
There are two types of data operations: 4-bit and 8-bit operations. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4-busline (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4-busline (for 8-bit operation, DB3 to DB0). For 8-bit MPU, the 8-bit data is transferred by 8-buslines (DB0 to DB7).

5.15. Supply Voltage for LCD Drive

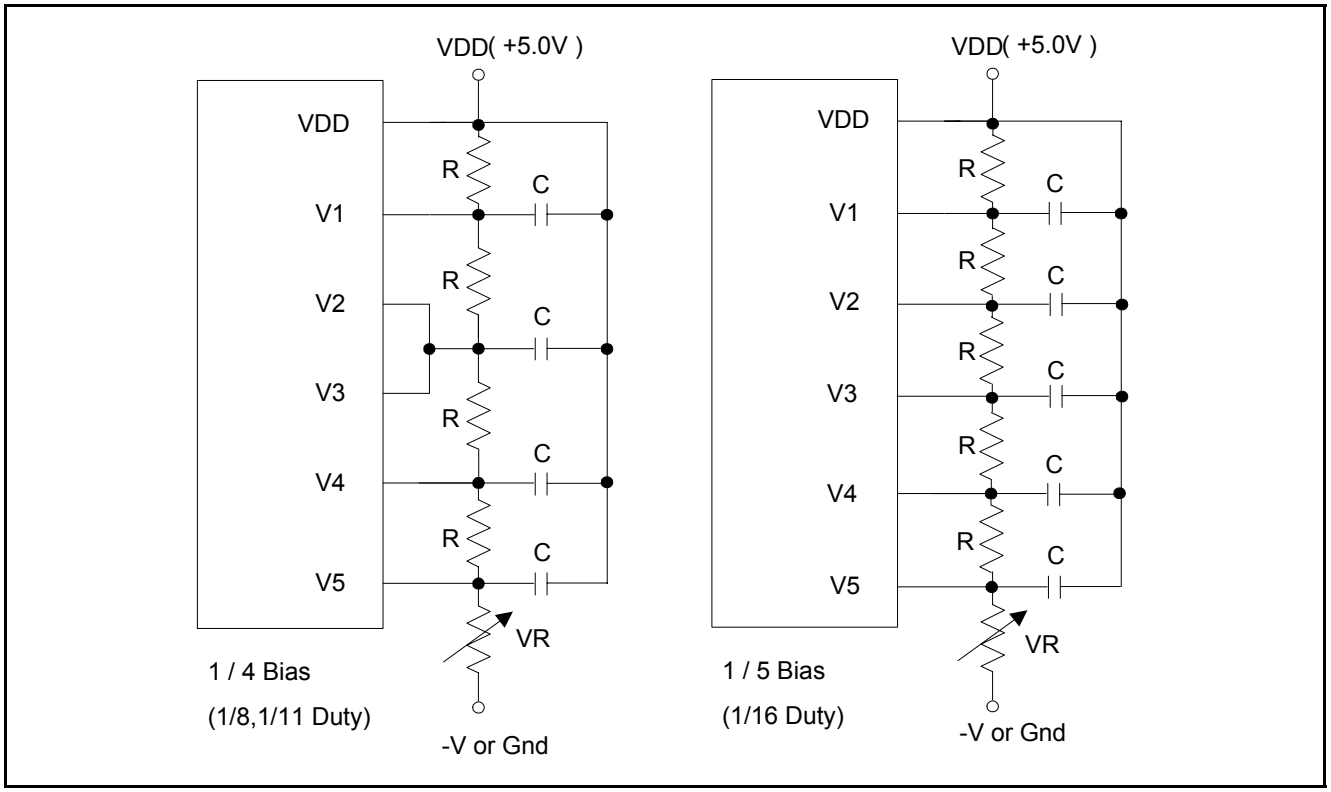
Different voltages can be supplied to SPLC780C's pins (V5 - 1) for obtaining LCD drive-waveform. The relationships between bias, duty factor and supply voltages are shown as belows:

Duty Factor / Supply Voltage	1/8, 1/11	1/16
	1/4	1/5
V1	VDD – 1/4 V_{LCD}	VDD – 1/5 V_{LCD}
V2	VDD – 1/2 V_{LCD}	VDD – 2/5 V_{LCD}
V3	VDD – 1/2 V_{LCD}	VDD – 3/5 V_{LCD}
V4	VDD – 3/4 V_{LCD}	VDD – 4/5 V_{LCD}
V5	VDD – V_{LCD}	VDD – V_{LCD}

5.15.1. The power connections for LCD (1/4 Bias, 1/5 Bias) are shown belows:



The bypass-capacitor improves the LCD display quality.



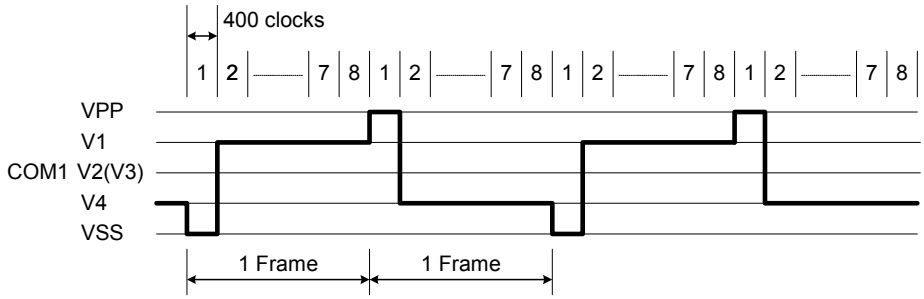
The bias voltage must have the following relations:

VDD > V1 > V2 ≧ V3 > V4 > V5.

5.15.2. The relationship between LCD frame's frequency and oscillator's frequency.

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

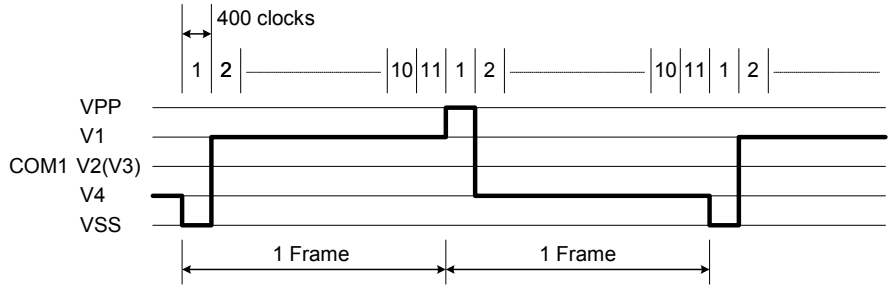
5.15.2.1. 1/8 Duty, TYPE-B waveform



1 frame = 4(μs) x 400 x 8 = 12800(μs) = 12.8ms

$$\text{Frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

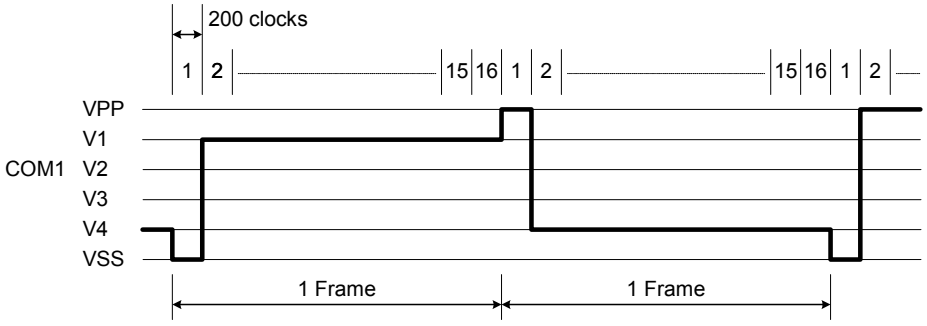
5.15.2.2. 1/11 Duty, TYPE-B waveform



1 frame = 4(μs) x 400 x 11 = 17600(μs) = 17.6ms

$$\text{Frame frequency} = \frac{1}{17.6(\text{ms})} = 56.8(\text{Hz})$$

5.15.2.3. 1/16 Duty, TYPE-B waveform



1 frame = 4(μs) x 200 x 16 = 12800(μs) = 12.8ms

$$\text{Frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

5.16. REGISTER --- IR (Instruction Register) and DR (Data Register)

SPLC780C contains two 8-bit registers: Instruction Register (IR) and Data Register (DR). Using combinations of the RS pin and the R/W pin selects the IR and DR, see below:

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and Address Counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

The IR can be written by MPU, but it cannot be read by MPU.

5.17. Busy Flag (BF)

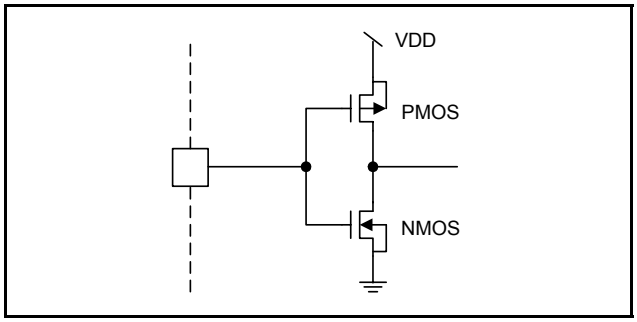
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag =1, SPLC780C is in busy state and does not accept any instruction until the busy flag = 0.

5.18. Address Counter (AC)

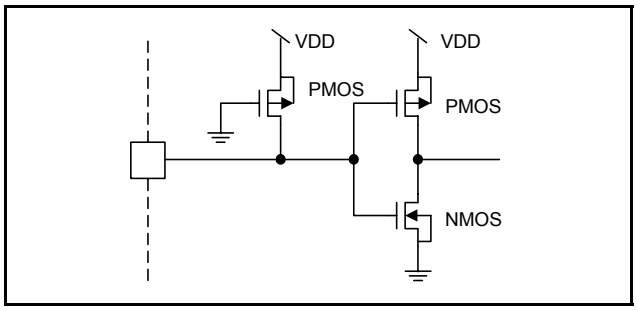
The Address Counter assigns addresses to Display Data RAM and Character Generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing to/reading from Display Data RAM or Character Generator RAM, AC is automatically incremented by one (or decremented by one). The contents of AC are output to DB0 - DB6 when RS = 0 and R/W = 1.

5.19. I/O Port Configuration

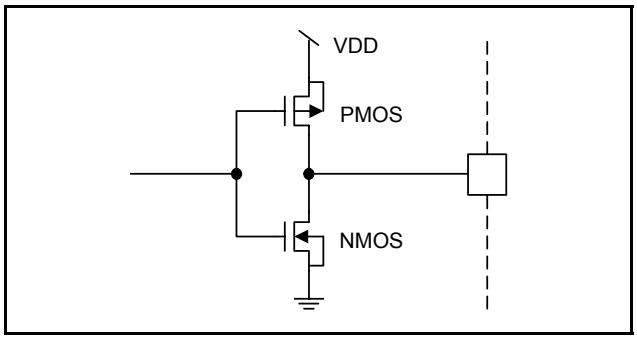
5.19.1. Input port: E



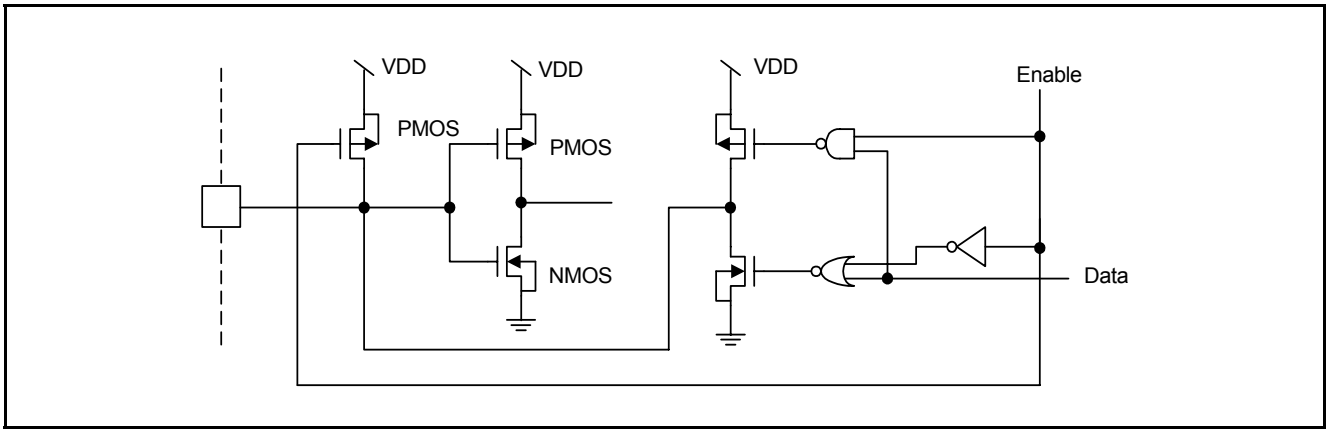
5.19.2. Input port: R / W, RS



5.19.3. Output port: CL1, CL2, M, D



5.19.4. Input / Output port: DB7 - 0



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{LCD}	VDD - 12V to VDD + 0.3V
Input Voltage Range	V_{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T_A	-30℃ to +80℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	0.2	0.4	mA	External clock (Note)
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.55	V	
Input High Voltage	V_{IH2}	0.7VDD	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	0.2VDD	V	
Input High Current	I_{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-5.0	-15	-30	μA	VDD = 3.0V
Output High Voltage (TTL)	V_{OH1}	0.75VDD	-	-	V	I_{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.2VDD	V	I_{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V_{OH2}	0.8VDD	-	-	V	I_{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.2VDD	V	I_{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R_{SEG}	-	-	30	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V_{LCD}	3.0	-	11	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 250KHz, VDD = 3.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

6.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

6.3.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190	270	350	KHz	VDD = 3.0V, Rf = 75KΩ±2%

6.3.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t r, t f	-	-	0.2	μs	

6.3.3. Write mode (Writing data from MPU to SPLC780C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_{PW}	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

6.3.4. Read mode (Reading data from SPLC780C to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_W	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

6.4. DC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	0.55	0.8	mA	External clock (Note)
Input High Voltage	V_{IH1}	2.2	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Voltage	V_{IH2}	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	1.0	V	Pin OSC1
Input High Current	I_{IH}	-2.0	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7) VDD = 5.0V
Input Low Current	I_{IL}	-20	-50	-100	μA	
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V_{OH2}	0.9VDD	-	VDD	V	I_{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.1VDD	V	I_{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R_{SEG}	-	-	30	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V_{LCD}	3.0	-	11	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 250KHz, VDD = 5.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

6.5. AC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

6.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190	270	350	KHz	VDD = 5.0V, Rf = 91KΩ±2%

6.5.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t r, t f	-	-	0.2	μs	

6.5.3. Write mode (Writing Data from MPU to SPLC780C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	80	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

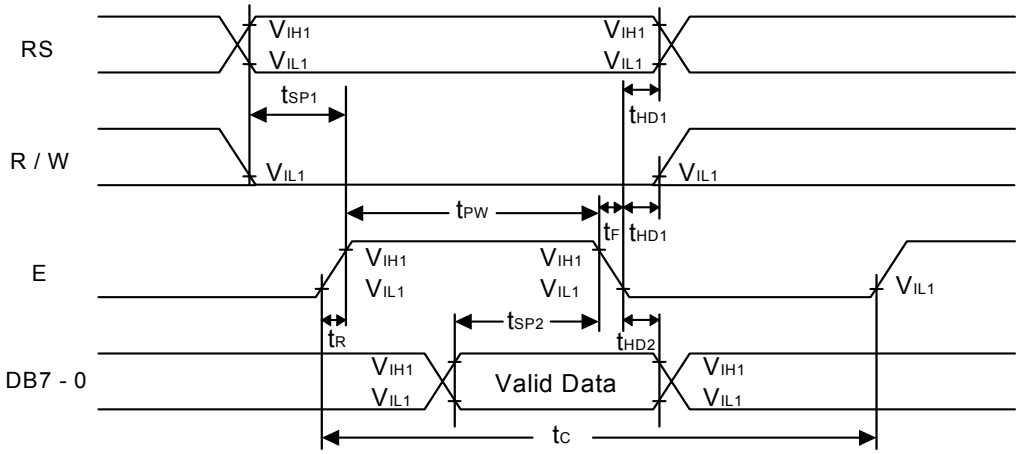
6.5.4. Read mode (Reading Data from SPLC780C to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	120	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

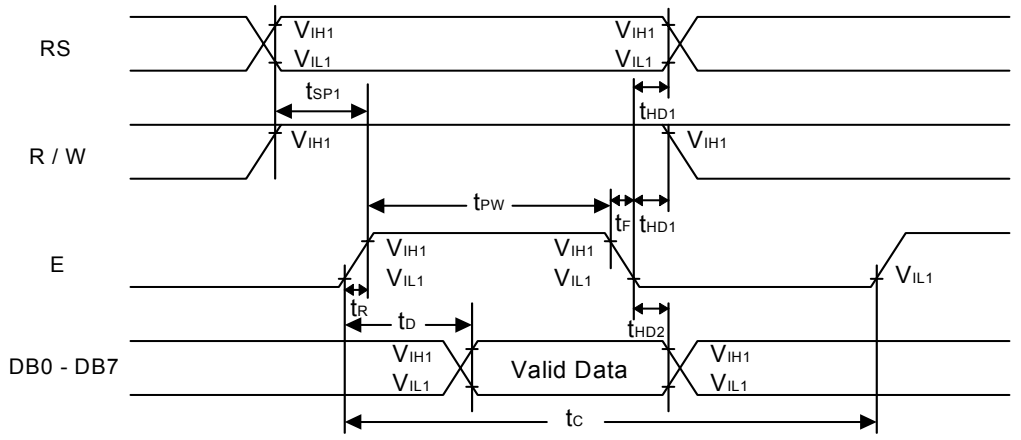
6.5.5. Interface mode with LCD Driver (SPLC100A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Clock pulse width high	t_{PWH}	800	-	-	ns	Pins: CL1, CL2
Clock pulse width low	t_{PWL}	800	-	-	ns	Pins: CL1, CL2
Clock setup time	t_{CSP}	500	-	-	ns	Pins: CL1, CL2
Data setup time	t_{DSP}	300	-	-	ns	Pins: D
Data hold time	t_{HD}	300	-	-	ns	Pins: D
M delay time	t_D	-1000	-	1000	ns	Pins: M

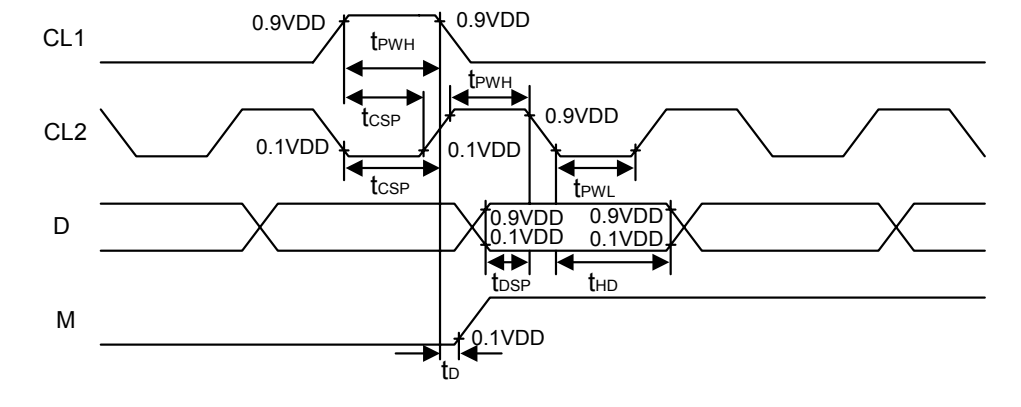
6.5.6. Write mode timing diagram (Writing Data from MPU to SPLC780C)



6.5.7. Read mode timing diagram (Reading Data from SPLC780C to MPU)



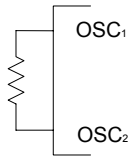
6.5.8. Interface mode with SPLC100A1 timing diagram



7. APPLICATION CIRCUITS

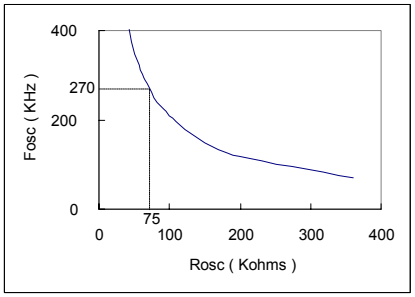
7.1. R-Oscillator

The oscillation resistor R_f is used only for the internal oscillaotr operation mode.

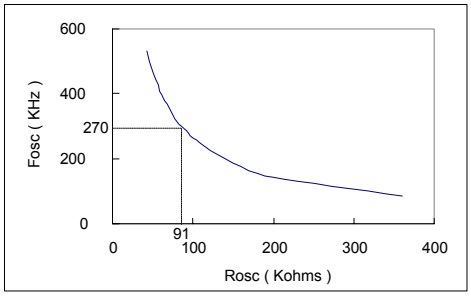


R_f : 75.0KΩ±2% (when VDD = 3.0V)
R_f : 91KΩ± 2% (when VDD = 5.0V)

Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.



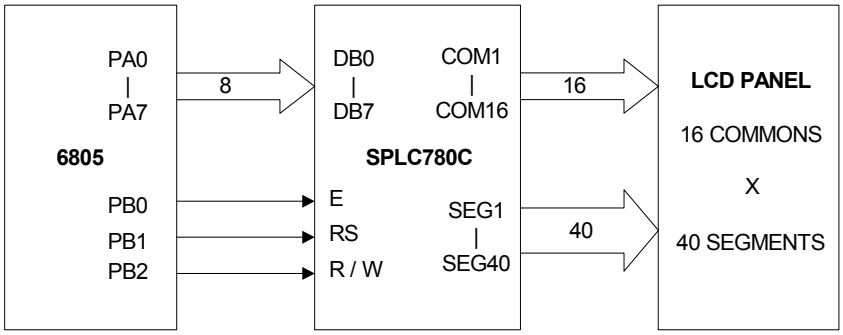
VDD = 3.0V



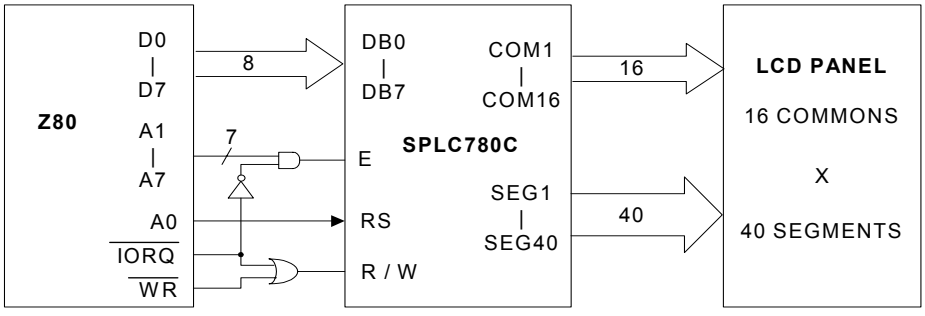
VDD = 5.0V

7.2. Interface to MPU

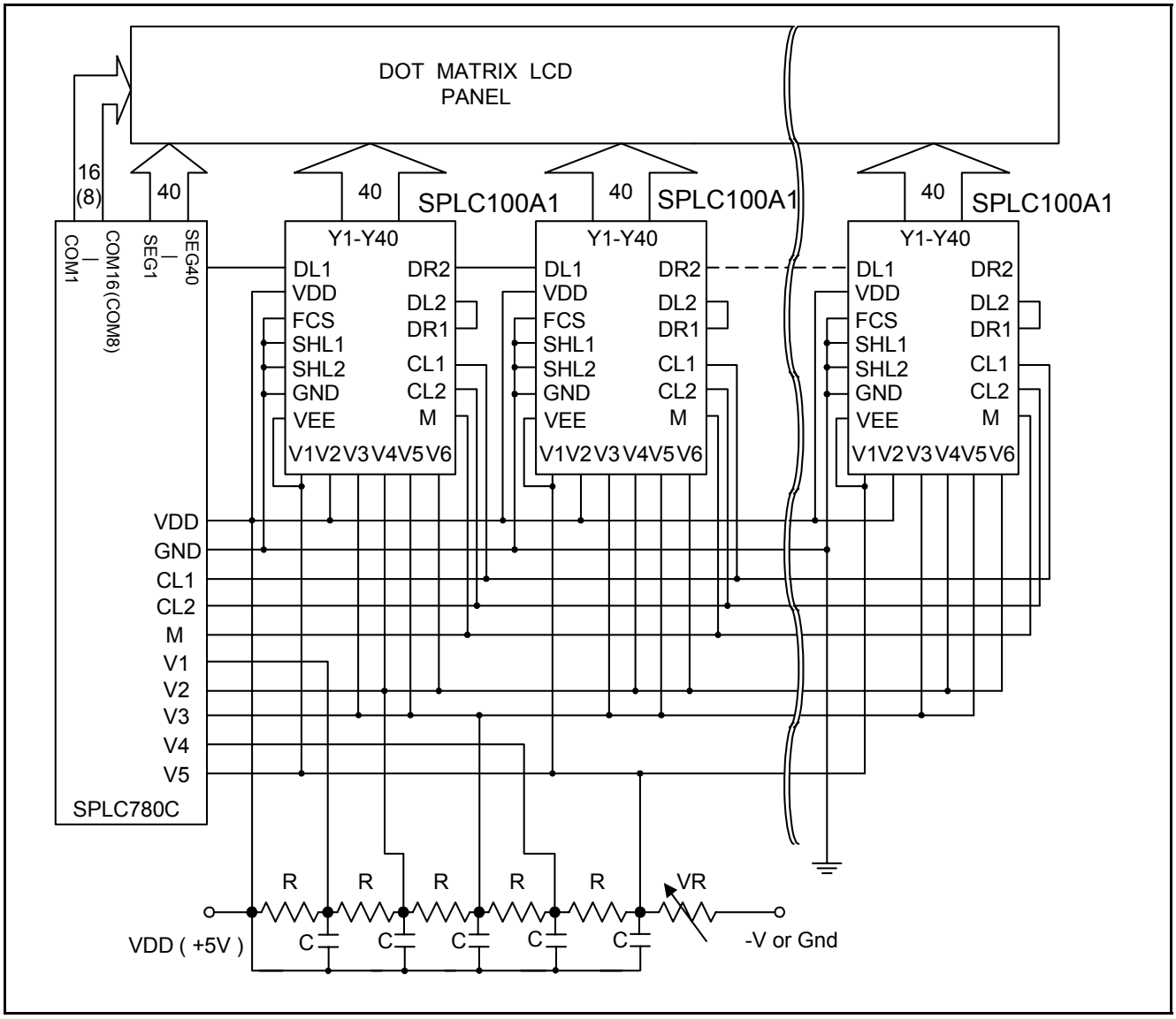
7.2.1. Interface to 8-bit MPU (6805)



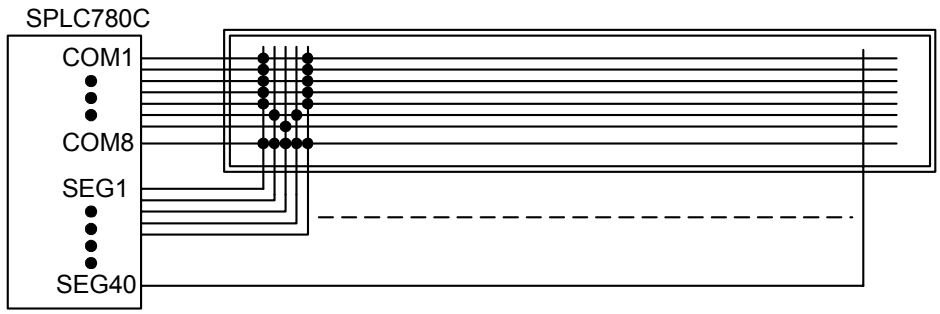
7.2.2. Interface to 8-bit MPU (Z80)



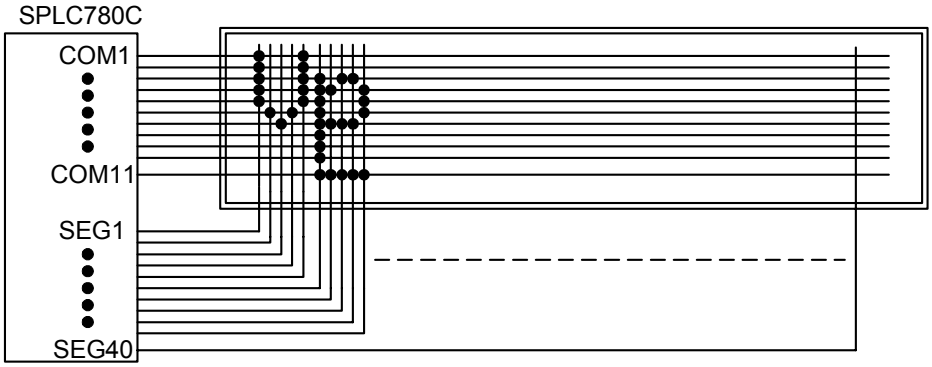
7.3. SPLC780C Application Circuit



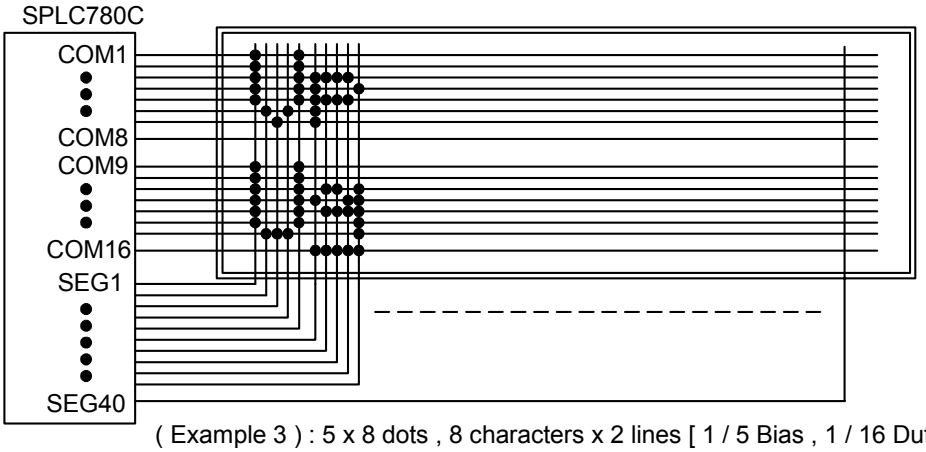
7.4. Applications for LCD



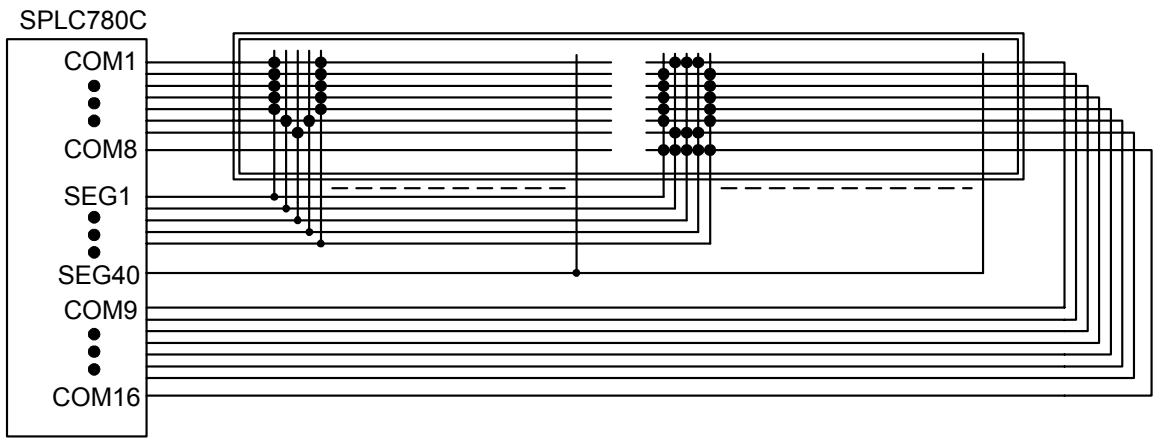
(Example 1) : 5 x 8 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]



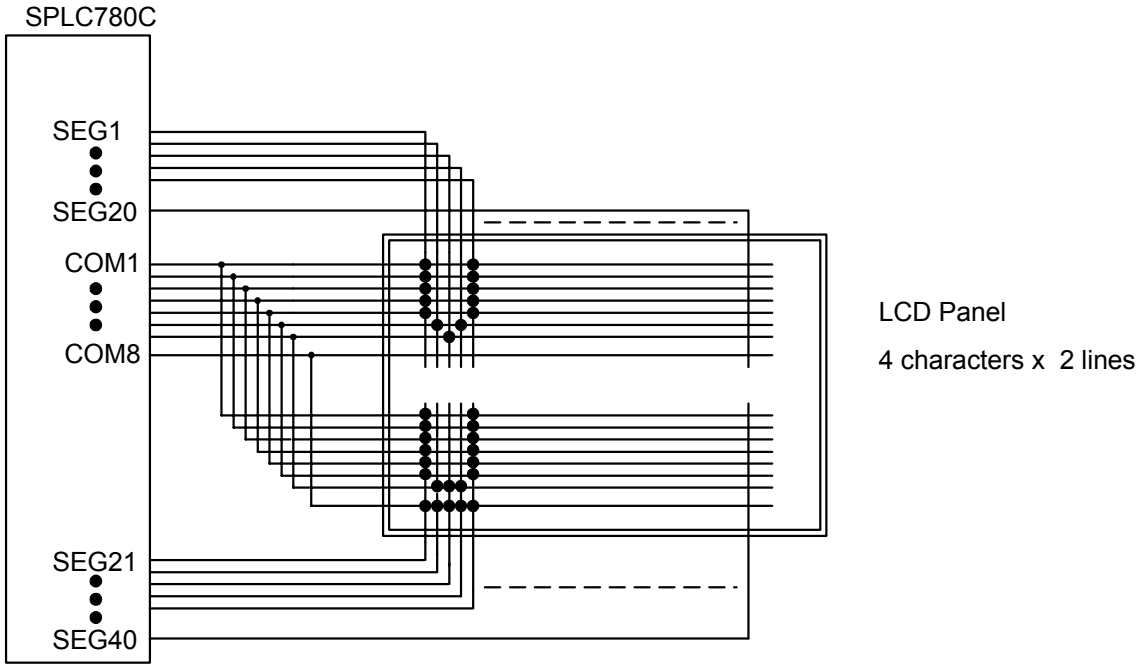
(Example 2) : 5 x 10 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]



(Example 3) : 5 x 8 dots , 8 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]



(Example 4) : 5 x 8 dots , 16 characters x 1 line [1 / 5 Bias , 1 / 16 Duty]



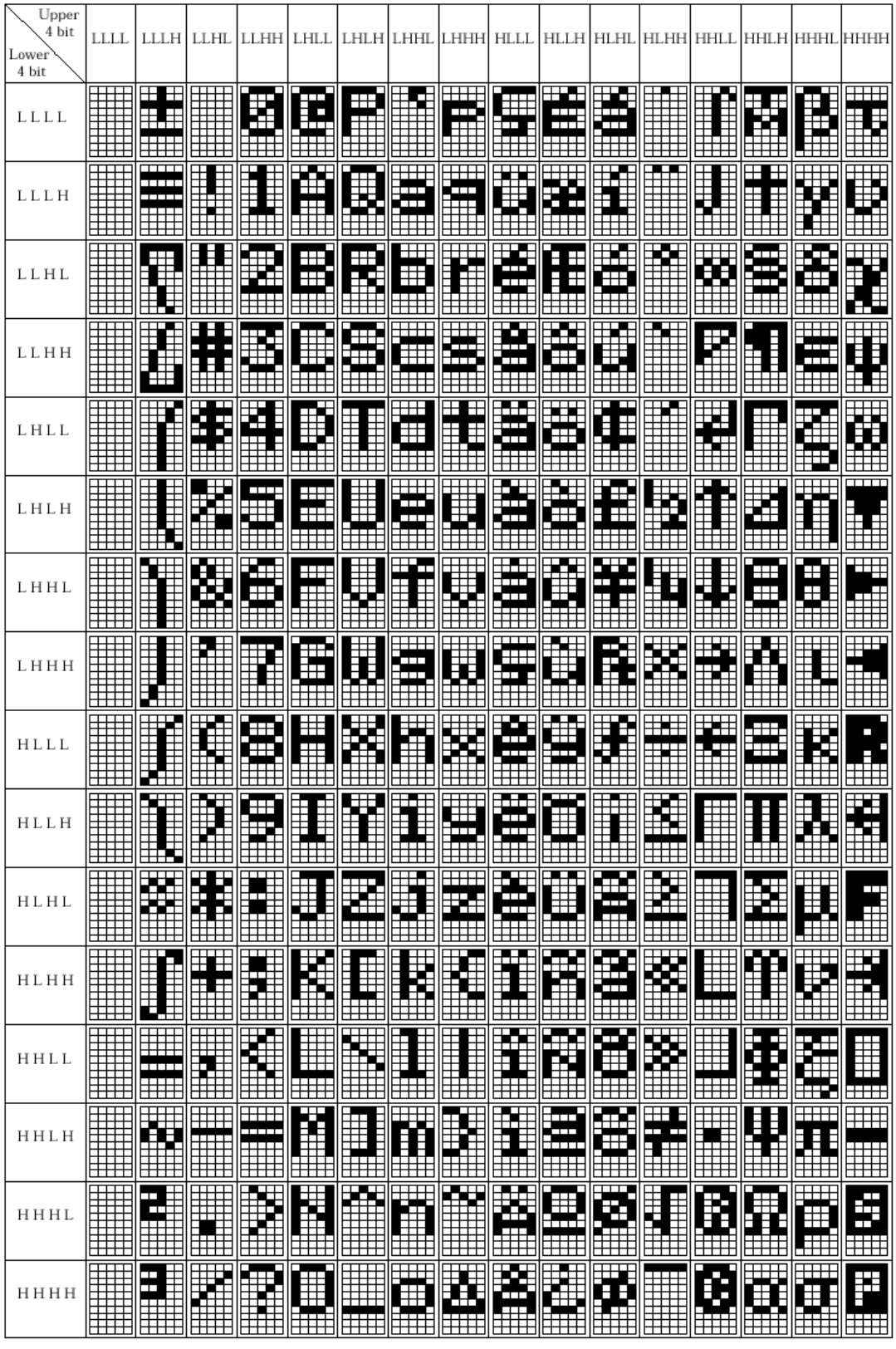
(Example 5) : 5 x 8 dots , 4 characters x 2 lines [1 / 4 Bias , 1 / 8 Duty]

8. CHARACTER GENERATOR ROM

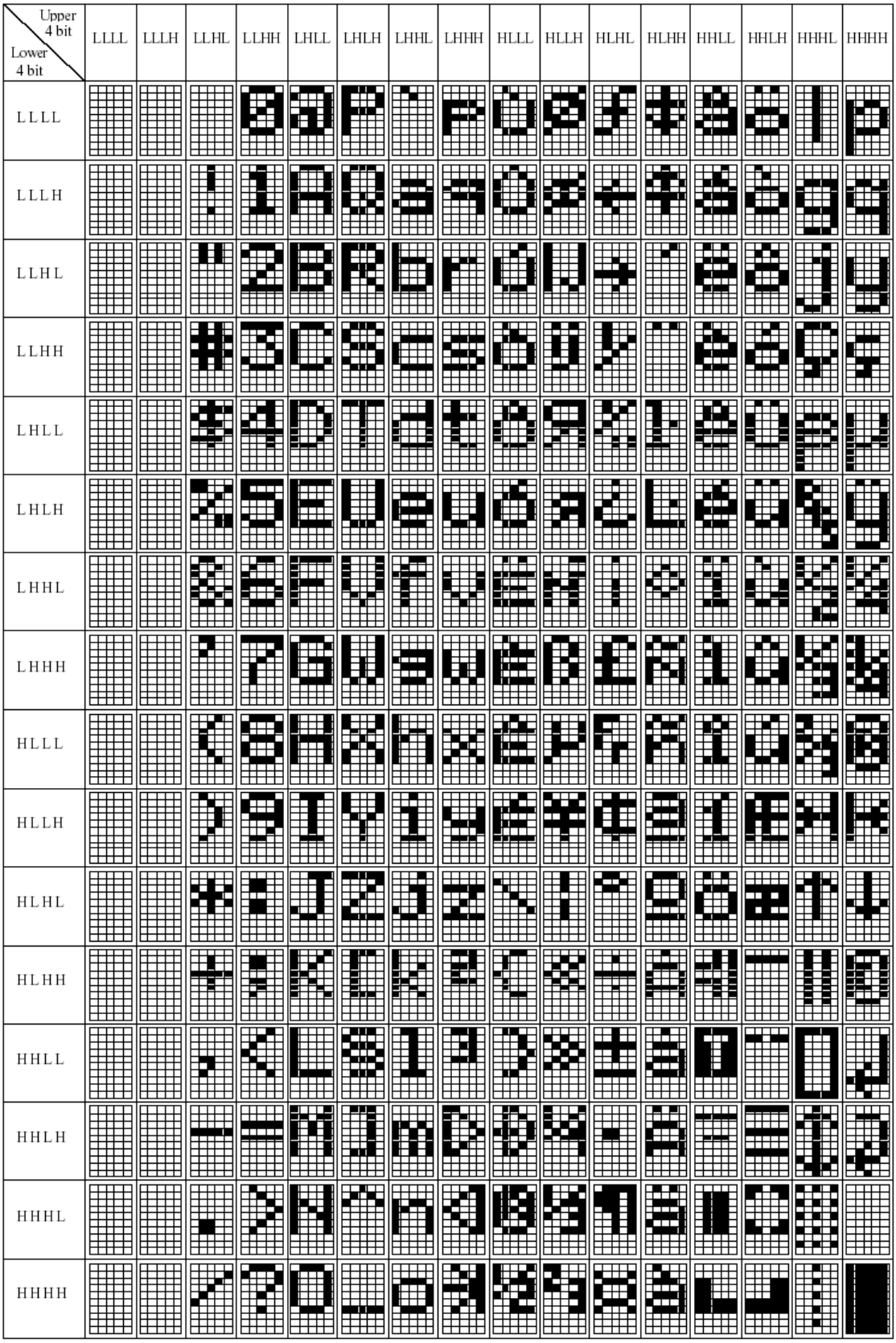
8.1. SPLC780C - 01

8.2. SPLC780C - 02

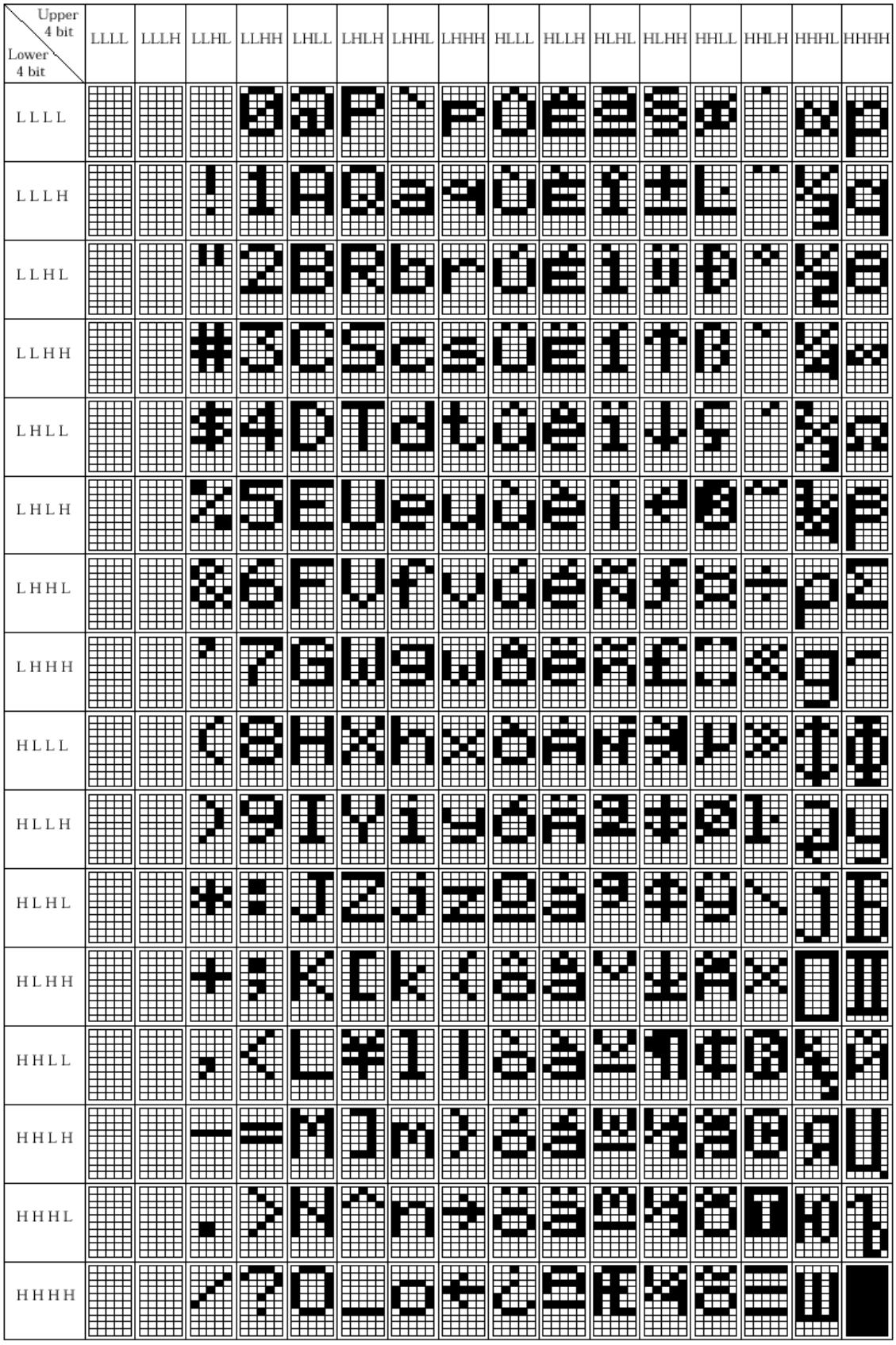
8.3. SPLC780C - 03



8.4. SPLC780C - 08

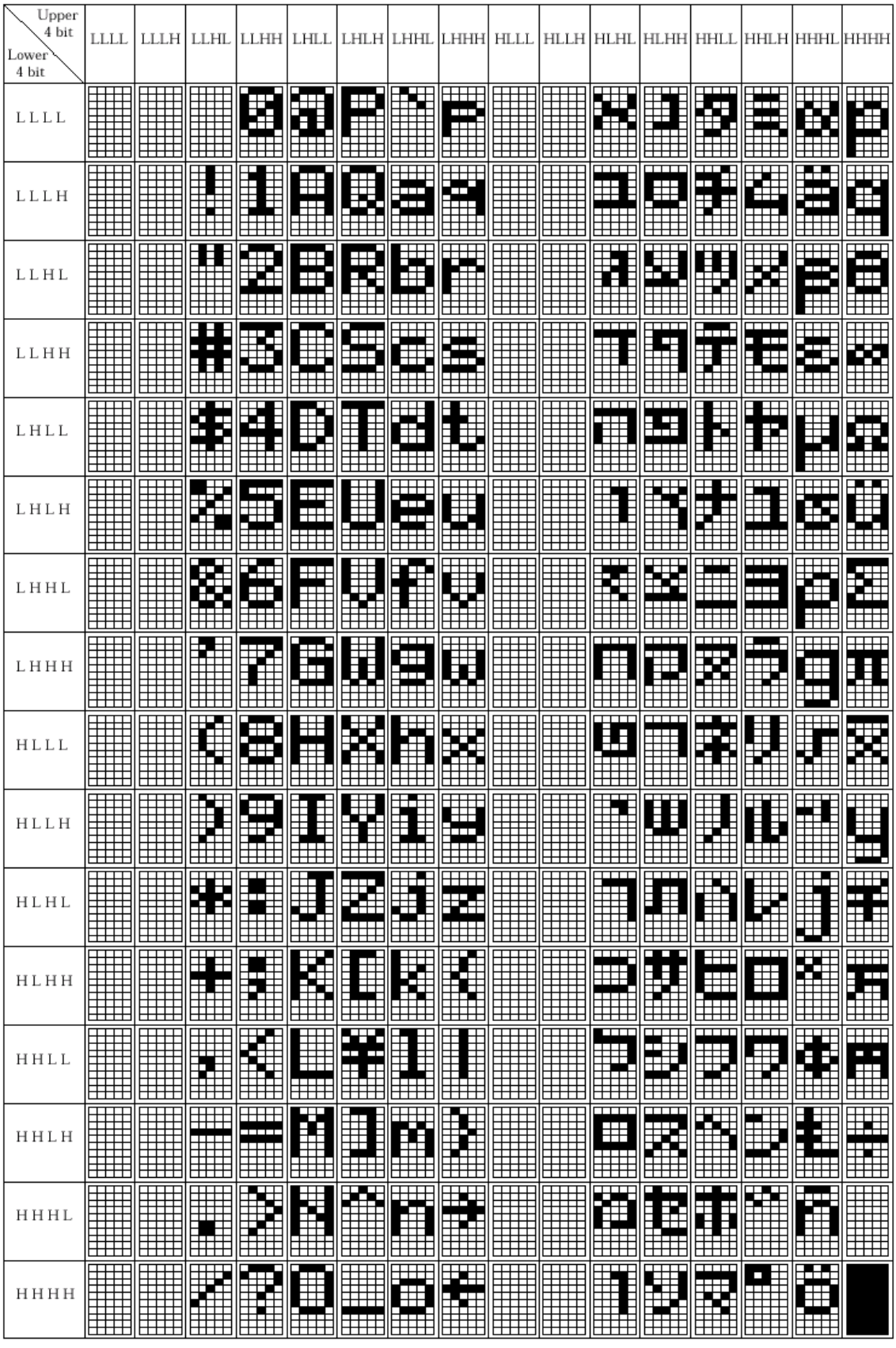


8.5. SPLC780C - 11



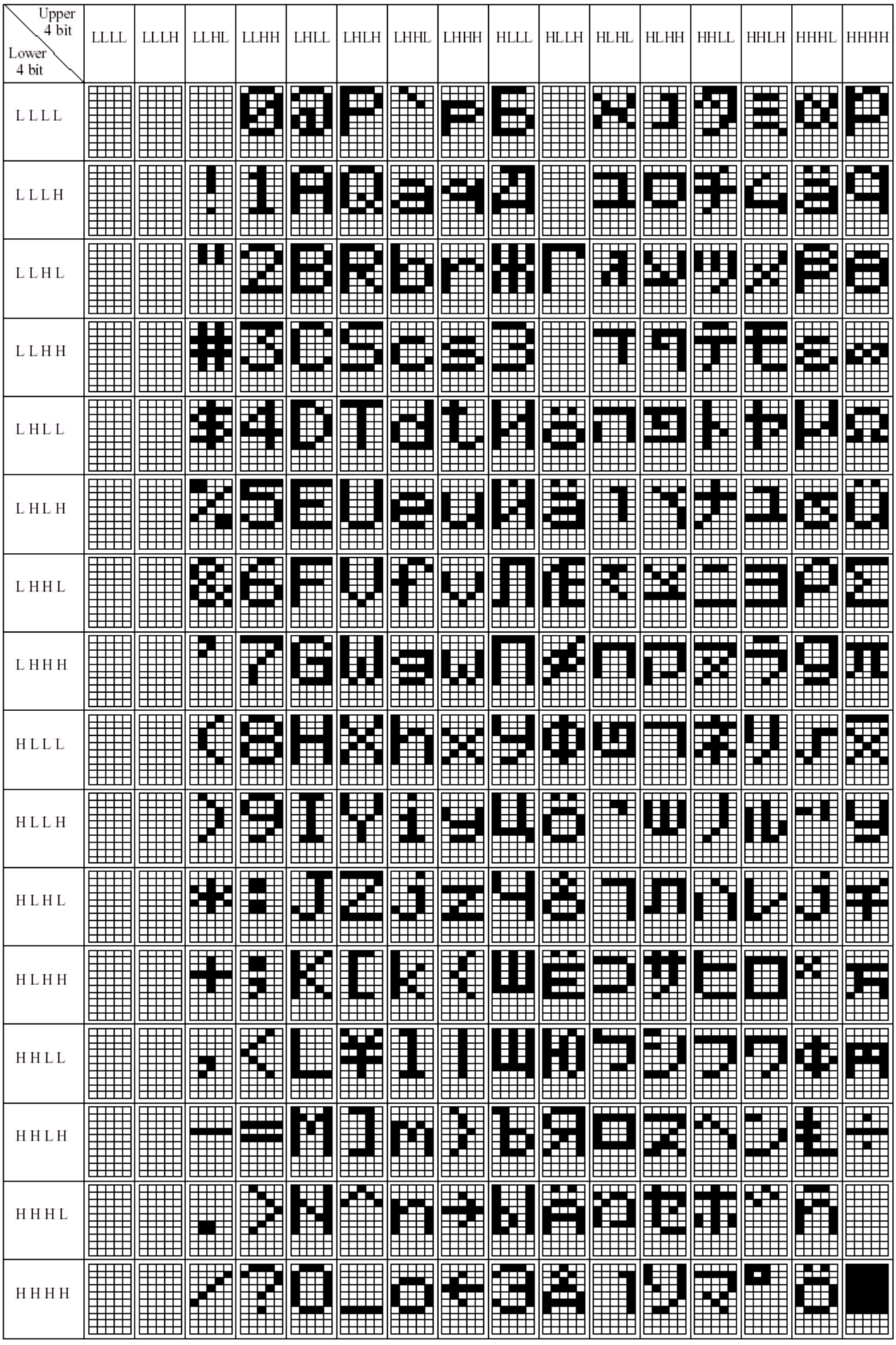
8.6. SPLC780C - 12

8.7. SPLC780C - 13

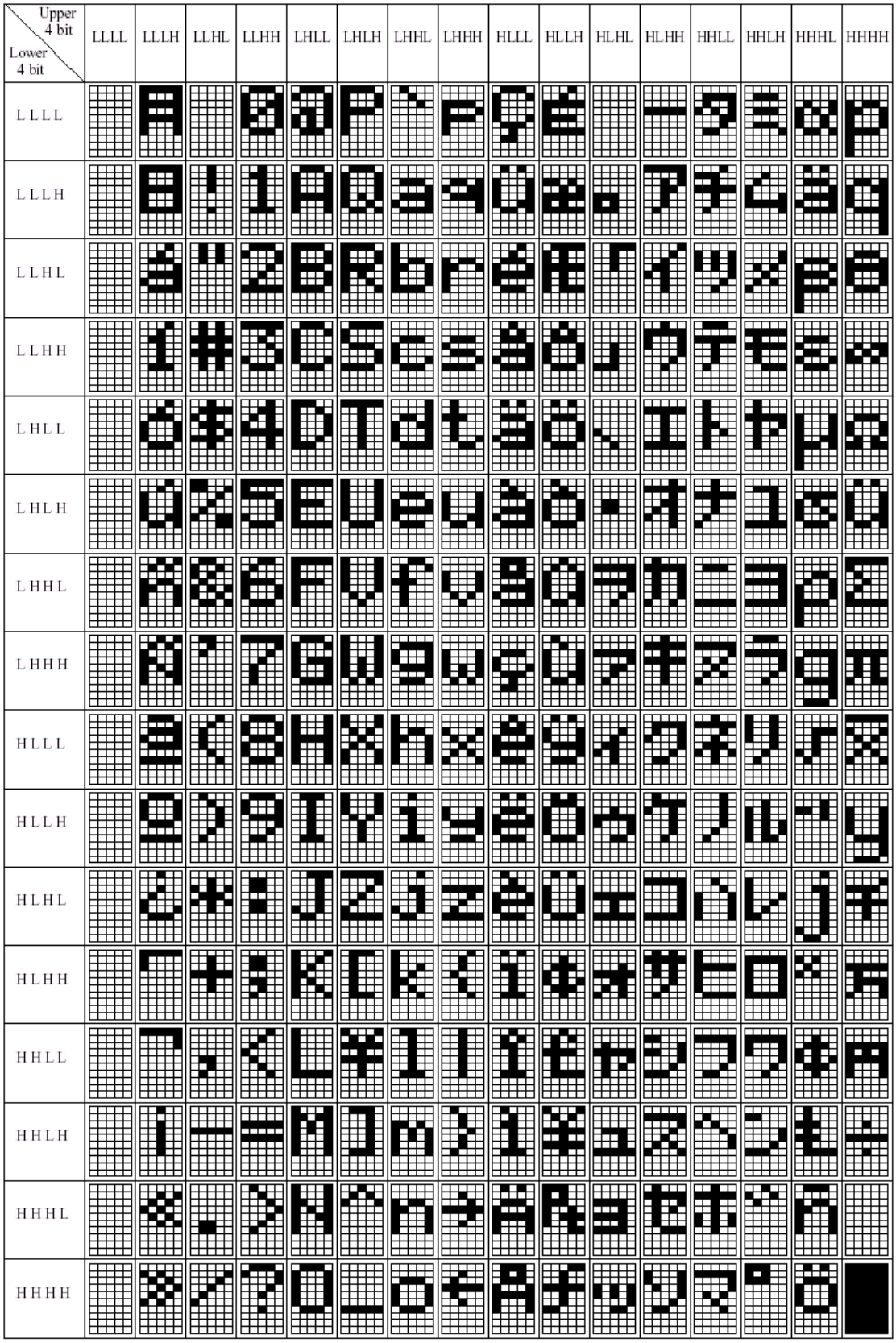


8.8. SPLC780C - 14

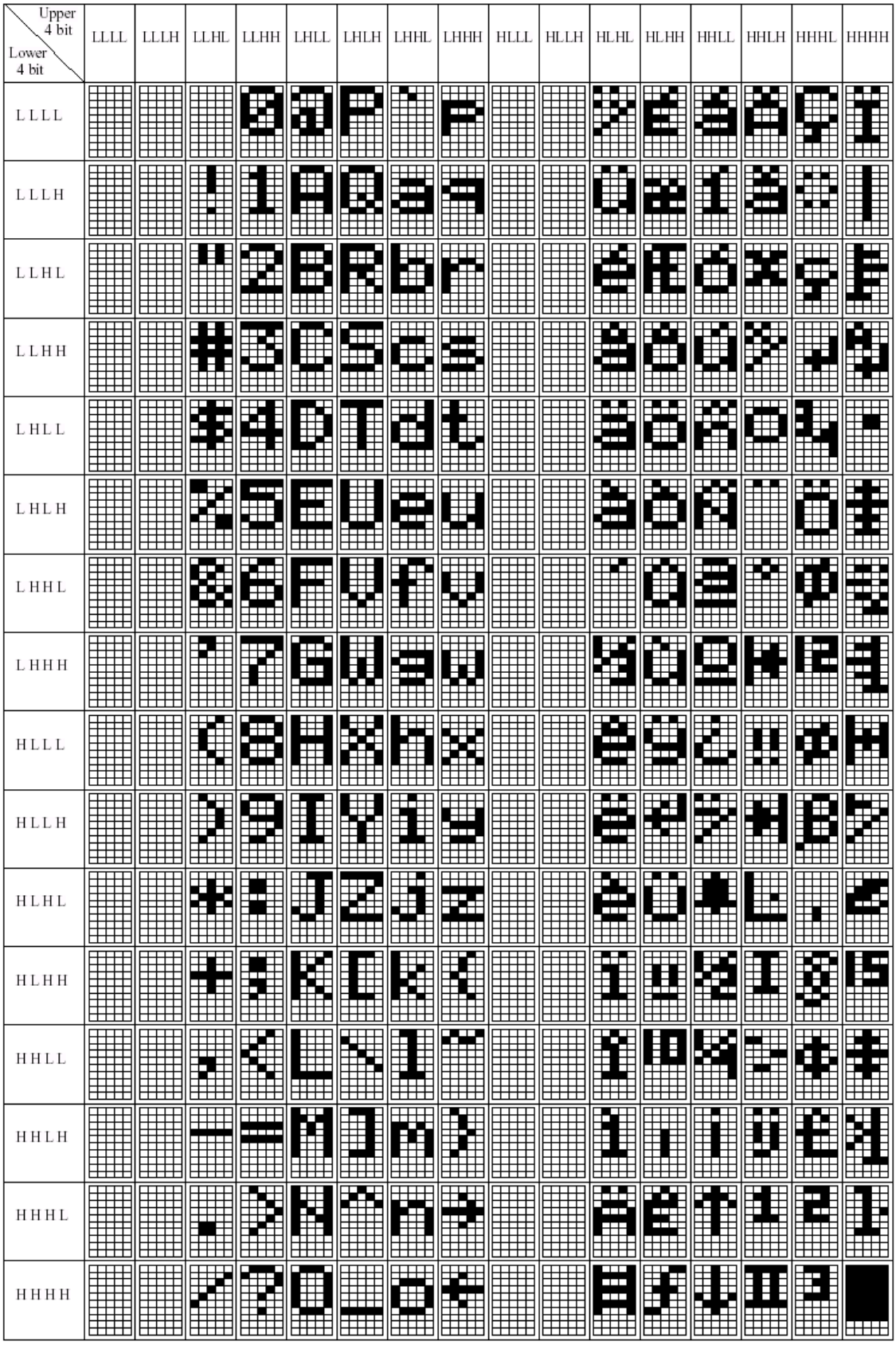
8.9. SPLC780C - 15



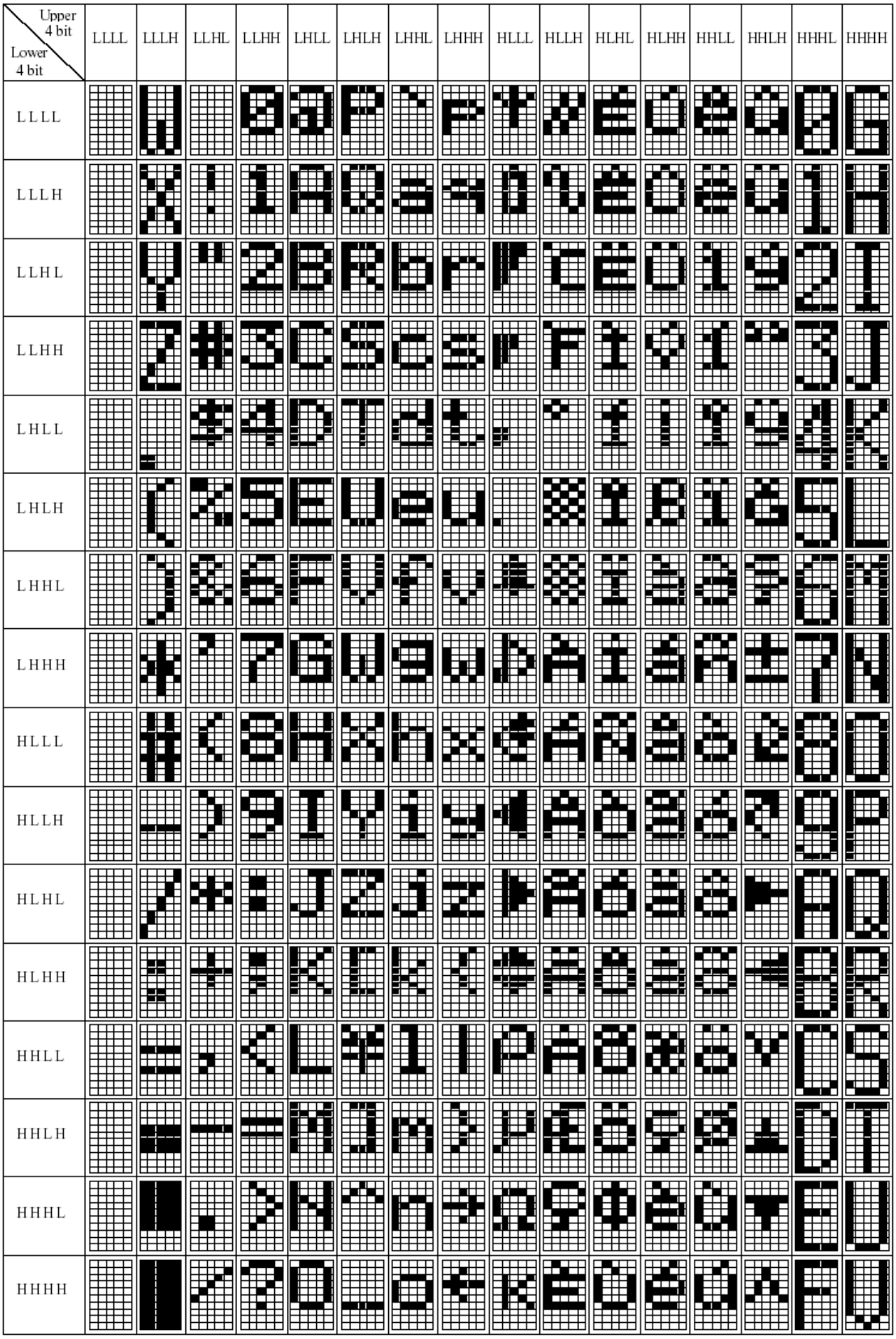
8.10. SPLC780C - 17



8.11. SPLC780C - 18

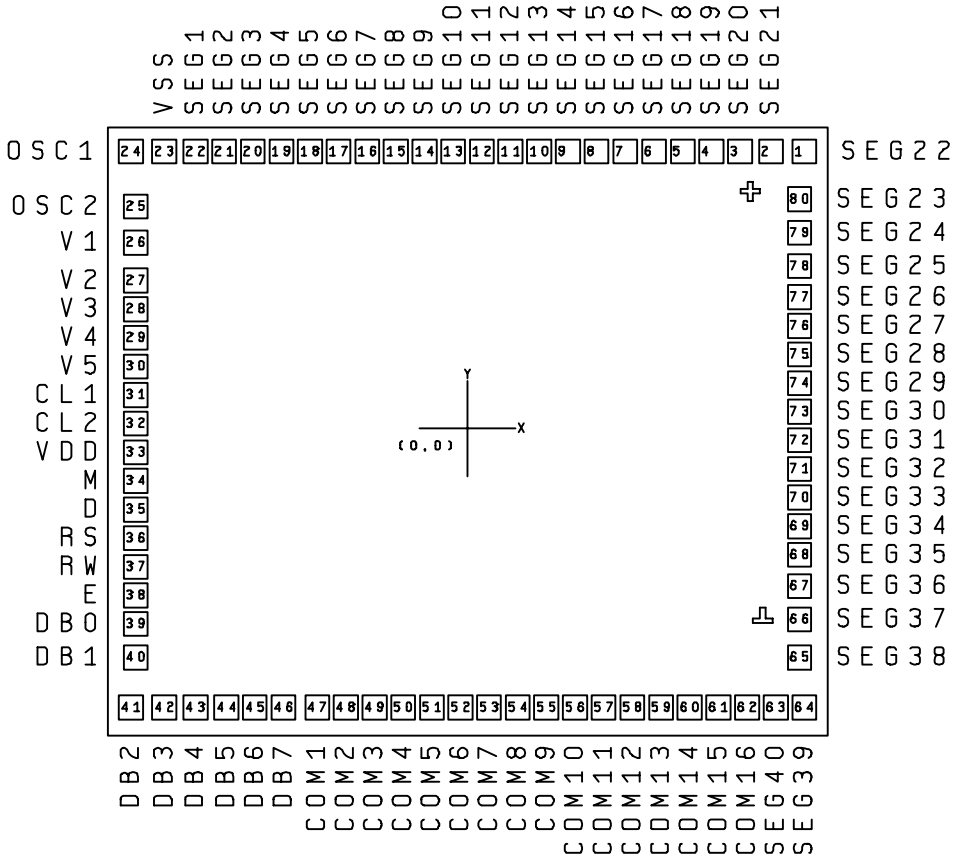


8.12. SPLC780C - 19



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3140μm x 2690μm

PAD Size: 94μm x 94μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPLC780C-nnnnV-C	Chip form
SPLC780C-nnnnV-PQ05	Package form - QFP 80L

Note1: Code number (nnnnV) is assigned for customer.

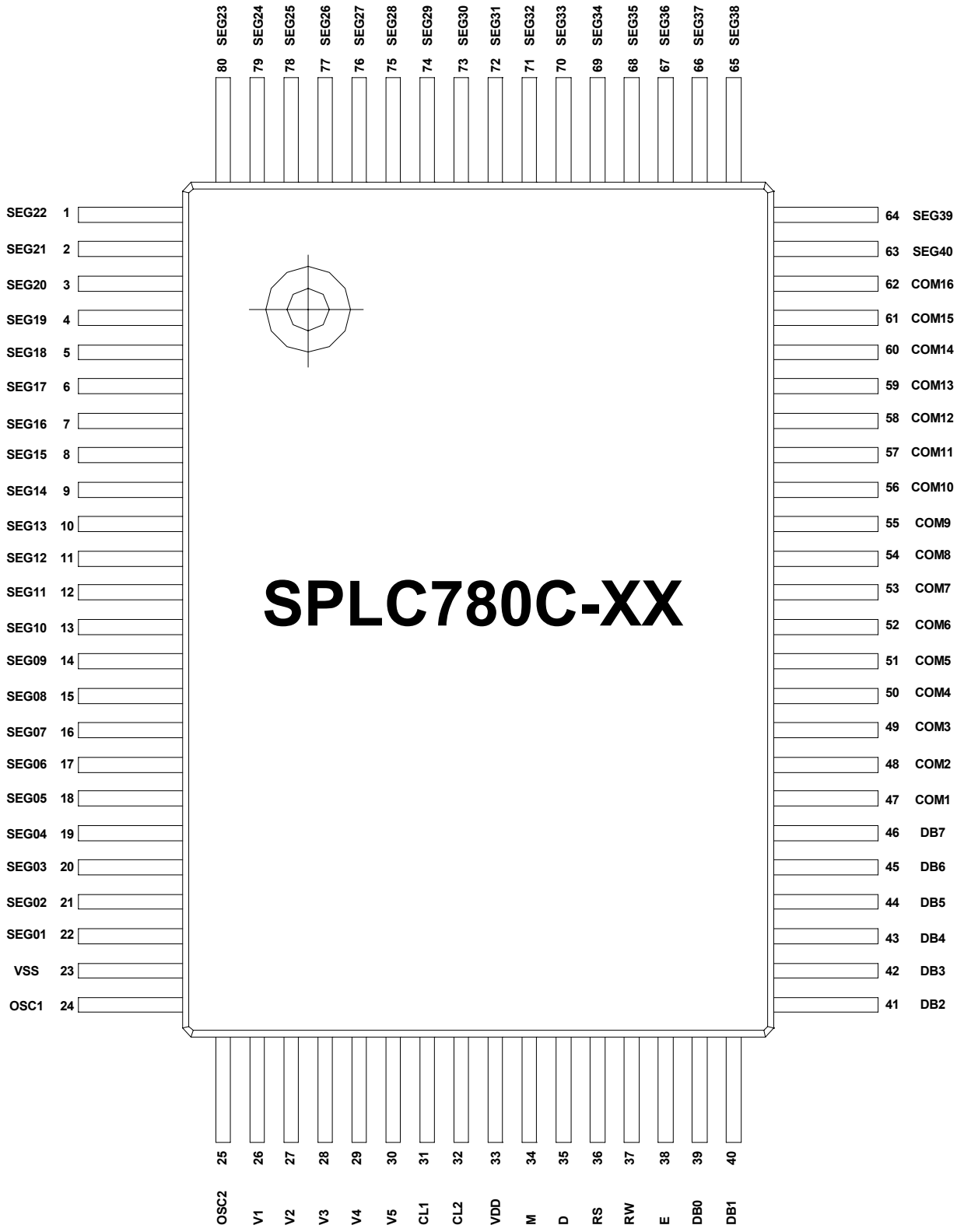
Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG22	1410	1164	41	DB2	-1410	-1165
2	SEG21	1270	1164	42	DB3	-1272	-1165
3	SEG20	1137	1164	43	DB4	-1140	-1165
4	SEG19	1017	1164	44	DB5	-1013	-1165
5	SEG18	897	1164	45	DB6	-890	-1165
6	SEG17	777	1164	46	DB7	-770	-1165
7	SEG16	657	1164	47	COM1	-637	-1165
8	SEG15	537	1164	48	COM2	-517	-1165
9	SEG14	417	1164	49	COM3	-397	-1165
10	SEG13	297	1164	50	COM4	-277	-1165
11	SEG12	177	1164	51	COM5	-157	-1165
12	SEG11	57	1164	52	COM6	-37	-1165
13	SEG10	-63	1164	53	COM7	83	-1165
14	SEG9	-183	1164	54	COM8	203	-1165
15	SEG8	-303	1164	55	COM9	323	-1165
16	SEG7	-423	1164	56	COM10	443	-1165
17	SEG6	-543	1164	57	COM11	563	-1165
18	SEG5	-663	1164	58	COM12	683	-1165
19	SEG4	-783	1164	59	COM13	803	-1165
20	SEG3	-903	1164	60	COM14	923	-1165
21	SEG2	-1023	1164	61	COM15	1043	-1165
22	SEG1	-1143	1164	62	COM16	1163	-1165
23	VSS	-1271	1164	63	SEG40	1283	-1165
24	OSC1	-1411	1164	64	SEG39	1410	-1165
25	OSC2	-1391	932	65	SEG38	1390	-963
26	V1	-1391	784	66	SEG37	1390	-802
27	V2	-1391	624	67	SEG36	1390	-662
28	V3	-1391	504	68	SEG35	1390	-532
29	V4	-1391	384	69	SEG34	1390	-412
30	V5	-1391	264	70	SEG33	1390	-292
31	CL1	-1391	144	71	SEG32	1390	-172
32	CL2	-1391	24	72	SEG31	1390	-52
33	VDD	-1391	-96	73	SEG30	1390	68
34	M	-1391	-216	74	SEG29	1390	188
35	D	-1391	-336	75	SEG28	1390	308
36	RS	-1391	-456	76	SEG27	1390	428
37	RW	-1391	-576	77	SEG26	1390	548
38	E	-1391	-696	78	SEG25	1390	683
39	DB0	-1391	-816	79	SEG24	1390	818
40	DB1	-1391	-955	80	SEG23	1390	963

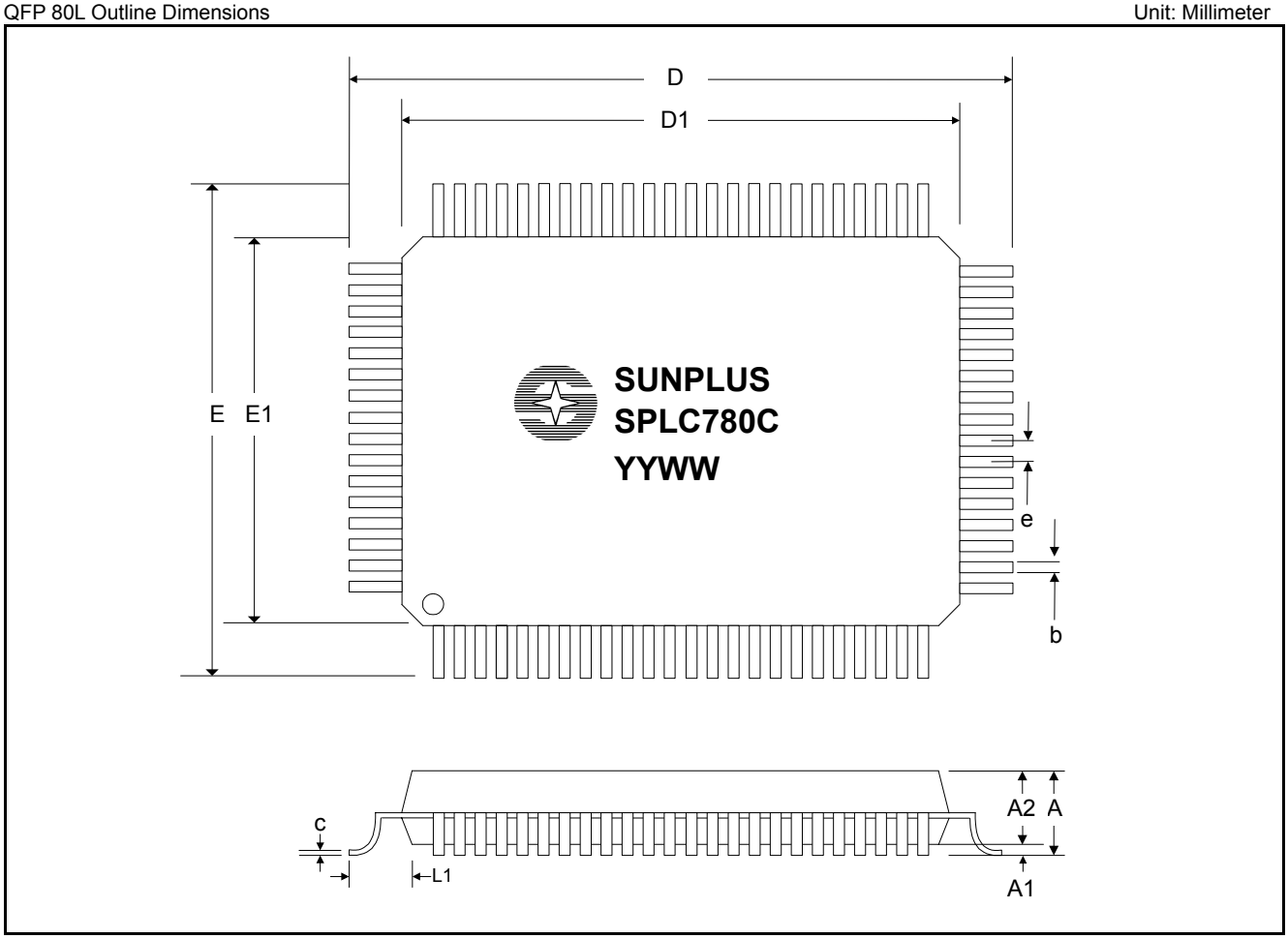
9.4. Package Configuration

QFP 80L Top View



9.5. Package Information

QFP 80L Outline Dimensions Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		0.80 REF		Millimeter
b	0.30	0.35	0.45	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Sunplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. SUNPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, SUNPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SUNPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SUNPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
JUN. 04, 2001	0.1	Original	
OCT. 02, 2001	1.0	1. Delete "*PRELIMINARY*" 2. Correct "*8.3 SPLC780C-03*" 3. Add "*8.4 SPLC780C-08*" and "*8.12 SPLC780C-19*"	 32 33, 41
JUL. 09, 2002	1.1	1. Update "*9.2 Ordering Information*" 2. Update "*9.5 Package Information*"	42 45