# Analysis:

- **2-Operands:**

  **NB:** All 2 operand instructions are the same except for cmp which has less by one mem access and two clk cycles.

| Instruction | Src | Dest | Mem Accesses | Clk Cycles |
|---|---|---|---|---|
| **ADD** | R0 | R0 | 1 | 12 |
| **ADD** | R0 | @R0 | 3 | 14 |
| **ADD** | R0 | (R0)+ | 3 | 15 |
| **ADD** | R0 | @(R0)+ | 4 | 16 |
| **ADD** | R0 | -(R0) | 3 | 15 |
| **ADD** | R0 | @-(R0) | 4 | 16 |
| **ADD** | R0 | X(R0) | 4 | 17 |
| **ADD** | R0 | @X(R0) | 5 | 18 |
| **ADD** | @R0 | R0 | 2 | 13 |
| **ADD** | @R0 | @R0 | 4 | 15 |
| **ADD** | @R0 | (R0)+ | 4 | 16 |
| **ADD** | @R0 | @(R0)+ | 5 | 17 |
| **ADD** | @R0 | -(R0) | 4 | 16 |
| **ADD** | @R0 | @-(R0) | 5 | 17 |
| **ADD** | @R0 | X(R0) | 5 | 18 |
| **ADD** | @R0 | @X(R0) | 6 | 19 |
| **ADD** | (R0)+ | R0 | 2 | 14 |
| **ADD** | (R0)+ | @R0 | 4 | 16 |
| **ADD** | (R0)+ | (R0)+ | 4 | 17 |
| **ADD** | (R0)+ | @(R0)+ | 5 | 18 |
| **ADD** | (R0)+ | -(R0) | 4 | 17 |
| **ADD** | (R0)+ | @-(R0) | 5 | 18 |
| **ADD** | (R0)+ | X(R0) | 5 | 19 |
| **ADD** | (R0)+ | @X(R0) | 6 | 20 |
| **ADD** | @(R0)+ | R0 | 3 | 15 |
| **ADD** | @(R0)+ | @R0 | 5 | 17 |
| **ADD** | @(R0)+ | (R0)+ | 5 | 18 |
| **ADD** | @(R0)+ | @(R0)+ | 6 | 19 |
| **ADD** | @(R0)+ | -(R0) | 5 | 18 |

| | | | | |
|---|---|---|---|---|
| **ADD** | @(R0)+ | @-(R0) | 6 | 19 |
| **ADD** | @(R0)+ | X(R0) | 6 | 20 |
| **ADD** | @(R0)+ | @X(R0) | 7 | 21 |
| **ADD** | -(R0) | R0 | 2 | 14 |
| **ADD** | -(R0) | @R0 | 4 | 16 |
| **ADD** | -(R0) | (R0)+ | 4 | 17 |
| **ADD** | -(R0) | @(R0)+ | 5 | 18 |
| **ADD** | -(R0) | -(R0) | 4 | 17 |
| **ADD** | -(R0) | @-(R0) | 5 | 18 |
| **ADD** | -(R0) | X(R0) | 5 | 19 |
| **ADD** | -(R0) | @X(R0) | 6 | 20 |
| **ADD** | @-(R0) | R0 | 3 | 15 |
| **ADD** | @-(R0) | @R0 | 5 | 17 |
| **ADD** | @-(R0) | (R0)+ | 5 | 18 |
| **ADD** | @-(R0) | @(R0)+ | 6 | 19 |
| **ADD** | @-(R0) | -(R0) | 5 | 18 |
| **ADD** | @-(R0) | @-(R0) | 6 | 19 |
| **ADD** | @-(R0) | X(R0) | 6 | 20 |
| **ADD** | @-(R0) | @X(R0) | 7 | 21 |
| **ADD** | X(R0) | R0 | 3 | 16 |
| **ADD** | X(R0) | @R0 | 5 | 18 |
| **ADD** | X(R0) | (R0)+ | 5 | 19 |
| **ADD** | X(R0) | @(R0)+ | 6 | 20 |
| **ADD** | X(R0) | -(R0) | 5 | 19 |
| **ADD** | X(R0) | @-(R0) | 6 | 20 |
| **ADD** | X(R0) | X(R0) | 6 | 21 |
| **ADD** | X(R0) | @X(R0) | 7 | 22 |
| **ADD** | @X(R0) | R0 | 4 | 17 |
| **ADD** | @X(R0) | @R0 | 6 | 19 |
| **ADD** | @X(R0) | (R0)+ | 6 | 20 |
| **ADD** | @X(R0) | @(R0)+ | 7 | 21 |
| **ADD** | @X(R0) | -(R0) | 6 | 20 |
| **ADD** | @X(R0) | @-(R0) | 7 | 21 |
| **ADD** | @X(R0) | X(R0) | 7 | 22 |
| **ADD** | @X(R0) | @X(R0) | 8 | 23 |
| | | | SUM | 1144 |

- **1-Operand:**

  **NB:** All 1 operand instructions are the same except for branch

| Inst | Operand | Memory Access | ClK Cycles |
|---|---|---|---|
| **INC** | R0 | 1 | 9 |
| **INC** | @R0 | 3 | 11 |
| **INC** | (R0)+ | 3 | 12 |
| **INC** | @(R0)+ | 4 | 13 |
| **INC** | -(R0) | 3 | 12 |
| **INC** | @-(R0) | 4 | 13 |
| **INC** | X(R0) | 4 | 14 |
| **INC** | @X(R0) | 5 | 15 |
| | | SUM | 99 |

- **Branch:**

  **NB:** All Branch instructions are the same

| Inst | Operand | Memory Access | ClK Cycles |
|---|---|---|---|
| **BR** | Offset | 1 | 7 |

- **No Operand:**

| Inst | Memory Access | ClK Cycles |
|---|---|---|
| **HLT** | 1 | 5 |
| **NOP** | 1 | 5 |
| **RESET** | 1 | 5 |

- **CPI Analysis:**

$$\boldsymbol{CPI} = \frac{\left[(\mathbf{1144} * \mathbf{8}) + \left(\mathbf{1144} - (\mathbf{64} * \mathbf{2})\right) + (\mathbf{99} * \mathbf{9}) + (\mathbf{7} * \mathbf{7}) + \mathbf{15}\right]}{\left[(\mathbf{64} * \mathbf{9}) + (\mathbf{8} * \mathbf{9}) + \mathbf{7} + \mathbf{3}\right]}$$

$$= \mathbf{16}$$