

PDP-11

Phase 2

Team Number 3

Team Members

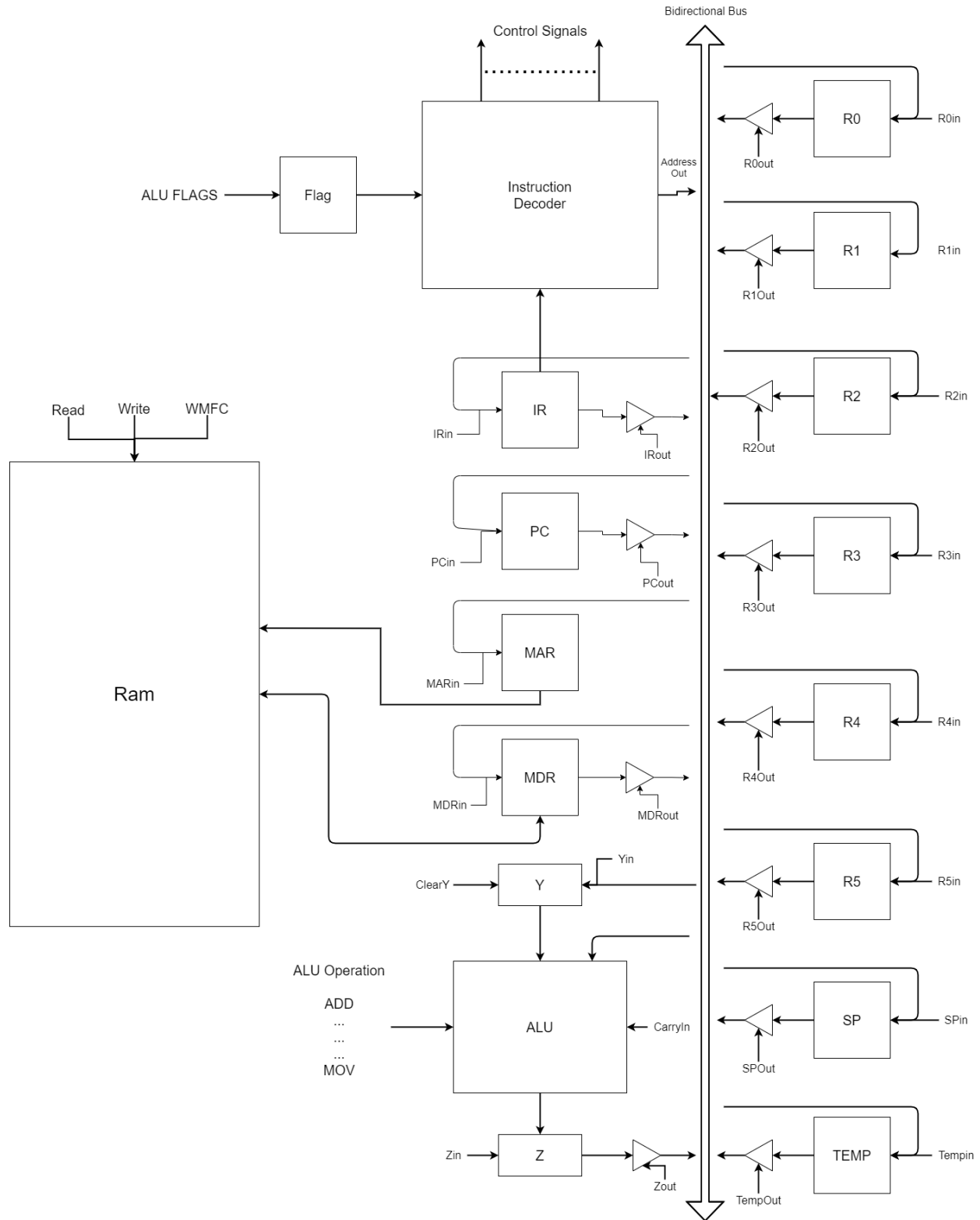
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Bus System Schematic:



Micro-Instructions:

Some microinstructions are changed and marked with yellow color in the next table.

octal	Instructions	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
"000"	PCout,MARin,Read,Yin,Clr-Carry-in,INC,Z-in	"0001"	"011"	"01"	"1"	"1101"	"01"	"0"	"0"	"0"	"0"
"001"	Zout,PCin,WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
"002"	MDRout,IRin	"0010"	"010"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"003"	uBranch[uPc <- [PLA]]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"004"	PCout,Yin,Branch else uPC <- [PLA] = 0	"0001"	"111"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
"005"	IR-Address-Out,Add,Zin	"0111"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"006"	Zout,PCin,End	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"007"	HLT,End	"1000"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"010"	Reset,End	"1001"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"011"	NOP,End	"0000"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"012"	Temp out, Carry-in =0, ADD, Z in	"0110"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"013"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"014"	Temp out, Carry-in =0, ADC, Z in	"0110"	"011"	"00"	"0"	"0001"	"00"	"0"	"0"	"0"	"0"
"015"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"016"	Temp out, Carry-in =0, SUB, Z in	"0110"	"011"	"00"	"0"	"0010"	"00"	"0"	"0"	"0"	"0"
"017"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"020"	Temp out, Carry-in =0, SBC, Z in	"0110"	"011"	"00"	"0"	"0011"	"00"	"0"	"0"	"0"	"0"
"021"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"022"	Temp out, Carry-in =0, AND, Z in	"0110"	"011"	"00"	"0"	"0100"	"00"	"0"	"0"	"0"	"0"
"023"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"024"	Temp out, Carry-in =0, OR, Z in	"0110"	"011"	"00"	"0"	"0101"	"00"	"0"	"0"	"0"	"0"
"025"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"026"	Temp out, Carry-in =0, XOR, Z in	"0110"	"011"	"00"	"0"	"0110"	"00"	"0"	"0"	"0"	"0"
"027"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"030"	INV, Z in	"0000"	"011"	"00"	"0"	"0111"	"00"	"0"	"0"	"0"	"0"
"031"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"032"	LSR, Z in	"0000"	"011"	"00"	"0"	"1000"	"00"	"0"	"0"	"0"	"0"
"033"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"034"	ROR, Z in	"0000"	"011"	"00"	"0"	"1001"	"00"	"0"	"0"	"0"	"0"
"035"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"036"	ASR, Z in	"0000"	"011"	"00"	"0"	"1010"	"00"	"0"	"0"	"0"	"0"
"037"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"040"	LSL, Z in	"0000"	"011"	"00"	"0"	"1011"	"00"	"0"	"0"	"0"	"0"
"041"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"042"	ROL, Z in	"0000"	"011"	"00"	"0"	"1100"	"00"	"0"	"0"	"0"	"0"
"043"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"044"	INC, Z in	"0000"	"011"	"00"	"0"	"1101"	"00"	"0"	"0"	"0"	"0"
"045"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"046"	DEC, Z in	"0000"	"011"	"00"	"0"	"1110"	"00"	"0"	"0"	"0"	"0"
"047"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"050"	CLR-Y, MOV, Z in (CLR instruction)	"0000"	"011"	"00"	"0"	"1111"	"00"	"1"	"0"	"0"	"0"
"051"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"052"	Temp out, Yin, MOV, Zin (MOV instruction)	"0110"	"011"	"00"	"1"	"1111"	"00"	"0"	"0"	"0"	"0"
"053"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"054"	(CMP) -->Temp out, SUB, END	"0110"	"000"	"00"	"0"	"0010"	"00"	"0"	"0"	"0"	"1"
101	Rsrc -> [Temp]	"0100"	"110"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
102	uBranch [uPC <- 170]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"

111	Rsrc -> MAR ; Read	"0100"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
112	uBranch [uPC <- 167]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
121	RsrcOut, MAR in; Read; Yin, INC, Zin	"0100"	"011"	"01"	"1"	"1101"	"01"	"0"	"0"	"0"	"0"
122	[Z] -> Rsrc	"0011"	"100"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
123	uBranch [uPC <- 166; uPC0 <- {IR9}]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
141	Rsrc_out, Yin, DEC, Z_in	"0100"	"011"	"00"	"1"	"1110"	"00"	"0"	"0"	"0"	"0"
142	Z -> ([Rsrc] & MAR); Read	"0011"	"100"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
143	uBranch [uPC <- 166; uPC0 <- {IR9}]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
161	PCout, MAR in, Read, Yin, INC, Zin	"0001"	"011"	"01"	"1"	"1101"	"01"	"0"	"0"	"0"	"0"
162	[Z] -> PC; WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
163	[MDR] -> Y	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
164	[Rsrc] <- [Y] -> Z	"0100"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
165	[Z] -> MAR; Read; WMFC	"0011"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
166	[MDR] -> MAR; Read; WMFC	"0010"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
167	[MDR] -> Temp	"0010"	"110"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
170	uBranch [uPC <- 201; uPC5, 4 <- {IR5, 4} ; uPC3 <- {IR5, {IR4}, {IR3}}]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
201	Rdistout, Yin	"0101"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
202	uBranch {mPC ← PLA(ALUs)}	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
211	Rdistout, MARin, Read	"0101"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
212	uBranch {mPC ← 267 }, WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
221	Rdistout, MARin, Read, Yin, INC, Zin	"0101"	"011"	"01"	"1"	"1101"	"01"	"0"	"0"	"0"	"0"
222	Zout, Rdestin	"0011"	"101"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
223	uBranch {mPC ← 266, mPC0 ← {IR3}}, WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
241	Rdistout, Yin, Dec, Zin	"0101"	"011"	"00"	"1"	"1110"	"00"	"0"	"0"	"0"	"0"
242	Zout, Rdestin, MARin, Read	"0011"	"101"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
243	uBranch {mPC ← 266, mPC0 ← {IR3}}, WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
261	PCout, MARin, Read, Yin, INC, Zin	"0001"	"011"	"01"	"1"	"1101"	"01"	"0"	"0"	"0"	"0"
262	Zout, PCin, WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
263	MDRout, Yin	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
264	Rdistout, Add, Zin	"0101"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
265	Zout, MARin, Read, WMFC	"0011"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
266	MDRout, MARin, Read, WMFC {mPC0 ← {IR3}}	"0010"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
267	MDRout, Yin	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
270	uBranch {mPC ← PLA(ALUs)}	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
274	Zout, MDRin, Write, end {mPC0 ← {IR9}}	"0011"	"000"	"10"	"0"	"0000"	"10"	"0"	"0"	"0"	"1"
275	Zout, Rdistin, end	"0011"	"101"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"