PDP-11

Phase 1

Team Number 3

Team Members

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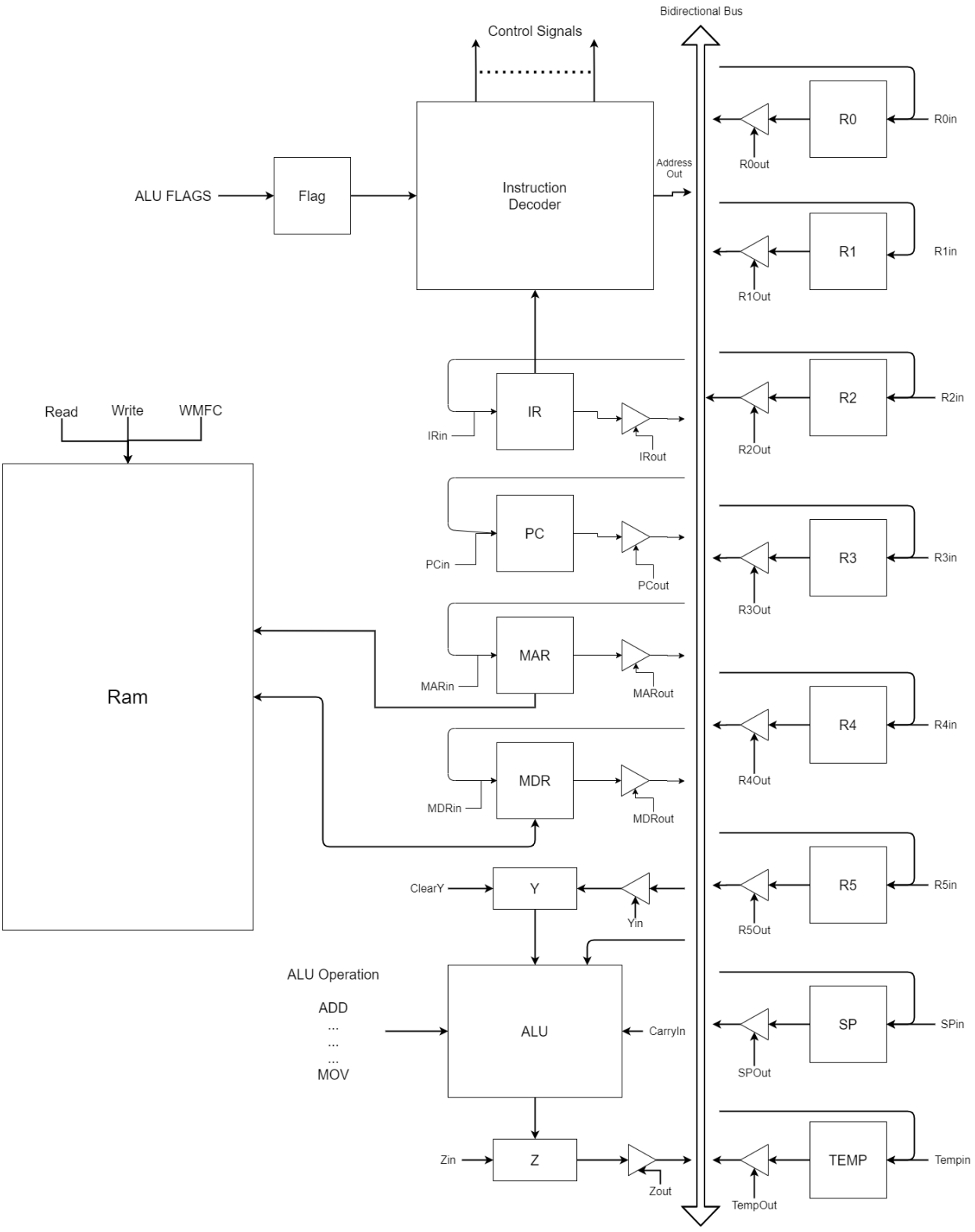
Bus System Schematic:



Instruction Set Architecture:

- **2-Operands Instructions:**

Op code				src						dst					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Instruction	Op code (Binary)
MOV	0000
ADD	0001
ADC	0010
SUB	0011
SBC	0100
AND	0101
OR	0110
XOR	0111
CMP	1000

- **1-Operand Instructions:**

OP code											dst				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Instruction	Op code (Binary)
INC	1001 00 0000
DEC	1001 00 0100
CLR	1001 00 1000
INV	1001 00 1100
LSR	1001 01 0000
ROR	1001 01 0100
ASR	1001 01 1000
LSL	1001 01 1100
ROL	1001 10 0000

- **Branch Instructions:**

OP code								Offset							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Instruction	Op code (Binary)
BR	1010 0000
BEQ	1010 0001
BNE	1010 0010
BLO	1010 0011
BLS	1010 0100
BHI	1010 0101
BHS	1010 0110

- **No Operand Instructions:**

OP code			
15	**14**	**13**	**12**

Instruction	Op code (Binary)
BR	1011
BEQ	1011
BNE	1011

- **Subroutine Instructions:**

OP code						
15	**14**	**13**	**12**	**11**	**10**	**9**

Instruction	Op code (Binary)
JSR	1110 000
RTS	1110 001
INT	1110 010
IRET	1110 011

Addressing Modes:

$b_5b_4b_3$	Name	Syntax
000	**Register Direct**	**Rn**
010	**Autoincrement**	**(Rn)+**
100	**Autodecrement**	**-(Rn)**
110	**Index Direct**	**X(Rn)**
001	**Register indirect**	**@Rn**
011	**Autoincrement indirect**	**@(Rn)+**
101	**Autodecrement indirect**	**@-(Rn)**
111	**Index indirect**	**@X(Rn)**

Micro-Instructions:

- **Words:**

F1 4 BITS		F2 3 BITS		F3 2 BITS		F4 1 BIT		F5 4 BITS	
"0000"	**No Transfer**	"000"	**No Transfer**	"00"	**No transfer**	"0"	**No transfer**	"0000"	**ADD**
"0001"	**PC out**	"001"	**Pc in**	"01"	**MAR in**	"1"	**Yin**	"0001"	**ADC**
"0010"	**MDR out**	"010"	**IR in**	"10"	**MDR in**			"0010"	**SUB**
"0011"	**Z out**	"011"	**Zin**					"0011"	**SBC**
"0100"	**RSrc out**	"100"	**RSrc in**					"0100"	**AND**
"0101"	**RDst out**	"101"	**RDst in**					"0101"	**OR**
"0110"	**Temp out**	"110"	**Temp in**					"0110"	**XOR**
"0111"	**Address out**	"111"	**Branch**					"0111"	**INV**
"1000"	**HLT**							"1000"	**LSR**
"1001"	**RESET**							"1001"	**ROR**
								"1010"	**ASR**
								"1011"	**LSL**
								"1100"	**ROL**
								"1101"	**INC**
								"1110"	**DEC**
								"1111"	**MOV**

F6 2 BITS		F7 1 BIT		F8 1 BIT		F9 1 BIT		F10 1 BIT	
"00"	**No action**	"0"	**No action**	"0"	**Carry-in=0**	"0"	**No actions**	"0"	**Continue**
"01"	**Read**	"1"	**Clear Y**	"1"	**Carry-in=1**	"1"	**WMFC**	"1"	**END**
"10"	**Write**								
"11"	**uBranch**								

octal	Instructions	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
"000"	PCout,MARin,Read,Clear Y,Set-Carry-in,Add,Z-in	"0001"	"011"	"01"	"0"	"0000"	"01"	"1"	"1"	"0"	"0"
"001"	Zout,PCin,WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
"002"	MDRout,IRin	"0010"	"010"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"003"	uBranch[uPc <- [PLA]]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"004"	PCout,Yin,**Branch else uPC <- [PLA] = 0**	"0001"	"111"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
"005"	IR-Address-Out,Add,Zin	"0111"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"006"	Zout,PCin,End	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"007"	HLT,End	"1000"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"010"	Reset,End	"1001"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"011"	NOP,End	"0000"	"000"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"
"012"	Temp out, Carry-in =0, ADD, Z in	"0110"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
"013"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"014"	Temp out, Carry-in =0, ADC, Z in	"0110"	"011"	"00"	"0"	"0001"	"00"	"0"	"0"	"0"	"0"
"015"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"016"	Temp out, Carry-in =0, SUB, Z in	"0110"	"011"	"00"	"0"	"0010"	"00"	"0"	"0"	"0"	"0"
"017"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"020"	Temp out, Carry-in =0, SBC, Z in	"0110"	"011"	"00"	"0"	"0011"	"00"	"0"	"0"	"0"	"0"
"021"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"022"	Temp out, Carry-in =0, AND, Z in	"0110"	"011"	"00"	"0"	"0100"	"00"	"0"	"0"	"0"	"0"
"023"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"024"	Temp out, Carry-in =0, OR, Z in	"0110"	"011"	"00"	"0"	"0101"	"00"	"0"	"0"	"0"	"0"
"025"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"026"	Temp out, Carry-in =0, XOR, Z in	"0110"	"011"	"00"	"0"	"0110"	"00"	"0"	"0"	"0"	"0"
"027"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"030"	Temp out, Carry-in =0, INV, Z in	"0110"	"011"	"00"	"0"	"0111"	"00"	"0"	"0"	"0"	"0"
"031"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"032"	Temp out, Carry-in =0, LSR, Z in	"0110"	"011"	"00"	"0"	"1000"	"00"	"0"	"0"	"0"	"0"
"033"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"034"	Temp out, Carry-in =0, ROR, Z in	"0110"	"011"	"00"	"0"	"1001"	"00"	"0"	"0"	"0"	"0"
"035"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"036"	Temp out, Carry-in =0, ASR, Z in	"0110"	"011"	"00"	"0"	"1010"	"00"	"0"	"0"	"0"	"0"
"037"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"040"	Temp out, Carry-in =0, LSL, Z in	"0110"	"011"	"00"	"0"	"1011"	"00"	"0"	"0"	"0"	"0"
"041"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"042"	Temp out, Carry-in =0, ROL, Z in	"0110"	"011"	"00"	"0"	"1100"	"00"	"0"	"0"	"0"	"0"
"043"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"044"	Temp out, Carry-in =0, INC, Z in	"0110"	"011"	"00"	"0"	"1101"	"00"	"0"	"0"	"0"	"0"
"045"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"046"	Temp out, Carry-in =0, DEC, Z in	"0110"	"011"	"00"	"0"	"1110"	"00"	"0"	"0"	"0"	"0"
"047"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"050"	Temp out, Clear Y, MOV, Z in	"0110"	"011"	"00"	"0"	"1111"	"00"	"1"	"0"	"0"	"0"
"051"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"052"	Temp out, Yin, MOV, Zin	"0110"	"011"	"00"	"1"	"1111"	"00"	"0"	"0"	"0"	"0"
"053"	uBranch[uPc <- 274]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
"054"	(CMP) -->Temp out, SUB, END	"0110"	"000"	"00"	"0"	"0010"	"00"	"0"	"0"	"0"	"1"
101	Rsrc -> [Temp]	"0100"	"110"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"

octal	Instructions	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
102	uBranch [uPC <- 170]	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
111	Rsrc -> MAR ; Read	"0100"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
112	uBranch [uPC <- 167]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
121	Rsrc -> MAR; Read; [Rsrc] + 1 -> Z	"0100"	"011"	"01"	"0"	"0000"	"01"	"1"	"1"	"0"	"0"
122	[Z] -> Rsrc	"0011"	"100"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
123	uBranch [uPC <- 166; uPC0 <- ~~[IR9]~~]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
141	[Rsrc] - 1 -> Z	"0100"	"011"	"00"	"0"	"0010"	"00"	"1"	"1"	"0"	"0"
142	Z -> ([Rsrc] & MAR); Read	"0011"	"100"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
143	uBranch [uPC <- 166; uPC0 <- ~~[IR9]~~]; WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
161	[PC] -> MAR; Read; [PC] + 1 -> Z	"0011"	"011"	"01"	"0"	"0000"	"01"	"1"	"1"	"0"	"0"
162	[Z] -> PC; WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
163	[MDR] -> Y	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
164	[Rsrc] + [Y] -> Z	"0100"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
165	[Z] -> MAR; Read; WMFC	"0011"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
166	[MDR] -> MAR; Read; WMFC	"0010"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
167	[MDR] -> Temp	"0010"	"110"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
170	uBranch [uPC <- 201; uPC5, 4 <- [IR5, 4] ; uPC3 <- ~~[IR5]~~	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
201	Rdistout,Yin	"0101"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
202	uBranch {mPC ← PLA(ALUs)}	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
211	Rdistout,MARin,Read	"0101"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
212	uBranch {mPC ← 267 },WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
221	Rdistout,MARin,Read,Clear Y,Set carry-in,Add,Zin	"0101"	"011"	"01"	"0"	"0000"	"01"	"1"	"1"	"0"	"0"
222	Zout,Rdestin	"0011"	"101"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
223	uBranch {mPC ← 266, mPC0 ← ~~IR9~~},WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
241	Rdistout,Dec,Zin	"0101"	"011"	"00"	"0"	"1110"	"00"	"0"	"0"	"0"	"0"
242	Zout,Rdestin,Marin,Read	"0011"	"101"	"01"	"0"	"0000"	"01"	"0"	"0"	"0"	"0"
243	uBranch {mPC ← 266, mPC0 ← ~~IR9~~},WMFC	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"1"	"0"
261	PCout,MARin,Read,Clear Y,Set Carry-in,Add,Zin	"0001"	"011"	"01"	"0"	"0000"	"01"	"1"	"1"	"0"	"0"
262	Zout,PCin,WMFC	"0011"	"001"	"00"	"0"	"0000"	"00"	"0"	"0"	"1"	"0"
263	MDRout,Yin	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
264	Rdistout,Add,Zin	"0101"	"011"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"0"
265	Zout,MARin,Read,WMFC	"0011"	"000"	"01"	"0"	"0000"	"01"	"0"	"0"	"1"	"0"
266	MDRout,MARin,Read,WMFC {mPC0 ← ~~IR9~~}	"0010"	"000"	"01"	"0"	"0000"	"01"	"0"	"1"	"0"	"0"
267	MDRout,Yin	"0010"	"000"	"00"	"1"	"0000"	"00"	"0"	"0"	"0"	"0"
270	uBranch {mPC ← PLA(ALUs)}	"0000"	"000"	"00"	"0"	"0000"	"11"	"0"	"0"	"0"	"0"
274	Zout,MDRin,Write,end {mPC0 ← ~~IR9~~}	"0011"	"000"	"10"	"0"	"0000"	"10"	"0"	"0"	"0"	"1"
275	Zout,Rdistin,end	"0011"	"101"	"00"	"0"	"0000"	"00"	"0"	"0"	"0"	"1"

Analysis:

- **2-Operands:**

  NB: All 2 operand instructions are the same except for cmp which has less by one mem access and two clk cycles.

Instruction	Src	Dest	Mem Accesses	Clk Cycles
ADD	R0	R0	1	12
ADD	R0	@R0	3	14
ADD	R0	(R0)+	3	15
ADD	R0	@(R0)+	4	16
ADD	R0	-(R0)	3	15
ADD	R0	@-(R0)	4	16
ADD	R0	X(R0)	4	17
ADD	R0	@X(R0)	5	18
ADD	@R0	R0	2	13
ADD	@R0	@R0	4	15
ADD	@R0	(R0)+	4	16
ADD	@R0	@(R0)+	5	17
ADD	@R0	-(R0)	4	16
ADD	@R0	@-(R0)	5	17
ADD	@R0	X(R0)	5	18
ADD	@R0	@X(R0)	6	19
ADD	(R0)+	R0	2	14
ADD	(R0)+	@R0	4	16
ADD	(R0)+	(R0)+	4	17
ADD	(R0)+	@(R0)+	5	18
ADD	(R0)+	-(R0)	4	17
ADD	(R0)+	@-(R0)	5	18
ADD	(R0)+	X(R0)	5	19
ADD	(R0)+	@X(R0)	6	20
ADD	@(R0)+	R0	3	15
ADD	@(R0)+	@R0	5	17
ADD	@(R0)+	(R0)+	5	18
ADD	@(R0)+	@(R0)+	6	19
ADD	@(R0)+	-(R0)	5	18

ADD	@(R0)+	@-(R0)	6	19
ADD	@(R0)+	X(R0)	6	20
ADD	@(R0)+	@X(R0)	7	21
ADD	-(R0)	R0	2	14
ADD	-(R0)	@R0	4	16
ADD	-(R0)	(R0)+	4	17
ADD	-(R0)	@(R0)+	5	18
ADD	-(R0)	-(R0)	4	17
ADD	-(R0)	@-(R0)	5	18
ADD	-(R0)	X(R0)	5	19
ADD	-(R0)	@X(R0)	6	20
ADD	@-(R0)	R0	3	15
ADD	@-(R0)	@R0	5	17
ADD	@-(R0)	(R0)+	5	18
ADD	@-(R0)	@(R0)+	6	19
ADD	@-(R0)	-(R0)	5	18
ADD	@-(R0)	@-(R0)	6	19
ADD	@-(R0)	X(R0)	6	20
ADD	@-(R0)	@X(R0)	7	21
ADD	X(R0)	R0	3	16
ADD	X(R0)	@R0	5	18
ADD	X(R0)	(R0)+	5	19
ADD	X(R0)	@(R0)+	6	20
ADD	X(R0)	-(R0)	5	19
ADD	X(R0)	@-(R0)	6	20
ADD	X(R0)	X(R0)	6	21
ADD	X(R0)	@X(R0)	7	22
ADD	@X(R0)	R0	4	17
ADD	@X(R0)	@R0	6	19
ADD	@X(R0)	(R0)+	6	20
ADD	@X(R0)	@(R0)+	7	21
ADD	@X(R0)	-(R0)	6	20
ADD	@X(R0)	@-(R0)	7	21
ADD	@X(R0)	X(R0)	7	22
ADD	@X(R0)	@X(R0)	8	23
			SUM	1144

- **1-Operand:**

  NB: All 1 operand instructions are the same except for branch

Inst	Operand	Memory Access	ClK Cycles
INC	R0	1	9
INC	@R0	3	11
INC	(R0)+	3	12
INC	@(R0)+	4	13
INC	-(R0)	3	12
INC	@-(R0)	4	13
INC	X(R0)	4	14
INC	@X(R0)	5	15
		SUM	99

- **Branch:**

  NB: All Branch instructions are the same

Inst	Operand	Memory Access	ClK Cycles
BR	Offset	1	7

- **No Operand:**

Inst	Memory Access	ClK Cycles
HLT	1	5
NOP	1	5
RESET	1	5

- **CPI Analysis:**

$$\boldsymbol{CPI} = \frac{\left[(\mathbf{1144} * \mathbf{8}) + \left(\mathbf{1144} - (\mathbf{64} * \mathbf{2})\right) + (\mathbf{99} * \mathbf{9}) + (\mathbf{7} * \mathbf{7}) + \mathbf{15}\right]}{\left[(\mathbf{64} * \mathbf{9}) + (\mathbf{8} * \mathbf{9}) + \mathbf{7} + \mathbf{3}\right]}$$

$$= \mathbf{16}$$