Use 'F', 'D', 'X', 'M', 'W' for stages, '-' for a stall, '=' for indicating delayed fetching due to waiting for branch resolution, and 'b' for all blanks.

[For the spacing concern of the Webcourses, the timeline is put in rows, and instructions are put in columns. The first column is filled out for your reference.]

	LD R2,0(R1)	DADDI R3,R2,#2	DADDI R2,R2,R3	SD 0(R1),R2	DSUB R4,R1,R3	BNEZ R4,
1	F					
2	D	F				
3	X	D	F			
4	M	-	-	B		
5	W	X	D	F	B	
6		M	X	D	F	B
7		W	M	X	D	F
8		B	W	M	X	-
9		B	B	W	M	D
10			B	B	W	X
11			B	B	B	M
12				B	B	W
13				B	B	B
14					B	B

15					B	B
16						B

Answer 1:
F
Answer 2:
D
Answer 3:
F
Answer 4:
-
Answer 5:
-
Answer 6:
b
Answer 7:
X
Answer 8:
D
Answer 9:
F
Answer 10:
b
Answer 11:
M
Answer 12:
X
Answer 13:
D
Answer 14:
F
Answer 15:
b
Answer 16:
W
Answer 17:
M

Answer 18:

X

Answer 19:

D

Answer 20:

F

Answer 21:

b

Answer 22:

b

Answer 23:

W

Answer 24:

M

Answer 25:

X

Answer 26:

-

Answer 27:

b

Answer 28:

b

Answer 29:

b

Answer 30:

W

Answer 31:

M

Answer 32:

D

Answer 33:

=

Answer 34:

b

Answer 35:

b

Answer 36:

W

Answer 37:

X

Answer 38:

F

Answer 39:

b

Answer 40:

b

Answer 41:

b

Answer 42:

M

Answer 43:

D

Answer 44:

b

Answer 45:

b

Answer 46:

W

Answer 47:

X

Answer 48:

b

Answer 49:

b

Answer 50:

b

Answer 51:

M

Answer 52:

b

Answer 53:

b

Answer 54:

W

Answer 55:

b

Answer 56:

b

Answer 57:

b

Answer 58:

b

Answer 59:

b

Question 2

2 / 2 pts

Use the following code fragment from **Question 1**:

Use the classic RISC five stage integer pipeline and assume all memory accesses take 1 clock cycle.

Show the timing of this instruction sequence for the basic 5-stage RISC pipeline, but **without any forwarding or bypassing** hardware. Furthermore, assume that a register write at the WB stage happens in the first half of the clock cycle, while a register read at the ID stage happens in the second half of the clock cycle. This means that a write at WB stage can ”forward” value through the register file to a read at the ID stage (trivia: MIPS R2000/R3000 has such a feature).

Use 'F', 'D', 'X', 'M', 'W' for stages, -' for stall, '=' for indicating delayed fetching due to waiting for branch resolution, and 'b' for all other blanks.

[For the spacing concern of the Webcourses, the timeline is put in rows and instructions are put in columns. The first column is filled out for your reference]

	LD R2,0(R1)	DADDI R3,R2,#2	DADDI R2,R2,R3	SD 0(R1),R2	DSUB R4,R1,R3	BNEZ R4,I
1	F					
2	D	F				
3	X	-	B			
4	M	-	B	B		
5	W	D	F	B	B	
6		X	-	B	B	B
7		M	-	B	B	B
8		W	D	F	B	B

9		B	X	-	B	B
10		B	M	-	B	B
11			W	D	F	B
12			B	X	D	F
13			B	M	X	-
14			B	W	M	-
15			B	B	W	D
16				B	B	X
17				B	B	M
18				B	B	W
19				B	B	B
20				B	B	B
21					B	B
22					B	B

Answer 1:

F

Answer 2:

-

Answer 3:

b

Answer 4:

-

Answer 5:

b

Answer 6:

b

Answer 7:

D

Answer 8:

F

Answer 9:

b

Answer 10:

b

Answer 11:

X

Answer 12:

-

Answer 13:

b

Answer 14:

b

Answer 15:

b

Answer 16:

M

Answer 17:

-

Answer 18:

b

Answer 19:

b

Answer 20:

b

Answer 21:

b

Answer 22:

W

Answer 23:

D

Answer 24:

F

Answer 25:

b

Answer 26:

b

Answer 27:

b

Answer 28:

b

Answer 29:

X

Answer 30:

-

Answer 31:

b

Answer 32:

b

Answer 33:

b

Answer 34:

b

Answer 35:

M

Answer 36:

-

Answer 37:

b

Answer 38:

b

Answer 39:

b

Answer 40:

W

Answer 41:

D

Answer 42:

F

Answer 43:

b

Answer 44:

b

Answer 45:

b

Answer 46:

X

Answer 47:

D

Answer 48:

F

Answer 49:

b

Answer 50:

b

Answer 51:

M

Answer 52:

X

Answer 53:

-

Answer 54:

b

Answer 55:

b

Answer 56:

W

Answer 57:

M

Answer 58:

-

Answer 59:

b

Answer 60:

b

Answer 61:

b

Answer 62:

W

Answer 63:

D

Answer 64:

=

Answer 65:

b

Answer 66:

b

Answer 67:

X

Answer 68:

F

Answer 69:

b

Answer 70:

b

Answer 71:

M

Answer 72:

D

Answer 73:

b

Answer 74:

b

Answer 75:

W

Answer 76:

X

Answer 77:

b

Answer 78:

b

Answer 79:

b

Answer 80:

M

Answer 81:

b

Answer 82:

b

Answer 83:

b

Answer 84:
W
Answer 85:
b
Answer 86:
b
Answer 87:
b
Answer 88:
b
Answer 89:
b
Answer 90:
b

Question 3
1 / 1 pts

Use the following code fragment:

```
LD R2,0(R1)              ;load R2 from address 0+R1
DADDI R3,R2,#2           ;R3=R2+2
SD 0(R1),R2               ;store R2 at address 0+R1
DSUB R4,R1,R3             ;R4=R1-R3
BNEZ R4,target           ;branch to target if R4=!0
DMUL R3, R4, R5          ;R3=R4*R5
```

There are 5 true-dependence(s), 2 anti-dependence(s), 1 output-dependence(s) and 1 control dependence(s).

Answer 1:
5
Answer 2:
2
Answer 3:
1
Answer 4:
1

Question 4

2 / 2 pts

Suppose we have a conditional branch that has an outcome shown in the table. What are the instances of the branch that will be correctly predicted using **2-bit prediction counter**? Show the old counter state, prediction generated by the predictor, whether the prediction is correct, and the new state of the counter (after updated by the outcome of the current branch).

Show the prediction outcome for **2-bit counter**.

For the counter state, to make it easier, you can use decimal numbers. For example, for 2-bit counters the state can be 0, 1, 2, or 3 (0 and 1 indicate a predict not taken, and 2 and 3 indicate a predict taken).

Show the prediction outcome for **2-bit counter**. Use T/N for 'Prediction Direction' and y/n for 'Mispredicted?'

Old Counter State	Prediction Direction	Actual Outcome	Mispredicted?	New Counter State
0	N	T	y	1
1	N	T	Y	2
2	T	T	N	3
3	T	N	Y	2
2	T	N	Y	1
1	N	T	Y	2
2	T	T	N	3
3	T	T	N	3
3	T	T	N	3
3	T	T	N	3
3	T	N	Y	2

2	T	T	N	3
3	T	T	N	3
3	T	N	Y	2

Answer 1:
1
Answer 2:
N
Answer 3:
y
Answer 4:
2
Answer 5:
2
Answer 6:
T
Answer 7:
n
Answer 8:
3
Answer 9:
3
Answer 10:
T
Answer 11:
y
Answer 12:
2
Answer 13:
2
Answer 14:
T
Answer 15:
y
Answer 16:

1

Answer 17:

1

Answer 18:

N

Answer 19:

y

Answer 20:

2

Answer 21:

2

Answer 22:

T

Answer 23:

n

Answer 24:

3

Answer 25:

3

Answer 26:

T

Answer 27:

n

Answer 28:

3

Answer 29:

3

Answer 30:

T

Answer 31:

n

Answer 32:

3

Answer 33:

3

Answer 34:

T

Answer 35:

n

Answer 36:

3

Answer 37:

3

Answer 38:

T

Answer 39:

y

Answer 40:

2

Answer 41:

2

Answer 42:

T

Answer 43:

n

Answer 44:

3

Answer 45:

3

Answer 46:

T

Answer 47:

n

Answer 48:

3

Answer 49:

3

Answer 50:

T

Answer 51:

y

Answer 52:

2

Quiz score: 7 out of 7