



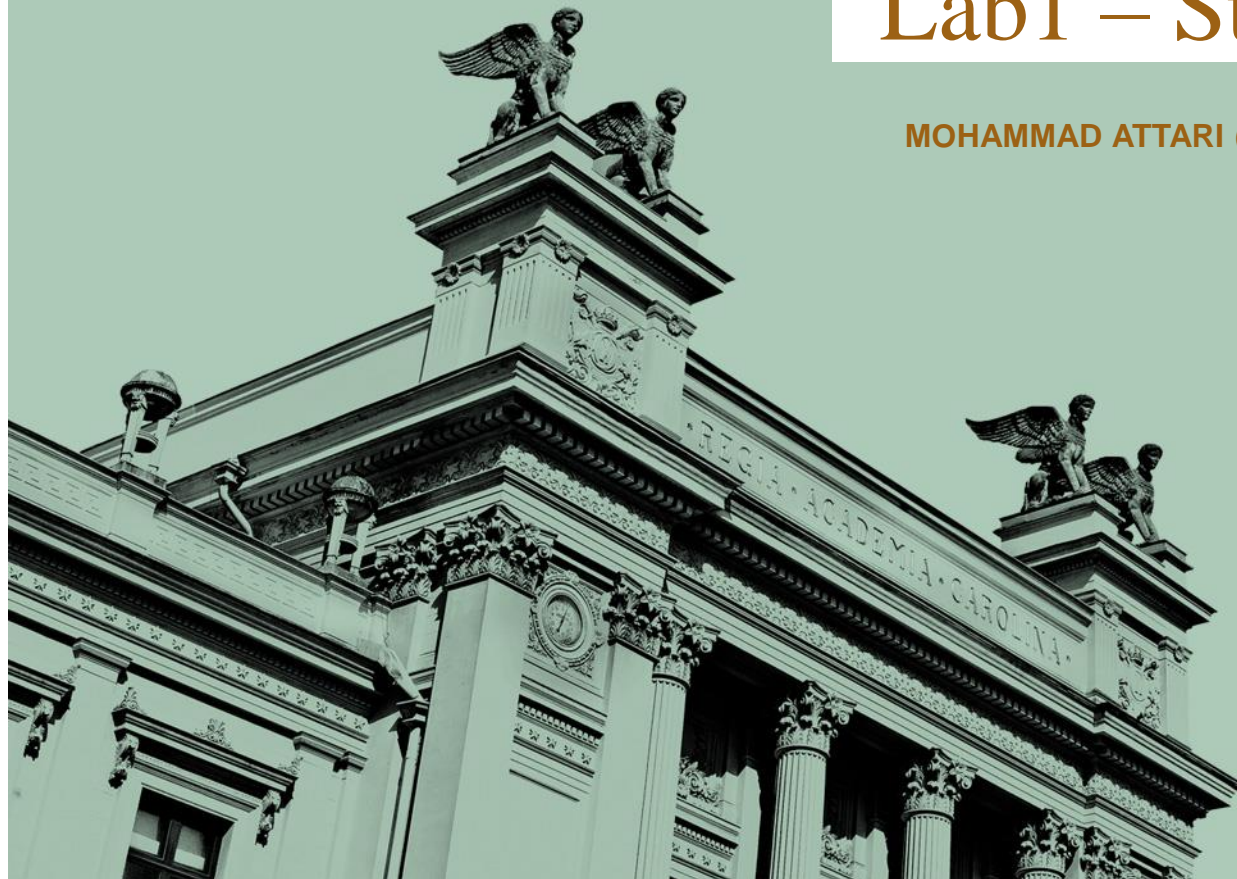
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Introduction to Structured VLSI Design

Lab1 – State Machine Modeling

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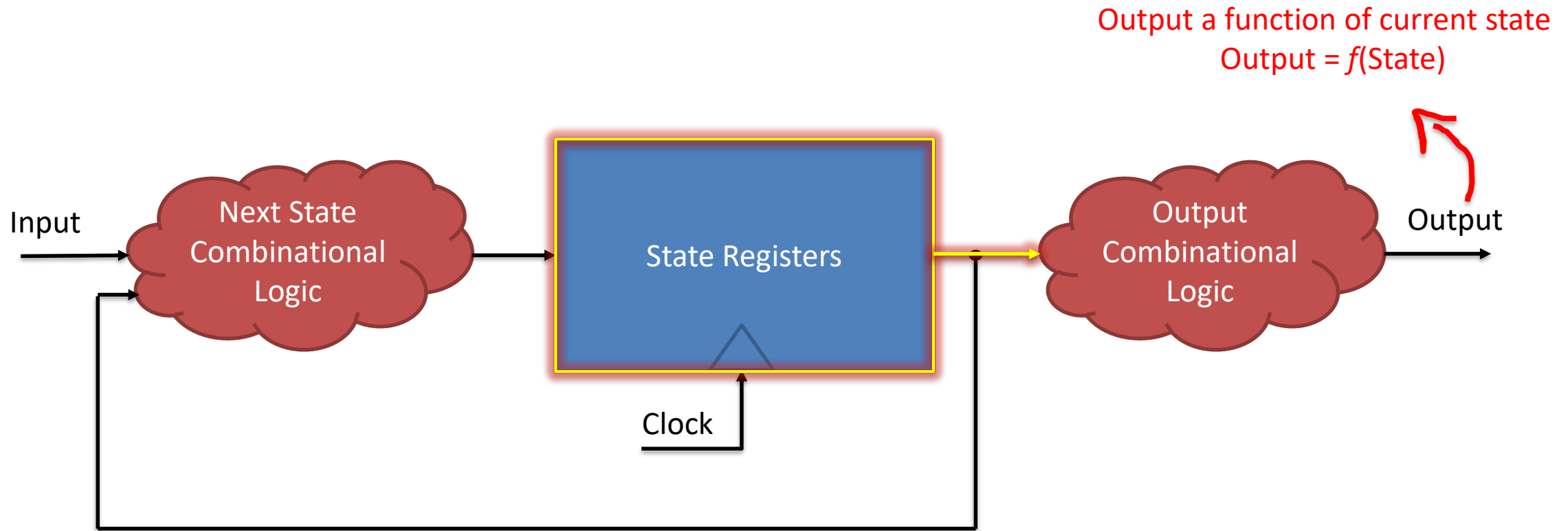
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Learning Outcomes

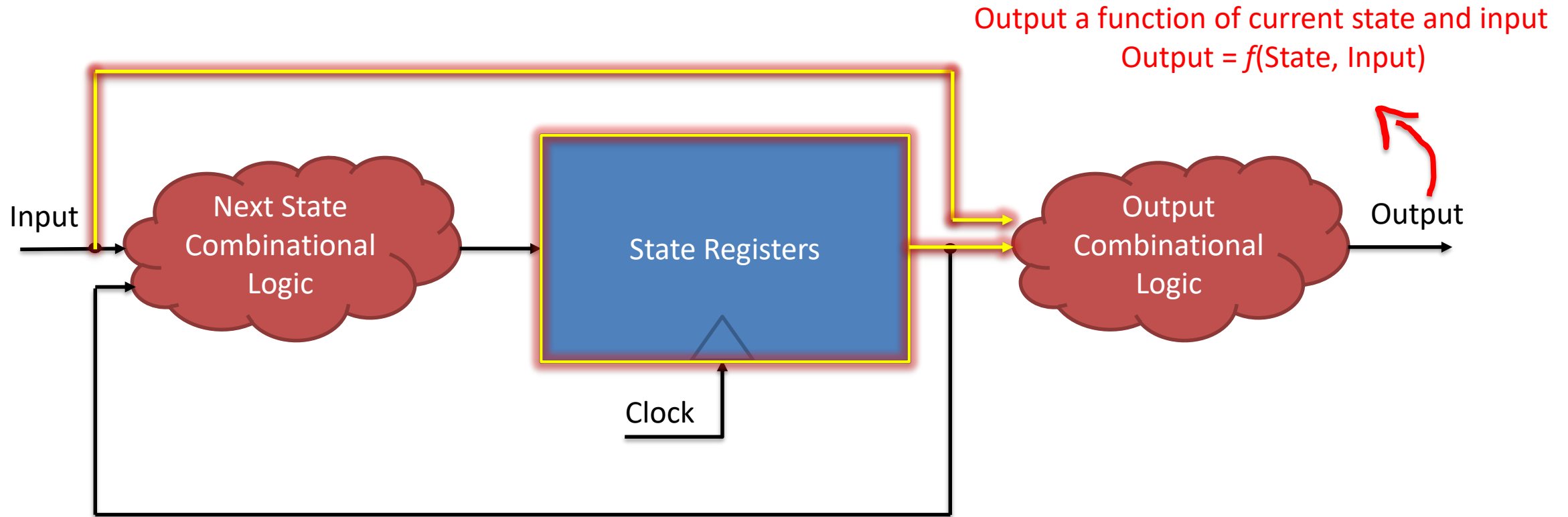
- VHDL modelling for synthesis
 - Registers (state)
 - Combinational logic
 - Avoid latches
- State machines
 - Mealy
 - Moore
- Testbench
- Xilinx Vivado



Moore Machine

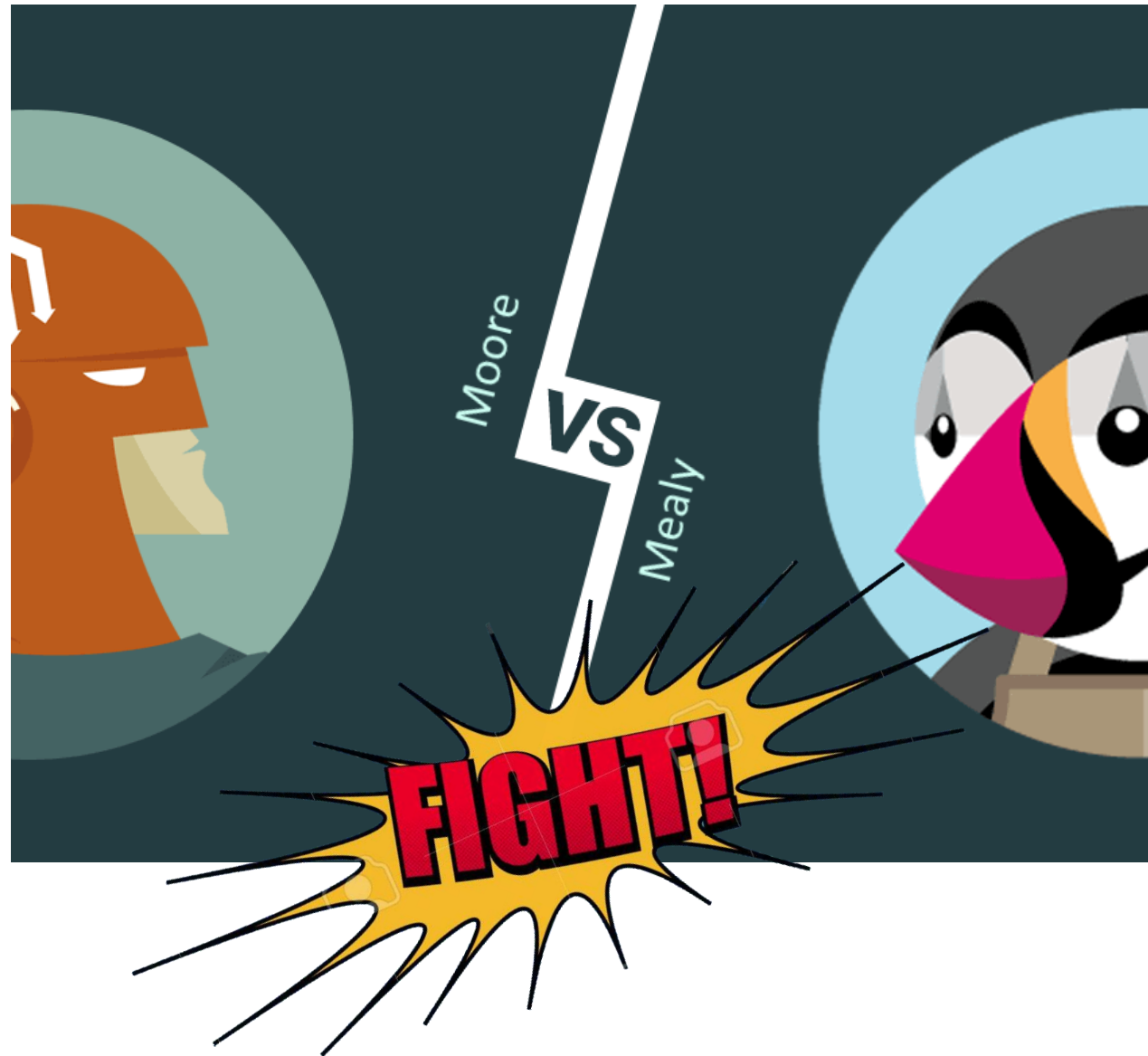


Mealy Machine

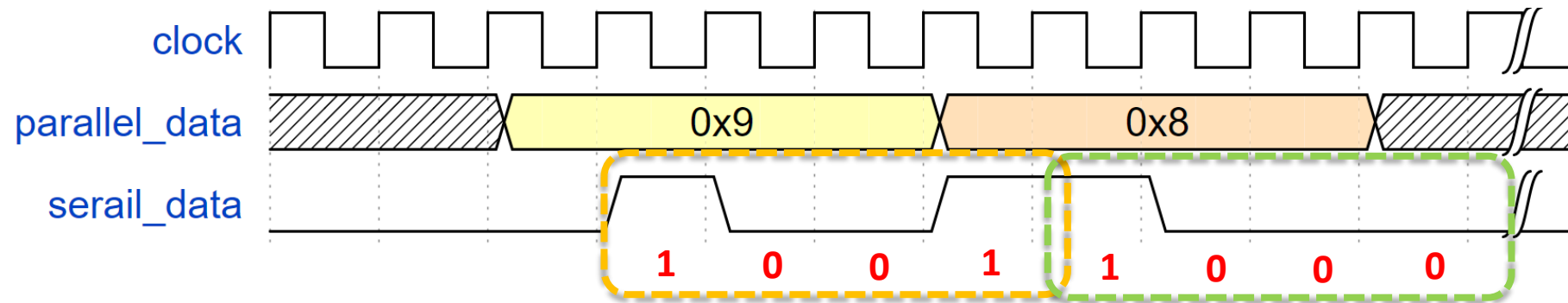


Moore vs. Mealy

- Mealy
 - Fewer states
 - React faster
- Moore
 - Safer
 - Synchronous



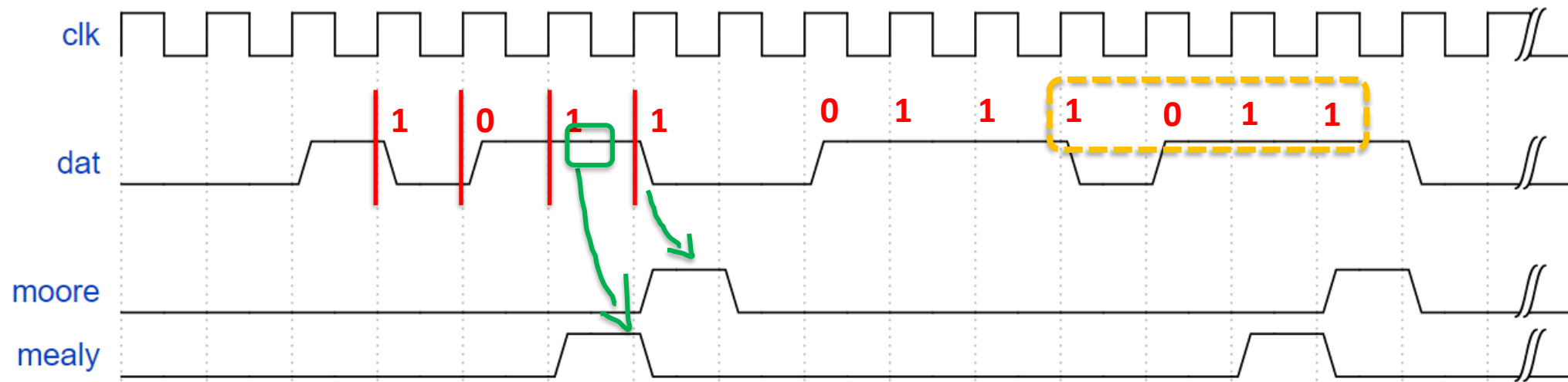
Parallel to Serial Converter



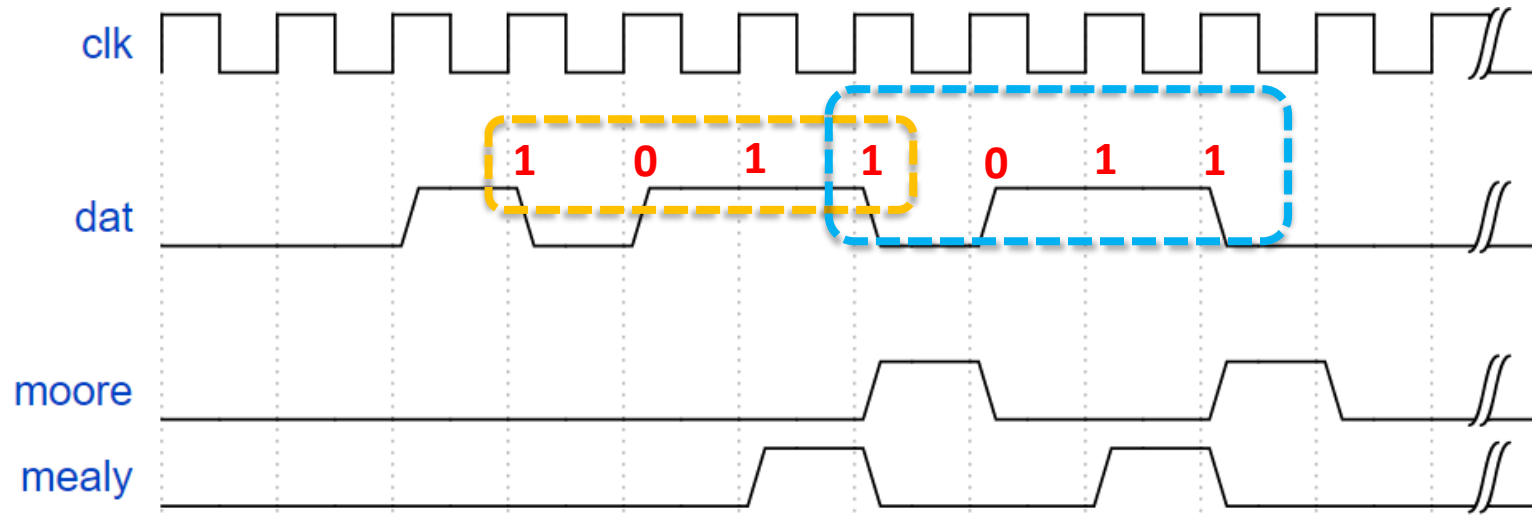
Most significant bit first

Sequence Detector

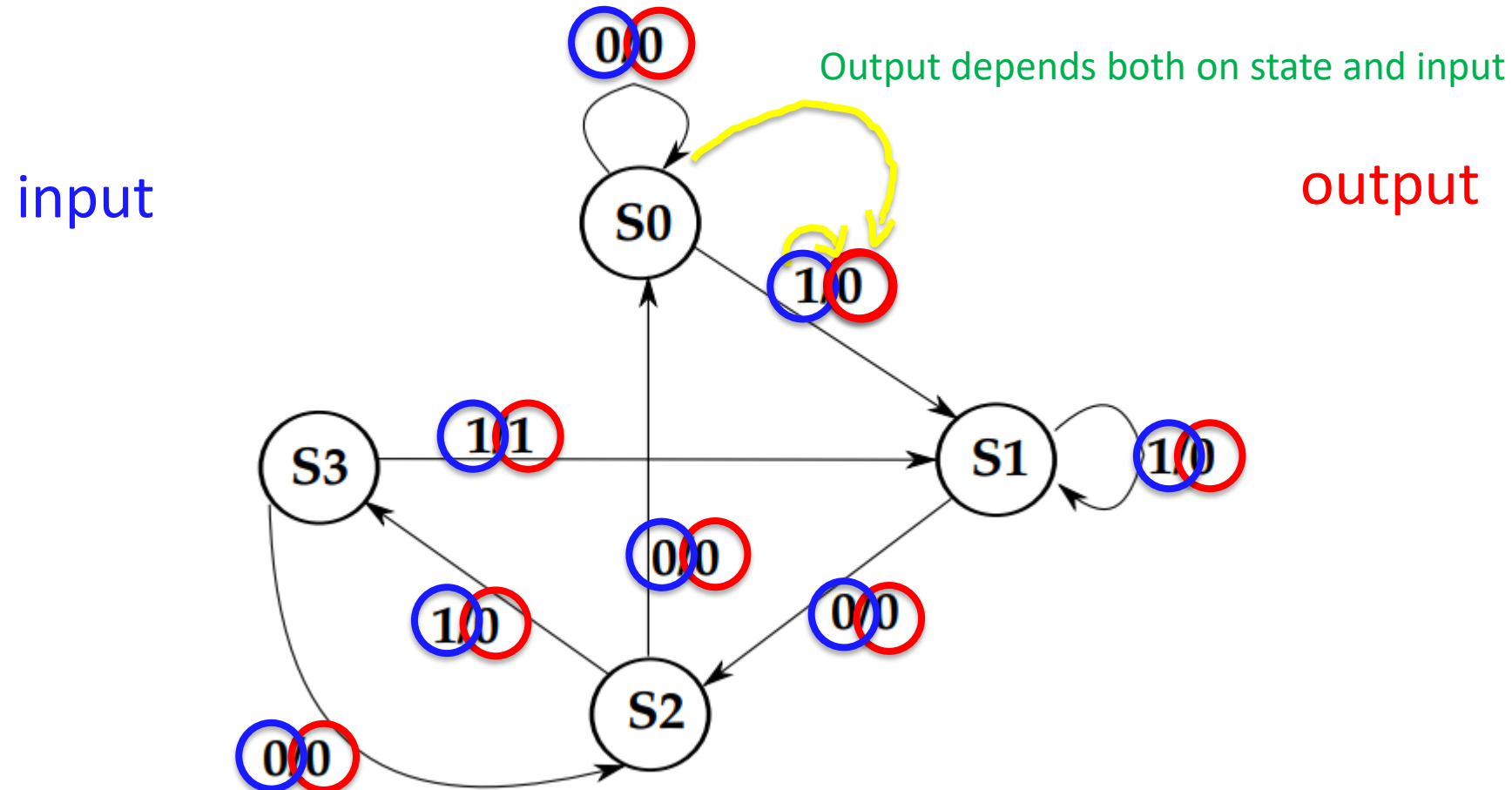
- Detect the sequence **1011**



Sequence in Sequence



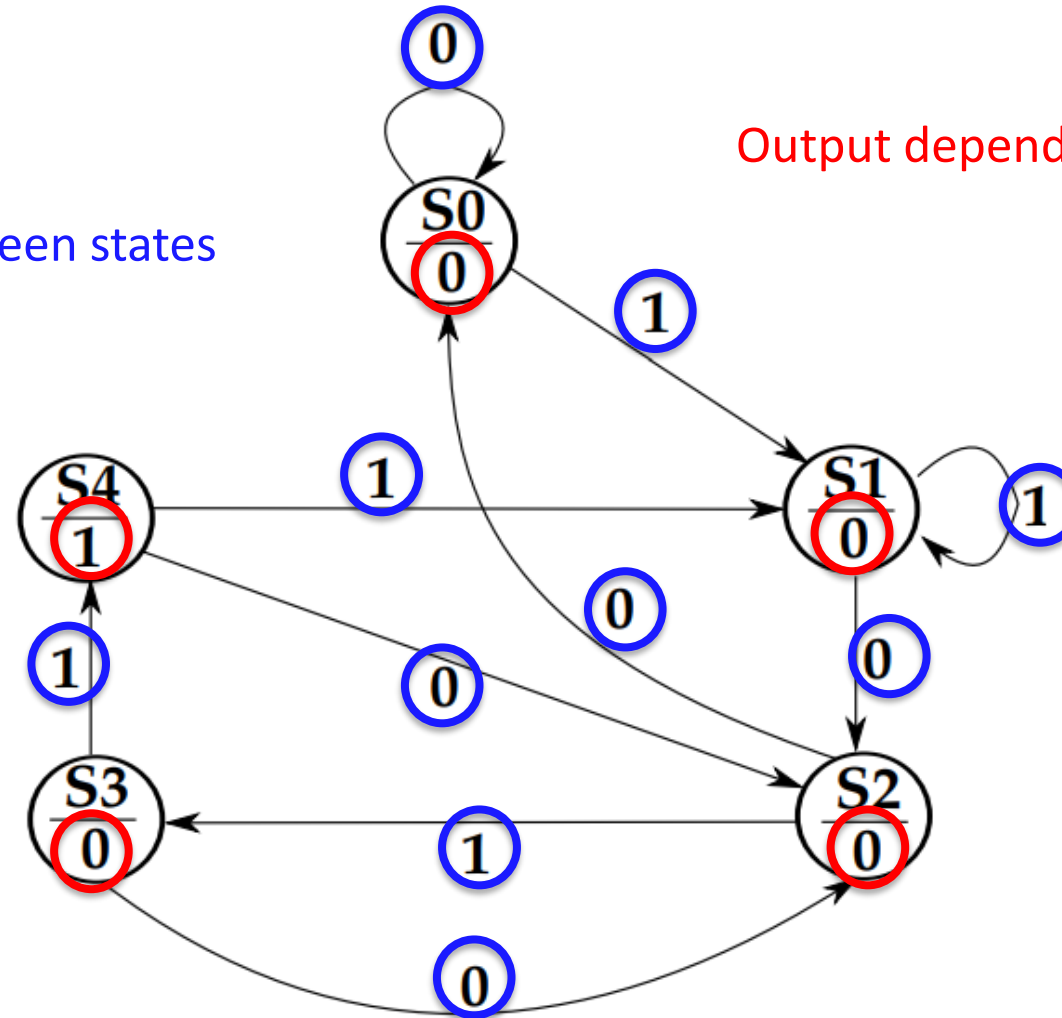
Mealy State Machine



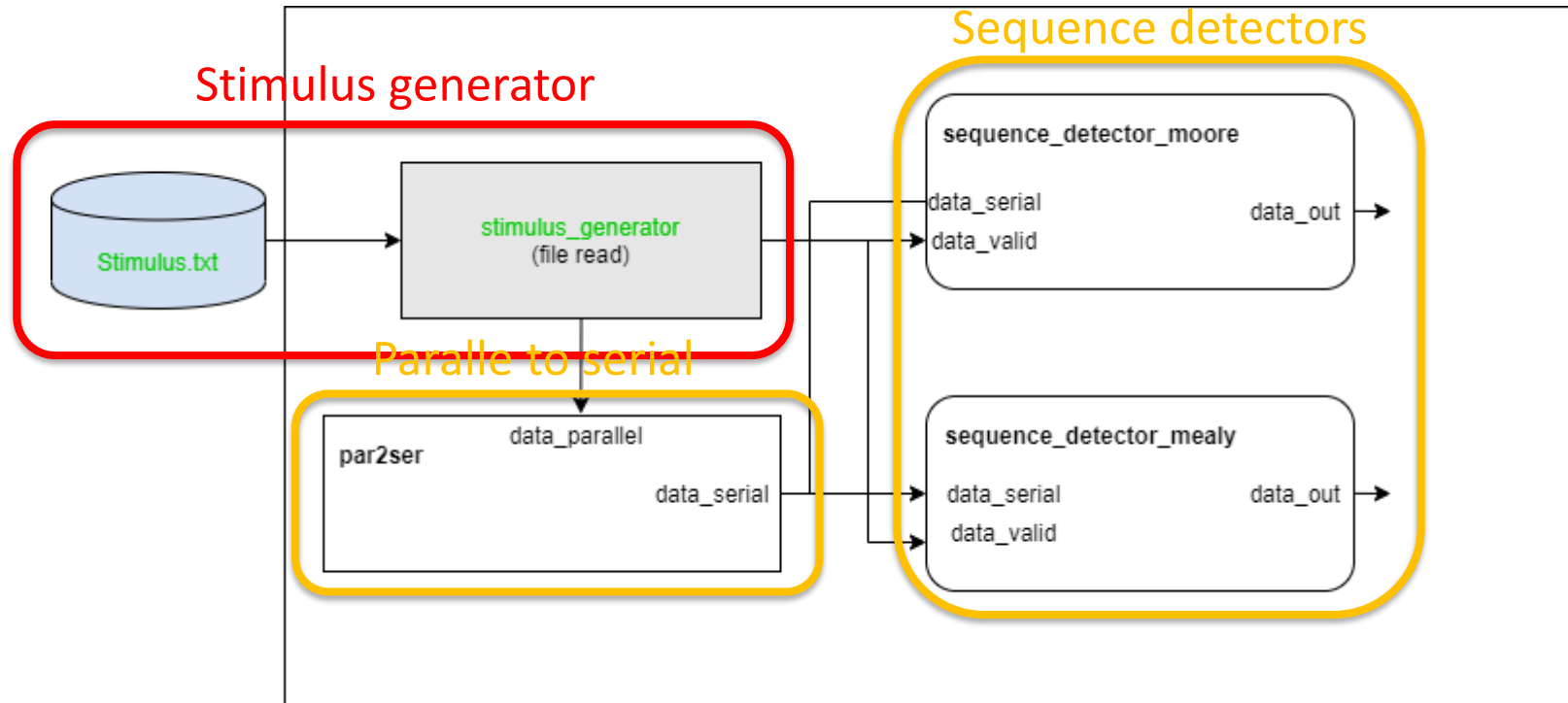
Moore State Machine

Input causes transition between states

Output depends only on state



Testbench



Vivado Design Suite

Vivado 2018.1 - [D:/Work_Space/Vivado/vls_lab1/vls_lab1.xpr] - Vivado 2018.1

File Edit Flow Tools Reports Window Layout View Run Help

20000 ns

Synthesis Complete

Default Layout

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Scope Sources

Name	Design Unit	Block Type
test	test(behavior)	VHDL En...
sequence_decoder(...)	FILE_READ(BEHAVE)	VHDL En...
CLOCKGENERATOR...		VHDL En...

Objects

Name	Value	Date
s_in	0	Logi
clk	1	Logi
rst	1	Logi
d_out1	0	Logi
d_out2	U	Logi
flag	0	Logi
count[3:0]	3	Arra
inputbus[11:0]	56c	Arra
inputbus_temp[...	5b0	Arra
M[11:0]	b60	Arra

detector.vhd x FSM_test.vhd x Untitled 7* x

Name Value

s_in	1
clk	1
rst	1
d_out1	0
d_out2	U
flag	0
count[3:0]	5
inputbus[11:0]	5e5
inputbus_temp[11:0]	e5f
M[11:0]	cbf

162.227400 us

130 us 135 us 140 us 145 us 150 us 155 us 160 us 165 us 170 us 175 us 180 us 185 us 190 us

1 2 3 4 5 6 7 8 9 a b 0 1 2

5e5 bcb 797 22f e5f cbf 97f 2ff 5ff bff 7ff fff e45 e45 0

bcb 797 22f e5f cbf 97f 2ff 5ff bff 7ff fff e45 c6b 0

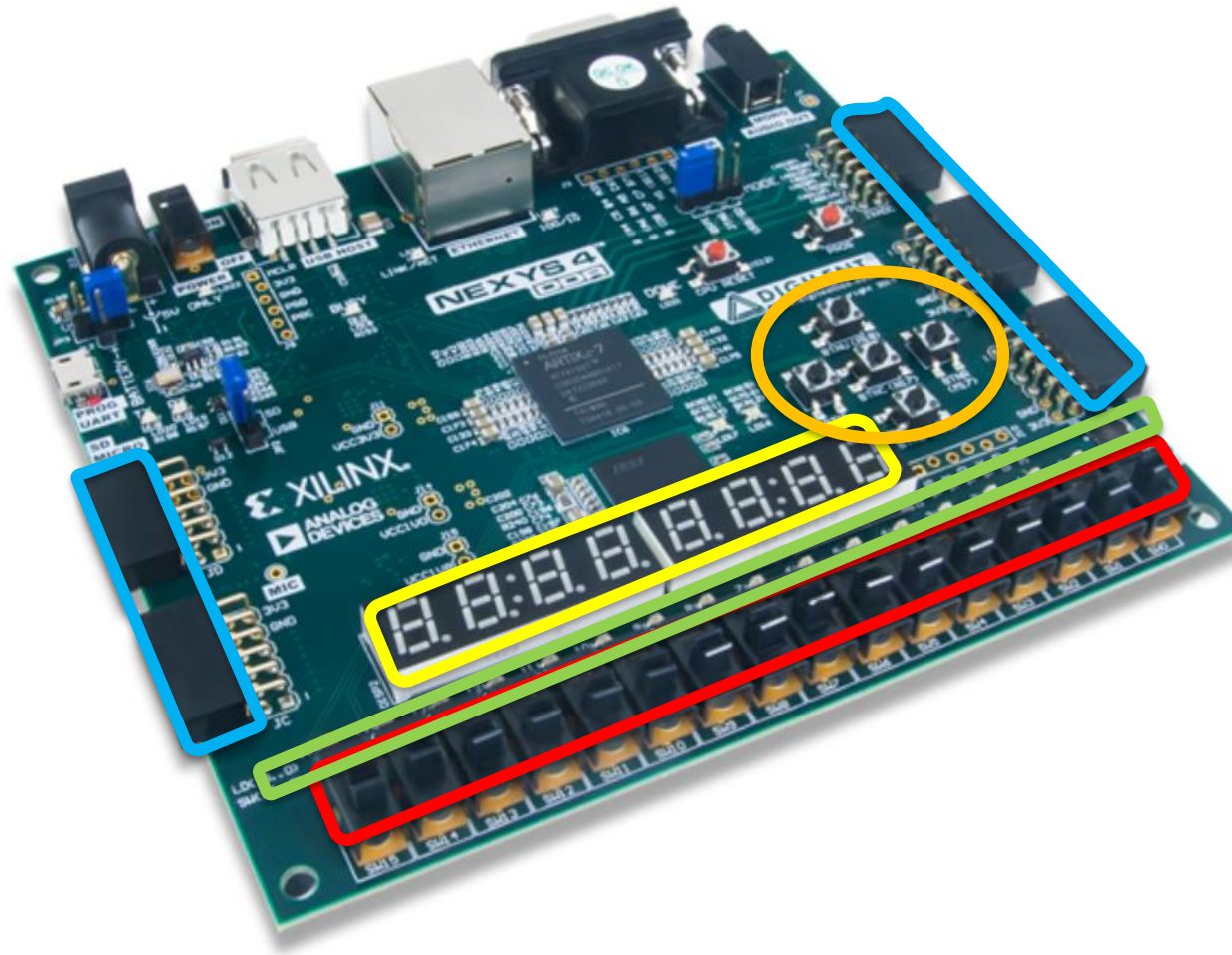
Tcl Console

Messages Log

```
run 20000 ns
run 20000 ns
run 20000 ns
run 20000 ns
```

Type a Tcl command here

Nexys 4 FPGA (Labs 2-5)



Lab1 Assignment

- Draw the state diagrams
- Implement FSM in VHDL
- Show simulation
- Demonstrate understanding

?

