DDAK

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1 Positive - edge triggered flip-flop

D	S	R	Q	State
	0	0	Previous	no change
0	0	1	0	Reset
1	1	0	1	Set
	1	1	—	Invalid

a) $Q = 0$

$S = 0$, $R = 0$ → no change

Q SR : $0_{,,}$

b) $Q = 0$

$S = 1$, $R = 0$ → set

Q SR : $1_{,,}$

c) $Q = 0$ → clock 2, $D = 0$ → reset

$D = 1$ → set

$Q D : 1_{,,}$

d) $Q = 1$

$D = 0$ → reset

$Q D : 0_{,,}$

Clock   clock 1   clock 2   clock 3   clock 4

QSR

QD
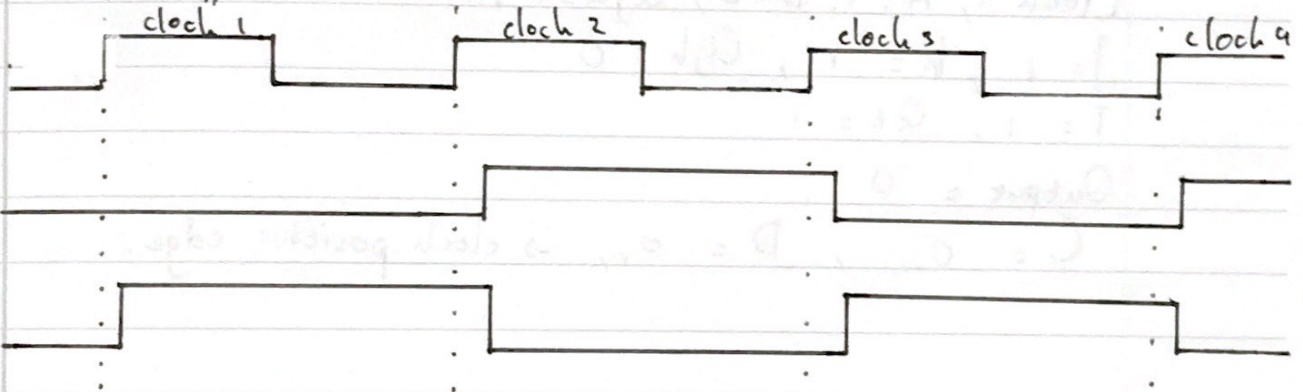
Output = Qjk NOR Qt

2

J = A NAND B

K = Qjk XOR B

T = Not Qjk

T	J	K	Q'
0	0	0	Q
0	1		0
1	0		1
1	1	1	$\bar{Q}$

Clock 1, A = 1, B = 1

J = 0 → Q/0

Qjk = 0 (Qawal = 0, pasti 0)

T = 1 → toggle

Qt = 0 (present state T awal = 1)

Clock 2, A = 1, B = 0, Qjk = 0, Qt = 0

J = 1 → 1/$\bar{Q}$

Qjk = 1 (Qawal = 0, pasti 1)

T = 1 → toggle

Qt = 1

Output = 1 NOR 0

= 0

A = 0,, , B = 0,, → clock positive edge sehingga A dan
B sama saja

Clock 3, A = 0, B = 1, Qjk = 1, Qt = 1

J = 1 , K = 0 , Qjk = 1

T = 0 , Qt = 1

Output = 0

Clock 4, A = 1, B = 0, Qjk = 1, Qt = 0

J = 1 , K = 1 , Qjk = 0

T = 0 , Qt = 1

Output = 0

C = 0,, , D = 0,, → clock positive edge.

3   a   LDI R28, $75 → 1110 kkkh dddd kkkk   (7) (28) (5)

     1110 | 28 = 1100 | 7 = 0111 | 5 = 0101

     : 1110 0111 1100 0101 ,,

   b   ADD R9, R14 → 0000 11rd dddd rrrr   (9) (14)

     0000 | 9 = 01001 | 14 = 01110

     = 0000 1100 1001 1110 ,,

   c   AND R0, R10 → 0010 00rd dddd rrrr   (0) (10)

     0010 | 0 = 00000 | 10 = 01010

     : 0010 0000 0000 1010 ,,

   d   LSR R9 → 1001 010d dddd 0110   (9)

     1001 | 9 = 01001

     = 1001 0100 1001 0110 ,,

4   1   PC = 0x0007   (program direplika di AVR)

     2   r0 = $83

     3   ZH : ZL = 0x0034

     4   r0 = 0x06

     5   PC = 0x0001