SPI SLAVE

Design Document

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1. Introduction

Serial Peripheral Interface (SPI) is a serial communication protocol that is used to connect low-speed devices. It is a full-duplex synchronous serial communication, which means that data can be simultaneously transmitted from both directions. The main advantage of the SPI is to transfer the data without any interruption. Many bits can be sent or received at a time in this protocol. In this protocol, devices are communicated in the master-slave relationship. The master device controls the slave device, and the slave device takes the instruction from the master device. The simplest configuration of the Serial Peripheral Interface (SPI) is a combination of a single slave and a single master. But, one master device can control multiple slave devices.

The SPI protocol uses the four wires for the communication. There are shown in the figure 1.

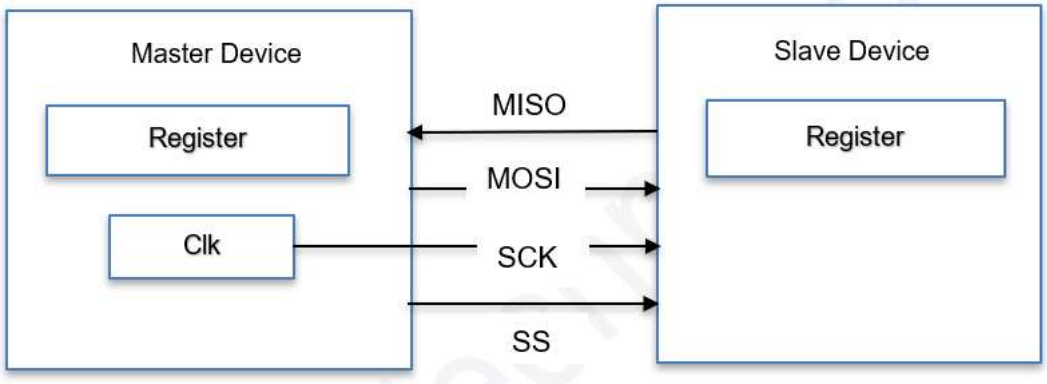

Figure 1: SPI block diagram

1. **MOSI:** MOSI stands for Master Output Slave Input. It is used to send data from the master to the slave.
2. **MISO:** MISO stands for Master Input Slave Output. It is used to send data from the slave to the master.
3. **SCK or SCLK (Serial Clock):** It is used to the clock signal.
4. **SS/CS (Slave Select / Chip Select):** It is used by the master to send data by selecting a slave.

Applications of SPI

Memory: SD Card, MMC, EEPROM, and Flash.
Sensors: Temperature and Pressure.
Control Devices: ADC, DAC, digital POTS, and Audio Codec.
Others: Camera Lens Mount, Touchscreen, LCD, RTC, video game controller, etc.

2. SPI Slave Block Diagram and Pin Description

SPI Slave block diagram is shown in figure 2.

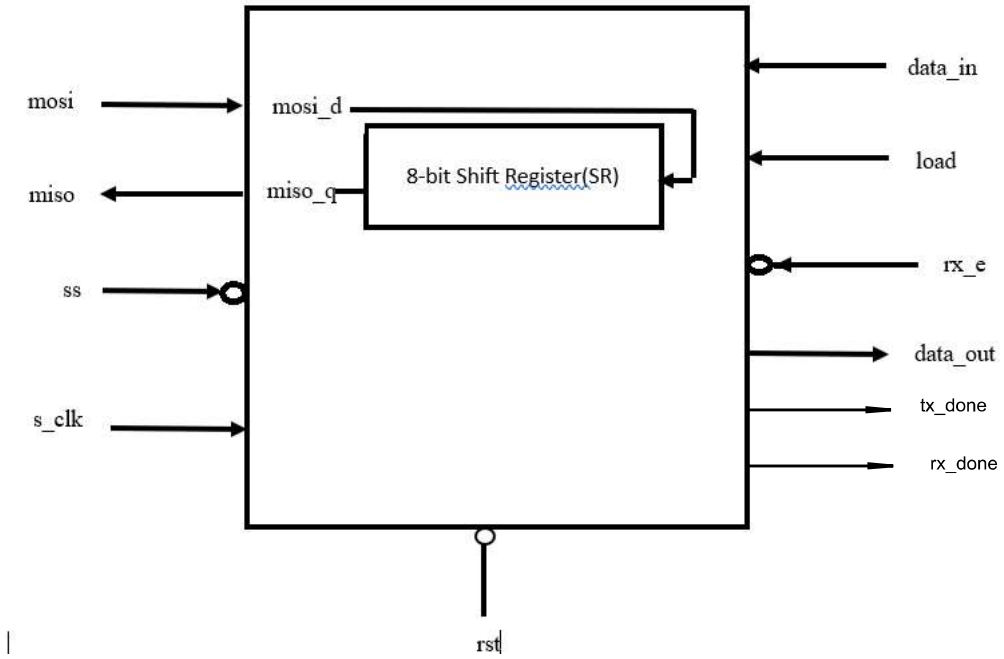

Figure 2: SPI Slave Block Diagram

Pin Name	Default value	Direction	Width	Description
rst	--	Input	1	Active low reset
s_clk	Decide by the mode of SPI	Input	1	Clock signal is provided by the master.
ss	1'b1	Input	1	When ss='0', slave is selected by the master for communication.
mosi	1'b0	Input	1	Data bit is received over mosi transmitted by the master.
miso	1'b0	Output	1	Data bit is transmitted over miso to the master.
data_in	8'd0	Input	8	The to be transmitted by the slave is stored in data_in

load	1’b0	Input	1	When load=1, data_in is loaded into shift register
rx_e	1’b0	Input	1	If rx_e = 0, data reception enabled. Received data loaded onto data_out.
data_out	8’d0	Output	8	Received byte is loaded on to data_out when rx_e=0
rx_done	1’b0	Output	1	When rx_count=7, rx_done is ‘1’. Indicates completion of a byte reception.
tx_done	1’b0	Output	1	When tx_count=7, tx_done is ‘1’. Indicates completion of a byte transmission.

Table 1: Pin Description

Registers			
Name	Default Value	Width	Description
rx_count	3’d0	3	Increments by one after reception of every bit (Counts from 0 to 7).
tx_count	3’d0	3	Increments by one after transmission of every bit (Counts from 0 to 7).
sr	8’d0	8	Mosi is shifted into the LSB of sr at rising edge of s_clk and MSB of sr is shifted

			onto miso at the falling edge of s_clk.

Table 2: Registers Description

3. Transaction Structure

1. Master should pull down the slave select to enable the slave.
2. Master should provide the s_clk for transaction.
3. Data from master is received over **mosi** and shifted into LSB of sr.
4. Upon receiving one bit of data, slave transmits one bit of data to the master i.e., MSB of sr is shifted onto **miso.**
5. tx_count increments by one after the transmitting every bit.
6. rx_count increments by one after the receiving every bit.
7. If load='1', data_in is loaded into sr for transmission.
8. If (rx_e==0 and rx_count==4'd7) then the received byte from sr is loaded into data_out bus.

4. Verification Goals

For SPI Slave block Test bench acts as a MASTER system as well as configurations register block. Since SPI Slave is an interface block testbench should cover the ports at both sides of the slave block.

1. Slave should be capable of shifting the received bit at the rising edge of s_clk.
2. Slave should be capable of transmitting the bit at the falling edge of s_clk.
3. Count of transmitted and received bits should be updated to indicate the completion of transaction.

Serial No.	Test Cases	Results
1.	Transaction occurs only when ss=0	If ss=0, all the ports and registers take the default value.
2.	Full duplex verification	Data transmission and reception are done together. Data is loaded into sr when load=1 and transmitted over miso bit by bit during falling edge of s_clk. Data is received bit by bit through mosi and shifted into LSB of sr during rising edge of s_clk. After receiving 8 bits data is loaded into data_out.

Table 3: Test Cases

5.Simulation Results

a. 05h is transmitted to the master and 55h is received from the master

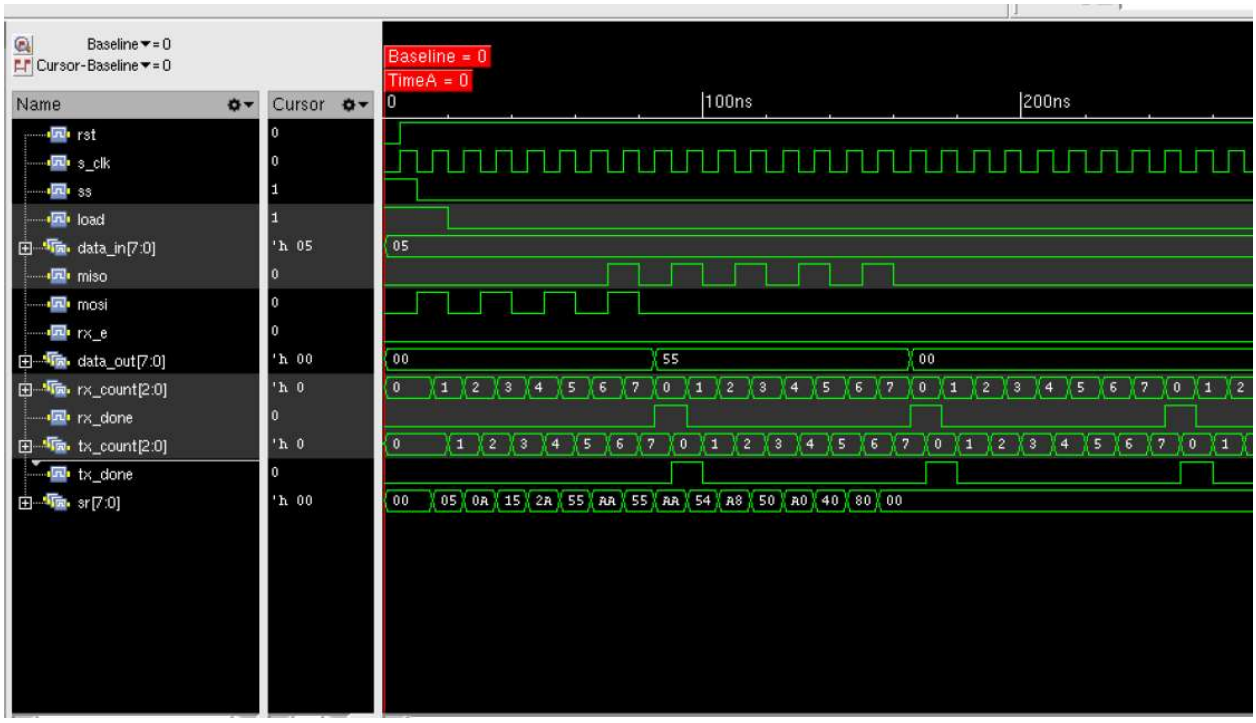

Figure 3: Simulation Waveform