

TVL S143 02 AC0 Engineering Specification

1. Scope

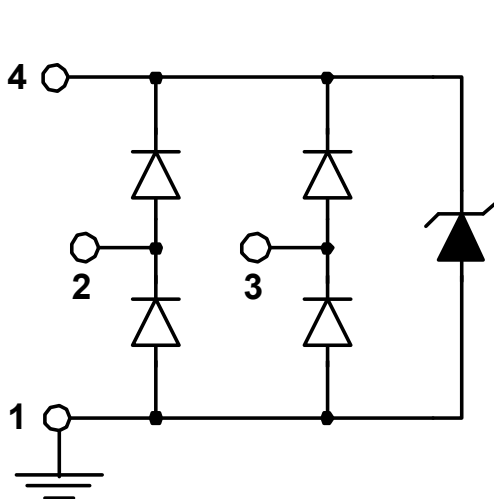
TVL S143 02 AC0's are TVS arrays designed to protect high-speed signal lines from overvoltage hazard of Electrostatic Discharge (**ESD**), Electrical Fast Transients (**EFT**) and **Lightning**. These interfaces can be used for USB2.0 power and data lines protection, notebook and personal computers, monitors and flat panel displays, IEEE 1394 Firewire ports, etc. The ESD protection of TVS arrays meets the immunity standard of IEC 61000-4-2, level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

2. Explanation of Part Number

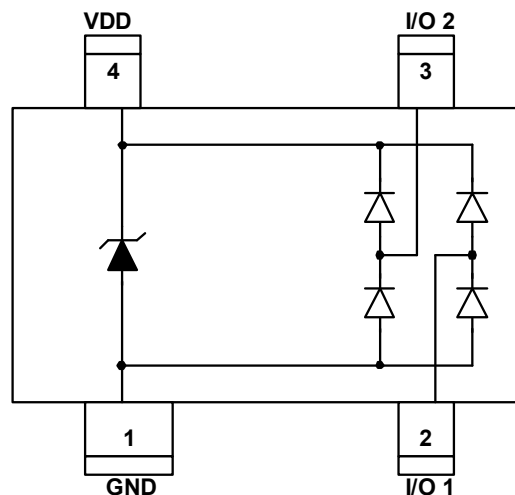
<u>TV</u>	<u>L</u>	<u>S143</u>	<u>02</u>	<u>AC0</u>
(1)	(2)	(3)	(4)	(5)

- (1) Product Type : TV=TVS Diode
- (2) Capacitance Code : L=Low Capacitance
- (3) Package Size Code
- (4) Channel Code : 02=2 Channels
- (5) Specialized Specification Code

3. Circuit Diagram /Pin Configuration



Circuit Diagram



Pin Configuration
SOT143-4L (Top View)

4. Specifications

4.1. ABSOLUTE MAXIMUM RATINGS

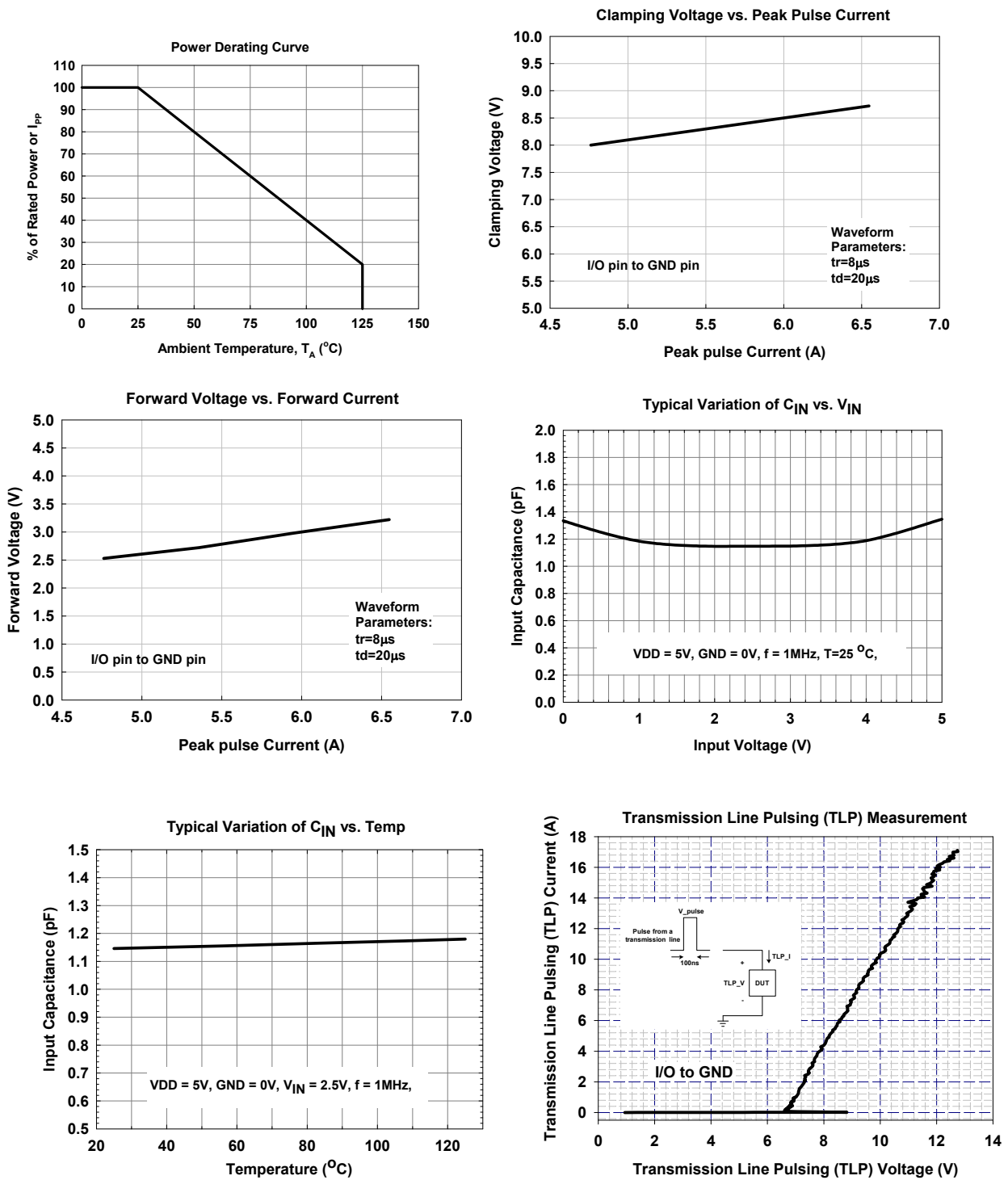
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I _{PP}	6	A
Operating Supply Voltage (VDD-GND)	V _{DC}	6	V
ESD per IEC 61000-4-2 (Air)	V _{ESD}	17	kV
ESD per IEC 61000-4-2 (Contact)		12	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V _{IO}	(GND – 0.5) to (VDD + 0.5)	V

Notes: Pins are plated with pure tin.

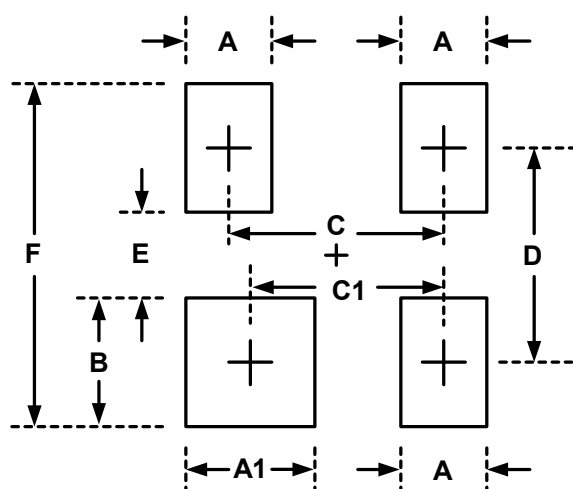
4.2. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Pin 4 to pin 1, T=25 °C			5	V
Reverse Leakage Current	I _{Leak}	V _{RWM} = 5V, T=25 °C, Pin 4 to pin 1			2	μA
Channel Leakage Current	I _{CH_Leak}	V _{Pin 4} = 5V, V _{Pin 1} = 0V, T=25 °C			1	μA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C Pin 4 to Pin 1	6.2			V
Forward Voltage	V _F	I _F = 15mA, T=25 °C Pin 1 to Pin 4		0.8	1	V
Clamping Voltage	V _{CL}	I _{PP} =5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.1	9	V
ESD Holding Voltage	V _{hold}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground.		13		V
Channel Input Capacitance	C _{IN}	V _{pin4} = 5V, V _{pin1} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Any Channel pin to Ground		1.2	1.4	pF
Channel to Channel Input Capacitance	C _{CROSS}	V _{pin4} = 5V, V _{pin1} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Between Channel pins		0.1	0.12	pF
Variation of Channel Input Capacitance	ΔC _{IN}	V _{pin4} = 5V, V _{pin1} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Channel_x pin to Ground - Channel_y pin to Ground		0.04	0.06	pF

4.3. TYPICAL CHARACTERISTICS



5. LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	1.00	0.039
A1	1.40	0.055
B	1.40	0.055
C	1.92	0.076
C1	1.72	0.068
D	2.20	0.087
E	0.80	0.031
F	3.60	0.141

Notes: This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

6. Application information

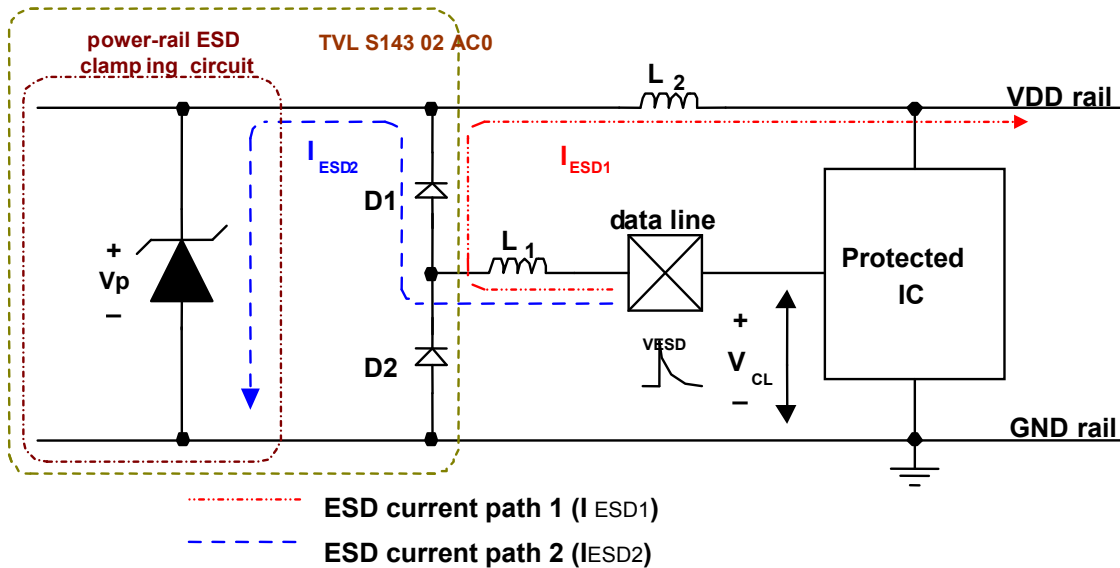
The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

$$V_{CL} = \text{Fwd voltage drop of D1} + \text{Breakdown voltage drop of D3} + \text{supply voltage of VDD rail} + L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

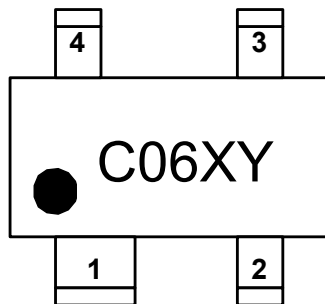
An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL} ! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The TVL S143 02 AC0 has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.



7. MARKING CODE

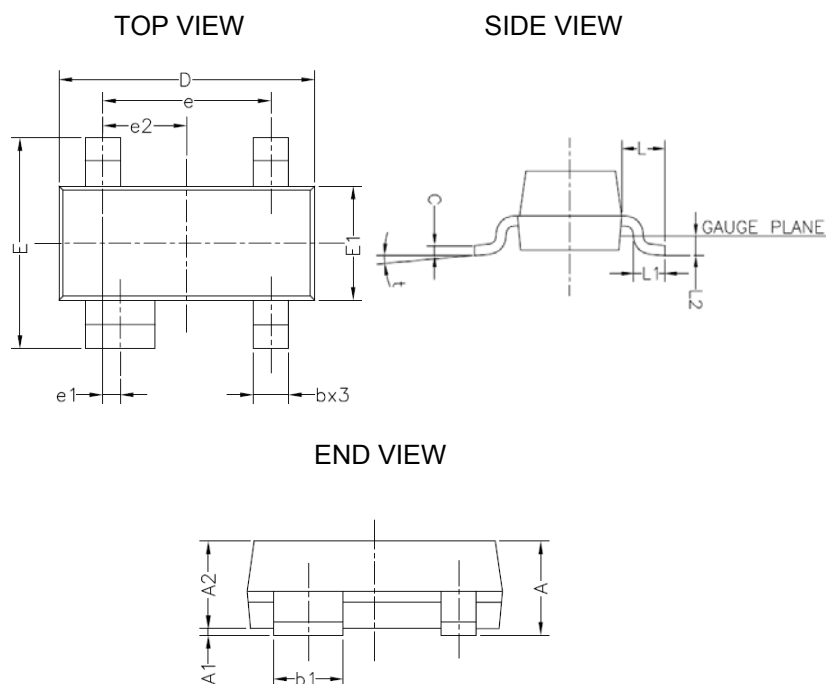
Marking Code: C06XY



C06= Device Code
X= Date Code
Y=Control Code

8. Mechanical Details

SOT-143-4L PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.95	1.17	0.037	0.046
A1	0.05	0.1	0.002	0.004
A2	0.9	1.1	0.035	0.043
b	0.35	0.5	0.014	0.020
b1	0.76	0.89	0.030	0.035
C	0.09	0.18	0.004	0.007
D	2.8	3.04	0.110	0.120
E1	1.2	1.4	0.047	0.055
E	2.25	2.55	0.089	0.100
e1	0.20 BSC		0.0078 BSC	
e2	0.96 BSC		0.0377 BSC	
e	1.8	2.02	0.071	0.080
L	0.55 REF.		0.0216 BSC	
L1	0.3	0.6	0.012	0.024
L2	0.25 REF		0.0098 BSC	
t	0~9°		0~9°	

8.1. Taping Quantity:
3000pcs/ Tube