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Predictable Success

Synthesizing OpenSPARC Design in 90nm Technology Library

Overview

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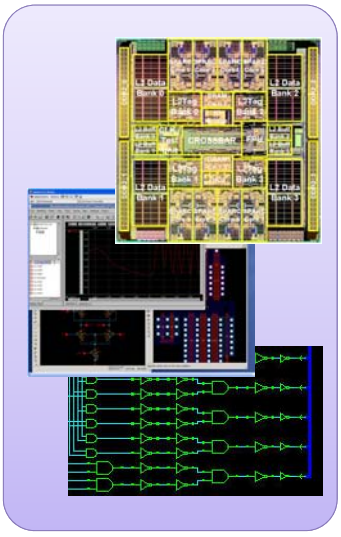
- Expediency of using OpenSPARC in educational process
- Capabilities of 90nm Educational Design Kit
- Use of OpenSPARC in Synopsys University Programs

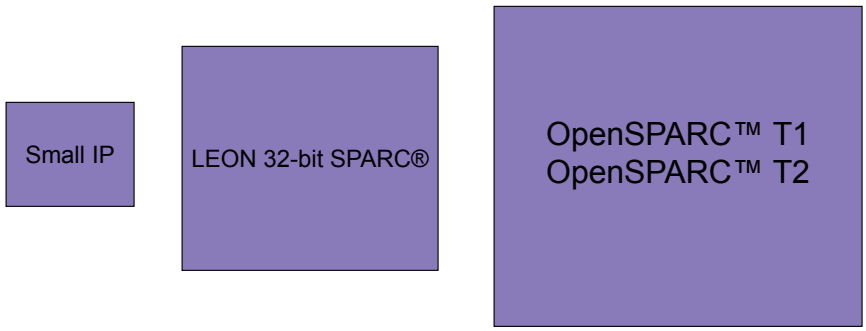
Expediency of Using OpenSPARC in Educational Process

Necessary Means in University Designs

- Open Source hardware IPs
- EDA tools from most well-known vendors (e.g. Synopsys)
- Open Source Educational Design Kits (EDKs)



Need for Open Source Processors



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Availability of OpenSPARC for Design

- Complete Solution
  - Full implementation - CPU core, FPU, L2 in Verilog
  - Tools – Verification suite, Simulation, Performance, Compiler optimization tools
  - Multiple OpenSource Operating Systems: Solaris 10, Linux, FreeBSD, etc
- All Open Source on the web
  - RTL (Verilog) of OpenSPARC design
  - Synthesis scripts for RTL
  - Verification test suites
  - UltraSPARC Implementation Specification
  - Full OpenSPARC simulation environment

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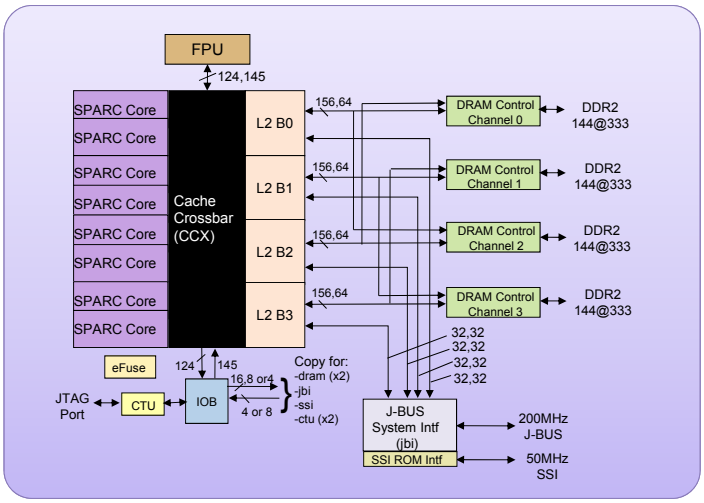
Attraction of OpenSPARC Architecture from the Viewpoint of Educational Process



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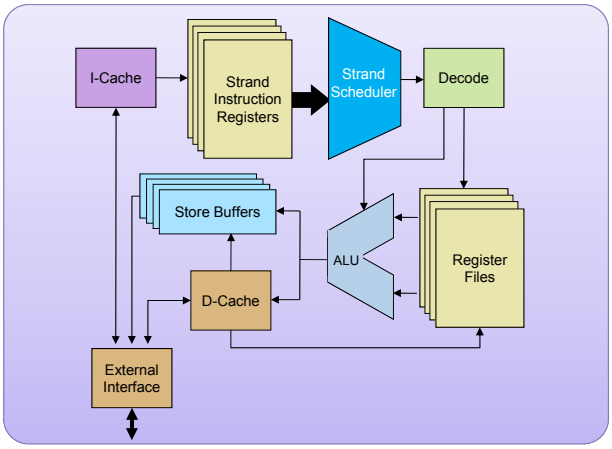
Attraction of Separate Functional Blocks of OpenSPARC from the Viewpoint of Educational Process



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OpenSPARC usage in Synopsys Curriculum

- Megacells design
- OpenSPARC Design
- Laboratory works preparation

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90nm EDK: OpenSPARC T1 Megacells

- Uses 90nm EDK 1P9M 1.2V/2.5V process
- Designed cells needed for OpenSPARC T1 core synthesis
- Contains 15 cells

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OpenSPARC T1 Megacells: Cell List

No	Functional name	Cell Name	Type	Size	Ports
1.	Data Cache (Data)	br_r_dcd	SRAM	9KB = 128 entries x 4 way x 16B x 9b	1
2.	FP register file	bw_r_frf	SRAM	8KB (128 x 78b)	1
3.	Instruction Cache (Data)	bw_r_icd	SRAM	16KB (32B line, 4 way)	1
4.	I and D cache tag	bw_r_idct	SRAM	128 entry x 33b x 4 way	1
5.	Integer register file	bw_r_irf	RF	32 entry x 72bit x 4 threads	3 Read, 2 Write
6.	Store buffer	bw_r_scm	CAM	Bank1: 32 entries x 38b, Bank2: 32 entries x 8b	1 look-up, 1 R/W
7.	iTLB, dTLB	bw_r_tlb	CAM	64-entry x 59 bits	1
8.	Reg file	bw_r_rf16x128d	RF	16 entry x 128b	1 read, 1 write
9.	Reg file	bw_r_rf16x160	RF	16 entry x 160b	1 read, 1 write
10.	Reg file	bw_r_rf16x32	RF	16 entry x 32b	1 read, 1 write
11.	Reg file	bw_r_rf32x108	RF	32 entry x 108b	1 read, 1 write
12.	Reg file	bw_r_rf32x152b	RF	32 entry x 152b	1 read, 1 write
13.	Reg file	bw_r_rf32x80	RF	32 entry x 80b	1 read, 1 write
14.	Reg file	bw_r_rf16x65	RF	16 entry x 65b	1 read, 1 write
15.	Reg file	bw_r_rf16x81	RF	16 entry x 81b	1 read, 1 write

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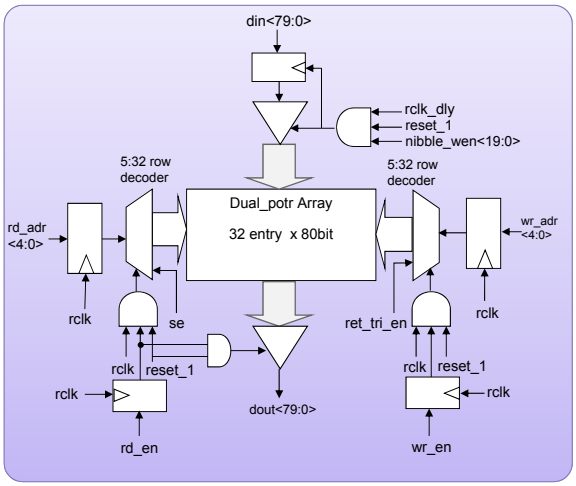
OpenSPARC T1 Megacells: Functional Block Diagram of RF32x80 Register File



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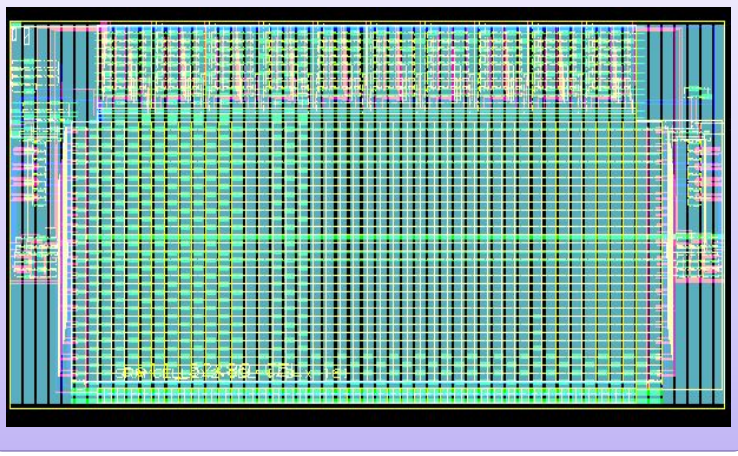
OpenSPARC T1 Megacells: Layout of RF32x80 Register File



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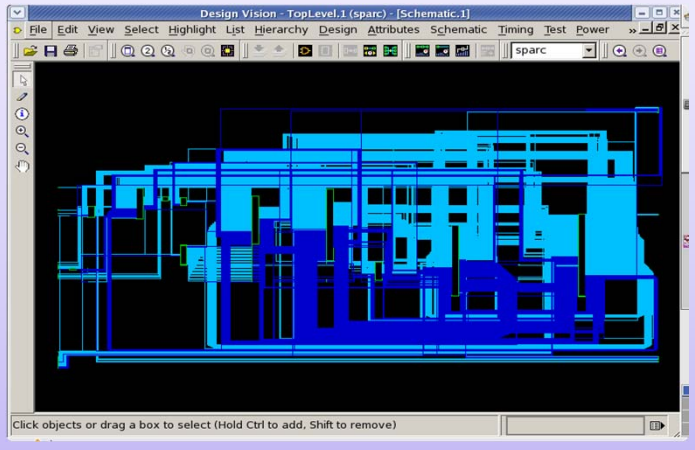
OpenSPARC Design



Design view of OpenSPARC

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Constraints for OpenSPARC design

```
set default_clk gclk
set default_clk_freq  1200
set default_setup_skew  0.1
set default_hold_skew  0.1
set default_clk_transition
0.04
set clk_list {{
gclk   1200.0   0.100
0.100   0.040
}}
```

Constraints for OpenSPARC synthesis

OpenSPARC T1 and 90nm educational technology library

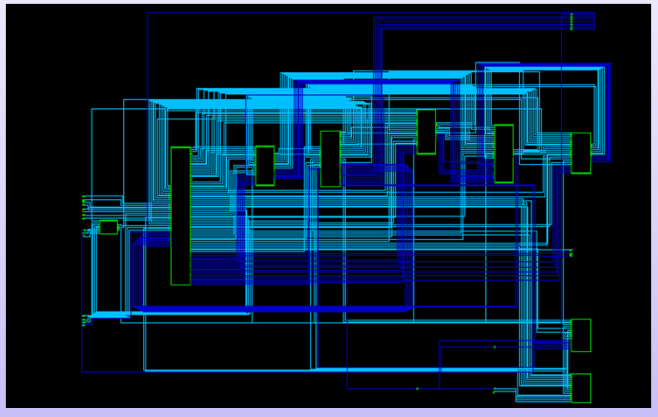
- **Using Synopsys Design Compiler to Synthesize an OpenSPARC T1 Floating-Point Unit**
  - Laboratory work 1. Reading the Design in Design Compiler and Synthesize the design with timing constraints
  - Laboratory work 2. Synthesize the design with area constraints

Laboratory1

In this lab the Floating-Point Unit (FPU) of the OpenSPARC T1 design is synthesized.
The following tasks are completed:

- Setting up Libraries
- Invoke Design Vision
- Read the design into GUI
- Compile and Synthesize the design using timing constraints

Laboratory1



Design view of OpenSPARC FPU

Laboratory 2

In this lab the Floating-Point Unit (FPU) of the OpenSPARC T1 design will be synthesized using area and timing cosntraints.

The following tasks will be completed in this lab:

- Create a Design Compiler script file
- Invoke dc_shell
- Synthesize the design using area constraints

Constraints used in laboratory work

```
set lib_name saed90nm_typ
current_design fpu

#Reset all constraints
reset_design


#create clocK
create_clock -period 2
[get_ports gclk]
```


Thank You!