Test bench of JK Flip flop

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb4 IS
END tb4;

ARCHITECTURE behavior OF tb4 IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT jk1
   PORT(
        j : IN  std_logic;
        k : IN  std_logic;
        clk : IN  std_logic;
        q : INOUT  std_logic;
        qbar : INOUT  std_logic
       );
   END COMPONENT;
```

```
  --Inputs
  signal j : std_logic := '0';
  signal k : std_logic := '0';
  signal clk : std_logic := '0';

        --BiDirs
  signal q : std_logic;
  signal qbar : std_logic;

  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN

        -- Instantiate the Unit Under Test (UUT)
  uut: jk1 PORT MAP (
       j => j,
       k => k,
       clk => clk,
       q => q,
       qbar => qbar
      );

  -- Clock process definitions
```

```
  clk_process :process
  begin
                clk <= '0';
                wait for clk_period/2;
                clk <= '1';
                wait for clk_period/2;
  end process;


  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
 j <= '0', '1' after 10 ns, '0'after 20 ns, '1' after 30 ns;
 k <= '0', '0' after 10 ns, '1' after 20 ns;
    wait;
  end process;

END;
```

Test Bench of Decoder

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb1 IS
END tb1;

ARCHITECTURE behavior OF tb1 IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT dec
   PORT(
        i : IN  std_logic_vector(1 downto 0);
        o : OUT  std_logic_vector(3 downto 0);
        en : IN  std_logic
       );
   END COMPONENT;
```

```
  --Inputs
  signal i : std_logic_vector(1 downto 0) := (others => '0');
  signal en : std_logic := '0';

        --Outputs
  signal o : std_logic_vector(3 downto 0);
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

  --constant <clock>_period : time := 10 ns;

BEGIN

        -- Instantiate the Unit Under Test (UUT)
  uut: dec PORT MAP (
       i => i,
       o => o,
       en => en
      );

  -- Clock process definitions


  -- Stimulus process
  stim_proc: process
```

```
  begin

    -- hold reset state for 100 ns.

    wait for 100 ns;


    --wait for <clock>_period*10;


   en <= '0', '1' after 50 ns;

i <= "00", "01" after 20 ns, "10" after 70 ns, "00" after 100 ns ;       -- insert stimulus here


    wait;

  end process;


END;
```