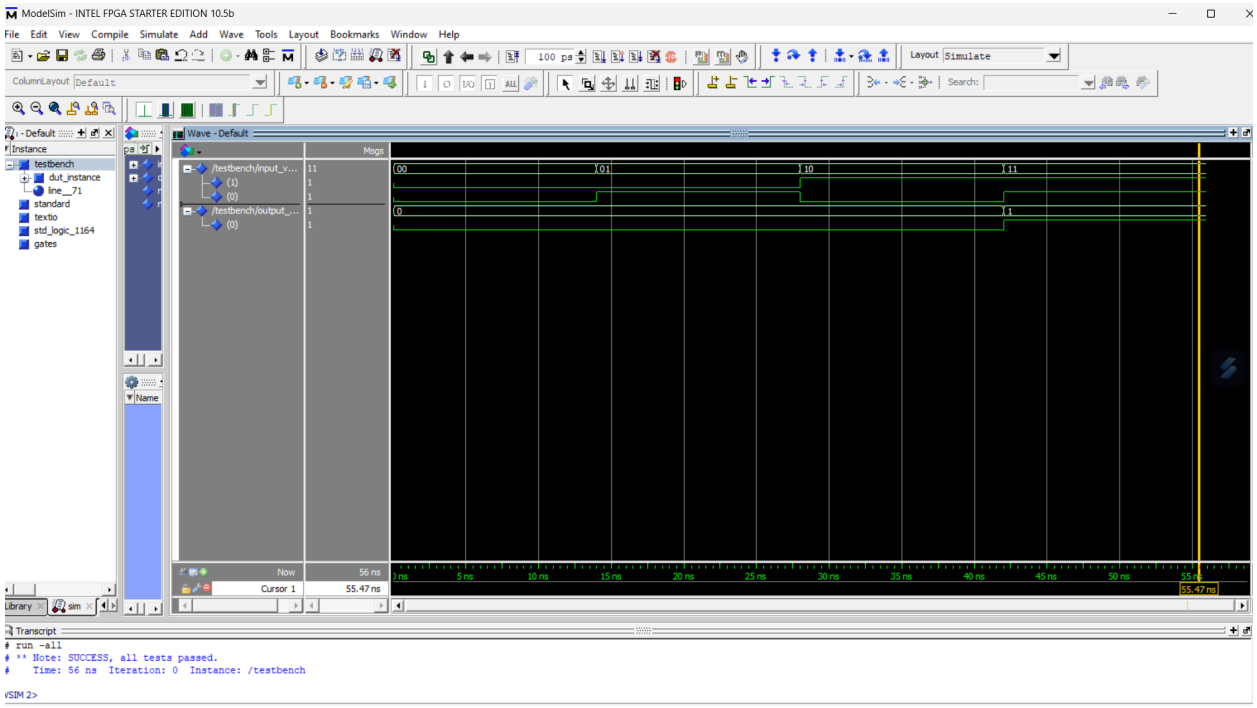
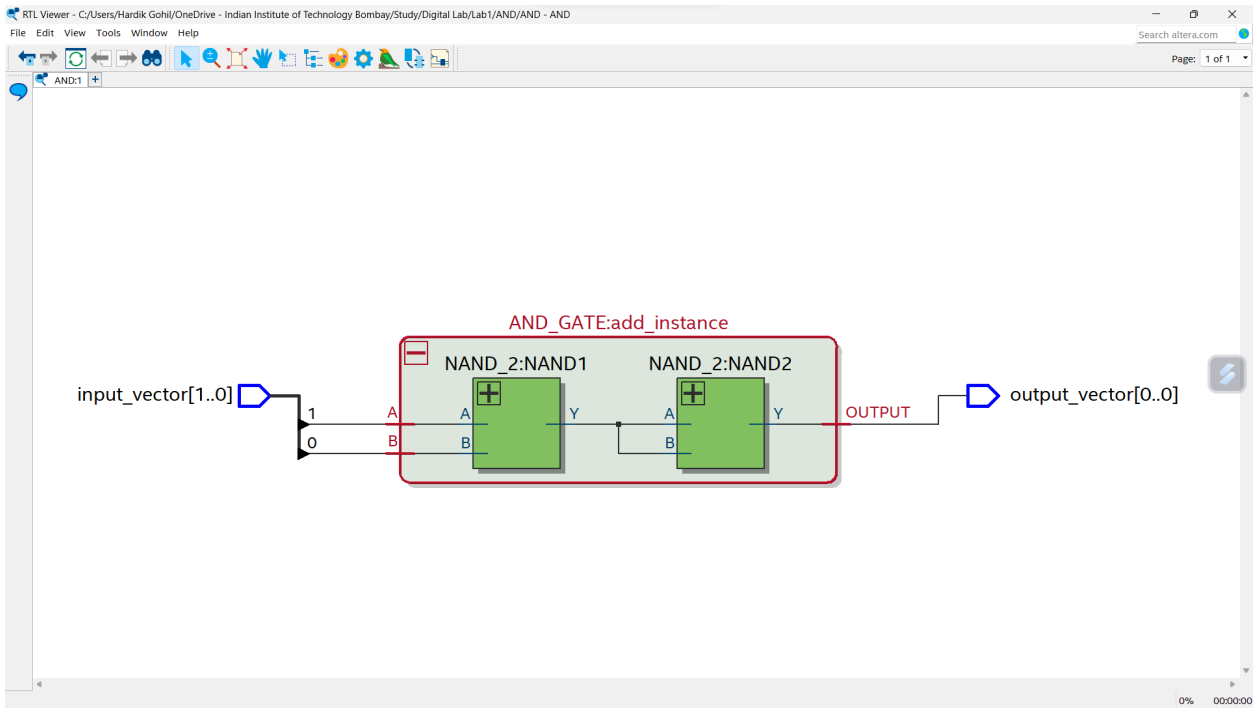
Lab 1 Report

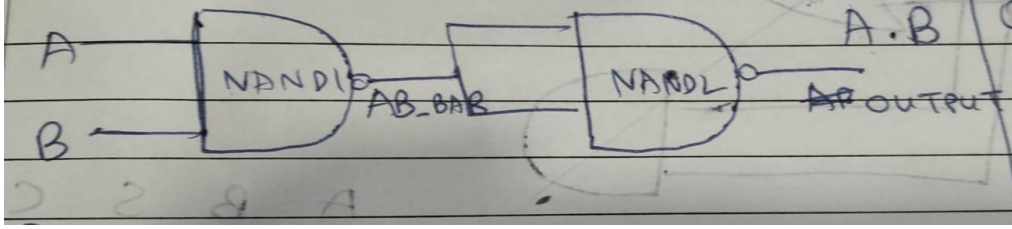
Experiment #1 : Design circuit elements using universal NAND gate

- AND Gate



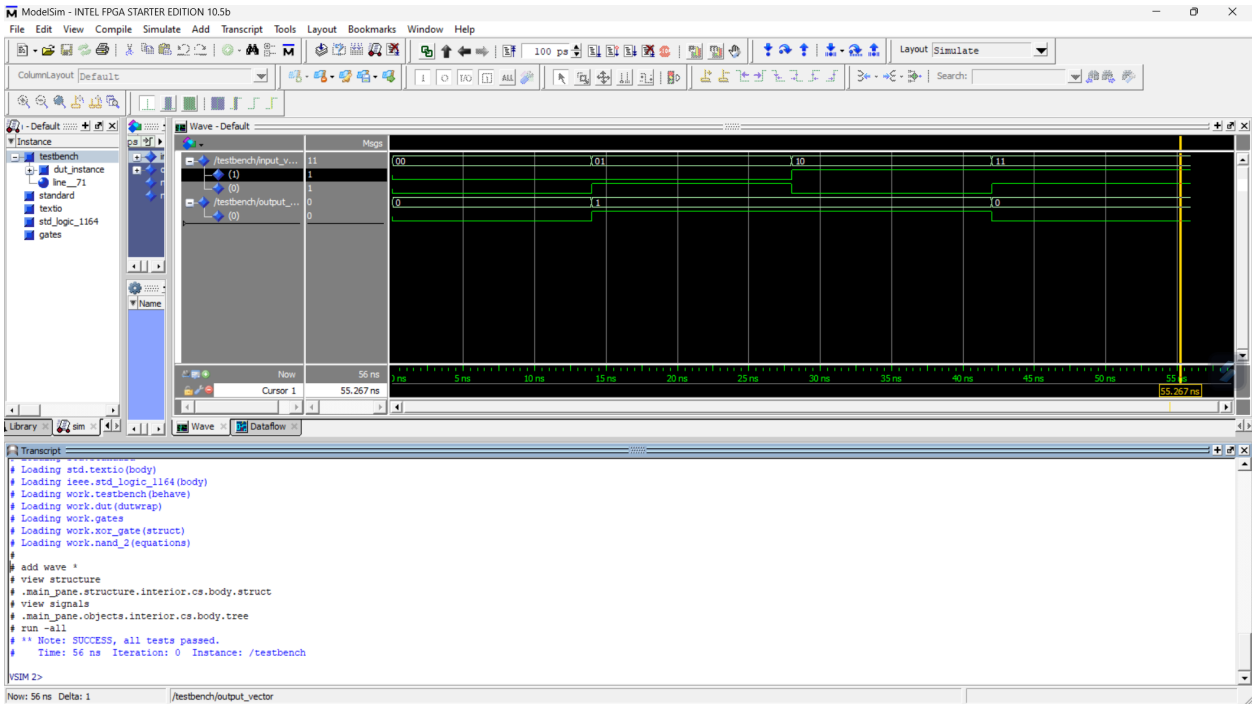


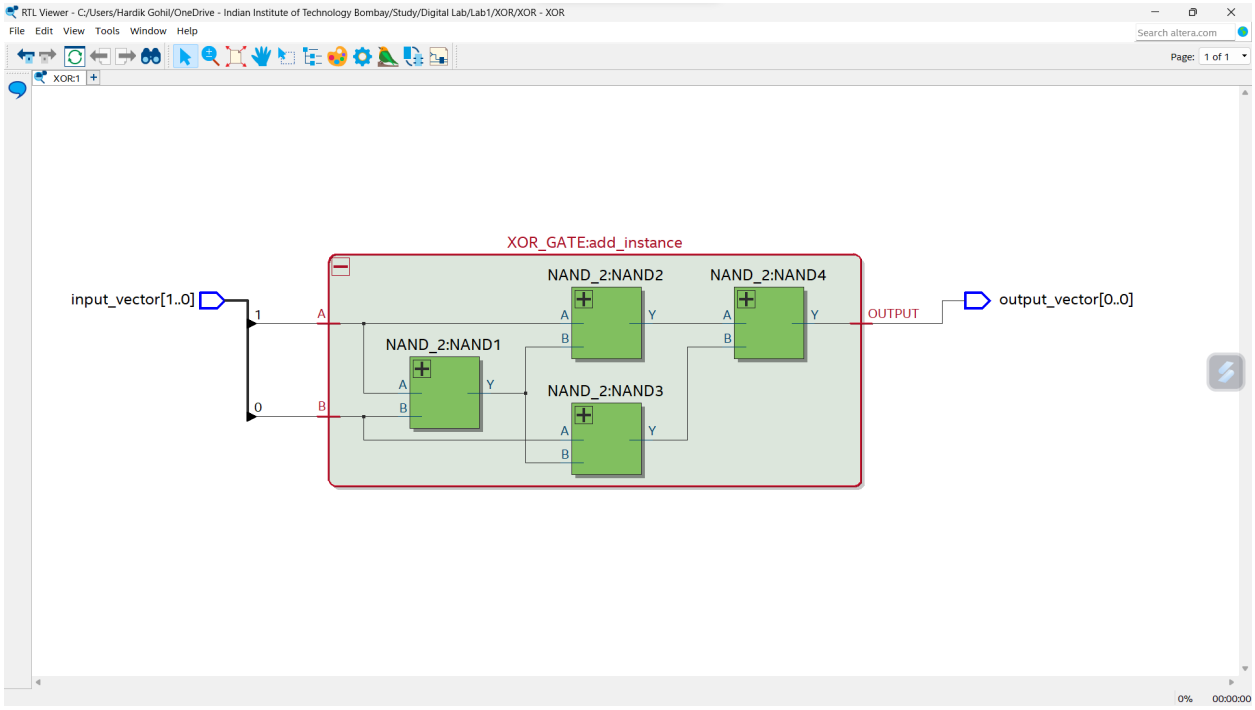
a) AND gate



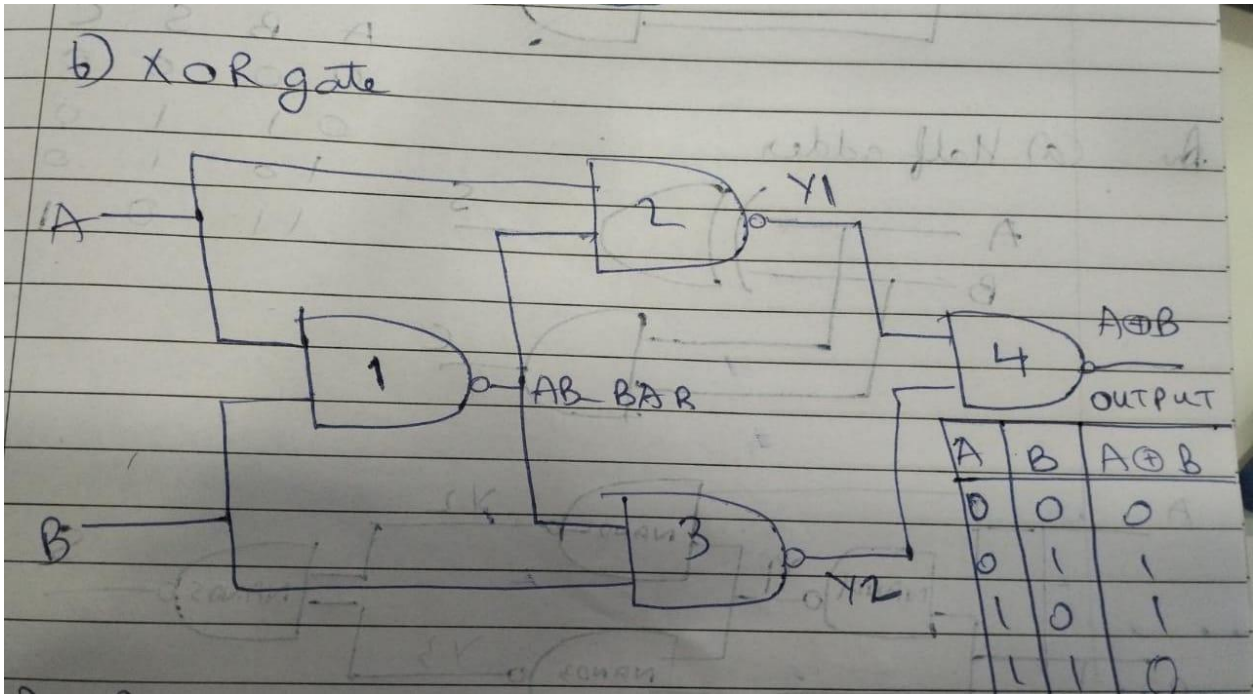
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

- XOR Gate


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
Wave - Default
Transcript
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.dut(dutwrap)
Loading work.gates
Loading work.xor_gate(struct)
Loading work.nand_2(equations)
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 56 ns Iteration: 0 Instance: /testbench
VSIM 2>
Now: 56 ns Delta: 1
/testbench/output_vector

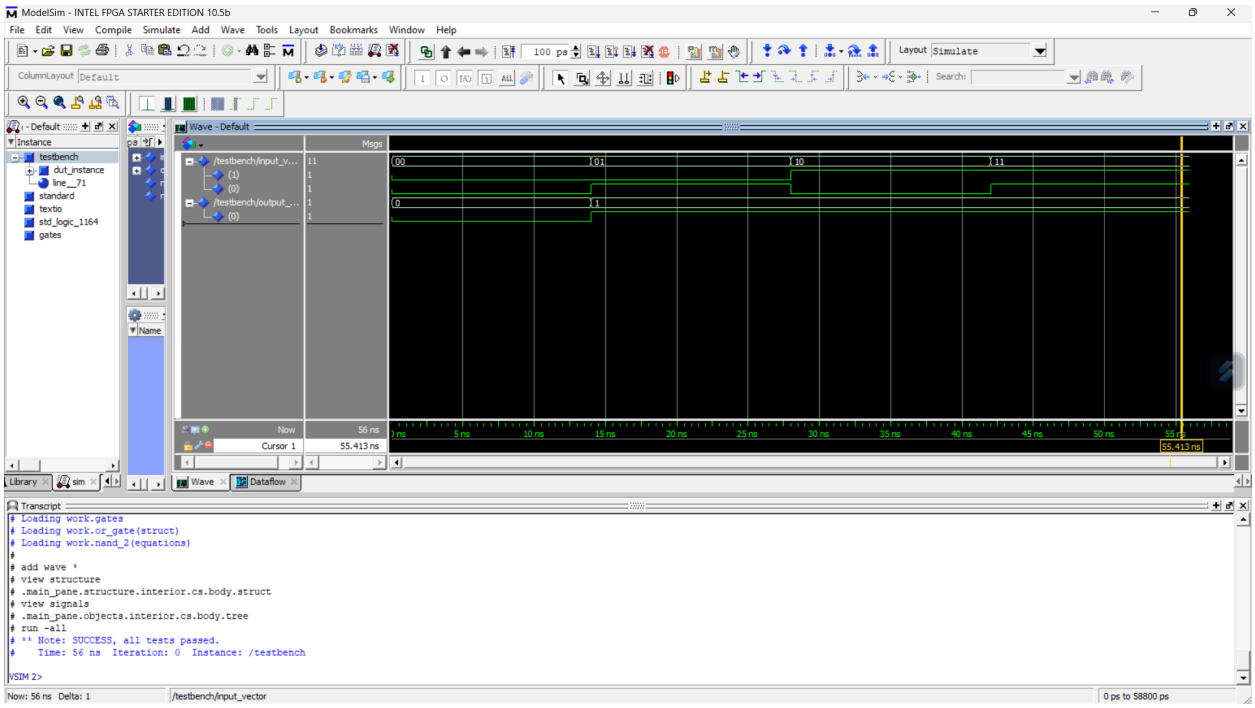

RTL Viewer - C:/Users/Hardik Gohil/OneDrive - Indian Institute of Technology Bombay/Study/Digital Lab/Lab1/XOR/XOR - XOR
File Edit View Tools Window Help
XOR:1
XOR_GATE:add_instance
input_vector[1..0]
1
0
A
B
NAND_2:NAND1
NAND_2:NAND2
NAND_2:NAND3
NAND_2:NAND4
Y
OUTPUT
output_vector[0..0]

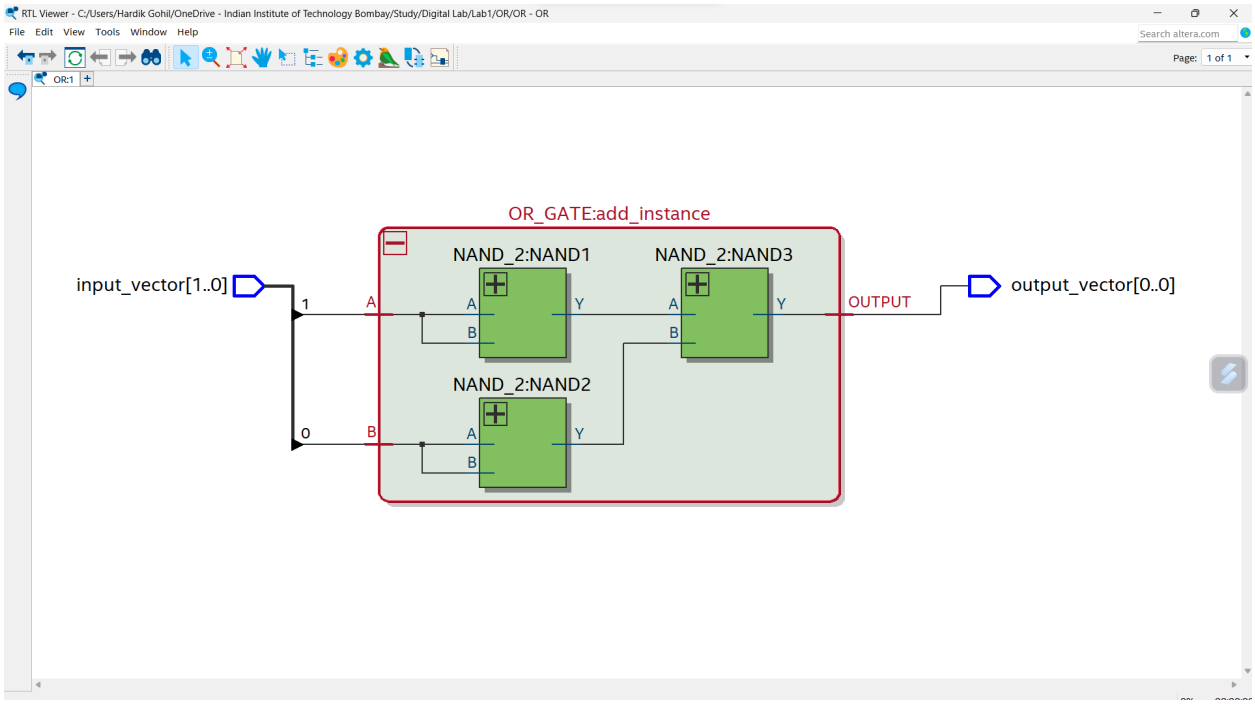
b) XOR gate

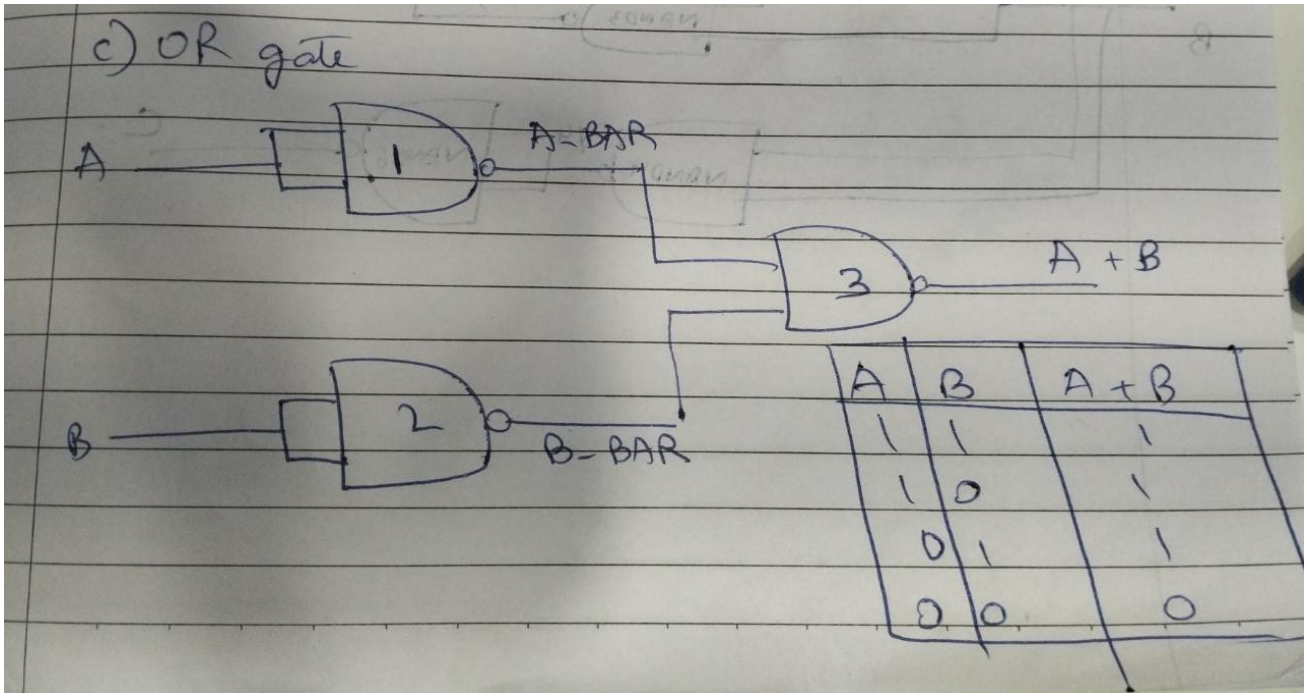


A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

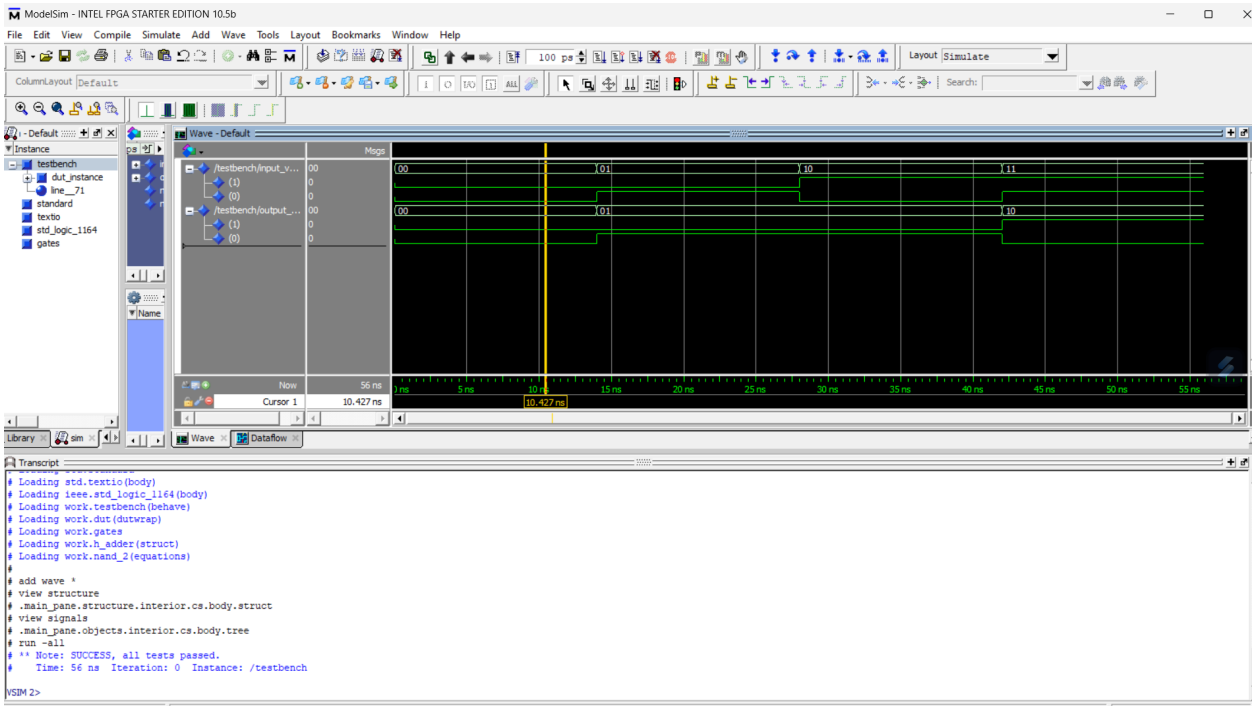
- OR Gate

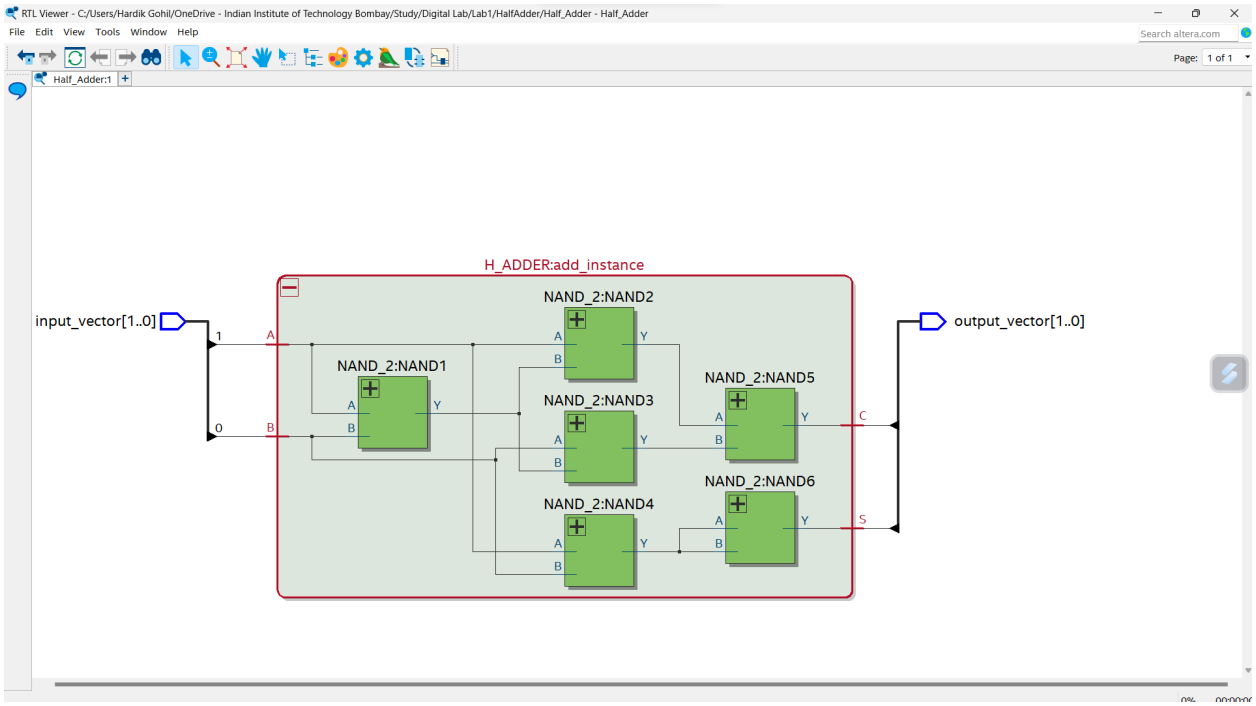

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/testbench/input_v...
/testbench/output_...
Now
Cursor 1
55.413 ns
Transcript
Loading work.gates
Loading work.or_gate(struct)
Loading work.nand_2(equations)
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 56 ns Iteration: 0 Instance: /testbench
VSIM 2>
Now: 56 ns Delta: 1
/testbench/input_vector
0 ps to 58800 ps

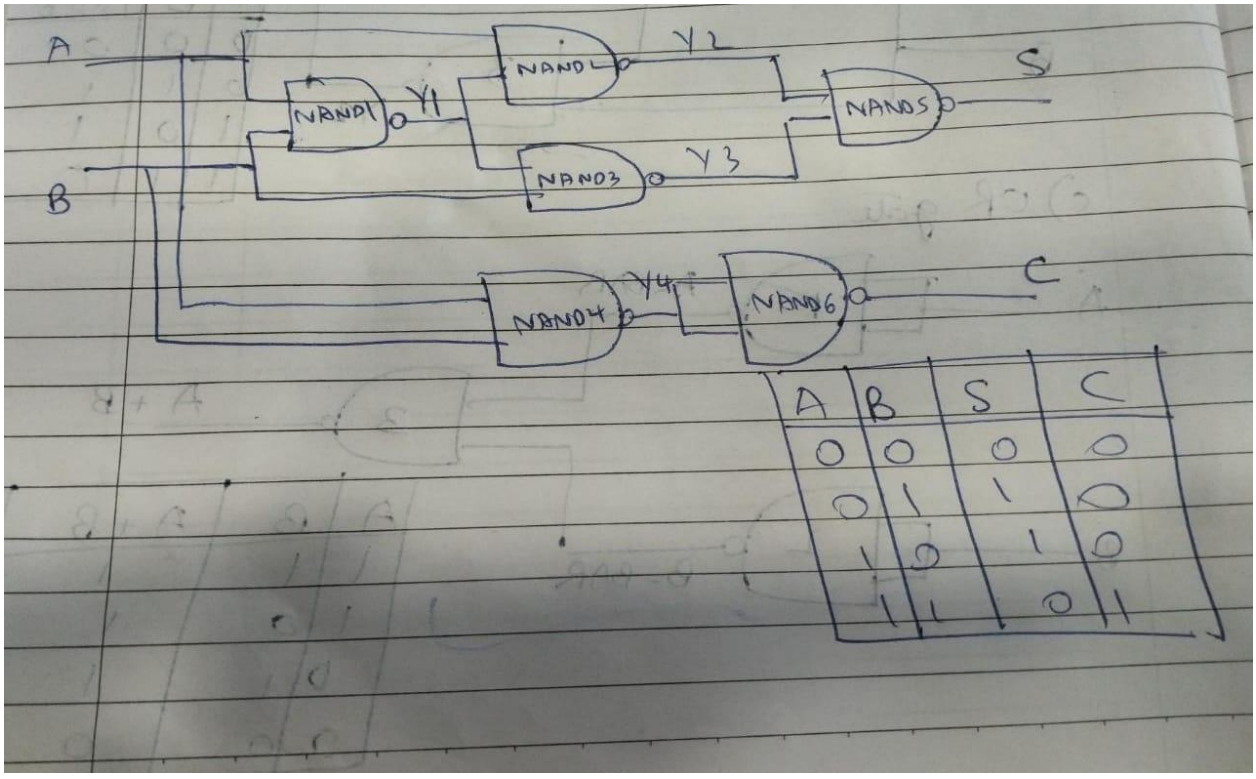

RTL Viewer - C:/Users/Hardik Gohil/OneDrive - Indian Institute of Technology Bombay/Study/Digital Lab/Lab1/OR/OR - OR
File Edit View Tools Window Help
OR:1
OR_GATE:add_instance
NAND_2:NAND1
NAND_2:NAND3
NAND_2:NAND2
input_vector[1..0]
output_vector[0..0]
OUTPUT
A
B
Y
1
0


c) OR gate
A
B
A-BAR
B-BAR
A + B
1
2
3
A B A+B
1 1 1
1 0 1
0 1 1
0 0 0

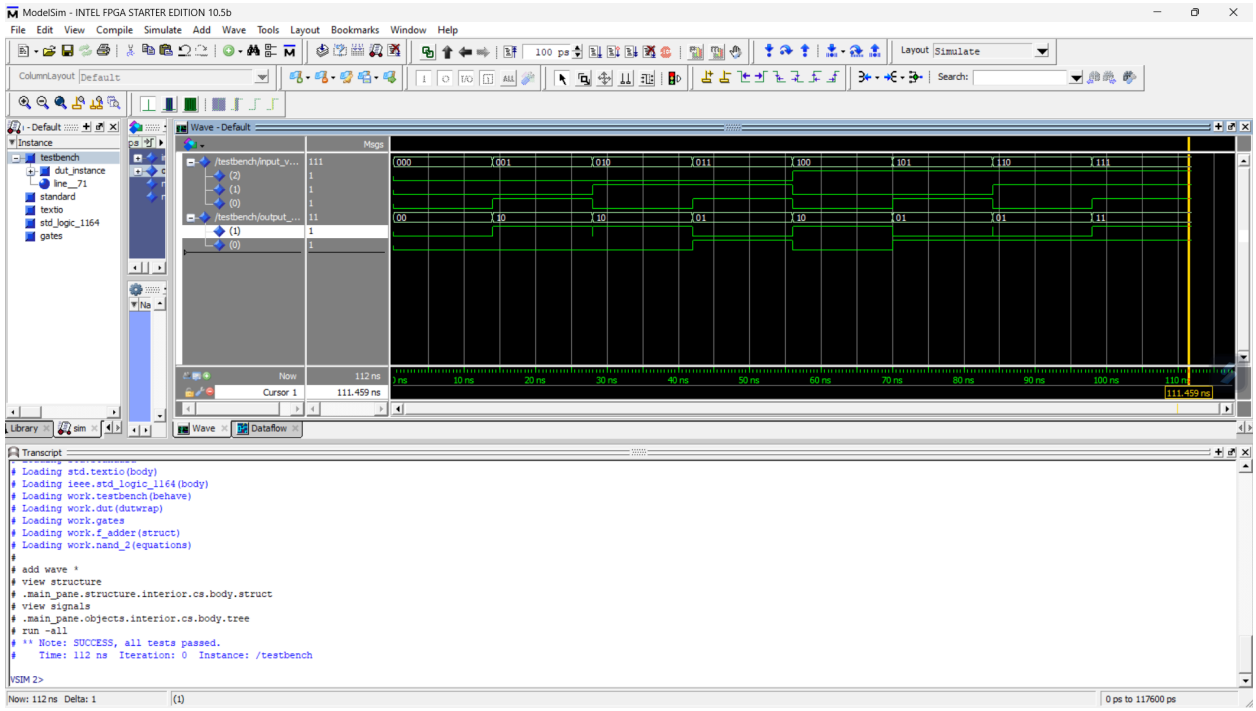
- Half adder

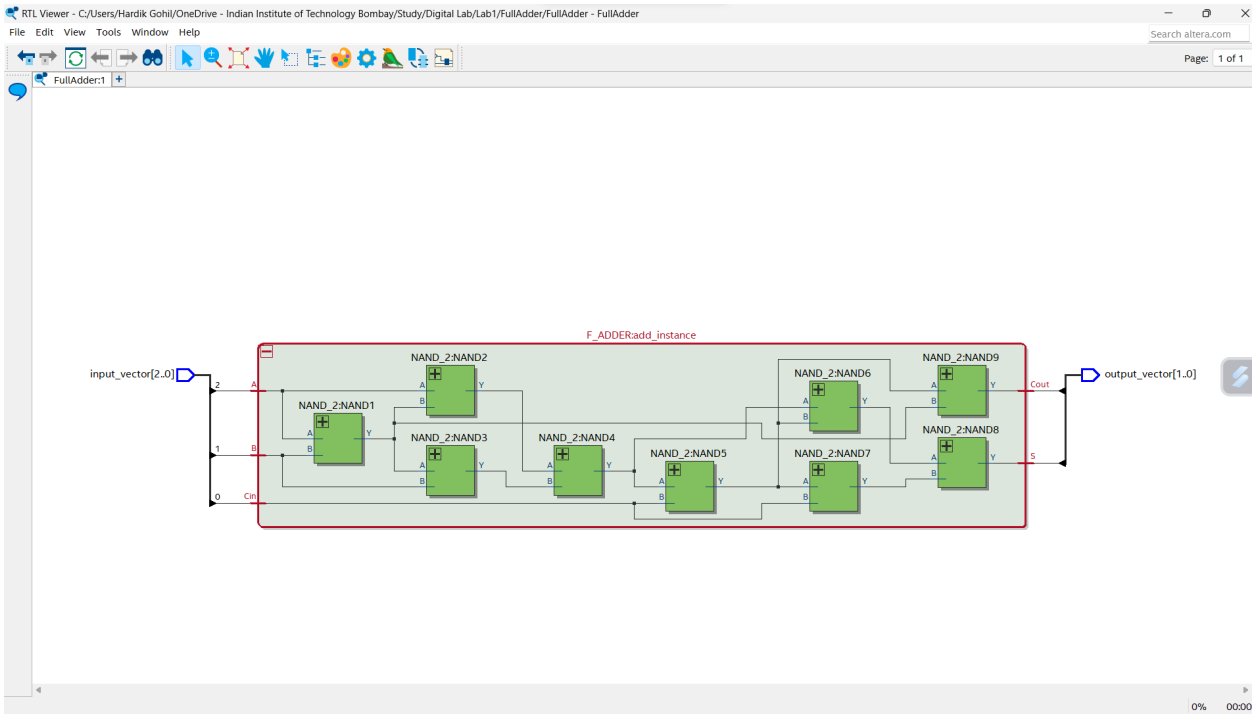

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Instance
testbench
dut_instance
line__71
standard
textio
std_logic_1164
gates
/testbench/input_v...
/testbench/output_...
Now
56 ns
Cursor 1
10.427 ns
Wave
Dataflow
Transcript
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.dut(dutwrap)
Loading work.gates
Loading work.h_adder(struct)
Loading work.nand_2(equations)
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 56 ns Iteration: 0 Instance: /testbench
VSIM 2>


RTL Viewer - C:/Users/Hardik Gohil/OneDrive - Indian Institute of Technology Bombay/Study/Digital Lab/Lab1/HalfAdder/Half_Adder - Half_Adder
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Half_Adder:1
H_ADDER:add_instance
input_vector[1..0]
output_vector[1..0]
NAND_2:NAND1
NAND_2:NAND2
NAND_2:NAND3
NAND_2:NAND4
NAND_2:NAND5
NAND_2:NAND6
A
B
Y
C
S
1
0


A
B
NAND1
NAND2
NAND3
NAND4
NAND5
NAND6
Y1
Y2
Y3
Y4
S
C
A B S C
0 0 0 0
0 1 1 0
1 0 1 0
1 1 0 1

- Full Adder


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/testbench/input_v...
/testbench/output_...
Now
Cursor 1
Transcript
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.dut(dutwrap)
Loading work.gates
Loading work.f_adder(struct)
Loading work.nand_2(equations)
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 112 ns Iteration: 0 Instance: /testbench
VSIM 2>


RTL Viewer - C:/Users/Hardik Gohil/OneDrive - Indian Institute of Technology Bombay/Study/Digital Lab/Lab1/FullAdder/FullAdder - FullAdder
File Edit View Tools Window Help
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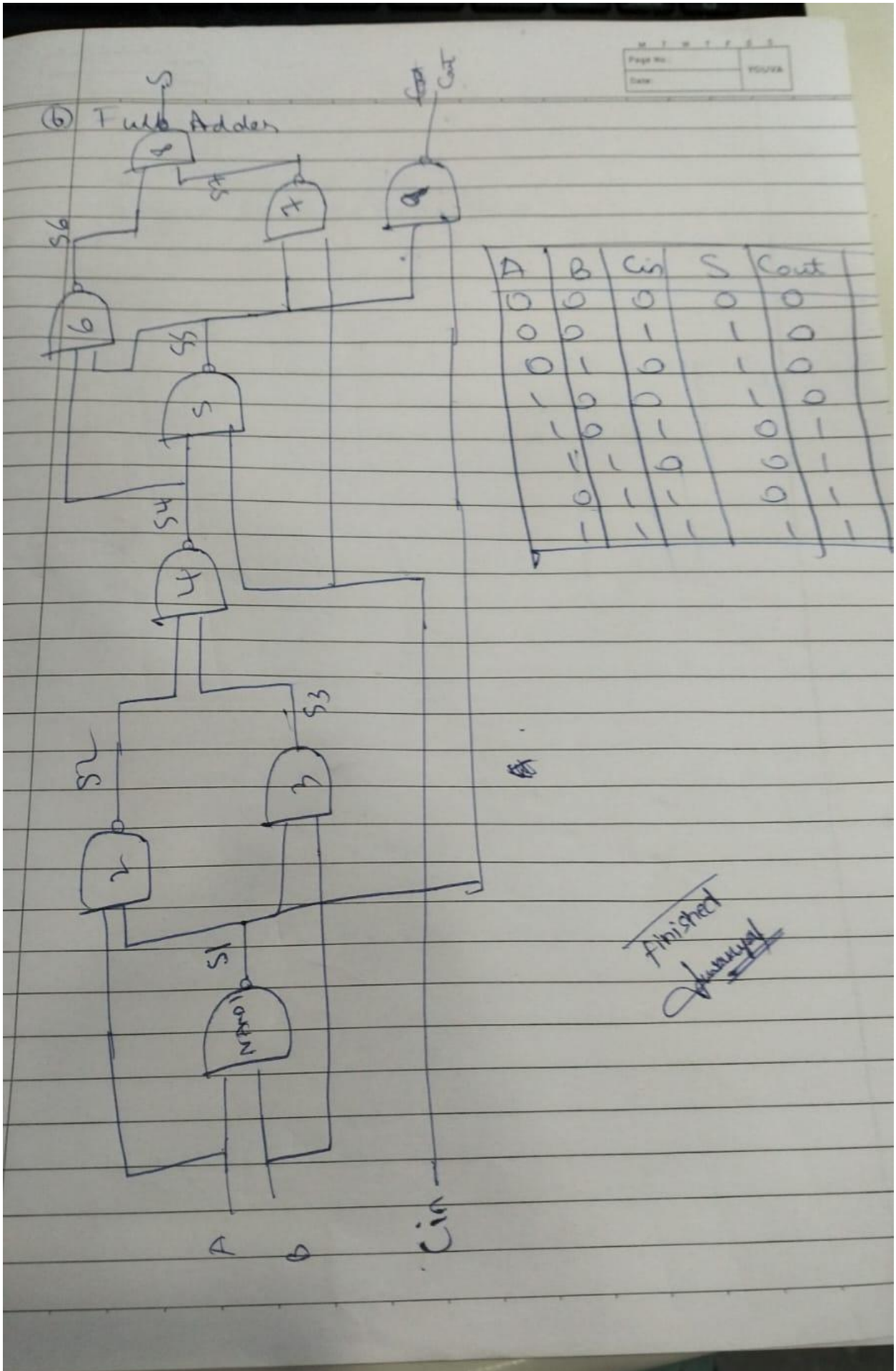
Page: 1 of 1
FullAdder:1
F_ADDER:add_instance
input_vector[2..0]
output_vector[1..0]
NAND_2:NAND1
NAND_2:NAND2
NAND_2:NAND3
NAND_2:NAND4
NAND_2:NAND5
NAND_2:NAND6
NAND_2:NAND7
NAND_2:NAND8
NAND_2:NAND9
Cout
S
Cin
0%
00:00



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Finished