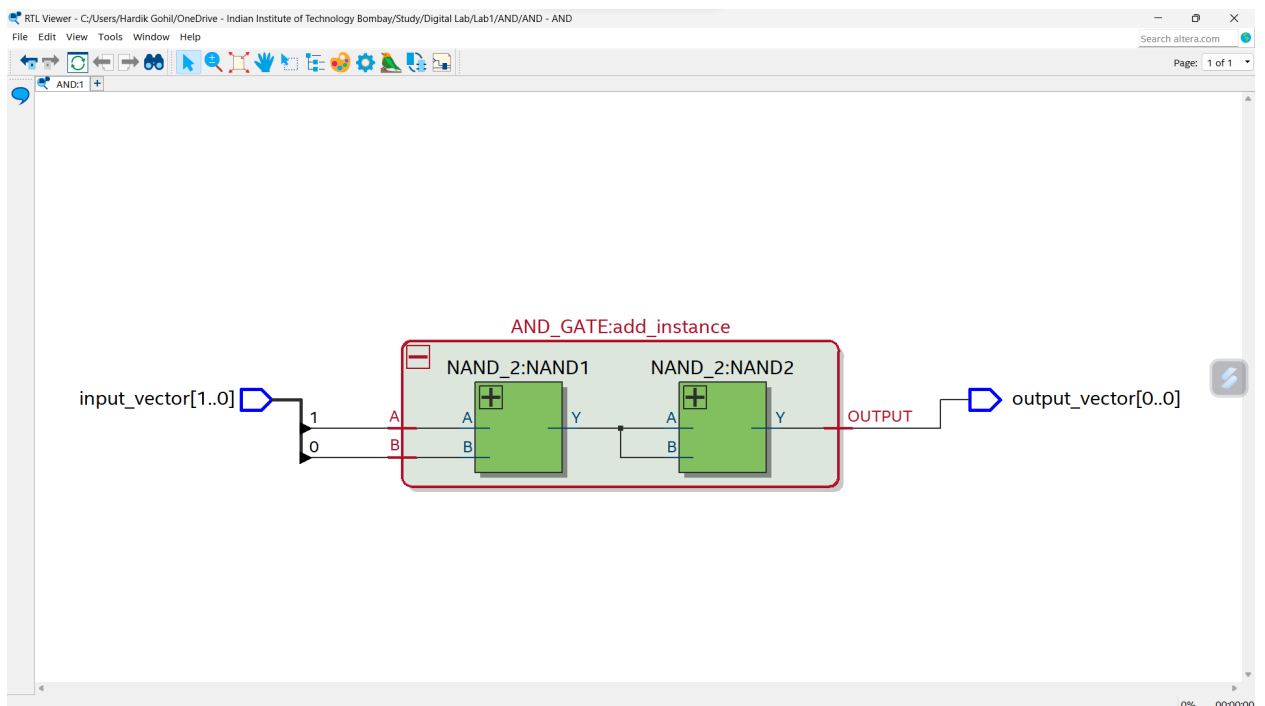
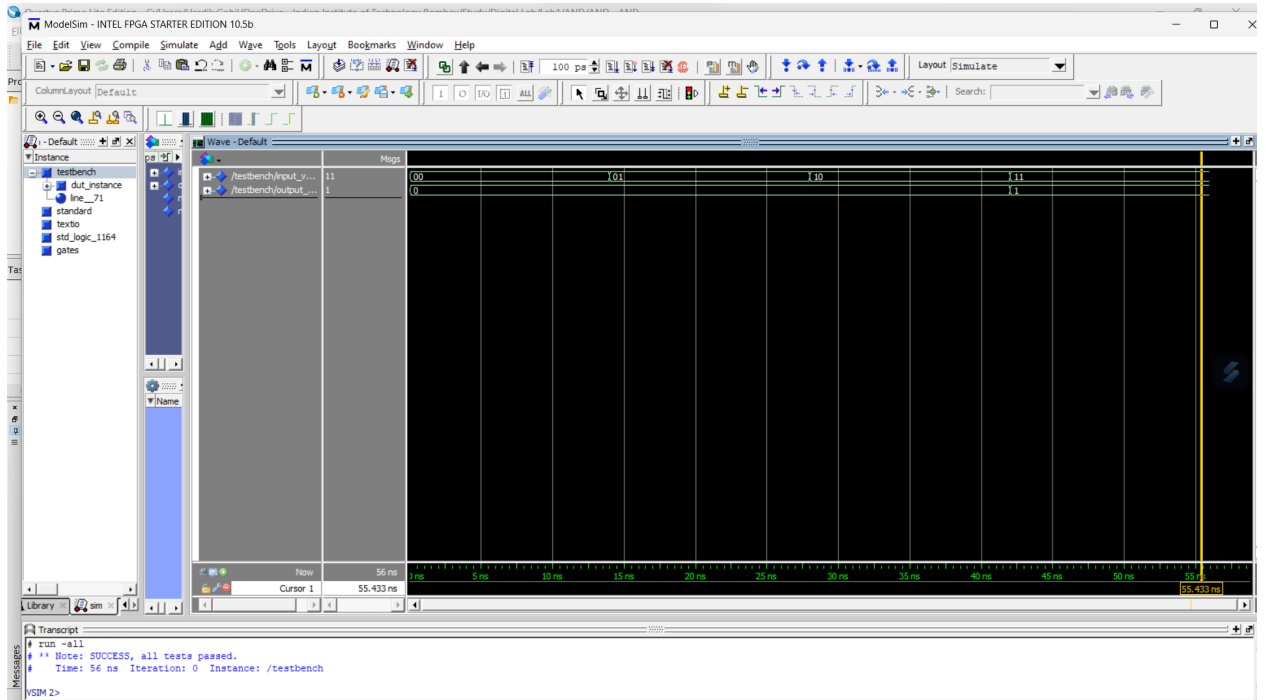


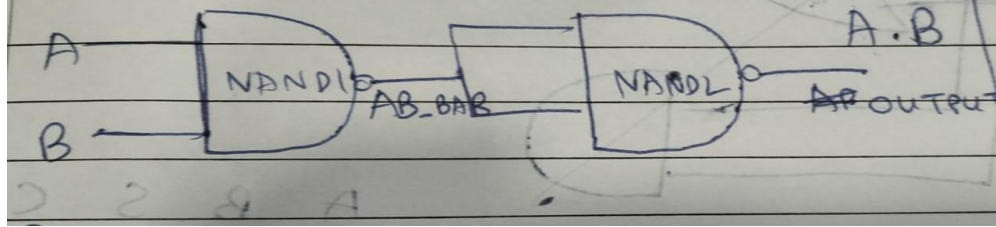
Lab 1 Report

Experiment #1 : Design circuit elements using universal NAND gate

- AND Gate

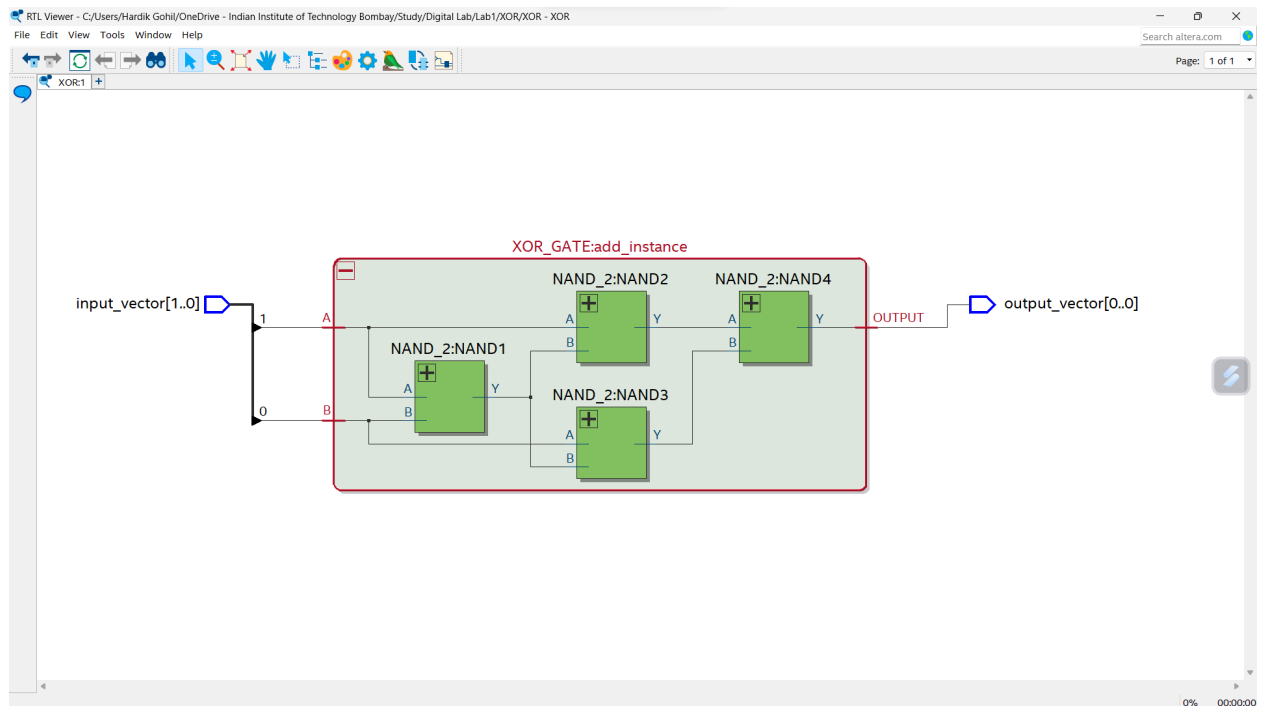
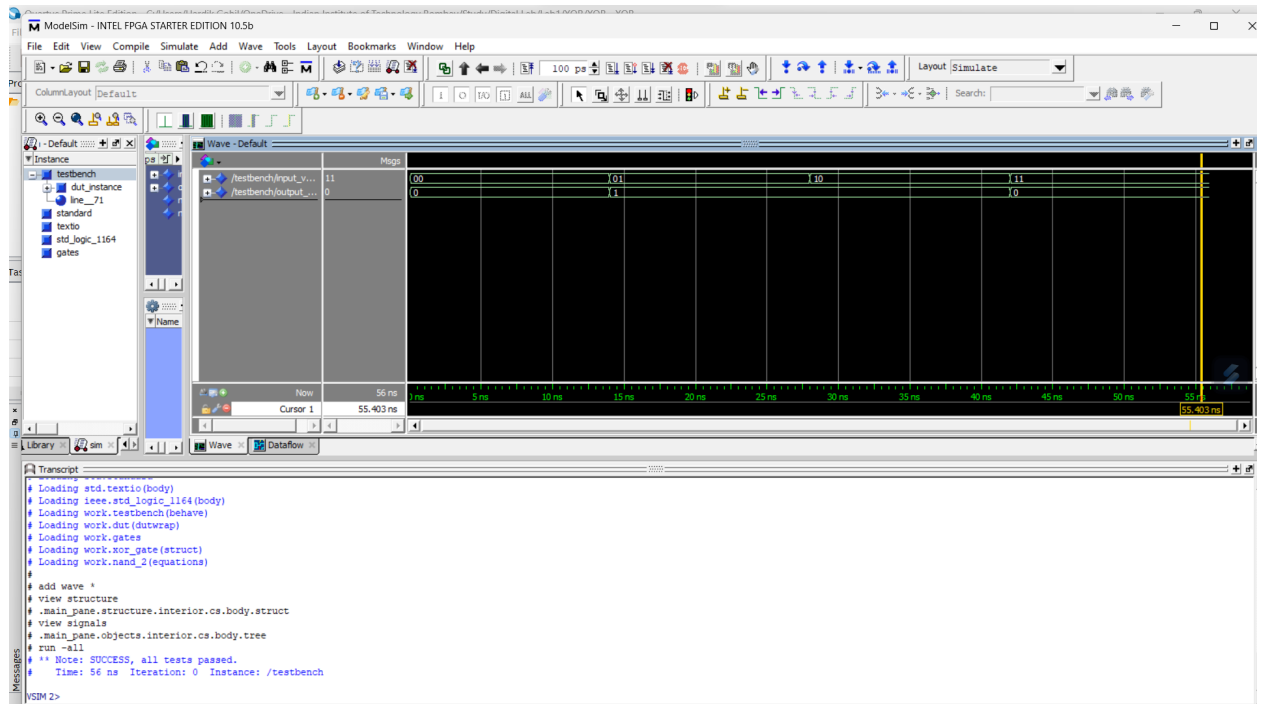


a) AND gate

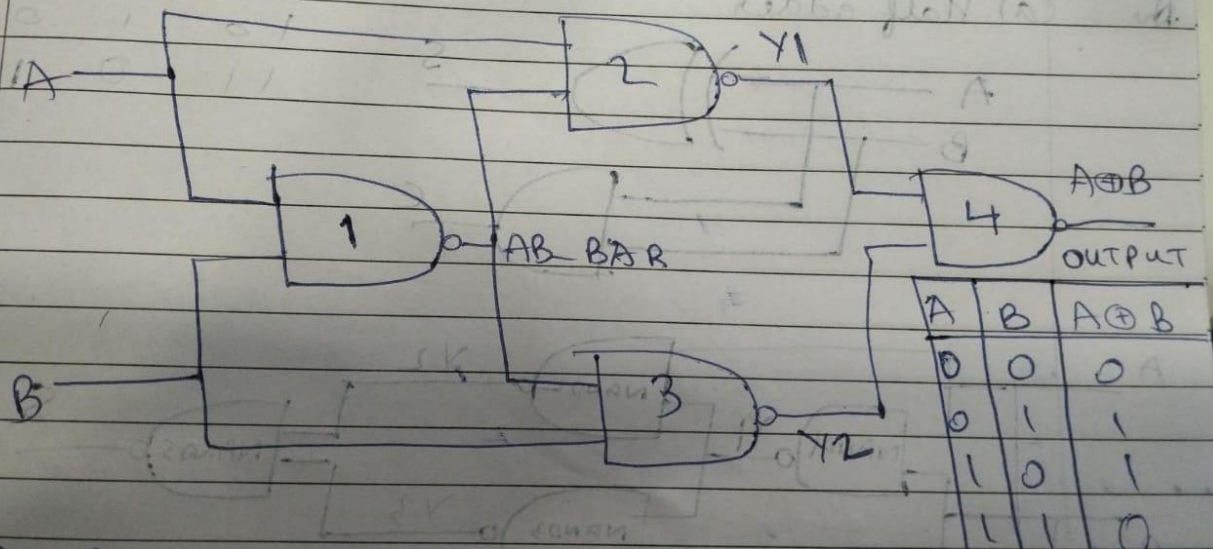


A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

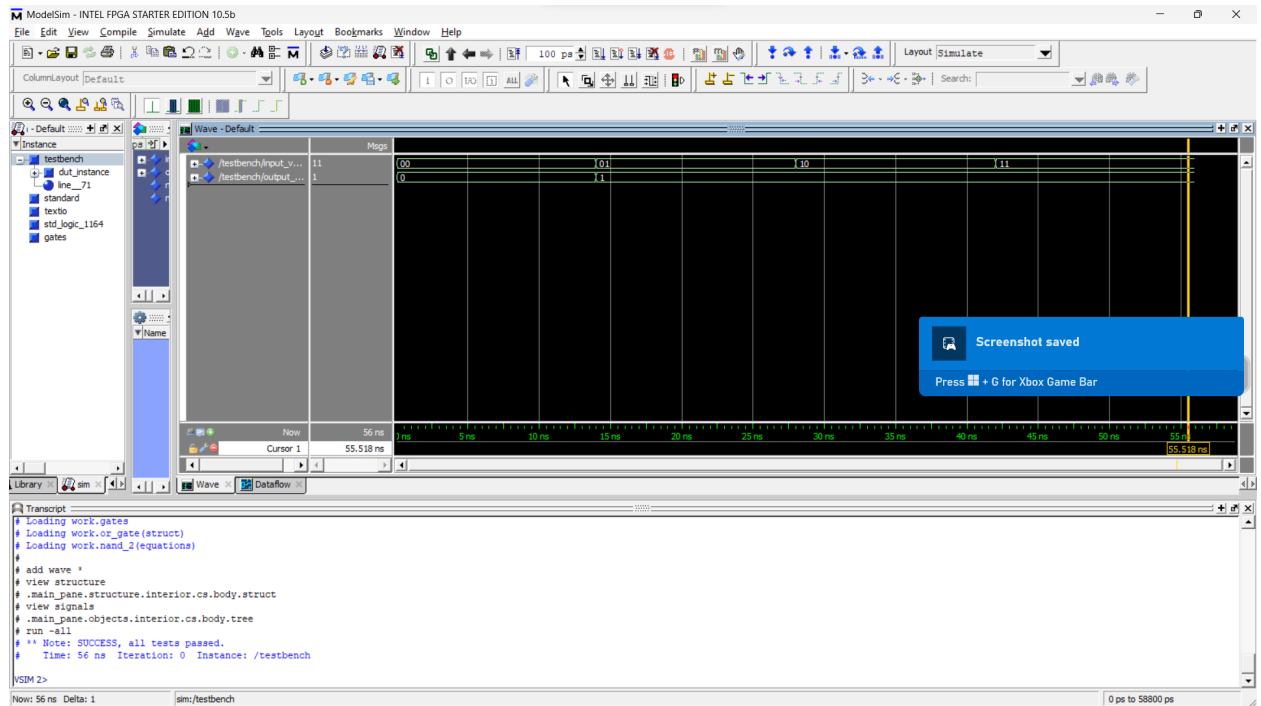
- XOR Gate

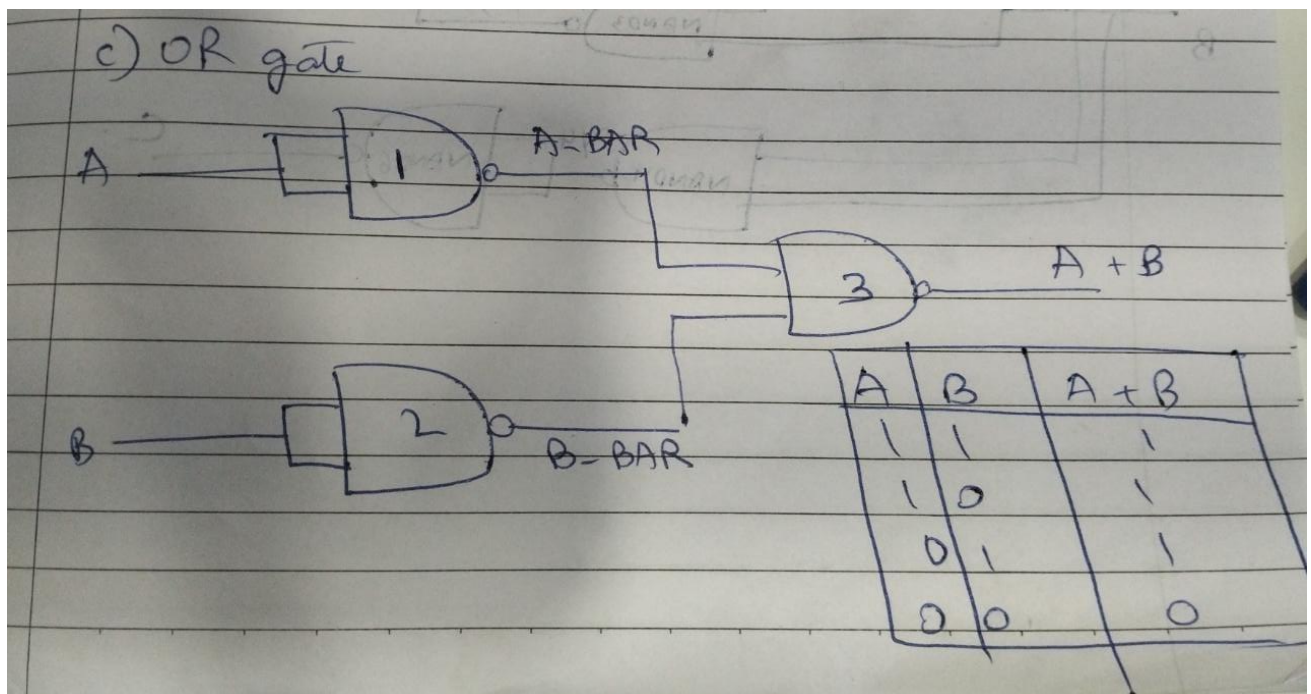
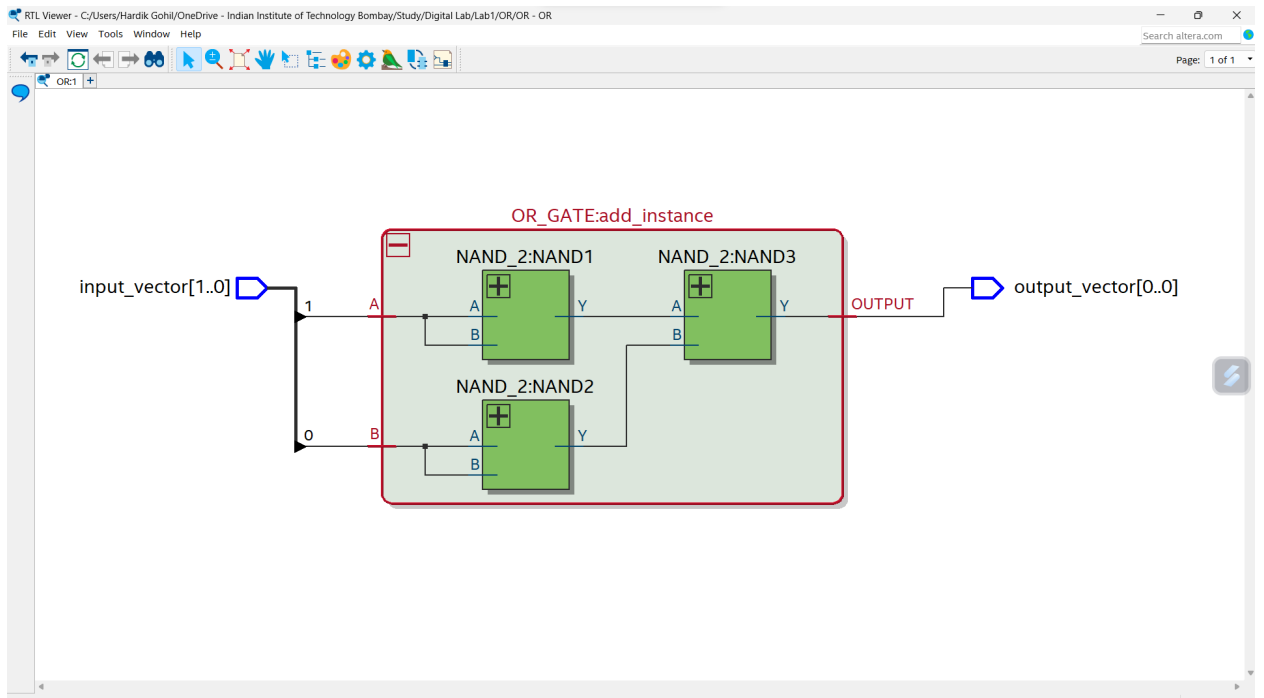


b) XOR gate

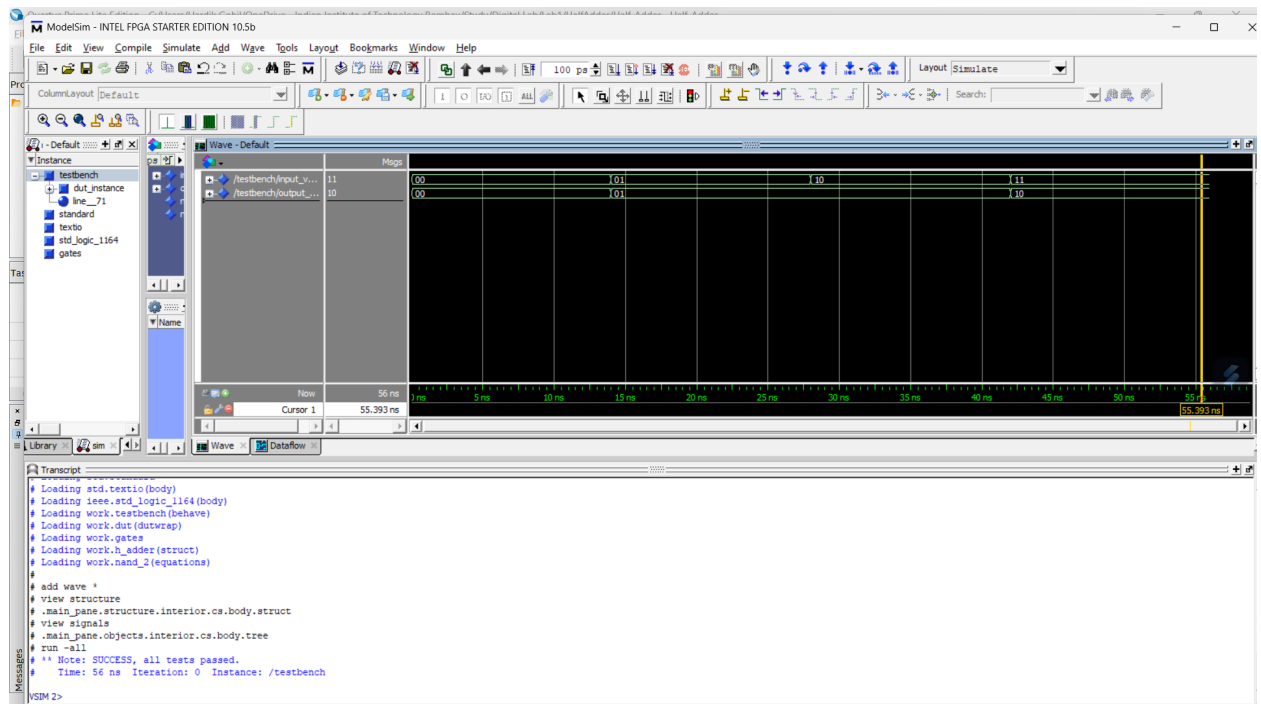


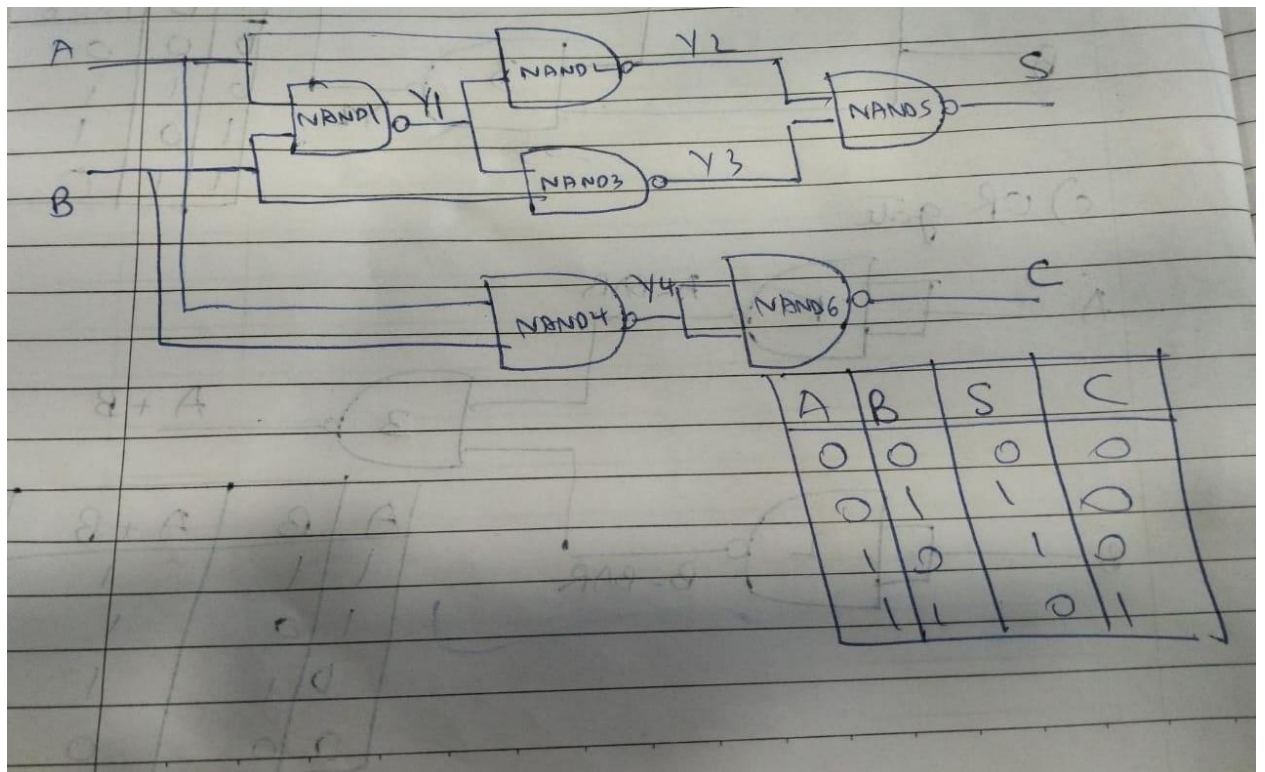
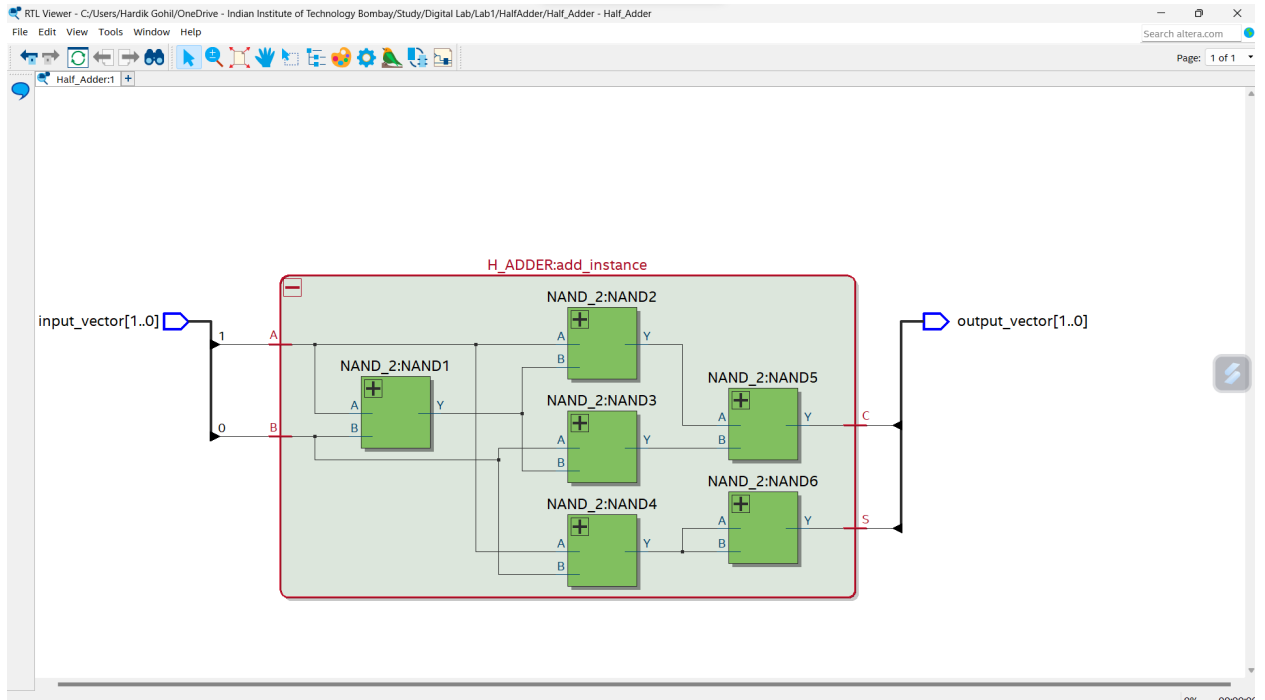
- OR Gate



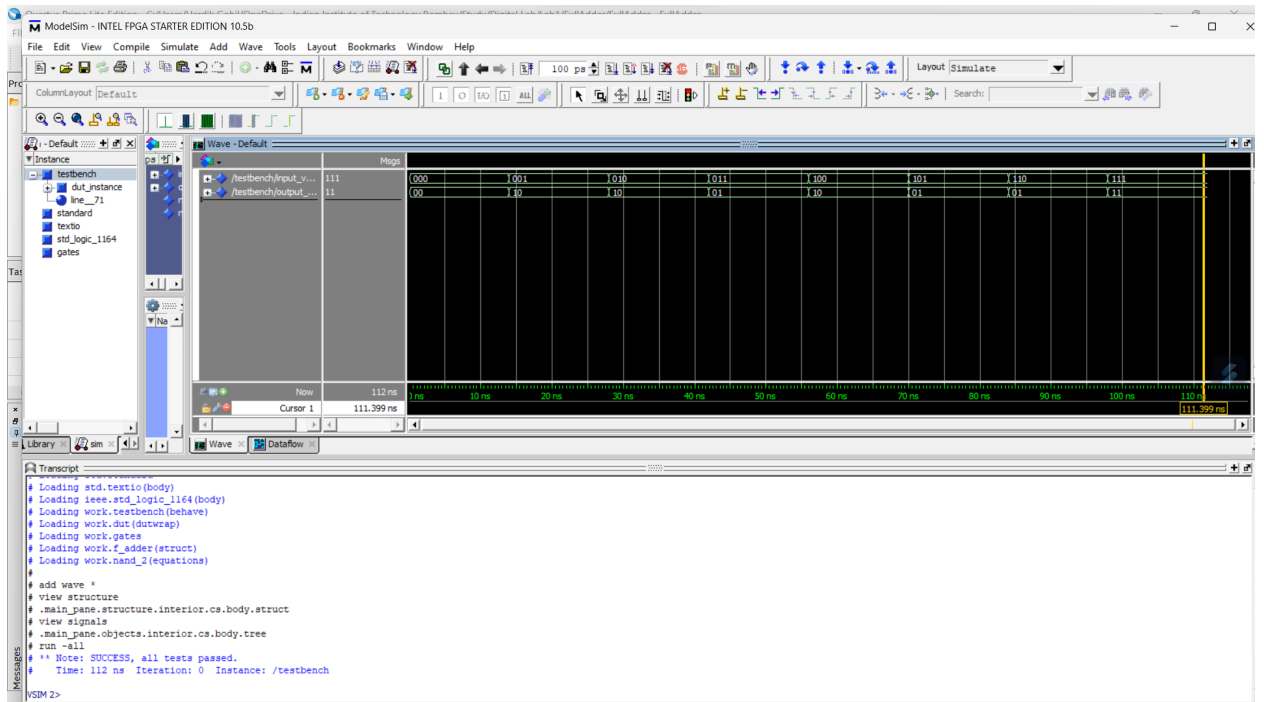


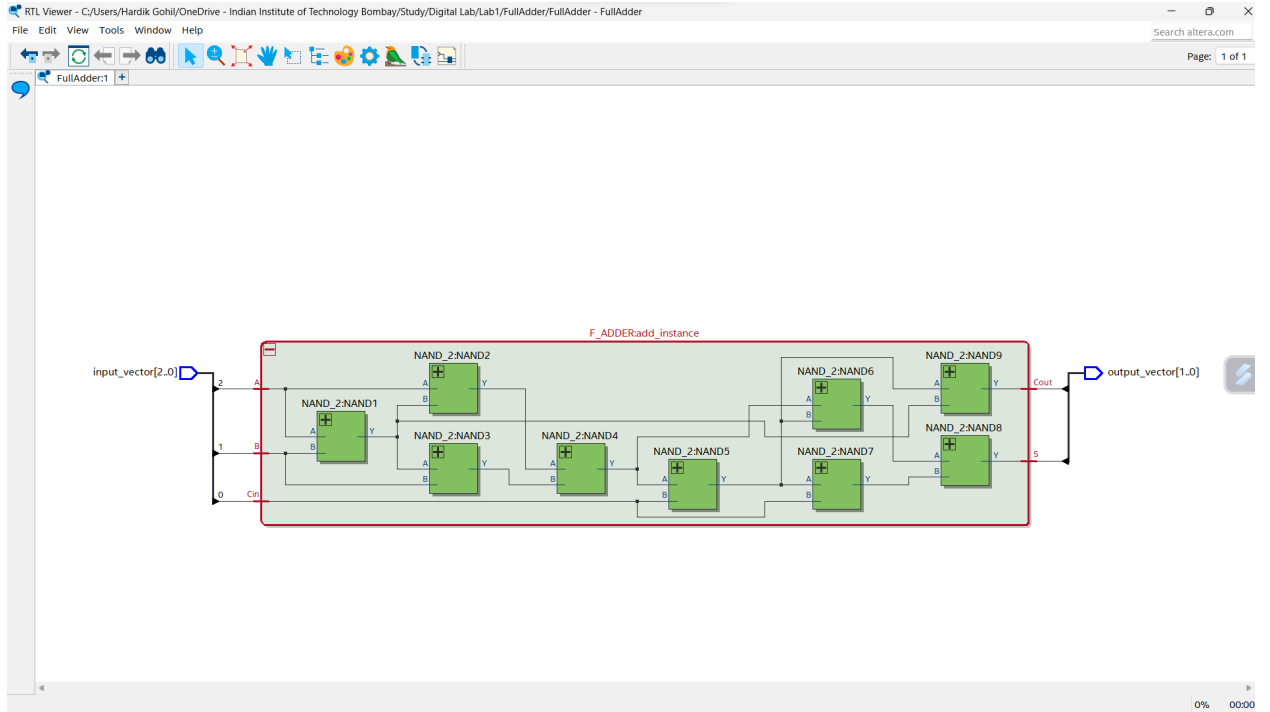
- Half adder



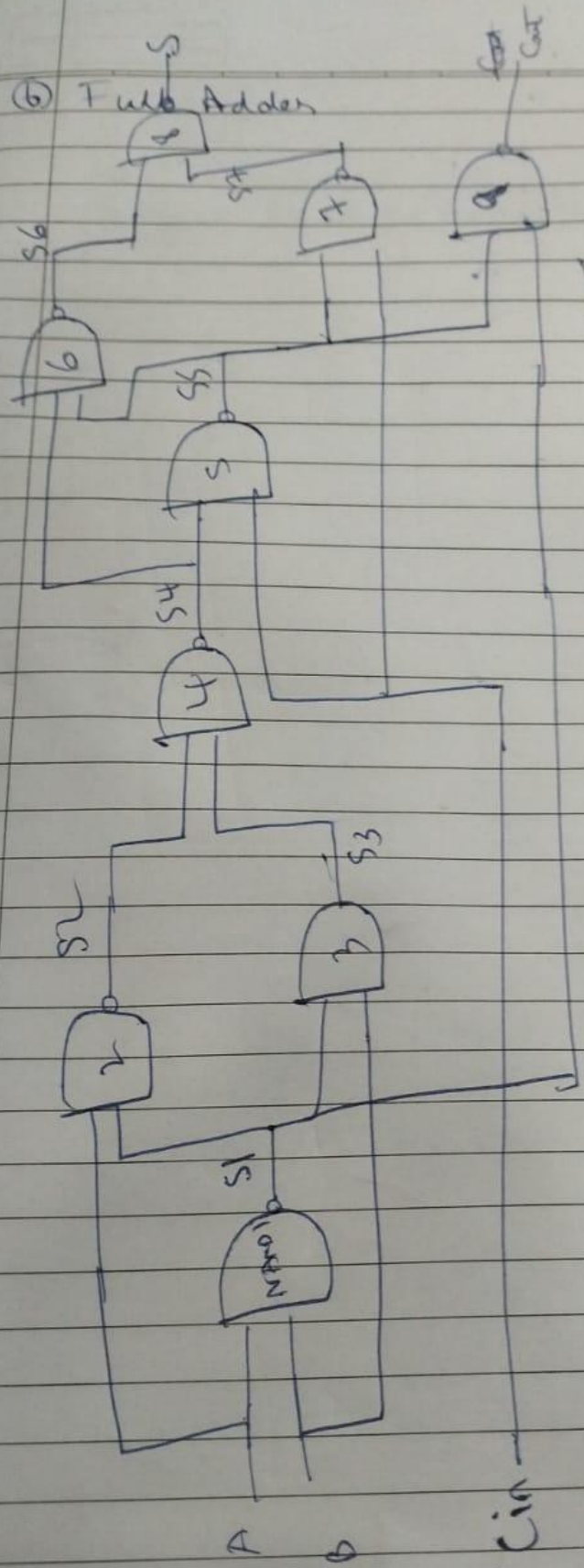


- Full Adder





⑥ Full Adder



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Finished
 Anurag