



EE224 - Digital Design

IITB CPU

Course Project 2023

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22b1293 - Hardik Pratap Gohil

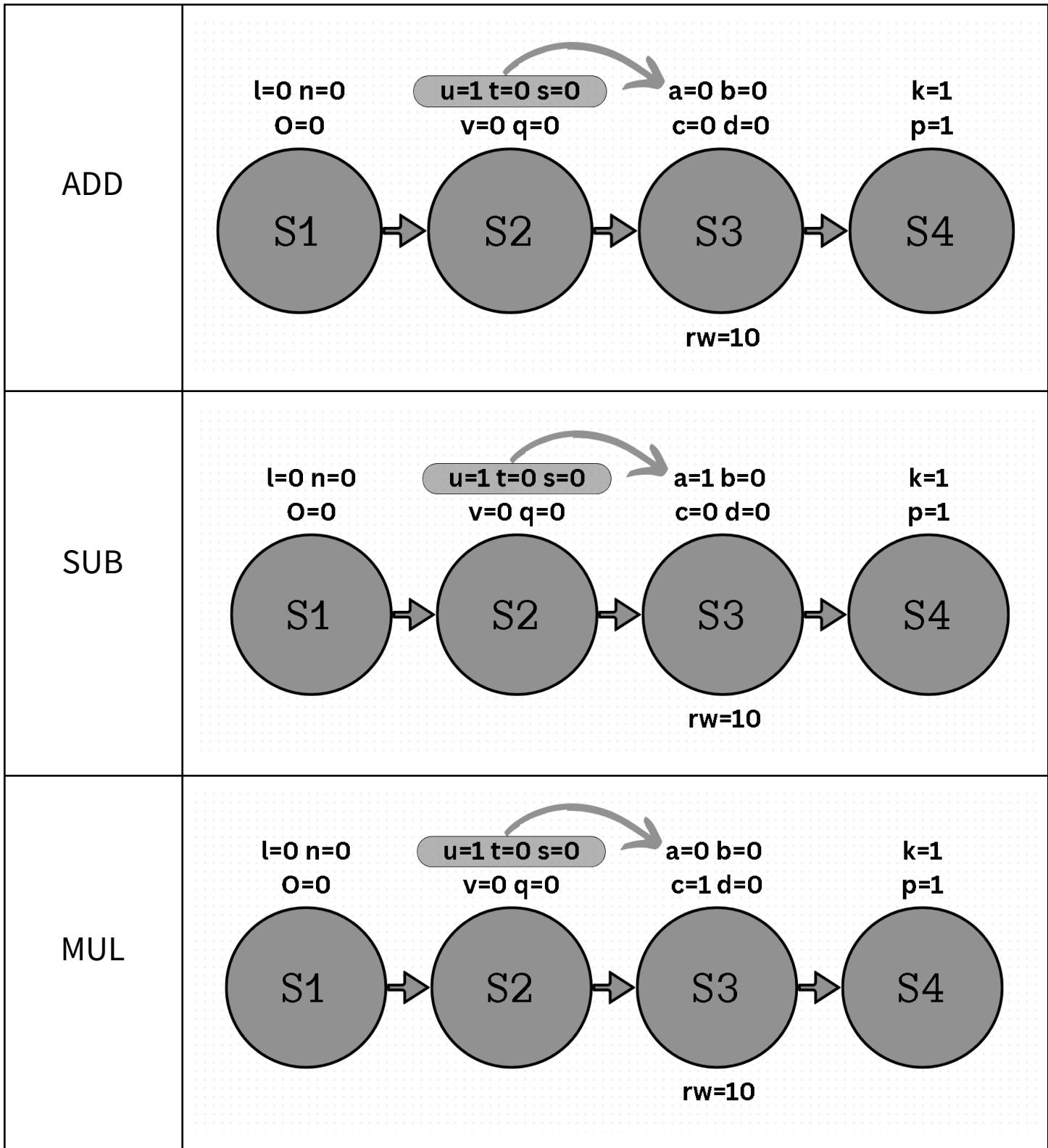
22b1254 - Bhanoth Preetam

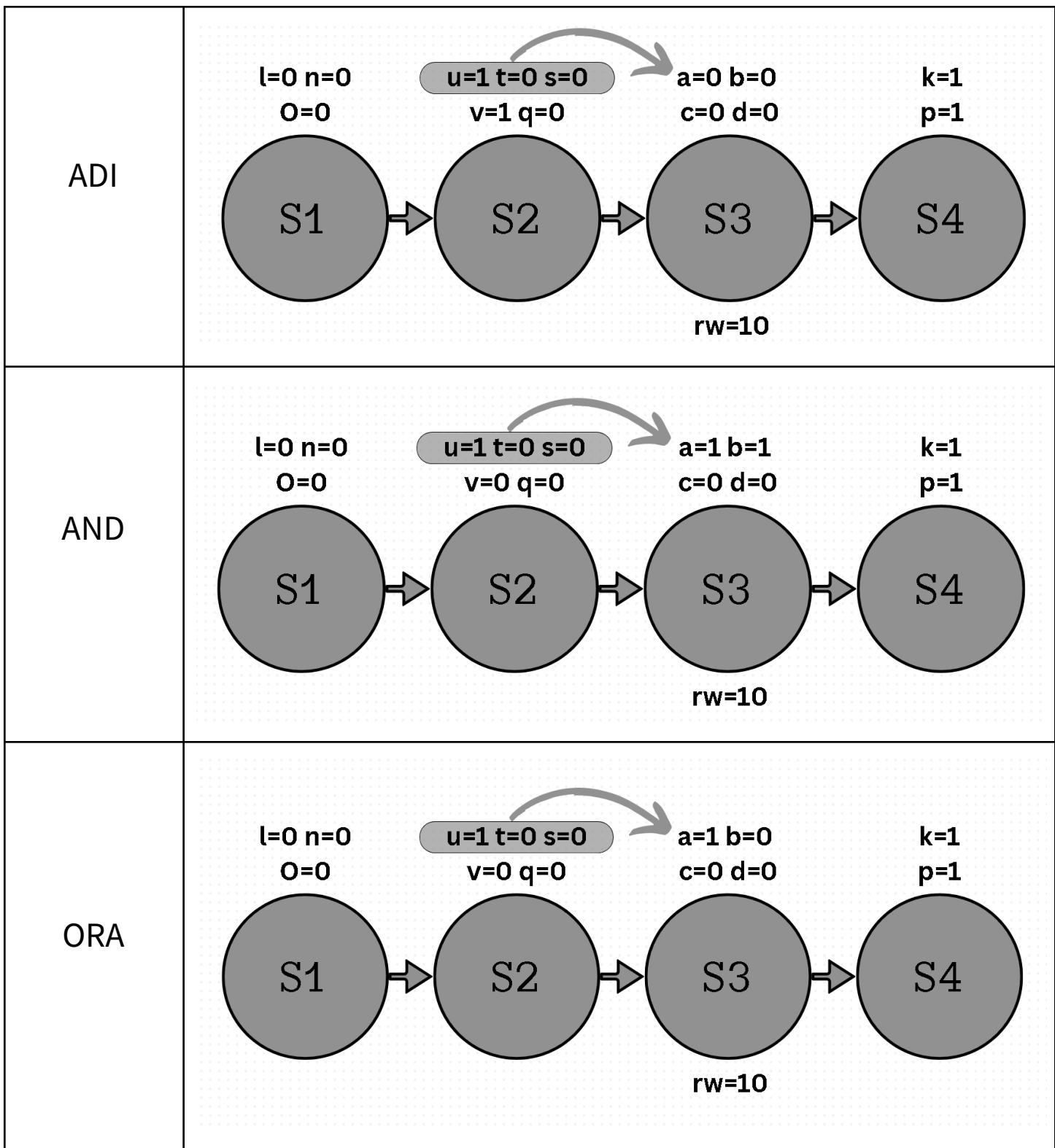
CPU Components

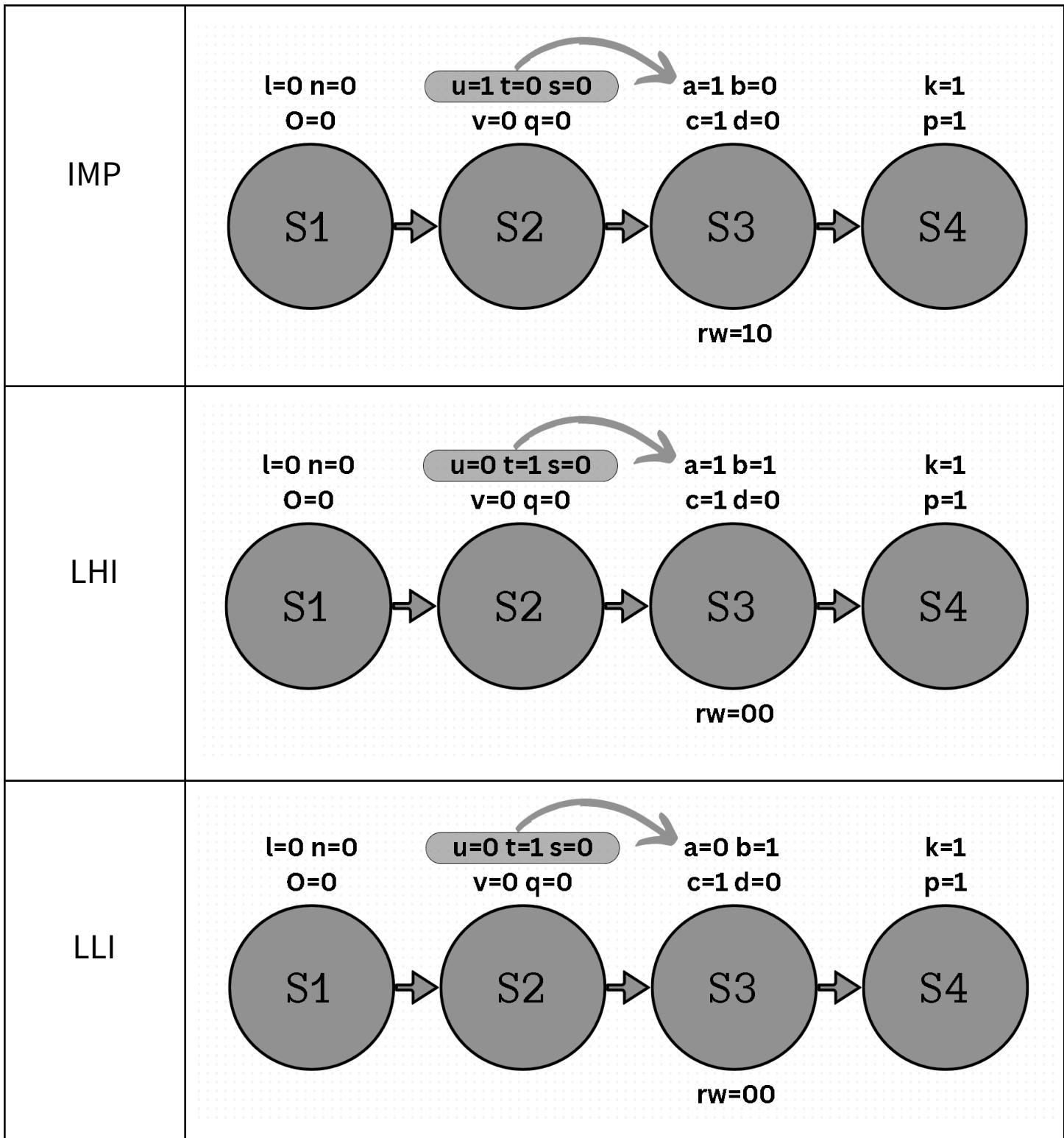
- Register 16 bit
- Register File
- Memory
- ALU
- MUX
- SE

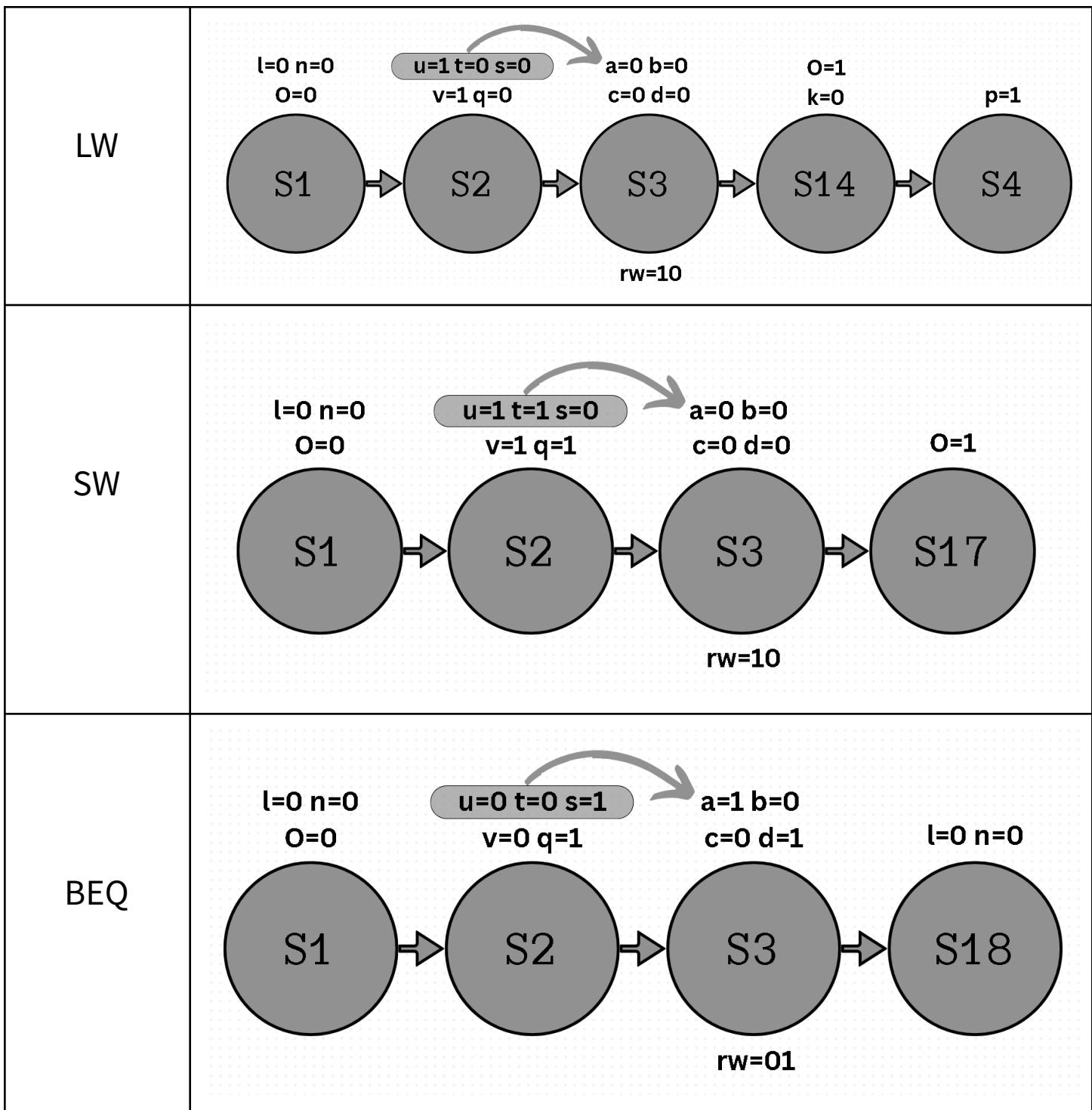
Preetam Bhanoth idhar

State Flow Diagram





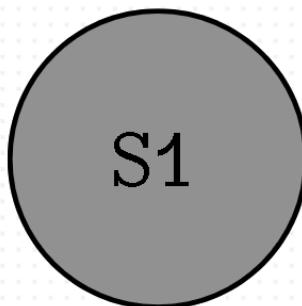




JAL

$l=0 n=0$

$O=0$

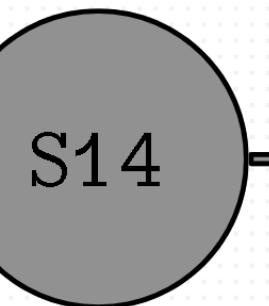


$u=0 t=0 s=1$

$v=0 q=0$



S14



$a=0 b=0$

$c=0 d=0$



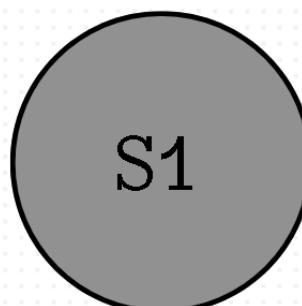
$rw=00$

$l=0 n=1$

JLR

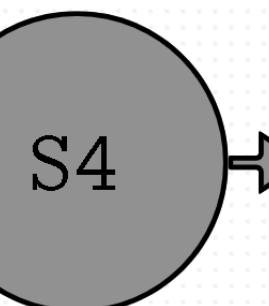
$l=0 n=0$

$O=0$



$p=0$

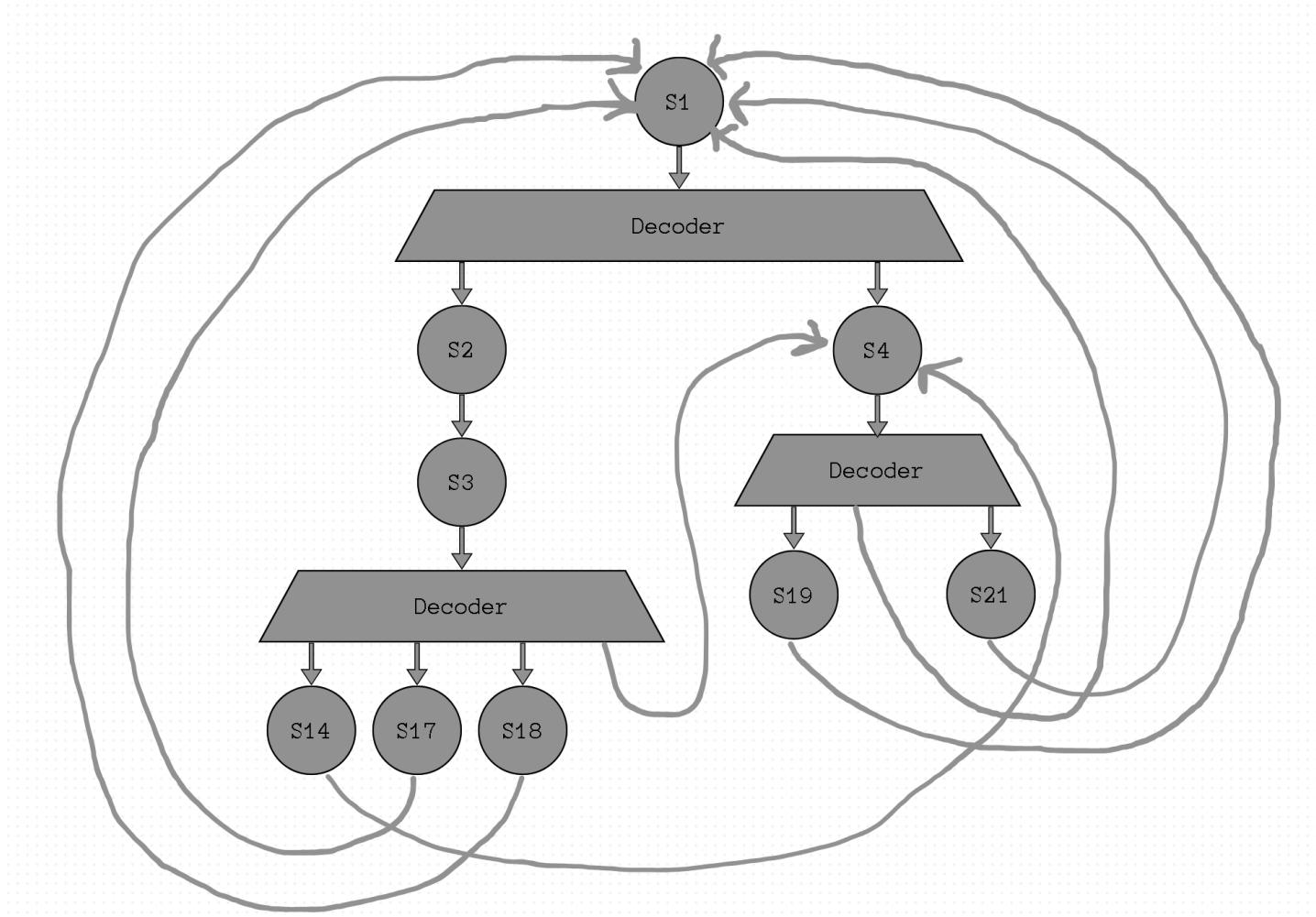
S4



S21

$l=1 n=0$

Net State Diagram



Hardware Flow Tables

S1

PC	—> Mem_add	Mem_R*
Memd_out	—> IR_in	IR_wr*
PC_out	—> ALU_A	
'2'	—> ALU_B	PC_w*
ALU_C	—> PC_in	

S2

IR_(7-9)	—> RF_A1	
IR_(10-12)	—> RF_A2	T1_wr*
RF_D1	—> T1	T2_wr*
RF_D2	—> T2	

S3

T1	—> ALU_A	ADD
T2	—> ALU_B	T3_wr*
ALU_C	—> T3	

S4

T3	→ RF_D3	RF_wr*
IR_(4-6)	→ RF_A3	

S14

T3	→ Mem_Add	Mem_k
Memd_out	→ T3	T3_w

S17

T3	→ Mem_Add	Mem_wr*
T2	→ Memd_out	

S3*

T1	→ ALU_A	Add
SE_6	→ ALU_B	T3_w*
ALU_C	→ T3	

Contributions:

Dhruv Meena: ALU, Register16bit, Report, Debugging, Register file

Hardik Gohil: MUX, Debugging, CPU controller, Testbench, Register file

Preetam: Design, Debugging, ALU, Memory Block, Sign extension, Register file

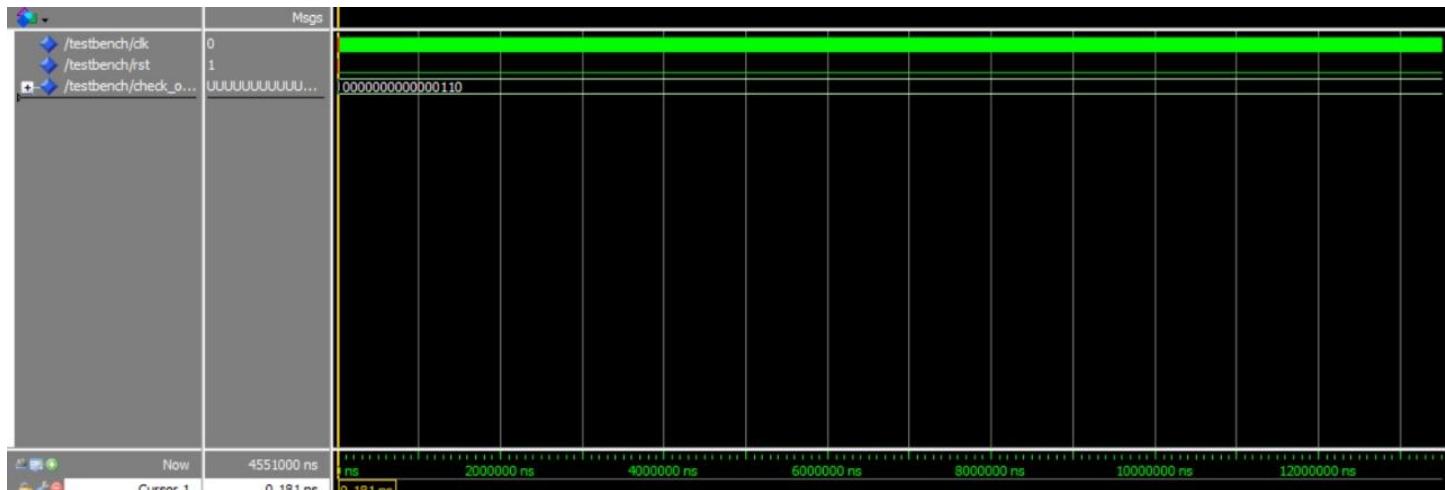
Mithin: ALU, Design, Debugging, CPU controller, Register file

Simulations

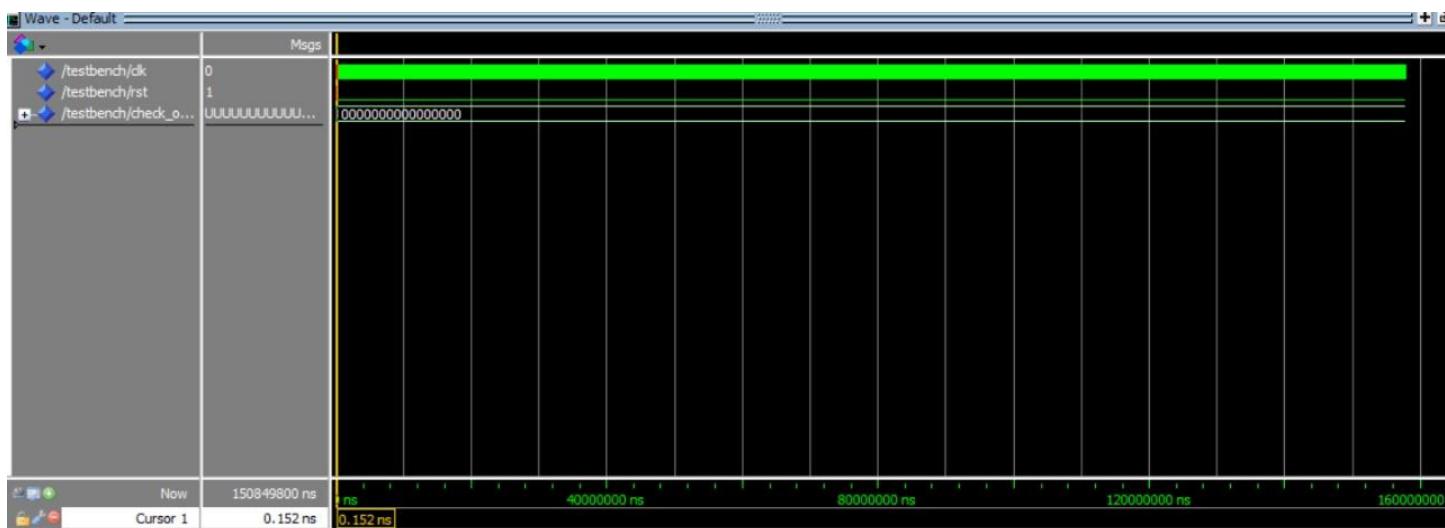
*all registers in register file have the number 3 / ...011 stored

OPcode	Rc	Rb	Ra
0 1 2 3	4 5 6	7 8 9	10 11 12

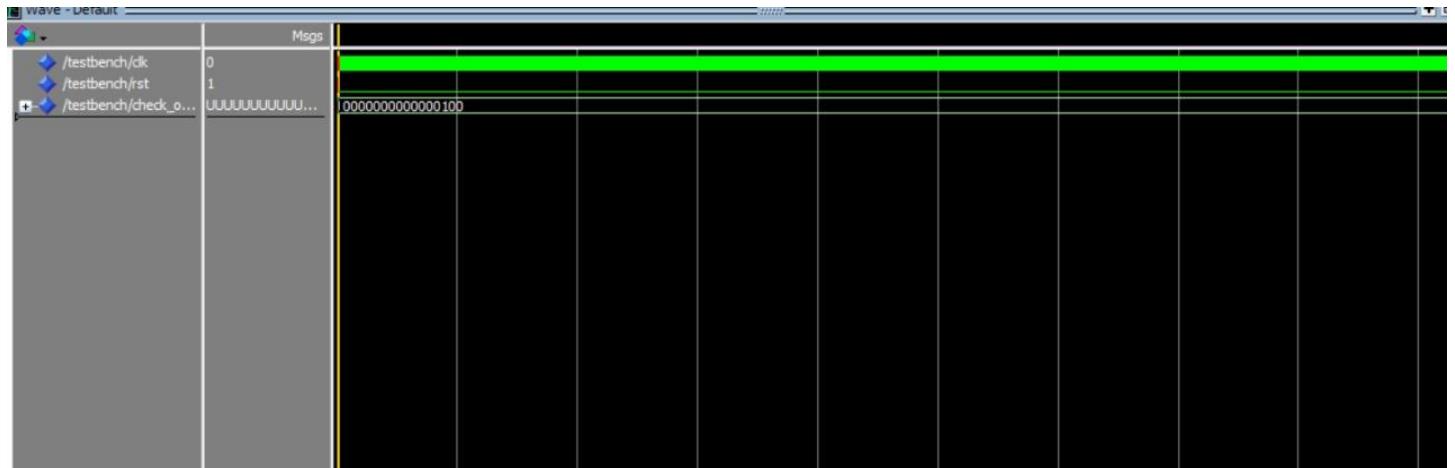
ADD 0000001011111111



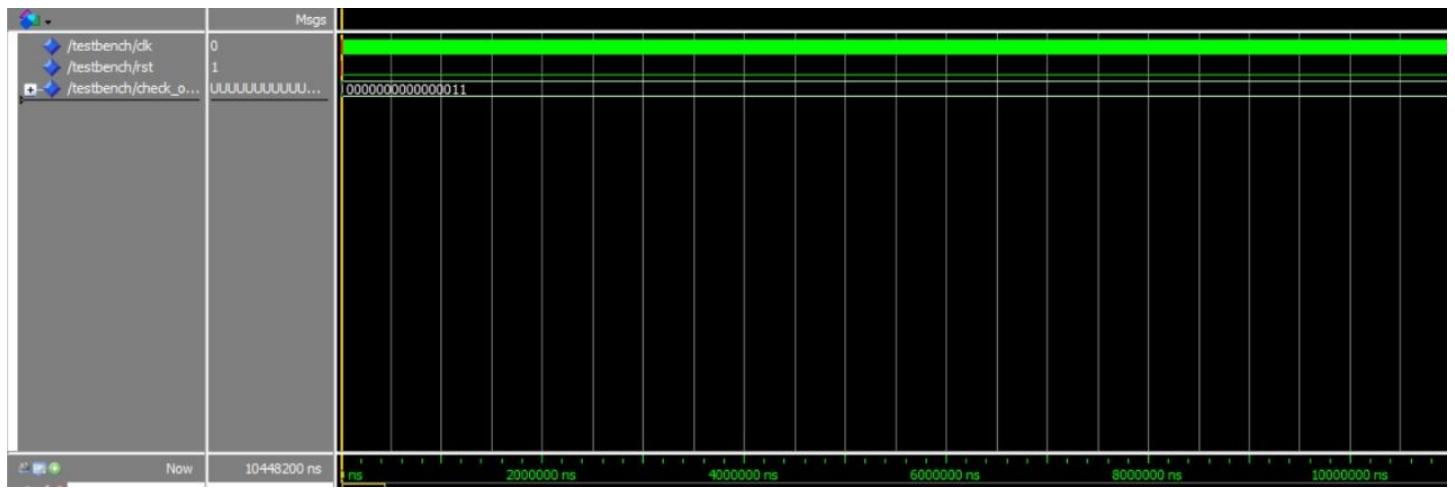
SUB 0010001011111111



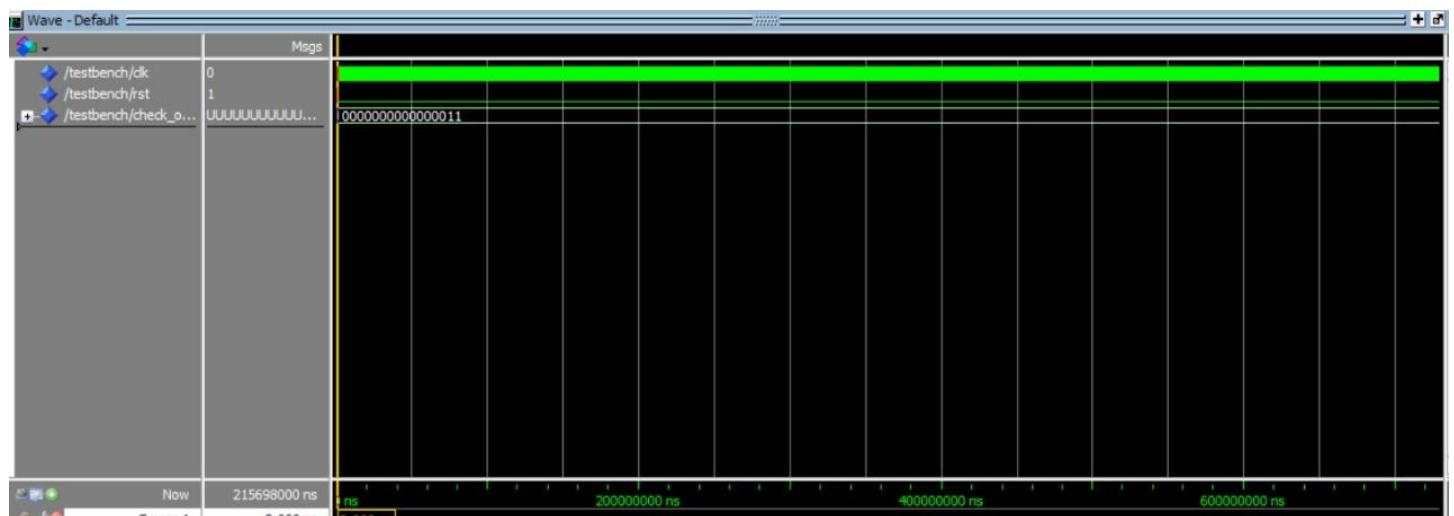
ADI 0001001111000001



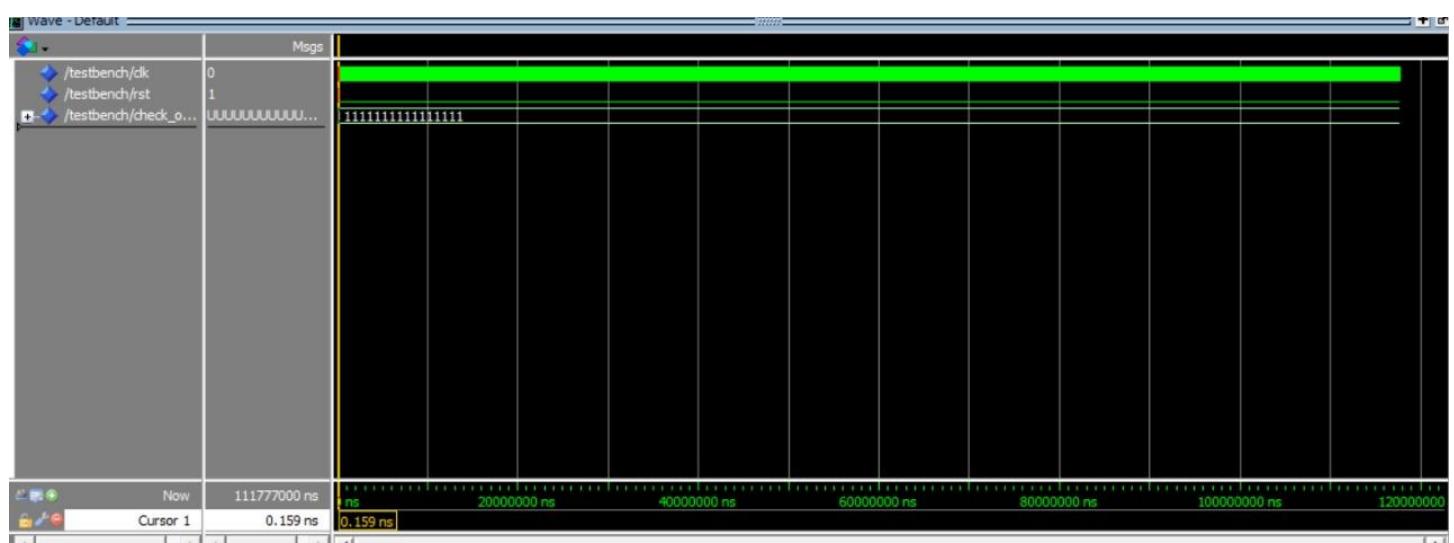
AND 0100001011111001



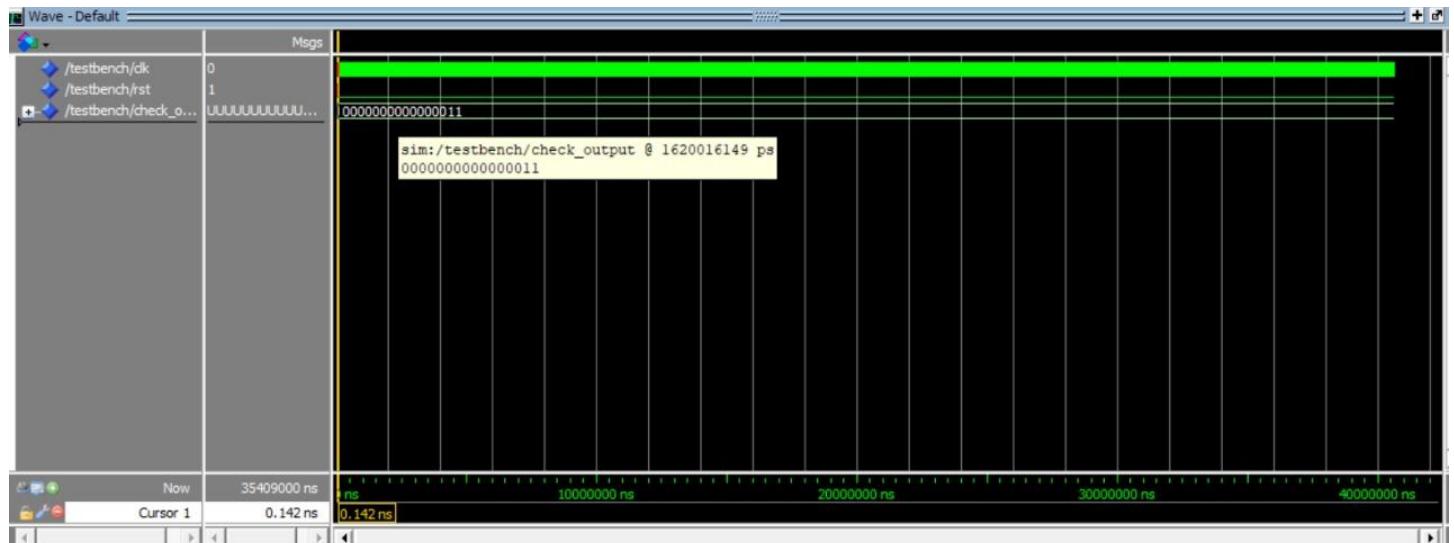
OR 0101001011111000



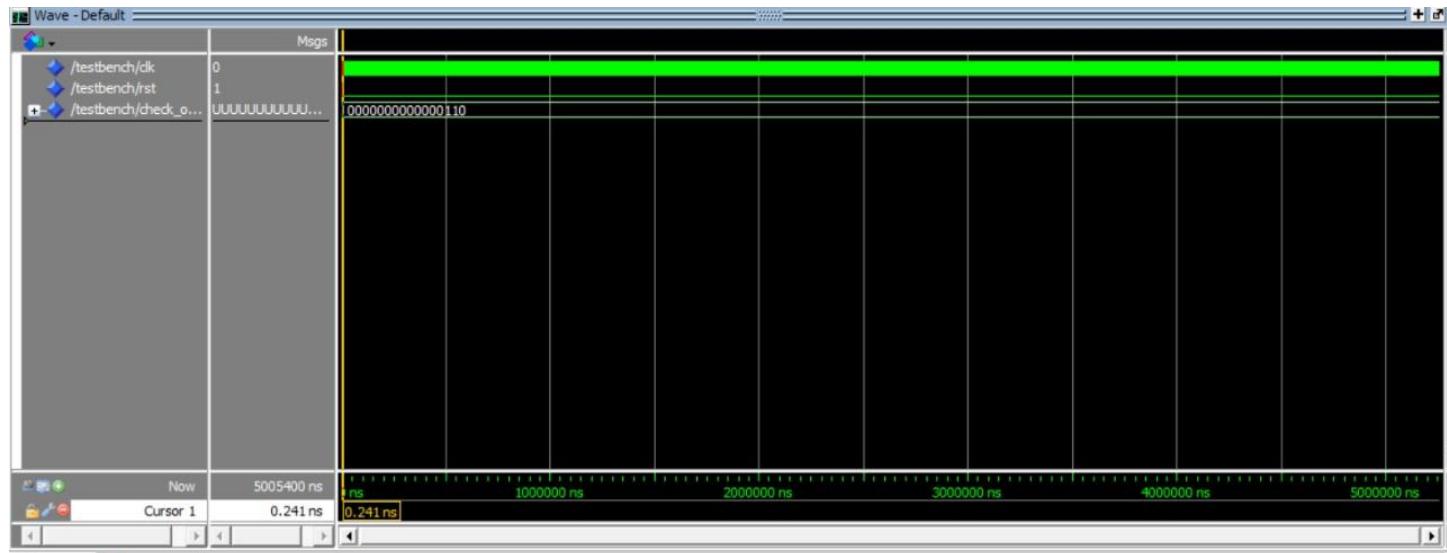
IMP 0110001011111000



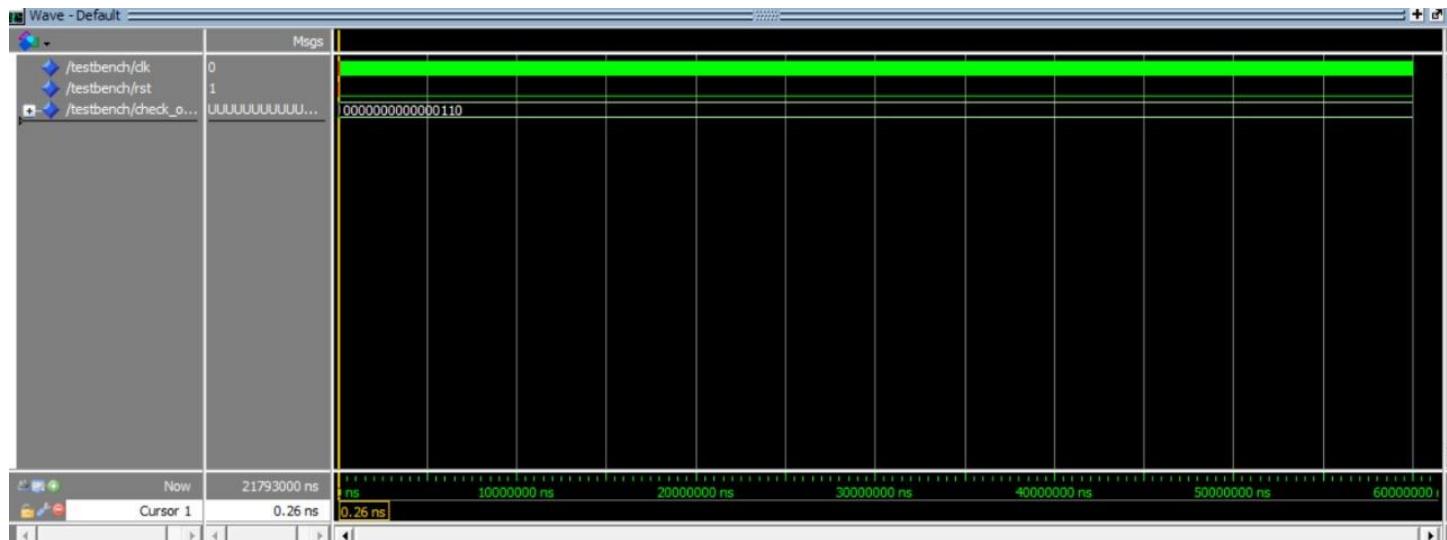
LLI 1001111000000011



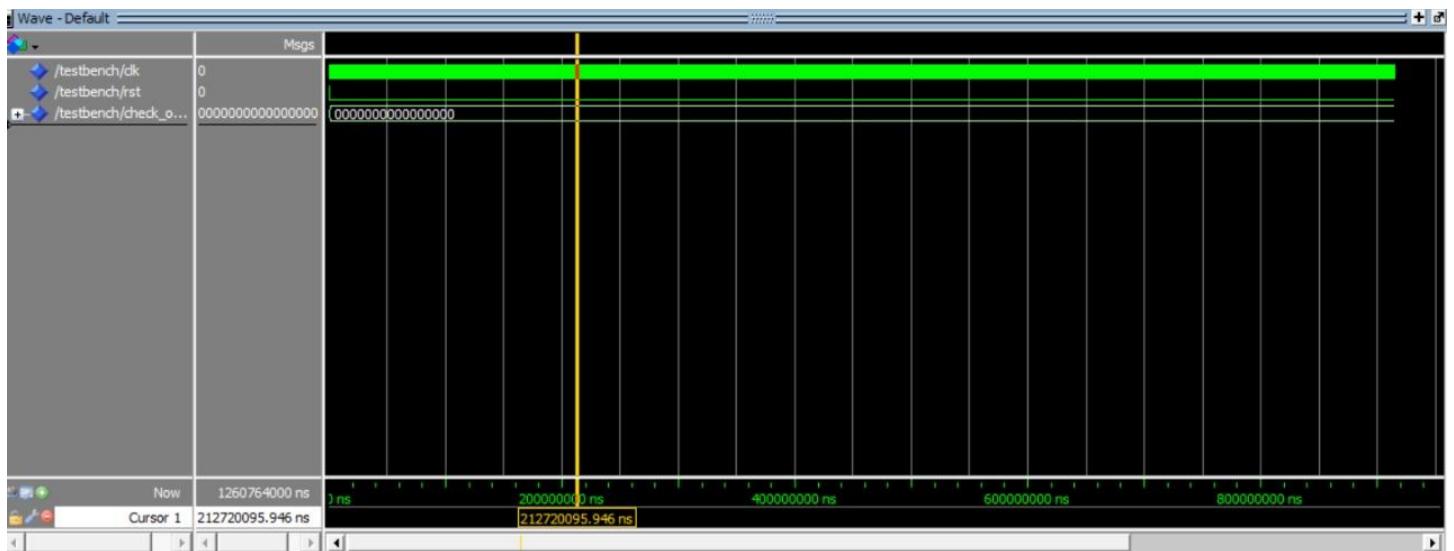
LW 1010111000000011



BEQ 1100111000000011



JAL 1101111000000011



JLR 1111001111000000

