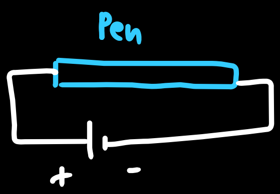
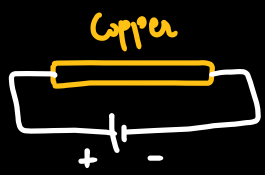
Semiconductors

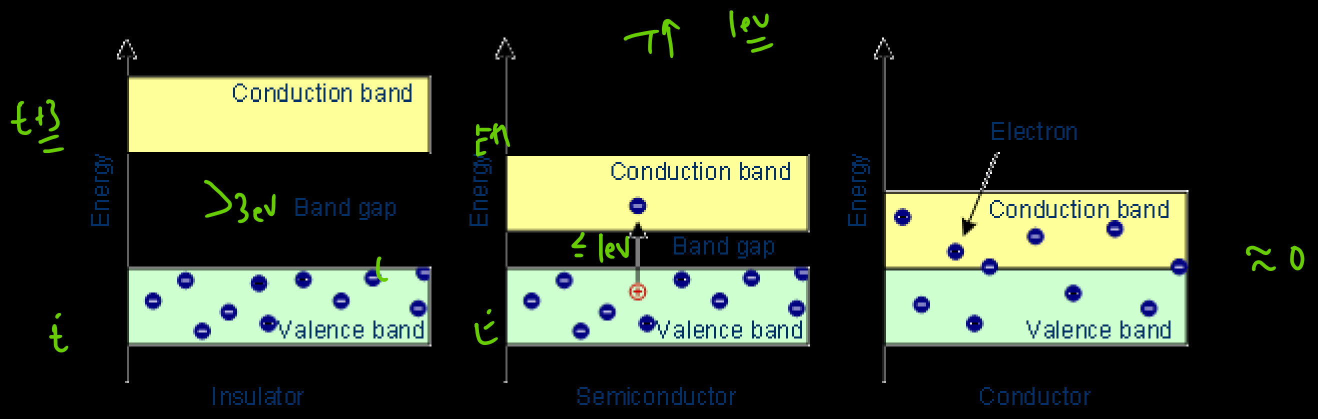
material conducts when e⁻s are found in conduction band.
i.e. free e⁻s



→ no current flow
∵ there are no free e⁻s



→ current flow



→ valence band e⁻s not able to reach conduction band

→ At room temperature huge band gap.

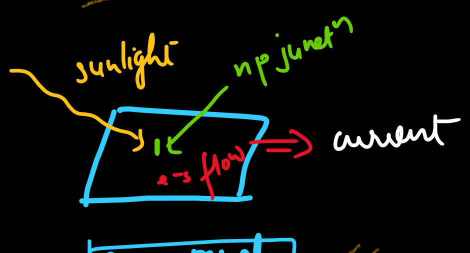
→ heat ⟹ 2-4 e⁻s may reach conduction band but that is not enough for conduction

→ At room temp → insulator

→ T↑ conduction possible

→ No band gap

→ At room temp e⁻s are already in conduction band

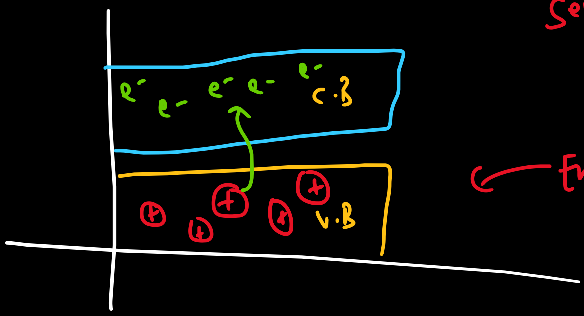


Solar panel

Holes :

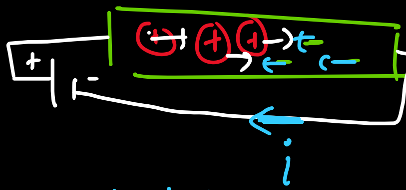
↓

absence of e^-



Semiconductors

← Energy → V.B to C.B



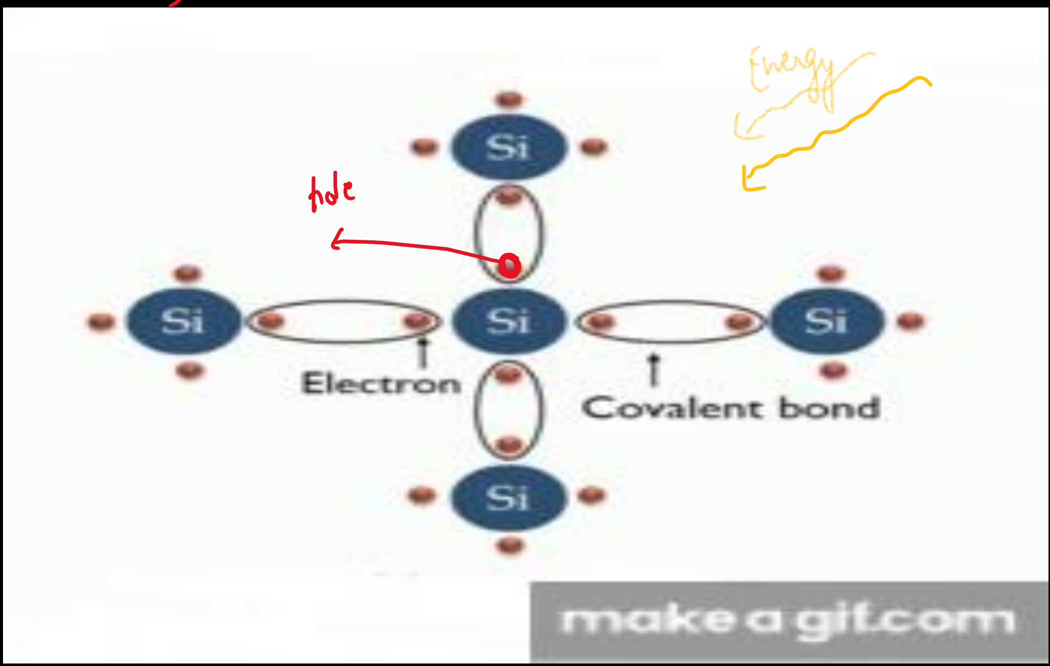
→ when a Potential difference is applied across a semi-conductor, there are 2 charge carriers → e^-s
→ + holes

Intrinsic Semiconductors : (Pure)

→ Si , Ge
→ tetravalent (4 e^-s)
→ 4 covalent bonds

→ octet complete

→ stable
⇒ no free e^-s



→ Energy ⇒ e^- out → hole

* $1e^-$ out ⇒ 1 hole

$\therefore \boxed{n_e = n_h}$

$n_e n_h = n_i^2$

n_i ← intrinsic charge carrier concentration

→ mass action law

Doping

dopant = impurity

semiconductor + impurity = extrinsic semiconductor

→ Types of dopants

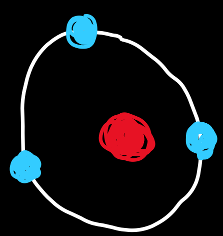
Tetravalent Si / Ge ← semiconductor

(i) Trivalent impurity

→ valency = 3

eg. Indium (In),

Boron (B), Aluminium (Al)



⇒ P-type semiconductor

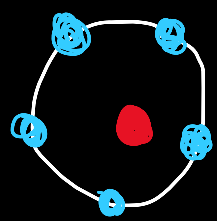
(ii) Pentavalent impurity

→ valency 5

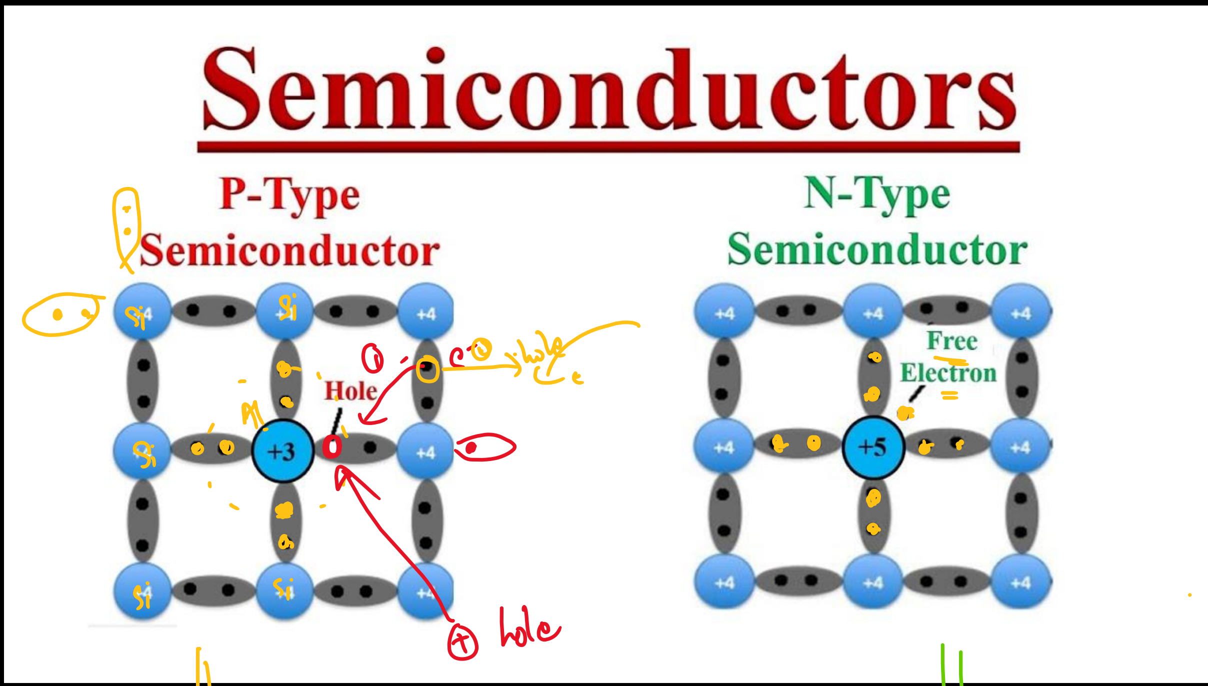
eg. Arsenic (As),

Antimony (Sb),

phosphorous (P)



⇒ N-type semi-conductor



→ neighbouring atom gives e^- → acceptor impurity

→ hole created

→ At room temp

$n_h > n_e$ (positive) → p type

→ free e^-s (donor impurity)

→ $n_e > n_h$ (negative) → N type

* If n_e & n_h represent the e^-s & hole concentration resp. in N-type & P-type, then

no of e / unit volume

no of holes / unit volume

$$n_e n_h = n_i^2$$

mass action law

where n_i: charge carrier concentration

Q intrinsic $n_e \times n_h = 25 \times 10^{10} = n_i^2$

$n_e = 5 \times 10^5$

$n_h = 5 \times 10^5$

$\xrightarrow{\text{impurity}}$

extrinsic

$n_e' = 6 \times 10^5$

$n_h' = ?$

→ pentavalent → $n_e > n_h$

$n_e' \times n_h' = n_i^2 = 25 \times 10^{10}$

$6 \times 10^5 \times n_h' = 25 \times 10^{10}$

→ $n_h' = 4.1 \times 10^5$

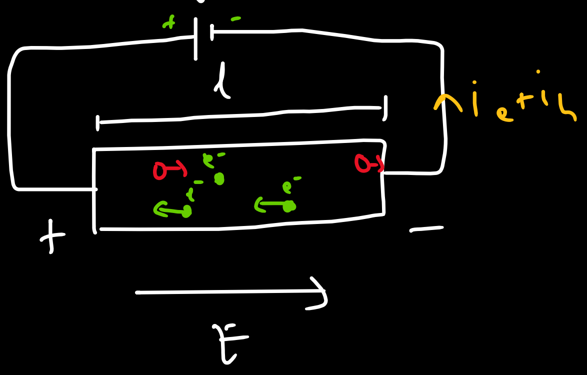
current electricity

$\boxed{i = neAv_d}$

$v_d \rightarrow$ drift speed

2 charge carriers → e^-s
→ holes

total current = i



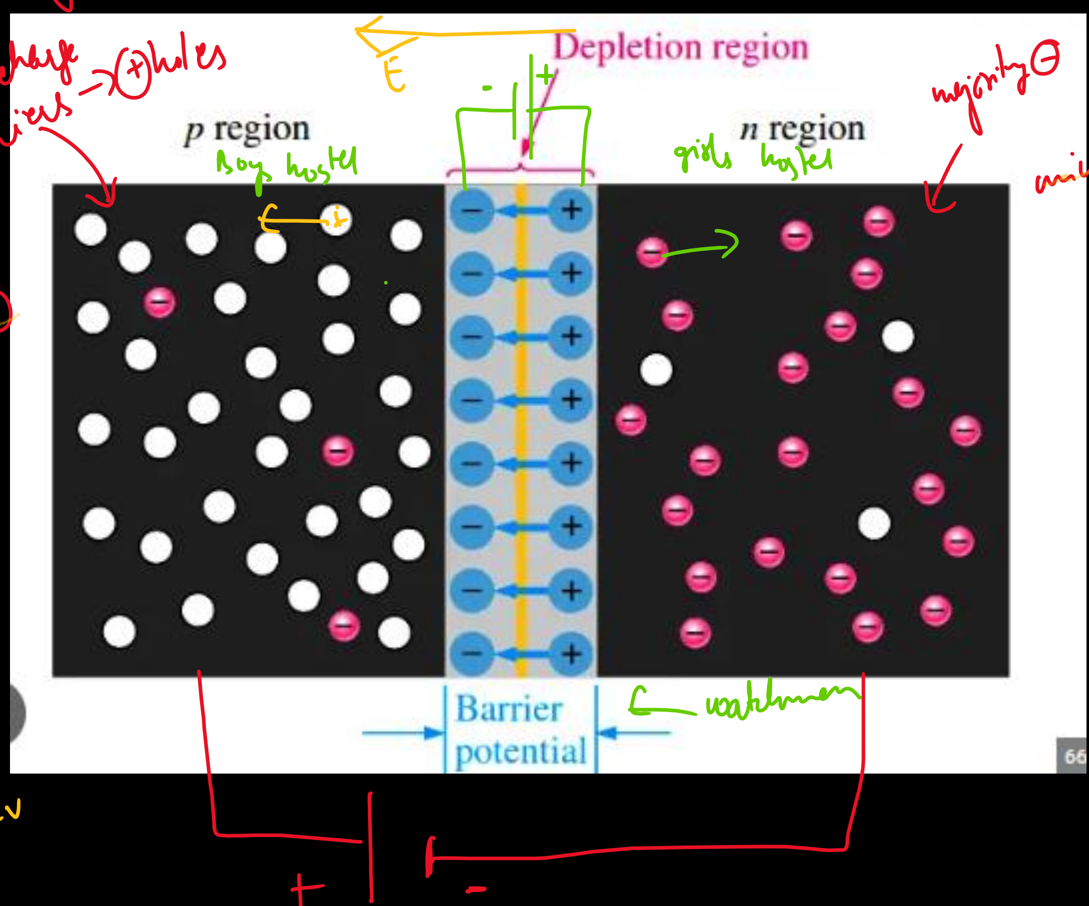
$i = i_h + i_e$

$= n_e A (v_d)_e +$

$n_h A (v_d)_h$

$i = eA(n_e v_e + n_h v_h)$

p-n junction diode:



$f = qE$

E 0.7eV

E 0.7eV

→ E 0.3eV no current

→ E

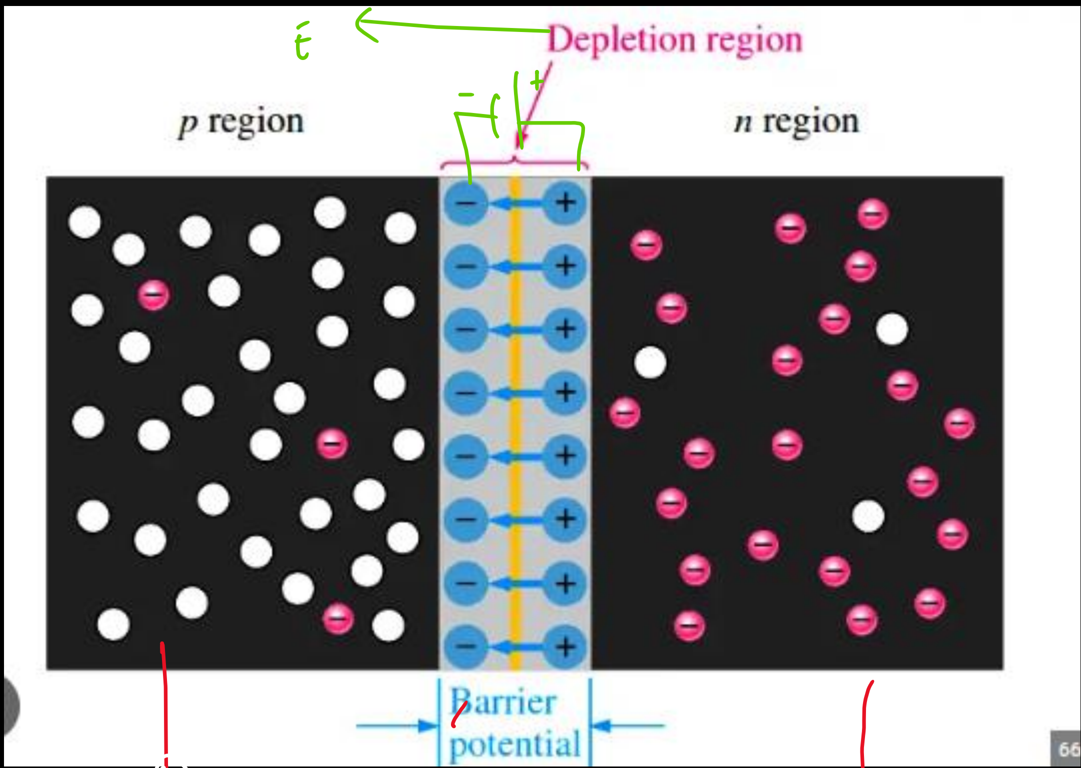
E 0.7eV

→ 10eV (R→0)

→ E 0.8 eV ⇓ current flows

Forward Biasing

E_B = Barrier potential



FB

$\vec{E}_B$

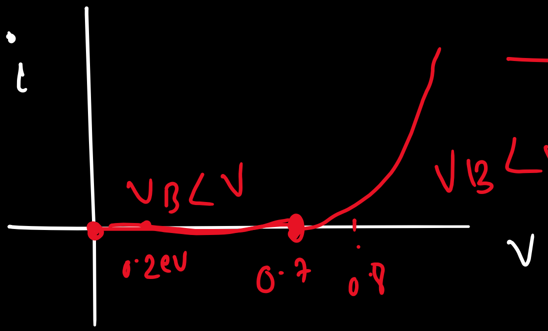
E

$\boxed{E_B < E}$

current flow

0.7eV

0.2eV



$\boxed{V_B \rightarrow \text{Knee potential}}$

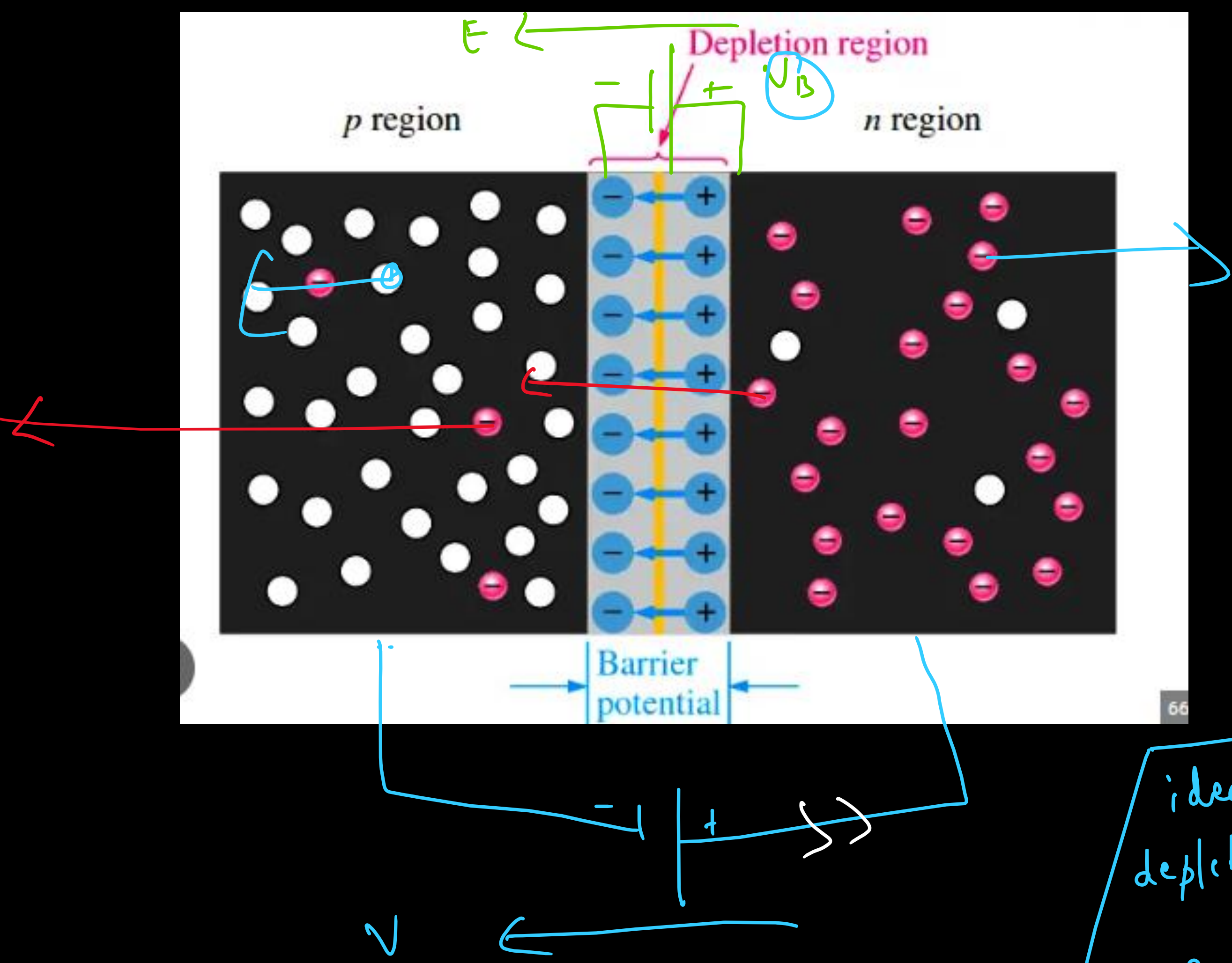
$E >> E_B$

very high current

$R \rightarrow 0$

ideal F.B.

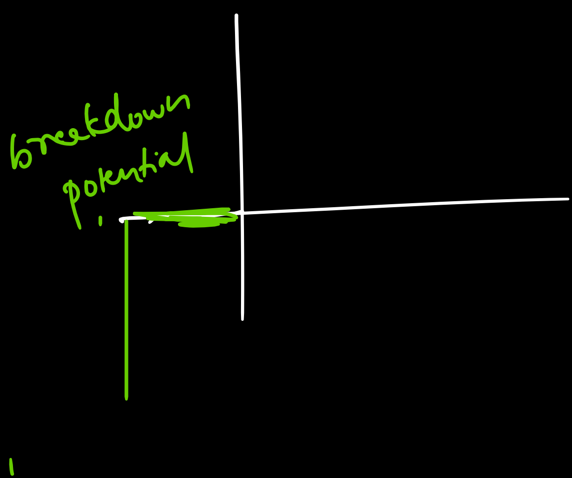
Reverse biasing:



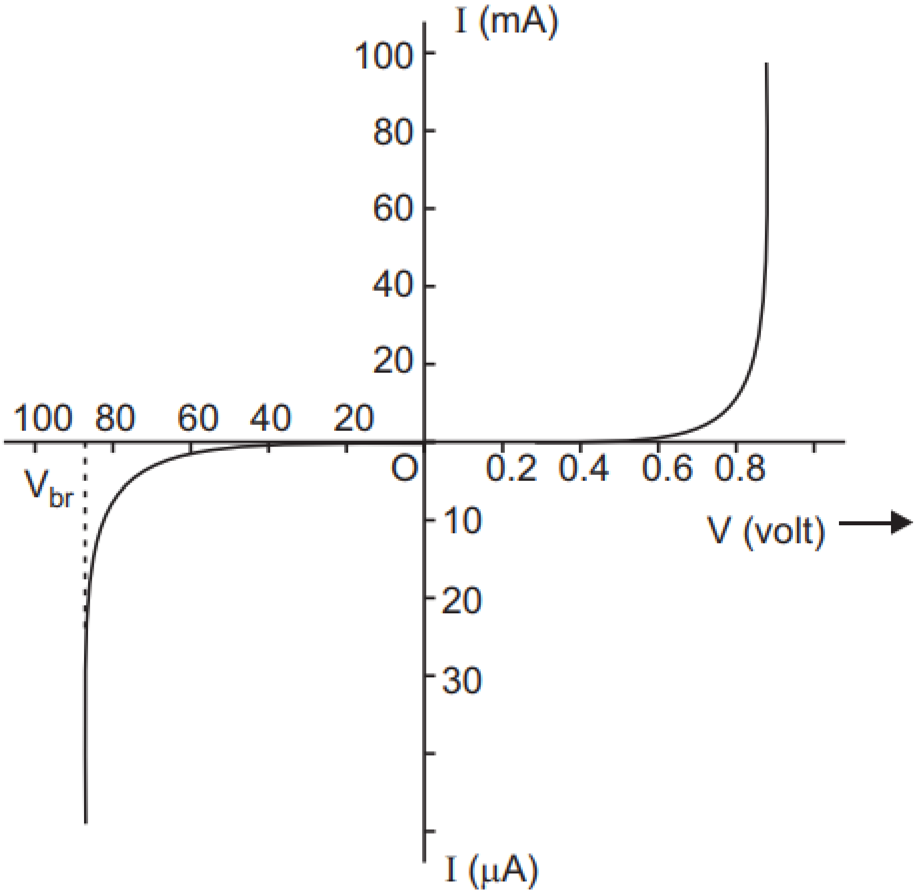
ideal Reverse Bias
depletion layer
$R \to \infty$

V_B very high

minority charge carriers
come into action
$\Rightarrow$ lot of current (breakdown)



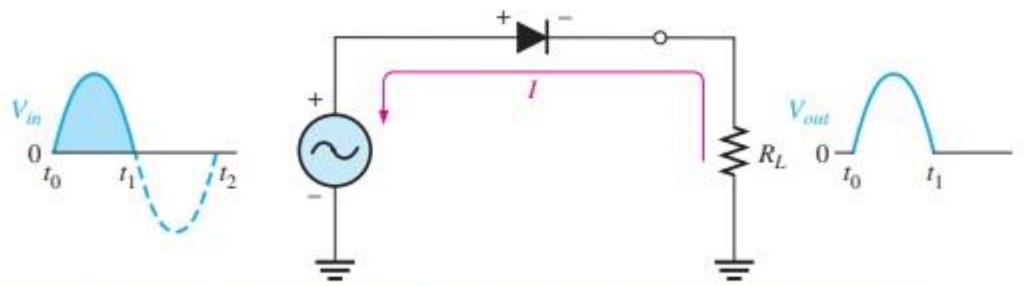
Zener diode



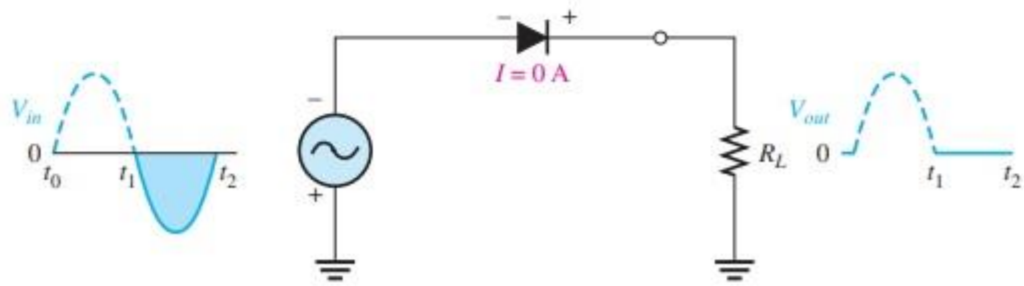
***V-I* characteristics of a silicon diode**

Voltage regulator :

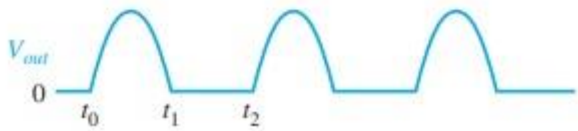
Half-Wave Rectifier Operation



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 60 Hz half-wave output voltage for three input cycles

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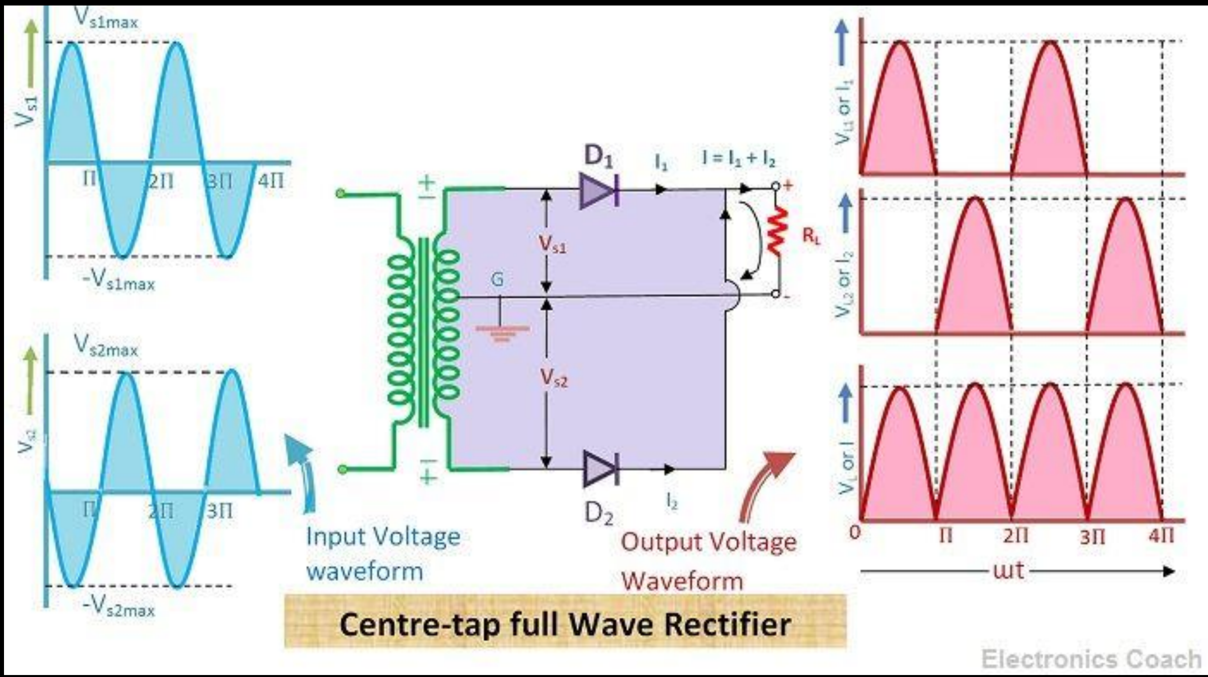
Vs1max
Vs1
Π
2Π
3Π
4Π
-Vs1max
Vs2max
Vs2
Π
2Π
3Π
-Vs2max
Input Voltage
waveform
G
Vs1
Vs2
D1
I1
I = I1 + I2
RL
D2
I2
Output Voltage
Waveform
Centre-tap full Wave Rectifier
VL1 or I1
VL2 or I2
VL or I
0
Π
2Π
3Π
4Π
ωt
Electronics Coach