Parul University

FACULTY OF ENGINEERING AND TECHNOLOGY

BACHELOR OF TECHNOLOGY

DIGITAL ELECTRONICS

(203105202)

3RD SEMESTER

ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT

Laboratory Manual

PREFACE

It gives us immense pleasure to present the first edition of Digital Electronics Practical Book for the B. Tech. 2nd year students for **PARUL UNIVERSITY.**

The Digital Electronics theory and laboratory course at **PARUL UNIVERSITY, WAGHODIA, VADODARA** is designed in such a way that students develop the basic understanding of the subject in the theory classes and then try their hands on the experiments to realize the various devices and circuits learnt during the theoretical sessions. The main objective of the Digital Electronics laboratory course is: Learning Digital Electronics through Experimentations. All the experiments are designed to understand the characteristic of various electronics devices and electronics circuits and also to expose the students to various electronics instruments and their uses.

The objective of this Digital Electronics Practical Book is to provide a comprehensive source for all the experiments included in the Digital Electronics laboratory course. It explains all the aspects related to every experiment such as: understanding of electronics devices, different electronics circuits using logic gates and how to calculate the desired results from the observations etc. It also gives sufficient information on how to interpret and discuss the obtained results.

We acknowledge the authors and publishers of all the books which we have consulted while developing this Practical book. Hopefully this *Digital Electronics Practical Book* will serve the purpose for which it has been developed.

INSTRUCTIONS TO STUDENTS

1. Be prompt in arriving to the laboratory and always come well prepared for the experiment.
2. Be careful while working on the equipments operated with high voltage power supply.
3. Work quietly and carefully. Give equal opportunity to all your fellow students to work on the instruments.
4. Every student should have his/her individual copy of the Digital Electronics Practical Book.
5. Every student has to prepare the notebooks specifically reserved for the Digital Electronics Practical work "Digital Electronics Practical Book".
6. Every student has to necessarily bring his/her Digital Electronics Practical Book, Digital Electronics Practical Class Notebook and Digital Electronics Practical Final Notebook, when he/she comes to the practical to perform the experiment.
7. Record your observations honestly. Never makeup reading or doctor them to get a better fit on the graph or to produce the correct result. Display all your observations on the graph (If applicable).
8. All the observations have to be neatly recorded in the Digital Electronics Practical Class Notebook (as explained in the Digital Electronics Practical Book) and verified by the instructor before leaving the laboratory.
9. If some of the readings appear to be wrong then repeat the set of observations carefully.
10. Do not share your readings with your fellow student. Every student has to produce his/her own set of readings by performing the experiment separately.
11. After verification of the recorded observations, do the calculation in the Digital Electronics Practical Class Notebook (as explained in the Digital Electronics Practical Book) and produce the desired results and get them verified by the instructor.
12. Never forget to mention the units of the observed quantities in the observation table. After calculations, represent the results with appropriate units.
13. Calculate the percentage error in the results obtained by you if the standard results are available and also try to point out the sources of errors in the experiment.
14. Find the answers of all the questions mentioned under the section 'Find the Answers' at the end of each experiment in the Digital Electronics Practical Book.
15. Finally record the verified observations along with the calculation and results in the Digital Electronics Practical Note Book.
16. Do not forget to get the information of your next allotment (the experiment which is to be performed by you in the next laboratory session) before leaving the laboratory from the Technical Assistant.
17. The grades for the Digital Electronics Practical course work will be awarded based on your performance in the laboratory, regularity, recording of experiments in the Digital Electronics Practical Final Notebook, lab quiz, regular viva-voce and end-term examination.

CERTIFICATE

This is to certify that

Mr./Ms.....

with enrolment no. ..... has successfully completed his/her laboratory experiments in the ***Digital Electronics (203105202)*** *from the department of ..... during the academic year .....*

Date of Submission: ..... Staff In charge: .....

Head of Department: .....

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Sr. No	Experiment Title	Page No		Date of Performance	Date of Assessment	Marks (out of 10)	Sign
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2	To study and implement all gates using Following Universal Gates						
	a. NAND						
	b. NOR						
3	Design NOR & OR using TTL logic						
4	To study and Design Adder Combinational Circuits.(Half Adder and Full Adder)						
5	To study and Design Subtractor Combinational Circuits.(Half Subtractor and Full Subtractor)						
6	To design and realize a combinational circuit to convert binary to gray/gray to binary code						
7	To study and Design Multiplexer						
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9	To study and Design SR flip-flop and D flip-flop						
10	To study and Design JK flip-flop and T flip-flop						
11	To realize and configure 4-bit ripple counter.						
12	To study and Design Shift register						

13	To study the D/A (DAC-0800)& A/D (ADC 0809)converters IC with its specification						
14	To study construction and working of any one memory IC from data sheets.						

EXPERIMENT NO. 1

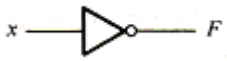
AIM : To study & Testing of various Logic Gates .

APPARATUS :

PROCEDURE:

- Connect different gates on the Digital Electronic Trainer kit.
- Give +5 V power supply and GND, which are available on the kit.
- Give the inputs from " Logic Level inputs " section present on the kit.
- Check the output from the LEDs and verify the truth table according to input and output combination.

OBSERVATION TABLE:

<table>
<tr><th>SR. No.</th><th>Name of Gate</th><th>Logic Symbol and Equation</th><th>Truth Table</th></tr>
<tr><td>1.</td><td>NOT</td><td> 

F =X'</td><td>
<table>
<tr><th>X</th><th>F</th></tr>
<tr><td>0</td><td></td></tr>
<tr><td>1</td><td></td></tr>
</table>
</td></tr>
<tr><td>2.</td><td>OR</td><td> 

F=X+Y</td><td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
<tr><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td></tr>
<tr><td>1</td><td>0</td><td></td></tr>
<tr><td>1</td><td>1</td><td></td></tr>
</table>
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<table>
<tr>
<td>3.</td>
<td>AND</td>
<td> 

F = X Y</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
<tr><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td></tr>
<tr><td>1</td><td>0</td><td></td></tr>
<tr><td>1</td><td>1</td><td></td></tr>
</table>
</td>
</tr>
<tr>
<td>4.</td>
<td>NOR</td>
<td> 

F= (X+Y)’</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
<tr><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td></tr>
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<tr><td>1</td><td>1</td><td></td></tr>
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<tr>
<td>5.</td>
<td>NAND</td>
<td> 

F=(X Y)’</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
<tr><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td></tr>
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<table>
<tr>
<td>6.</td>
<td>X-OR
(Exclusive OR)</td>
<td> 

F=X⊕Y</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
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<tr><td>0</td><td>1</td><td></td></tr>
<tr><td>1</td><td>0</td><td></td></tr>
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</tr>
<tr>
<td>7.</td>
<td>X-NOR
(Exclusive NOR)</td>
<td> 

F=XOY</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>F</th></tr>
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<tr>
<td>8.</td>
<td>BUFFER</td>
<td> 

F=X</td>
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<table>
<tr><th>X</th><th>F</th></tr>
<tr><td>0</td><td></td></tr>
<tr><td>1</td><td></td></tr>
</table>
</td>
</tr>
</table>

Draw Pin Diagram of above mentioned Logic gates (74XX Series Digital ICs):

CONCLUSION :

QUESTIONS:

1. Which IC contains NAND gate?
2. How many gates are there in 7408?
3. Explain Modulus-2 Addition using Logic gate.

ANSWERS:

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EXPERIMENT NO. 2

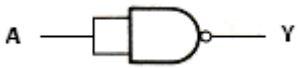
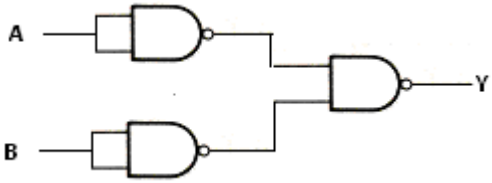
AIM: To study and implement all gates using Following Universal Gates

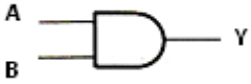
1. NAND
2. NOR

APPARATUS:

THEORY:

NAND Gate as an Universal Gate

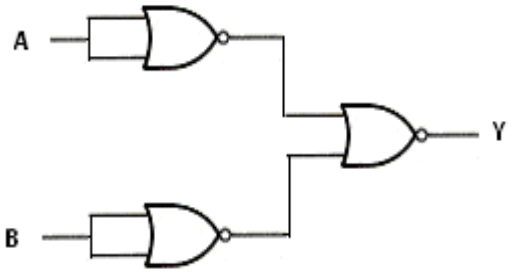
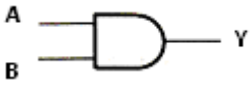
1.	NOT Gate using NAND Gate	Truth Table	NOT Gate
		<table><tr><th>A</th><th>Y</th></tr><tr><td>0</td><td></td></tr><tr><td>1</td><td></td></tr></table>	
2.	**OR Gate using NAND Gate**	**Truth Table**	**OR Gate**
		<table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table>	

3.	AND Gate using NAND Gate	Truth Table	AND Gate
		<table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table>	

PART B.

NOR Gate as a Universal Gate

1.	NOT Gate using NOR Gate	Truth Table	NOT Gate
		<table><tr><th>A</th><th>Y</th></tr><tr><td>0</td><td></td></tr><tr><td>1</td><td></td></tr></table>	
2.	**OR Gate using NOR Gate**	**Truth Table**	**OR Gate**
		<table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table>	

3.	AND Gate using NOR Gate	Truth Table	AND Gate
			

A	B	Y
0	0	
0	1	
1	0	
1	1	

PROCEDURE:

1. Connect the circuit for NOT gate by using only NAND gate on trainer kit as shown in diagram.
2. Apply different combinations of input and verify the Truth Table.
3. Fill the outputs in above blank Truth Table.
4. Repeat the same procedure for other gates by NAND gate and NOR gate.

CONCLUSION:

QUESTIONS:

1. Why NAND and NOR are called Universal Gates?
2. Design XOR Gate using NOR Gate.
3. Which ICs are used for NAND and NOR Gate?

ANSWERS:

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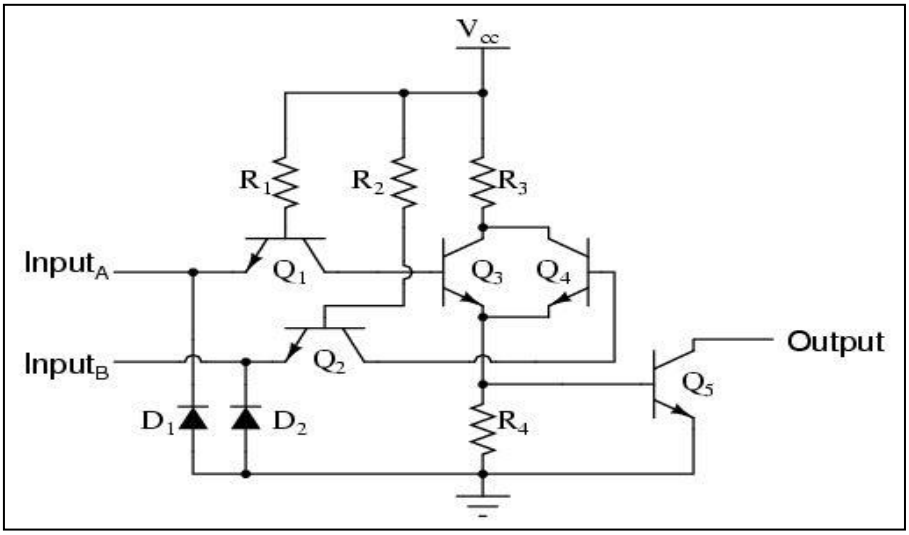
EXPERIMENT NO. 3

AIM: Design NOR & OR using TTL logic

APPARATUS:

THEORY:

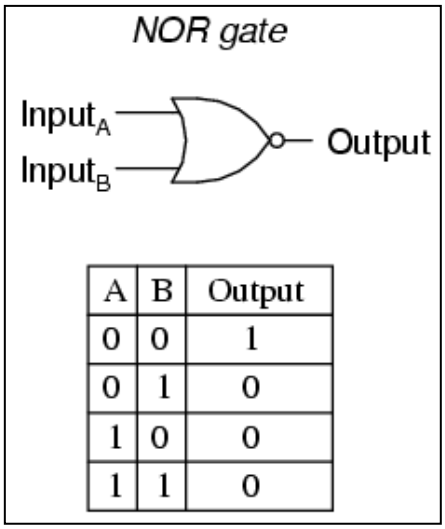
A:: NOR using TTL Logic



Transistors Q_1 and Q_2 are both arranged in the same manner that we've seen for transistor Q_1 in all the other TTL circuits. Rather than functioning as amplifiers, Q_1 and Q_2 are both being used as two-diode "steering" networks. If input A is left floating (or connected to V_{cc}), current will go through the base of transistor Q_3, saturating it. If input A is grounded, that current is diverted away from Q_3's base through the left steering diode of "Q_1," thus forcing Q_3 into cutoff. The same can be said for input B and transistor Q_4: the logic level of input B determines Q_4's conduction: either saturated or cutoff.

Notice how transistors Q_3 and Q_4 are paralleled at their collector and emitter terminals. In essence, these two transistors are acting as paralleled switches, allowing current through resistors R_3 and R_4 according to the logic levels of inputs A and B. If *any* input is at a "high" (1) level, then at least one of the two transistors (Q_3 and/or Q_4) will be saturated, allowing current through resistors R_3 and R_4, and turning on the final output transistor Q_5 for a "low" (0) logic level output. The only way the output of this circuit can ever assume a "high" (1) state is if *both* Q_3 and Q_4 are cut off, which means *both* inputs would have to be grounded, or "low" (0).

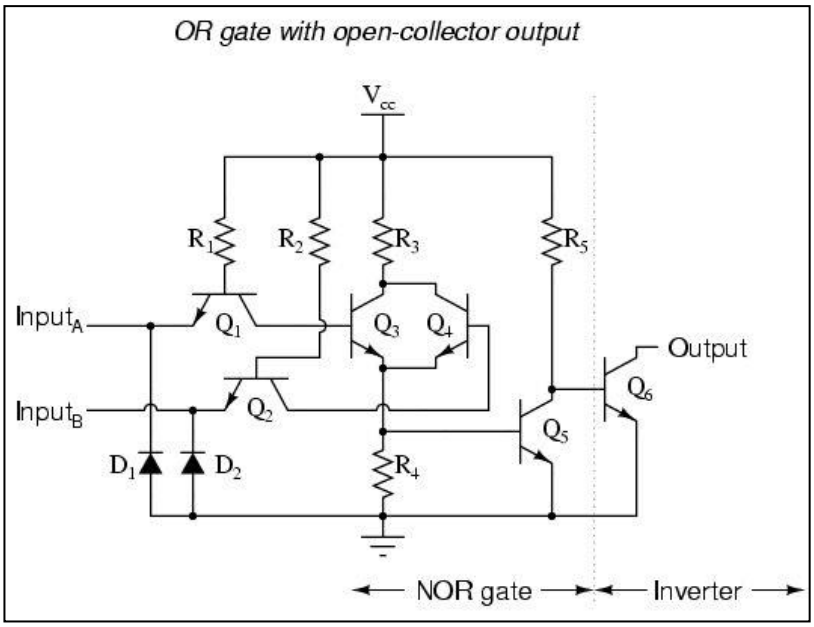
This circuit's truth table, then, is equivalent to that of the NOR gate:

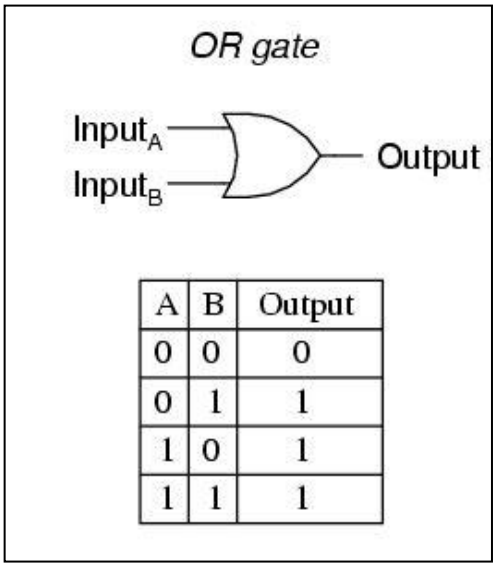


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

B: OR using TTL Logic:

In order to turn this NOR gate circuit into an OR gate, we would have to invert the output logic level with another transistor stage, just like we did with the NAND-to-AND gate example:





A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

PROCEDURE :

- Apply power supply to transistor via 3 resistor according circuit diagram.
- Take 5 NPN transistors (2N3904 / BC457) and make connections according to circuit diagram. Q1 and Q2 Emitter is used as input terminal and from Q5 transistor's collector , take output. (to check the output connect LED at output side or connect voltmeter to measure the voltage according to logic 1 and logic 0).
- Take 2 diodes (ST 1N4007 PN Junction Diode) connect them according to circuit diagram.
- For OR gate take another, transistor and resistor and connect them according to circuit diagram and take output from Q6 collector terminal.

CONCLUSION:

QUESTIONS:

1. Exlapin TTL Logic in brief?
2. Expalin difference between TTL and CMOS Logic Family?.
3. Design NOT using TTL Logic?

ANSWERS :

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EXPERIMENT NO. 4

AIM: To study and Design Combinational circuits: Half adder and full adder.

APPARATUS:

THEORY:

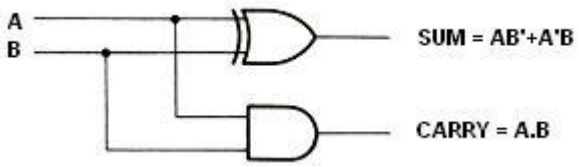
PART A: HALF-ADDER:

A Combinational circuit that performs the addition of two bits is known as a half-adder.

It requires two binary inputs and two outputs. The input variables indicate augends and addend bits; the output variables indicate the sum and carry.

S = A'B + AB'
C = AB

(I) Logic Diagram :



(II) Truth Table:

Input		Output	
A	**B**	**SUM**	**CARRY**
0	**0**		
0	**1**		
1	**0**		
1	**1**		

PART B: FULL-ADDER:

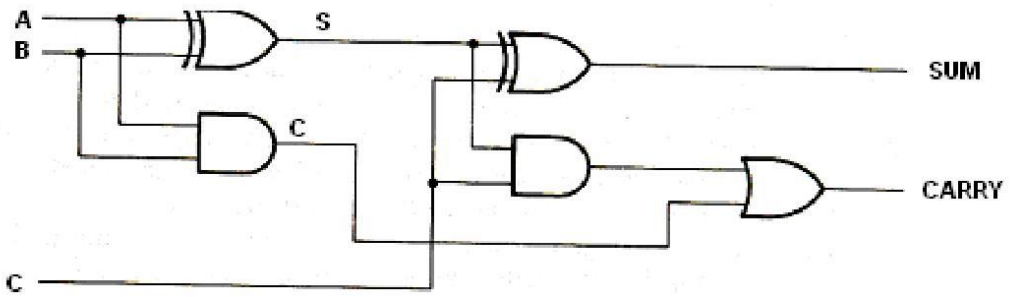
A Combinational circuit that performs the addition of two significant bits and a previous carry [three bits] is known as a full-adder.

A full-adder can be implemented with two half-adders.

It requires three binary inputs and two outputs. Two of the three input variables indicate two significant bits to be added. The third input represents the carry from the previous lower significant position.

(III) Logic Diagram :

$S = A \oplus B \oplus C$, $C = (A \oplus B)\, Cn\text{-}1 + AB$



(IV) Truth Table:

Input			Output	
A	**B**	**C**	**SUM**	**CARRY**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

PROCEDURE:

- Connect the circuit as shown in gate diagram.
- Apply different input combinations.
- See the output for different combinations and complete truth table.
- Compare practical and theoretical values from truth table.

CONCLUSION:

QUESTIONS:

1. Define combinational circuit.
2. How to Convert Half Adder into Full adder?
3. How many number of NAND gate is required to make full adder.

ANSWERS:

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EXPERIMENT NO. 5

AIM : To study and Design Combinational circuits: Half substractor and full substractor.

APPARATUS:

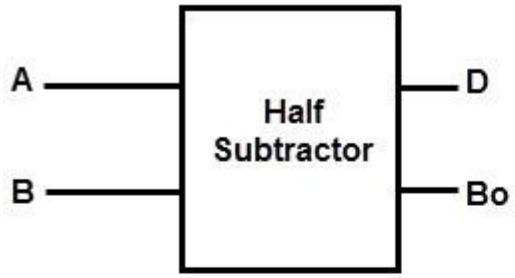
THEORY:

PART A:HALF-SUBSTRACTOR:

A Combinational circuit that performs the subtraction of two bits is known as a half-sub tractor. It requires two binary inputs and two outputs. The input variables indicate augends and addend bits; the output variables indicate the difference and borrow

$$D = A'B + AB'$$
$$B = A'B$$

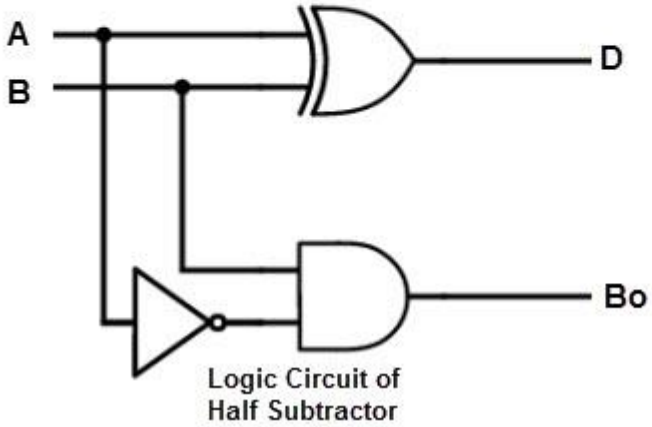
(I) Logic Diagram :



Block Diagram

A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table



Logic Circuit of
Half Subtractor

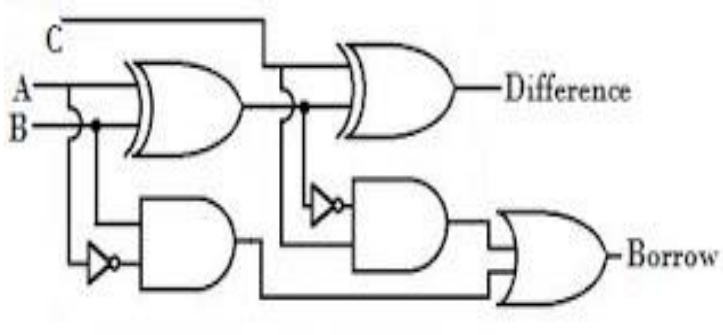
(II) Truth Table:

Input		Output	
A	**B**	**DIFF**	**BORROW**
0	**0**		
0	**1**		
1	**0**		
1	**1**		

PART B: FULL- SUBSTRACTOR

A Combinational circuit that performs the subtraction of two significant bits and a previous borrow [three bits] is known as a full-subtractor. A full-subtractor can be implemented with two half-subtrator. It requires three binary inputs and two outputs. Two of the three input variables indicate two significant bits to be subtracted. The third input represents borrow from the previous lower significant position.

(III) LOGIC DIAGRAM :



(IV) TRUTH TABLE:

Input			Output	
A	**B**	**C**	**DIFF.**	**BORROW**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

PROCEDURE:

- Connect circuit for different subtractor as shown in gate diagram.
- Apply logic voltage level to inputs of circuit from logic switches.
- See the outputs for different input combinations and complete truth table.
- Compare practical and theoretical values from truth table.

CONCLUSION:

QUESTIONS:

1. How many NOT Gate required for full subtractor?
2. Construct & find equation of half subtractor using K-Map.
3. Construct & find equation of full subtractor using K-Map.

ANSWERS:

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EXPERIMENT NO. 6

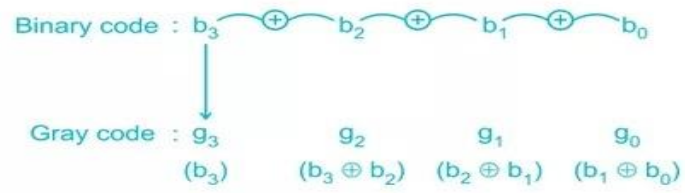
AIM: To design and realize a combinational circuit to convert binary to gray/gray to binary code.

APPRATUS:

THEORY:

PART A: BINARY TO GRAY CODE CONVERSION:

The logical circuit which converts binary code to equivalent gray code is known as **binary to gray code converter**. The gray code is a non weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray code can be obtained by reflecting an n-1 bit code about an axis after 2^{n-1} rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis. Reflection of Gray codes is shown below.



(Conversion Technique)

Example for Converting Binary number $(1110)_2$ to Gray code (1001)

OBSERVATION TABLE:

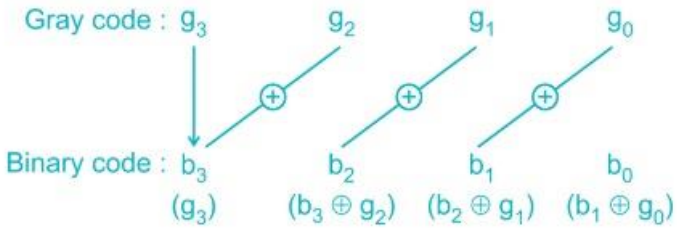
Sr. No	Binary Code				Gray Code			
	B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0				
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				

5	**0**	**1**	**0**	**1**				
6	**0**	**1**	**1**	**0**				
7	**0**	**1**	**1**	**1**				
8	**1**	**0**	**0**	**0**				
9	**1**	**0**	**0**	**1**				
10	**1**	**0**	**1**	**0**				
11	**1**	**0**	**1**	**1**				
12	**1**	**1**	**0**	**0**				
13	**1**	**1**	**0**	**1**				
14	**1**	**1**	**1**	**0**				
15	**1**	**1**	**1**	**1**				

CIRCUIT DIAGRAM:

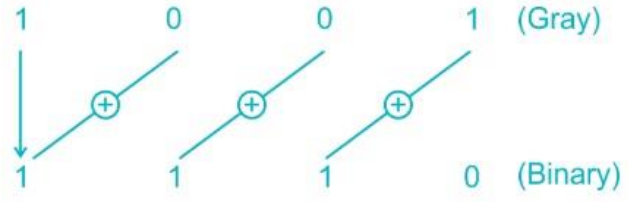
PART B: BINARY TO GRAY TO BINARY CODE CONVERSION:

Gray Code is unit Distance code i.e. between two Successive codes the number of changes in bits 1. Let Gray Code be g_3 g_2 g_1 g_0. Then the respective Binary Code can be obtained as follows:



(Conversation Process from Gray to Binary Code)

Example for Converting Binary number $(1001)_2$ to Gray code (1110)



OBSERVATION TABLE:

Sr. No	Gray Code				Binary Code			
	G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0				
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				

13	**1**	**1**	**0**	**1**				
14	**1**	**1**	**1**	**0**				
15	**1**	**1**	**1**	**1**				

CIRCUIT DIAGRAM:

PROCEDURE:

- The circuit connections are made as shown in fig.
- Pin (14) is connected to +Vcc and Pin (7) to ground.
- In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs G0, G1, G2, and G3 are taken for all the 16 combinations of the input.
- In the case of gray to binary conversion, the inputs G0, G1, G2 and G3 are given at respective pins and outputs B0, B1, B2, and B3 are taken for all the 16 combinations of inputs.
- The values of the outputs are tabulated.

CONCLUSION:

QUESTIONS:

1) Find equation of Binary to Gray code conversion using K-Map
2) List out applications of Code Convertors
3) Find equation of Gray to binary code conversion using K-Map**.**

ANSWERS:

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EXPERIMENT NO: 7

AIM: To Study and Design of multiplexer

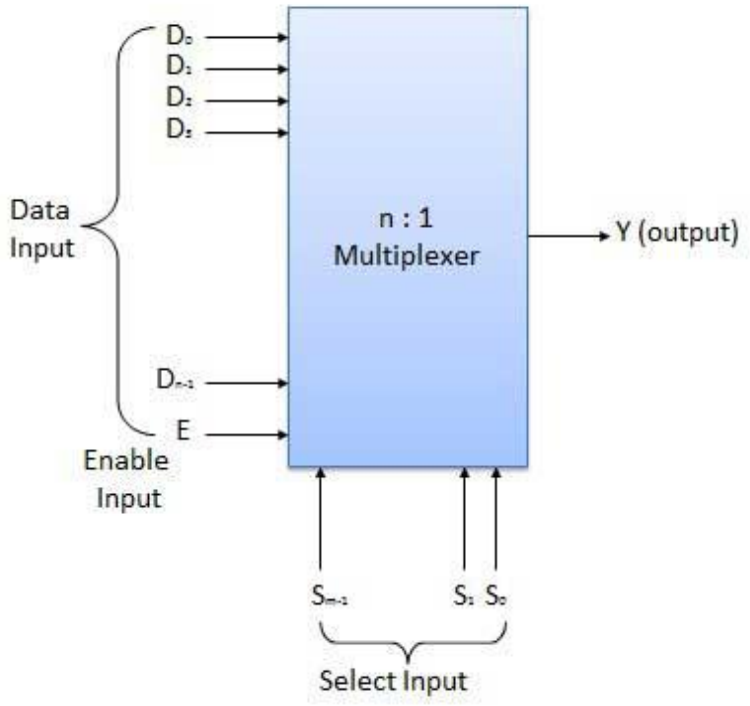
APPRATUS:

THEORY:

A Multiplexer is a special type of combination circuit which select one of the 'n'data inputs and routes it to the output. The selection of one of the 'n' input is done with the help of select inputs

To select n inputs, we need 'm' select lines such that 2^m =n.

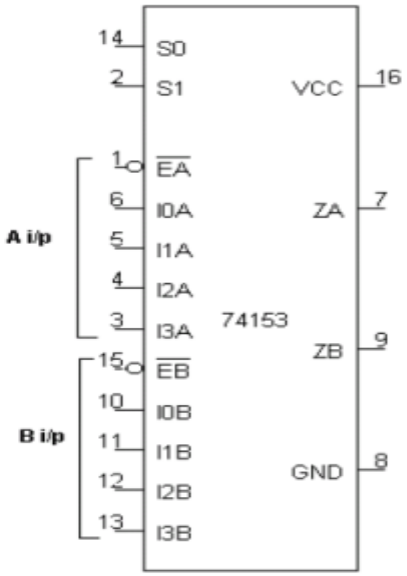
BLOCK DIAGRAM:



TYPES :

1) 2 *1 Multiplexer 2) 4*1 Multiplexer 3) 8*1 Multiplexer 4)16 *1 Multiplexer

Pin Details: -



Truth Table: -

CHANNEL – A							
INPUTS					SELECT LINES		O/P
Ea	Ioa	I1a	I2a	I3a	S1	S2	Za(v)
1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1

CHANNEL – B							
INPUTS					SELECT LINES		O/P
Ea	Iob	I1b	I2b	I3b	S1	S2	Za(v)
1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1

PROCEDURE:

- The Pin [16] is connected to + Vcc.
- Pin [8] is connected to ground.
- The inputs are applied either to „A“ input or „B“ input.
- If MUX „A“ has to be initialized, Ea is made low and if MUX „B“ has to be initialized, Eb is made low.
- Based on the selection lines one of the inputs will be selected at the output and thus verify the truth table.

PIN DIAGRAM (IC 74151):

LOGIC SYMBOL 8:1 MUX:

INTERNAL DIGRAM 8:1 MUX:

TRUTH TABLE 8:1 MUX:

CONCLUSION:

QUESTIONS:

1) What are different types of MUX?
2) List o:ut applications of MUX and explain any one in detail.
3) Make 8:1 MUX using 4:1 and 2:1 MUX.

ANSWERS:

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EXPERIMENT NO.8

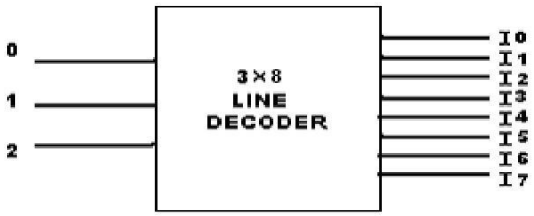
AIM: To Study and Design Decoder circuit.

APPARATUS:

THEORY:

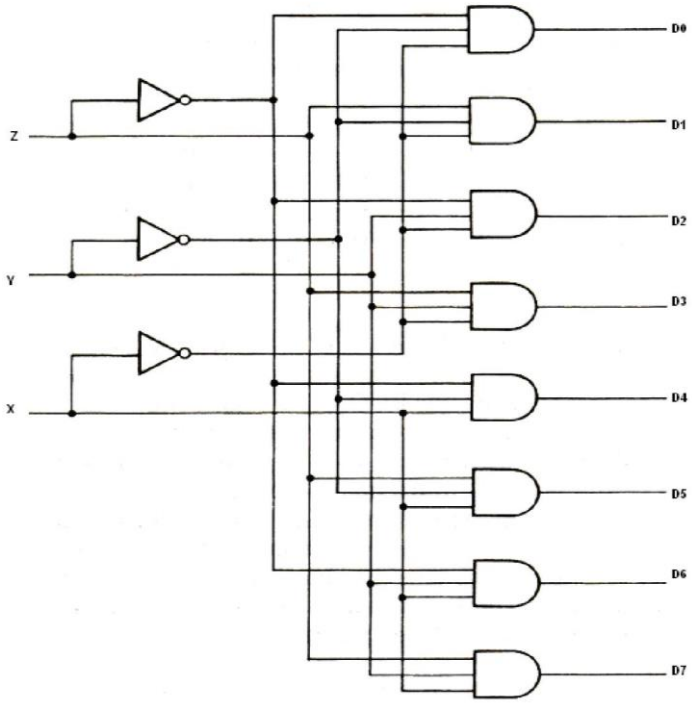
DECODER: It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique o/p lines. If the n-bit decoded information has unused or don't care combinations, the decoder o/p will have less than 2^n o/ps.

BLOCK DIAGRAM:



CIRCUIT DIAGRAM:

3:8 DECODER



TRUTH TABLE:

INPUT			OUTPUT							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

BCD TO DECIMAL DECODER CIRCUIT:
INTRODUCTION:

LOGIC DIGRAM:

TRUTH TABLE:

PROCEDURE:

- Here D0, D1, D2, D3, D4, D5, D6, D7 outputs are connected to output LED indicator.
- Control inputs X, Y, Z are connected to logic switches.
- Now keep Enable input to LOW level by logic switch.
- Now vary input control signals X, Y, Z and observe the outputs D0 to D7.
- The output is low corresponding to control signals X, Y, Z signals.
- Now connect Enable input to +5V and see the output for different combination of control signals.

CONCLUSION:

QUESTIONS:

1. List out different types of decoder circuits and explain 2:4 decoder in detail.
2. Write applications of a decoder and explain any one in detail.
3. Make 2:4 decoder using 1:4 DEMUX.

ANSWERS:

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EXPERIMENT NO.9

AIM : To Study and Design SR flip flop and D flip flop

PART A:: To Study and Design SR flip-flop

APPARATUS:

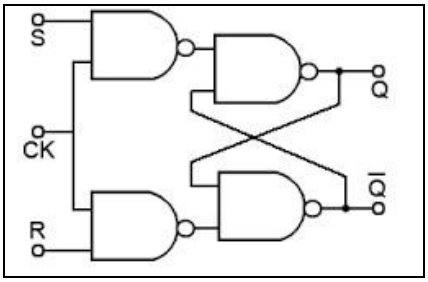
THEORY:

Flip flop‟s are sequential circuit which store 1-bit of data at a time. It is used to build the counter and shift register in digital circuit.

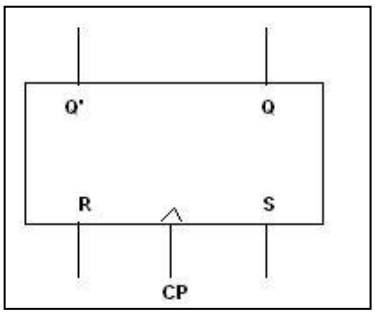
Clock R-S FLIP FLOP:

In some applications it becomes necessary to set or reset the RS-FF in synchronism with clock pulse. This is achieved by adding two more NOR gates to the RS-FF as shown in fig. It responds to input data only when the clock input is 1. When the clock input is 0 circuits is independent of inputs R and S. Hence no change in the state of the FF occurs in between two clock pulses.

(I) LOGIC DIAGRAM:



(II) GRAPHICAL SYMBOL



(III) TRUTH TABLE:

Q	S	R	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(IV) DETAIL OPERATION OF RS FLIP-FLOP :

PROCEDURE: (For S-R Flip Flop)

- Connect circuit as shown in gate diagram of R-S flip flop.
- Feed the R and S inputs with the logic level source marked as „High" and „Low".
- Feed the clock pulse to clock input using the pulsar and observe the output for all combination of R and S.

CONCLUSION:

QUESTIONS:

1. What is the limitation of RS flip flop?
2. Why clock is required?
3. What is significance of preset and clear inputs?

ANSWERS:

PART B : To Study and Design D flip flop

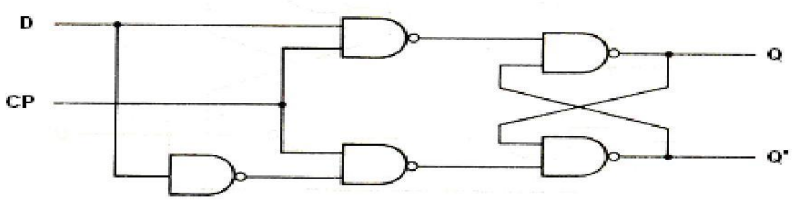
APPARATUS:

THEORY:

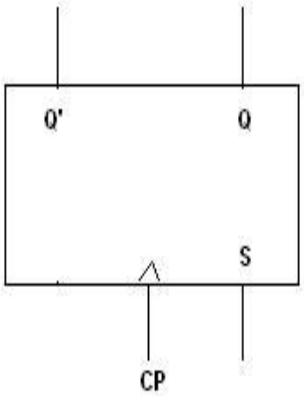
D FLIP FLOP:

The RS-FF can be modified to prevent the Race around state mentioned above by introducing an inverting forbidden gate in one of the inputs as shown in fig. The datas are stored in memory and are presented at Q during the clock pulse; hence the name data latch.

(I) LOGIC DIAGRAM:



(II) GRAPHICAL SYMBOL:



(III) TRUTH TABLE:

Q	D	Q(t+1)
0	0	
0	1	
1	0	
1	1	

(IV) DETAIL OPERATION OF D FLIP-FLOP :

PROCEDURE: (For D Flip-flop)

- Connect the circuit as shown in gate diagram of D flip flop.
- Feed the D input with the logic level source marked as “High” and “Low”.
- Feed the clock pulse with the help of pulsar circuit to the clock input and observe the output for all combination of D.

CONCLUSION:

QUESTIONS:

1. Design D flip flop using JK flip flop.
2. Why D flip flop is called as delayed flip flop?
3. Why D flip flop used to make register.

ANSWERS:

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EXPERIMENT NO. 10

AIM : To verify operation of JK flip flop and T flip flop.

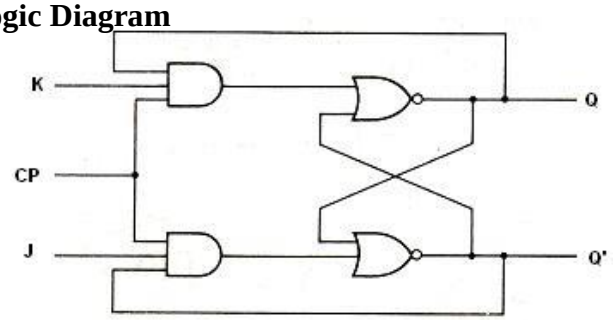
PART A: To verify operation of JK flip flop

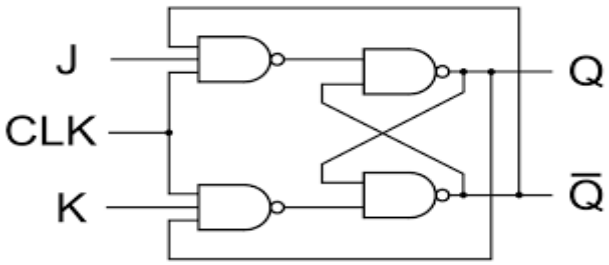
APPARATUS:

THEORY:

Flip flops are sequential circuit which store 1-bit of data at a time. It is used to build the counter and shift register in digital circuit.

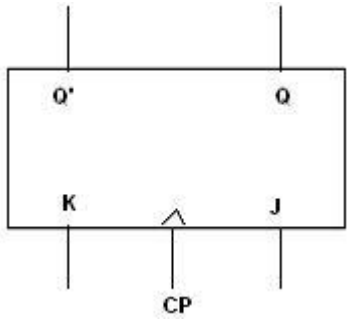
(I) Logic Diagram





JK Flip flop using NAND Gate

(II) Graphical Symbol



(III) Truth Table:

Q	J	K	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(IV)DETAIL OPERATION OF JK FLIP-FLOP :

PROCEDURE:

- Connect the circuit as shown in gate diagram of JK flip flop.
- Feed the JK input with the logic level source marked as “High” and “Low”
- Feed the clock pulse with the help of pulsar circuit to the clock input and observe the output for all combination of JK.

CONCLUSION:

QUESTIONS:

1. Convert JK Flipflop to T flipflop.
2. State difference between JK and SR.
3. Convert JK Flip flop to D flip flop.

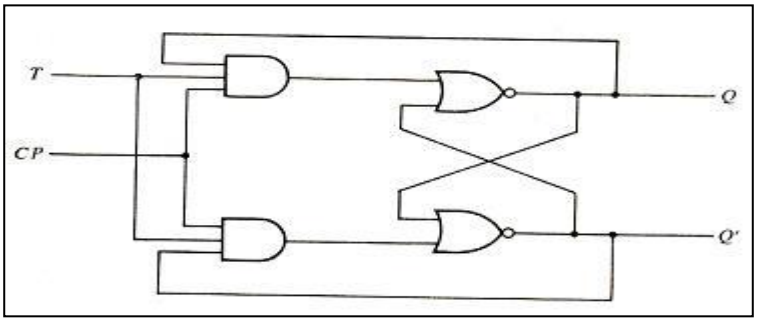
ANSWERS:

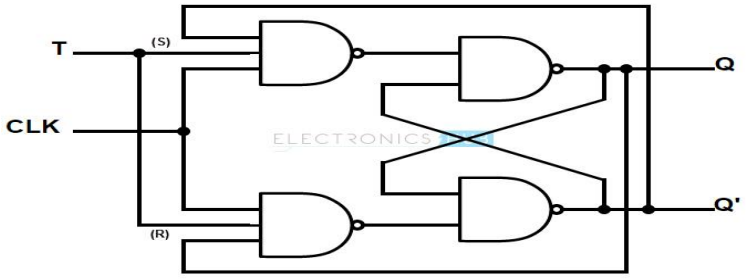
PART B: To verify operation of T flip flop

APPARATUS

THEORY:
It is possible to achieve toggling with the help of J-K flip flop by simply connecting J&K inputs to high level. Such type of flip flop is known as T flip flop.

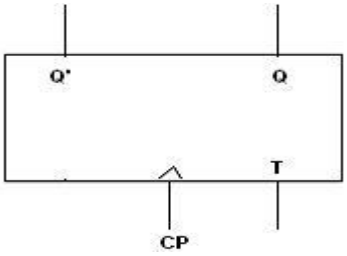
(I) Logic Diagram:





T FLIP –FLOP using NAND Gate

(II) Graphical Symbol:



(III) Truth Table:

Q	T	Q(t+1)
0	0	
0	1	
1	0	
Q	1	

IV) DETAIL OPERATION OF T FLIP-FLOP :

PROCEDURE:

- Connect the circuit as shown in gate diagram of T flip flop.
- Feed the D input with the logic level source marked as “High” and “Low”.
- Feed the clock pulse with the help of pulsar circuit to the clock input and observe the output for all combination of T.

CONCLUSION:

QUESTIONS:

1. What is the difference between JK and T flip-flop?
2. In T flip-flop, what is meaning of T?
3. Why T- flip-flop used in counter?

ANSWERS:

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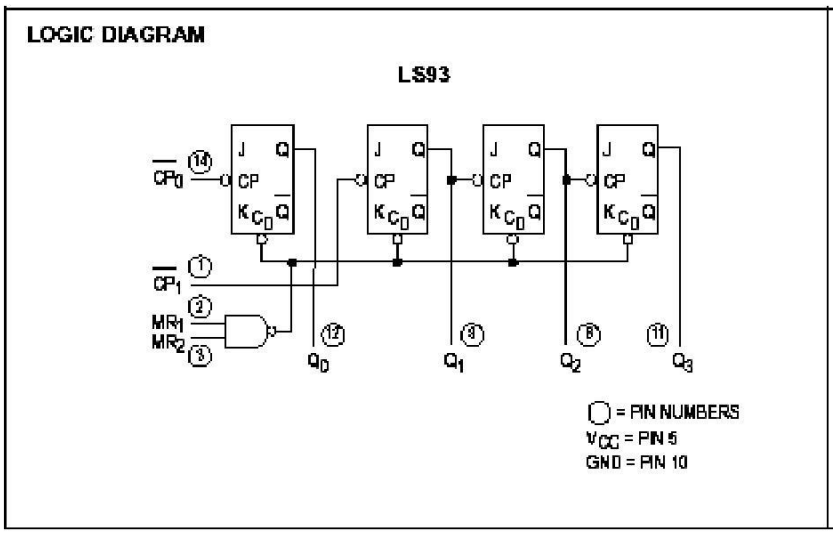
EXPERIMENT NO:11

AIM: To realize and configure 4-bit ripple counter.

APPARATUS:

CIRCUIT:



THEORY:

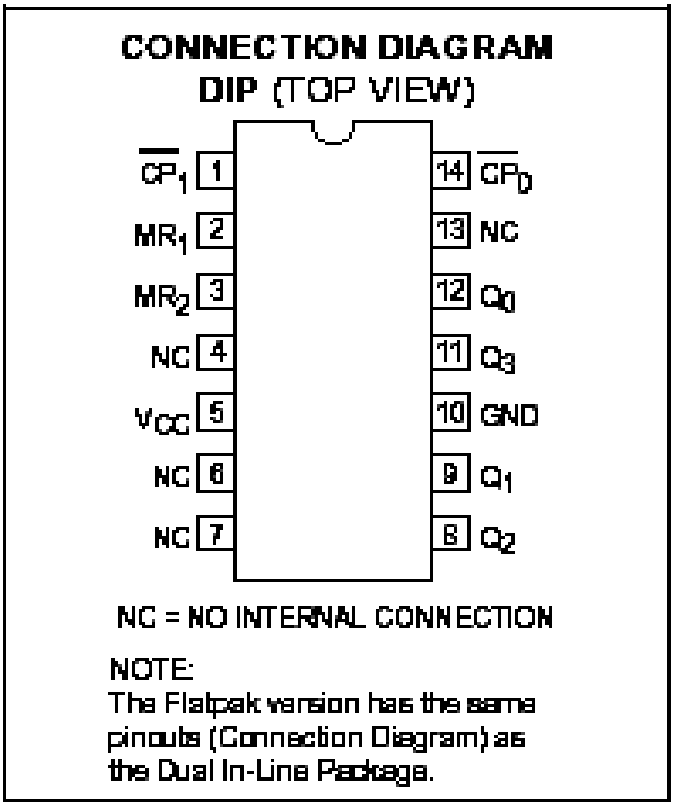
A counter is one of important digital electronic circuits. Here, we study the ripple counter or asynchronous counter. Counters are of two types which are synchronous counter & asynchronous counter. Ripple counter are constructed by using J-K flip-flops with J=1 & k=1. 4 J-K flip-flops are required for 4 bit counter. A square wave drives the first flip-flop. The output of flip-flop a drive B flip-flop derive c flip-flop which derives D flip-flop.

All the input J-K flip-flop are tied to +Vcc. Under these situations each flip-flop changes its state when a positive edge clock pulse occurs. This 4 bit counter is also known as modulo 16 counters.

Truth Table:

COUNT	2^0	2^1	2^2	2^3
0	0	0	0	0
1	1	0	0	0
	0	1	0	0
3	1	1	0	0
…	…	…	…	…
14	0	1	1	1
15	1	1	1	1

Pin Diagram:



PROCEDURE:-

- Connect +5 V DC supply
- Connect pulse input to clock 1 input of IC 74C93
- Connect Qa,Qb,Qc and Qd outputs to D1,D2,D3 and D4 inputs of BCD display.
- Connect jumper between the Clk 2 and Q4 output.
- Connect either pin 2 or pin 3 (reset output) to ground.
- Apply counting pulse by pushing switch. Apply one plus at a time.The BCD show „O" to „9" counting and then will show five other states after 10^{th} pulse. Then after 16^{th} pulse, output will reset to zero.
- You can also supply continue pulse by connecting clock generator output pulse.
- The output Qa, Qb, Qc, and Qd can also be connected to output indicators to observe binary outputs.

CONCLUSION:-

QUESTIONS:

1) List out different types of Counters .
2) What is Modulo Counter?

ANSWERS :

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EXPERIMENT- 12

AIM : To Study & Design Shift Registers

APPARTUS:

THEORY:

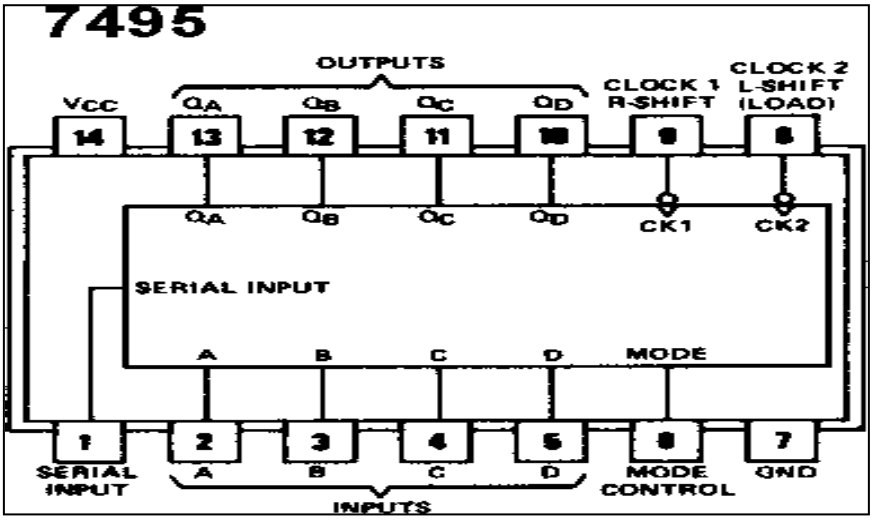
The binary data in a register cab be moved within the register from one flip flop to the other or outside it with application of clock pulse. The register that allow such data transfer are called as shift Register. They are used for data storage , data transfer and certain arithmetic and logic operations.

Modes of operation of Shift Register:

The various modes in which a shift register can operate are as follows:

1) Serial In serial out (SISO)
2) Serial In Parallel Out (SIPO)
3) Parallel In Serial Out (PISO)
4) Parallel In Parallel Out (PIPO)

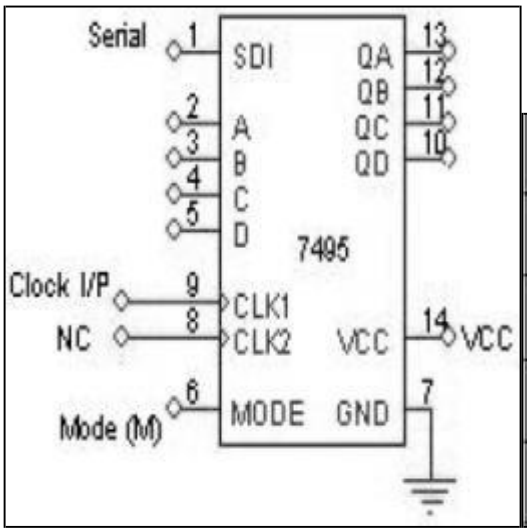
PIN Diagram Of IC 7495:



DETAIL DESCRIPTION OF OPERATING MODES OF SHIFT REGISTERS:

Serial In Parallel Out (SIPO):

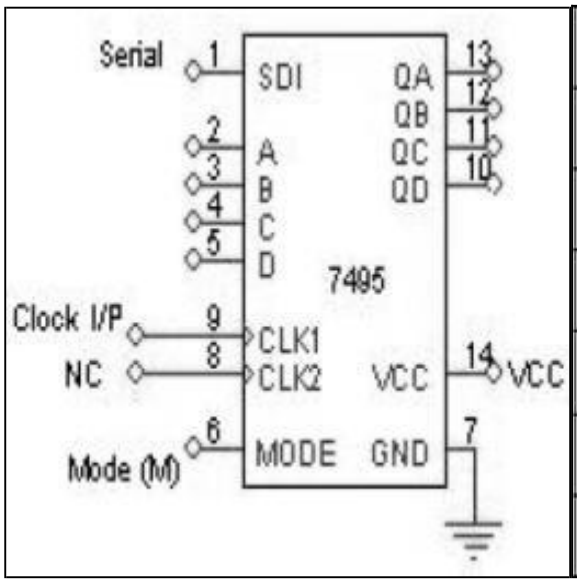
Circuit Diagram **Truth table**



Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

Serial In Serial Out (SISO):

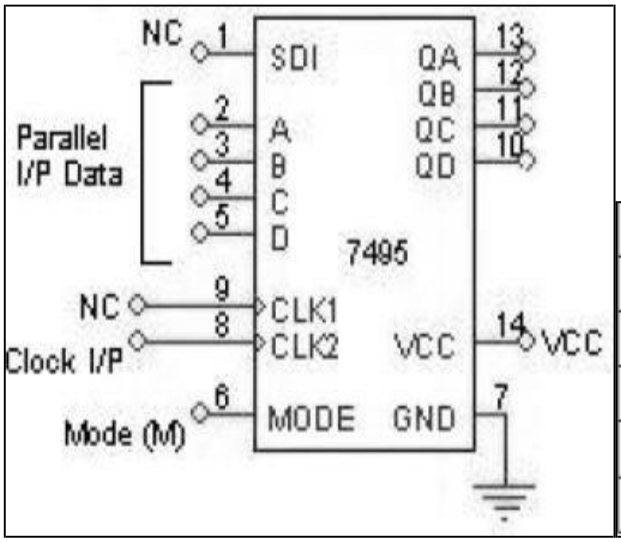
Circuit Diagram **Truth table**



Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2

Parallel In Serial Out (PISO):

Circuit Diagram

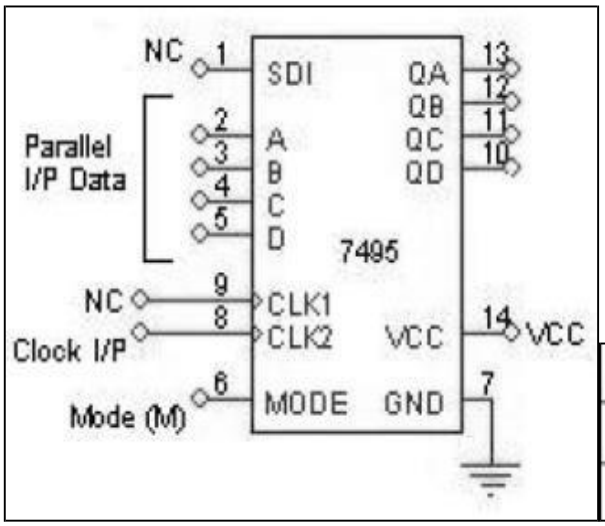


Truth table

Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

Parallel In Parallel Out (PIPO):

Circuit Diagram



Truth table

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

PROCEDURE:

Serial In Parallel Out (SIPO):-

- Connections are made as per circuit diagram.
- Apply the data at serial i/p
- Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
- Apply the next data at serial i/p.
- Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.

- Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register

Serial In Serial Out(SISO):-

- Connections are made as per circuit diagram.
- Load the shift register with 4 bits of data one by one serially.
- At the end of 4th clock pulse the first data „d0" appears at QD.
- Apply another clock pulse; the second data „d1" appears at QD.
- Apply another clock pulse; the third data appears at QD.
- Application of next clock pulse will enable the 4th data d3" to appear at QD. Thus the data applied serially at the input comes out serially at QD

Parallel In Serial Out (PISO):-

- Connections are made as per circuit diagram.
- Apply the desired 4 bit data at A, B, C and D.
- Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
- Now mode control M=0. Apply clock pulses one by one and observe the
- Data coming out serially at QD.

Parallel In Parallel Out (PIPO):-

- Connections are made as per circuit diagram.
- Apply the 4 bit data at A, B, C and D.
- Apply one clock pulse at Clock 2 (Note: Mode control M=1) and The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively

CONCLUSION:-

QUESTIONS:

1) List out application of shift Registers
2) Explain in detail any one application of shift register.

ANSWERS:

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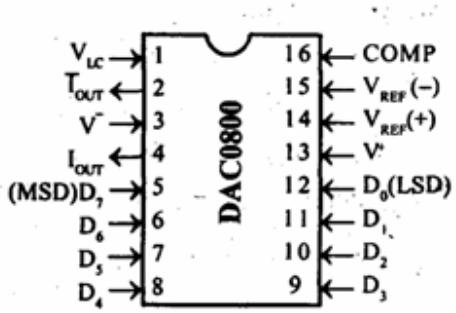
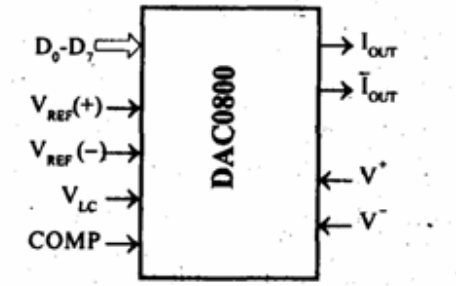
EXPERIMENT NO.13

AIM : To study the D/A (DAC- 0800) & A/D (ADS- 0809) converters IC with its specification

APPARATUS:

PART A : Pin Diagram of DAC- 0800 converter IC





Pin	Description
D_0-D_7	Digital input data
I_{OUT}	Current output
$\overline{I}_{OUT}$	Complement of output current
V^-	Negative supply voltage
V^+	Positive supply voltage
COMP	Compensation voltage
V_{LC}	Threshold control
$V_{REF}(+)$	Positive reference voltage
$V_{REF}(-)$	Negative reference voltage

MSD - Most Significant Digit
LSD - Least Significant Digit

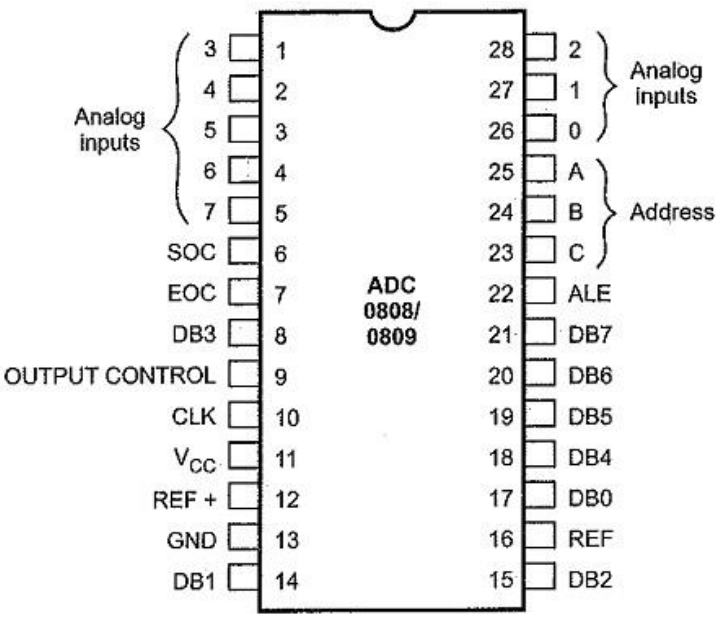
PROCEDURE:

CONCLUSION:

Questions:

1. **Explain the application of DAC-0800 IC.**

PART B : Pin Diagram of ADC- 0809 converter IC



Pin Number	Function
1 to 5 and 26,27,28	**Analog Inputs**
6	**SOC- Start of Command**
7	**EOC- End of Command**
8,14, 15, 18, 17, 19, 20, 21,	**DB0 to DB7**
23, 24, 25	**Address Pins**
9 and 10	**Output control and clock respectively**
11 and 13	**Vcc and GND**
12	**Reference Voltage**

PROCEDURE:

CONCLUSION:

Questions:

2. Explain the application of ADC-0809 IC.

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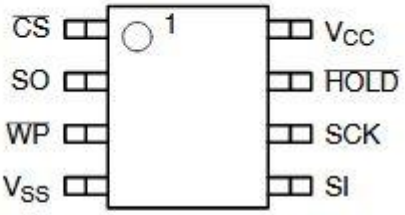
EXPERIMENT NO.14

AIM : To study the construction and working of any one memory IC from data sheets

APPARATUS:

THEORY : PIN CONFIGURATION & IC DETAILS

PIN CONFIGURATION



SOIC (V), TSSOP (Y), UDFN (HU4)

For the location of Pin 1, please consult the corresponding package drawing.

SOIC–8
V SUFFIX
CASE 751BD

UDFN–8
HU4 SUFFIX
CASE 517AZ

TSSOP–8
Y SUFFIX
CASE 948AL

Description

The CAT25010/20/40 are a EEPROM Serial 1/2/4−Kb SPI devices Internally organized as 128x8/256x8/512x8 bits. They feature a 16−byte page write buffer and support the Serial Peripheral Interface (SPI) protocol. The device is enabled through a Chip Select (CS) input. In addition, the required bus signals are a clock input (SCK), data input (SI) and data output (SO) lines. The HOLD input may be used to pause any serial communication with the CAT25010/20/40 device. These devices feature software and hardware write protection, including partial as well as full array protection.

PROCEDURE:

CONCLUSION:

Questions:

1. **Explain the Working of EEPROM.**

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