Anirudh Nakra

N-51 Nivedita Kuni, New Delhi, 110022 • (+91) 9013137732 • anirudhnakra4@gmail.com

EDUCATION

Delhi Technological University

Bachelor of Technology

Major: Electronics and Communication Engineering

Capstone Research: Circularly polarized antennas for 5G systems

New Delhi

Jul 2021(Expected)

CGPA: 8.9 (Till 7th Semester)

Last 60 Credit Hours CGPA: 9.77

Department rank 1: 7th semester, Department rank 1: 6th semester, Department rank 3: 5th semester, Department rank 3: 4th semester

Delhi Public School, RK Puram

Class 12, CBSE

Principal's Gold Medalist

Top 2.5 percentile of CBSE Board 2017 (all India)

Top 1.5 percentile of IEE Mains 2017

New Delhi Jul 2017

Percentage: 96.4%

PUBLICATIONS

1. Anirudh Nakra, Abhijeet Vats, Asok De "Design of High Bandwidth Circularly Polarized Antipodal Vivaldi Array for 5G Applications" Accepted at IEEE International Conference of Emerging Technologies (INCET) 2021

RESEARCH AND WORK EXPERIENCE

Research Intern, Neuromechanics group, Centre for Biomedical Engineering (Remote due to COVID-19) Indian Institute of Technology, Delhi

Sept 2020—Present

Delhi, India

- Working on devising a computational model and an IOT/Wearable based framework for COVID-19 prediction
- · Reviewing the effectiveness of oxygen saturation, ECG ST-segment elevation, respiratory rate in pandemic prediction models
- Analyzing and implementing various SIR, MLP-ICA, ANFIS, SVM, ANN like CDNet based ML models
- Review paper in preparation to be submitted to IEEE Reviews in Biomedical Engineering

Lead Undergraduate Researcher, Department of Electronics & Communication Engineering Delhi Technological University

Aug2020—Present

Delhi, India

- Working on "Design of High Bandwidth Circularly Polarized Antipodal Vivaldi Array for 5G Applications"
- CST and HFSS implementations of antennas such as printed lotus Quasi Yagi and Antipodal Vivaldi antenna
- CST implementation of high isolation 6 stage Wilkinson Power Splitter
- Design of broadside coupling based 90-degree phase shifter
- Designed the integrated system with an Axial Ratio that was 0.098 dB at the design frequency
- Ongoing refinement of design to fabricate the system

Lead Undergraduate Researcher, Department of Electronics & Communication Engineering Delhi Technological University

Aug2019—Present

Delhi, India

- Working on "Terrain Imaging for Locomotive Drivers Infra-Red, Enhanced Optical and Rangefinder Assisted."
- MATLAB implementation of rail line detection using Radon and Hough transform.
- · MATLAB implementation of night time object detection using modified DECOLOR and adaptive thresholding
- · Created a noise removal hybrid MRF-dark channel prior system via OpenCV and MATLAB
- Formulating fusion-based template matching and coupling system for better object detection results. Manuscript in preparation.
- Implemented moving image optical flow system and improving the results using "normal flow" methodology

Summer Research Intern, Department of Electronics & Communication Engineering Delhi Technological University

Jun-Jul 2020

Delhi, India

- Worked on old manuscript classification system of scripts such as Tamil, Telugu, Devanagari
- Analyzed different document matching systems: SWM, MODS, HWNet
- Created a literature review of different segmentation methodologies in complex scripts: Docstrum, Voronoi, XY Cut, Smearing
- · Surveyed HWNet based framework for robust word spotting and recognition in handwritten word images
- Studied and compared text document classification models on multilingual and monolingual text documents: LINGO, SVM, LanideNN

RADAR Intern

Jun-Aug 2019

Ghaziabad, U.P, India

Bharat Electronics (BEL), Sahibabad

- Trained on the basics, operations and applications of RADAR systems deployed by Indian Armed Forces
- · Worked on the company's venture 'Rohini Radar' comprehending the related industrial practice
- MATLAB simulation of various antennas and RADAR technologies such as CFAR, Patch Antennas, Pulse compression
- Awarded "Excellent" grade in BEL internship

PROJECTS

Construction of a novel CO-OFDMA WDM integrated RoF system

Aug2020- Oct 2020

- Synthesized a circuitry system for WDM- Coherent OFDMA system on Optisystem software
- Improving noise margins and increasing SNR by modifying the receiver system based on an intradyne based architecture
- · Suggested coherent intradyne based receiver and filter modifications to decrease BER and created a new RF-optical transmitter and receiver
- · Successful in creating a working model and working on a preliminary draft for a research paper

Digital Signatures: Applications and Implementations

2020- Oct 2020

- Literature review and identification of important SoC and software-based schemes for communication encryption such as hashing
- Simulating basic ciphers such as Caesar, different substitution cipher and ciphers like Vigenere, Base64, Playfair, RSA on C++ and Python
- Implementation of cryptographic algorithms like Secure hash, ECDSA, RSA
- · Application based study done comparing the effectiveness of the ciphers and algorithms in different situations

Comparison study on different microwave frequency antennas and their applications

Aug-Oct 2020

- Implemented different microstrip patch antennas and presented patch geometry modifications such as a circular or pentagonal shape
- Created Vivaldi and Quasi-Yagi antenna designs from scratch along with their parameter and dimensional calculations
- HFSS implementation of 5 antennas: microstrip patch, modified microstrip patch, UWB microstrip patch, Vivaldi and Quasi Yagi
- Comparison of the workings of different antennas based on parameters like radiation efficiency, return losses, Q/Qib, directivity, etc

Verilog implementation of Multiple Input Signature Register (MISR) and Type 1/Type 2 Linear Feedback Shift Register (LFSR)

Jan — Jun2020

- Created a literature review of LFSRs and analyzed their performance parameters such as power consumption, propagation delay
- Implemented on Verilog HDL and C++ Type 1 LFSR, Type 2 LFSR, MISR, Geffe generators, Cellular Automata
- · Created a novel communication scrambler using a modification of an existing LFSR polynomial
- Suggested improvements over existing systems such as GLFSR, Weighted PRNG, Low power LFSR design through VLSI logic

Radio Frequency Identification (RFID) Based Indoor Navigation System for Visually Impaired

Apr-June2020

- Created a navigational aid system for the visually impaired via RFID
- Created a hardware architecture to interface and use the system using MINI-MAX 51, EMIC module, SR-07 Kit, Parallax RFID reader
- Devised a framework and modified the A* algorithm to suit our needs by implemented a navigating software based on F, G and H costs.
- Implemented the whole system using Proteus 8.6 and MPLAB X IDE v8.63 in C language.

Design of a microprocessor-based traffic signal controller for a junction of four roads

Sept-Nov 2019

- Created a 8085 based traffic signal controller
- Setup was chosen as to emulate the actual traffic conditions with a roundabout
- The algorithm was implemented on MASM assembler and a presentation was given to the Laboratory Teacher in charge
- Awarded the highest grade based on the ppt, verbal presentation and actual code implementation

RELEVANT COURSEWORK & GRADES

Communication Systems (O)	Wireless Sensor Networks (O)	Microprocessors and Interfacing (O)
Digital Communications (A+)	Linear Integrated Circuits (O)	Analog Electronics- II (O)
Digital Signal Processing (O)	Embedded Systems (O)	Electromagnetics (A+)
Computer Vision (O)	Digital Electronics- II (O)	Computer Architecture (A+)
Machine Learning (O)	VLSI Design (O)	Testing & Diagnosis of Digital System Design (O)

Independent Studies:

MIT OCW 2018: Matrix Methods in Data Analysis, Signal Processing, and Machine Learning

IITD Robothlon 2019: Project workshops on IoT, AI&Ml, Robotics

Coding Blocks 2018: Certificate course on python fundamentals

Coursera: Computational Neuroscience (Ongoing) Coursera: Deep Learning Specialization (Ongoing)

TECHNICAL COMPETENCIES

- <u>Language skills</u>: Python (pandas,numpy,scipy), MATLAB, openCV, Embedded C, LaTeX, VHDL, Verilog HDL, C++, C, HTML, MASM
- <u>Technical Softwares</u>: HFSS, OrCAD Capture CIS, OrCAD PSpice A/D, Proteus, Xilinx ISE, Cadence Virtuoso, OptiSystem, Simulink,

LTSpice, Xilinx Vivado, Anaconda, Clion, Turbo C++

• General Software: Microsoft Word, Microsoft Excel, Adobe

Photoshop (Elementary), Blender (Elementary)

• Languages: Hindi, English, Korean (Elementary)