SUPPLEMENTARY MATERIAL

# BASICS OF XILINX VIVADO

Department of Electronics and Communication Engineering
Indian Institute of Technology, Roorkee

ECN 104 Digital Logic Design

## Designing a factorial calculator

This is a short assignment where you will be using the skills you have already learned over the semester to design a simple factorial calculator. The design specification for the calculator are following.

1. The calculator takes a single 32 bit number as input.
2. The input is unsigned, that is you don't have to take care of the sign (number can only be positive).
3. Output of the calculator includes a single 32 bit number which will be the result and a single bit output indicating the overflow.
4. Overflow occurs when more than 32 bits are required to represent the result.

### Hints

1. You may use barrel shifter (designed in assignment 2) for performing multiplication.
2. Try not use 'For loops' unless you are completely sure of what you are trying to do. 'For loops' in Verilog are not for repeated execution of statements.
3. To change the radix of a signal in simulation window use the first few steps of this guide: https://sites.google.com/a/temple.edu/ece2612/home/xilinx-vivado-debugging

## Important guidlines for submission

You should follow the following these guidelines carefully, failing to which your assignment might not be properly evaluated.

1. You need to submit only one **ZIP** file; .RAR, .TAR or any other archive format will **not** be accepted.
2. The ZIP file will only contain the following:
   (a) Source code of the factorial calculator.
   (b) Testbench for the calculator.
   (c) A **PDF** containing full screen screen-shots of your simulations, source code and elaborated design. Please note that the screenshots should clearly indicate the functioning of your module.
   **NOTE**: Word documents (*.docx), open document (*.odf) or any other format will not be accepted.
   (d) Name of the PDF should be your enrollment number, e.g. 171160XX.pdf.
   (e) Simulation results should clearly show all the typical cases, including normal factorial calculation and overflow.