Assignment - 3

Department of Electronics and Communication Engineering
Indian Institute of Technology, Roorkee

ECN 104 Digital Logic Design

Problem 1

[Weightage: 100%]

All the solution for this problem must be contained within a single verilog file named '`solution_1.v`' while all the testbenches must be contained within '`tb_1.v`'

Circular Queue Implementation

One way to implement a FIFO buffer is to add a control circuit to a register file. The registers in the register file are arranged as a circular queue with two pointers. The *write pointer* points to the head of the queue, and the *read pointer* points to the tail of the queue. The corresponding pointers advance one position for each write or read operation. You have to implement and test operation of a 8 word circular queue (consider eight bits in a word). A FIFO buffer usually contains two status signals, `full` and `empty`, to indicate that the FIFO is full (i.e., cannot be written) and empty (i.e., cannot be read), respectively. One of the two conditions occurs when the read pointer is equal to the write pointer.

Hint - 1

The most difficult design task of the controller is to derive a mechanism to distinguish the two conditions. One scheme is to use two FFs to keep track of the empty and full statuses. The FFs are set to 1 and 0 during system initialization and then modified in each clock cycle according to the values of the `wr` and `rd` signals.
You can also read more about circular buffers at: https://en.wikipedia.org/wiki/Circular_buffer or watch https://www.youtube.com/watch?v=ia__kyuwGag .

Table 1: Module attributes for problem 1

Atrribute	Name	Size (in bits)	Direction
Module Name	fifo	_	_
Testbench Name	fifo_tb	_	_
Clock signal	clk	1	Input
Reset signal	reset	1	Input
Read signal	rd	1	Input
Write signal	wr	1	Input
Data to write	w_data	8	Input
Data to read	r_data	8	Output
Empty signal	empty	1	Output
Full signal	full	1	Output