

# ASSIGNMENT 1

## INTRODUCTION TO VERILOG

ECN 104 - Digital Logic Design  
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## Hardware Description Languages

Hardware description language (HDL) is a convenient, device independent way of representing digital logic. HDLs are helpful describing, simulating and verifying digital circuits.

### Why not use C/C++, Java...?

C/C++, Java are programming languages which are very good at what they were designed for, that is programming. However describing digital circuits in programming language is difficult and often confusing, which led to development of HDLs.

### Which HDL to use?

Today many Hardware description languages are available, each of them are different from each other in terms of functionality, semantic and grammar. In this course however we will be using Verilog 2001.

## Using Verilog 2001

As a beginner we are going to describe and simulate simple combinational circuit with Verilog.

## Design Flow

## Verilog Syntax

### Modules

Module is the basic building block in Verilog, modules helps in organizing and structuring designs in logical and human readable form. Module can be considered as analogous to functions in programming languages.

Listing 1: Sample module indicating its structure

```
1 module module_name( ...module_input_and_outputs... );  
2     ...  
3     // Module functionality  
4     ...  
5 endmodule;
```

An example of AND gate would be

Listing 2: Illustrative AND gate module

```
1 module andGate (inputA, inputB, result);  
2     ...  
3     // AND gate functionality  
4     ...  
5 endmodule
```

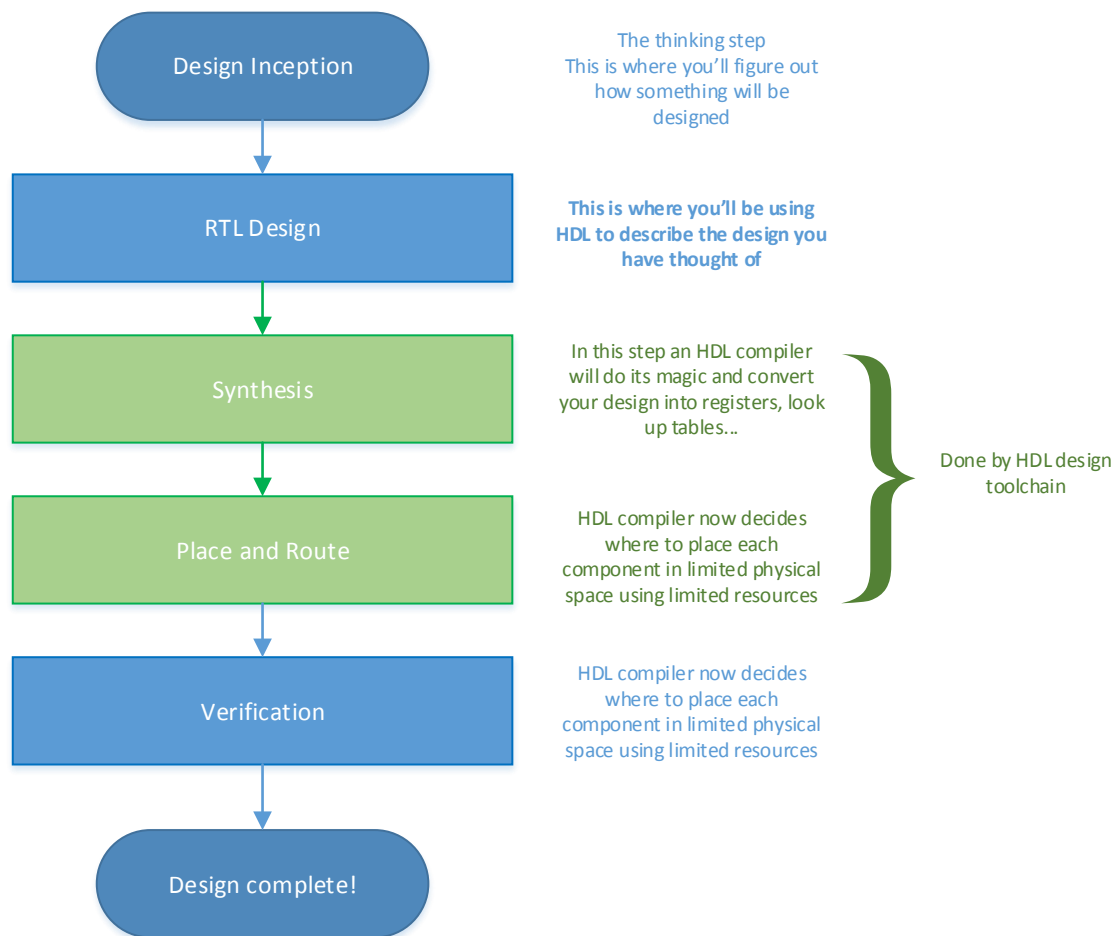


Figure 1: Example binary search tree constructed using names from Table ?? with insertion order and output port information.

## Instantiating modules

The process of creating objects of modules is called instantiation in Verilog. Modules are a

Listing 3: Illustrative AND gate module

```

1  // Define the top-level module called AndGate3 which is a three
2  // input AND gate. It instantiates 2 2-input AND gates.
3  // Interconnections will be explained later
4  module AndGate3(input1, input2, input3, result);
5      input input1, input2, input3; // Declare variables as input
6      output result; // declare result as an output
7
8      wire    result1; // To be explained later
9
10     // Instatiation of 2-input AND gates
11     AndGate2(input1, input2, result1);
12     AndGate2(result1, input3, result);
13 endmodule
14
15 // Define a module AndGate2 which is a 2-input AND gate.
16 module AndGate2(input1, input2, result);
17     // Assignment would be explained later
18     assign result = input1 & input2;
19 endmodule
  
```

## Comments

Comments in verilog are of two kinds:

### Single Line Comment

Two forward slashes represents beginning of a single line comment in verilog, any character after the two forward slashes will be ignored by verilog compiler until the end of line.

Listing 4: Single line comment

```
1 ...  
2 // This is a single line comment  
3 ...
```

### Block Comment

Block comments in verilog are used to comment more than one line, they start with '/\*' and ends with '\*/'. Anything between these two character sequences is ignored by the compiler.

Listing 5: Block comment

```
1 ...  
2 /*  
3 This is a block comment  
4 */  
5 ...
```

## Numerical Literals

### Sized Numbers

To represent digital circuits accurately Verilog allows defining numbers of fixed size. These numbers have the following format:

<size>'<character for base><number>

For example:

Listing 6: Example of sized numbers

```
1 6'b010010 // (18) 32-bit number in binary  
2 24'hc0ffee // (12648430) 24-bit number  
3 16'd255 // (255) 16-bit decimal number
```

### Unisized Numbers

Verilog also includes support for unisized numbers. These numbers are assumed to be of a particular size depending upon the compiler/machine.

## Constants

Global constants can be declared in Verilog. When Verilog code is processed all these constants will be replaced by their respective values. NOTE: Verilog constants always start with backtick ``.

Listing 7: Declaration and use of constants

```
1 `define A 2'200 // NOTE: Constant declarations do  
2 `define B 2'b01 // not end with semicolon!  
3 `define C 2'210  
4 `define D 2'b11  
5  
6 // Using constants  
7 wire [A:0] wire_a = `A; // Notice the backtick
```

```

8  wire [B:0] wire_b = `B;
9  wire [C:0] wire_c = `C;
10 wire [D:0] wire_d = `D;

```

## Wires

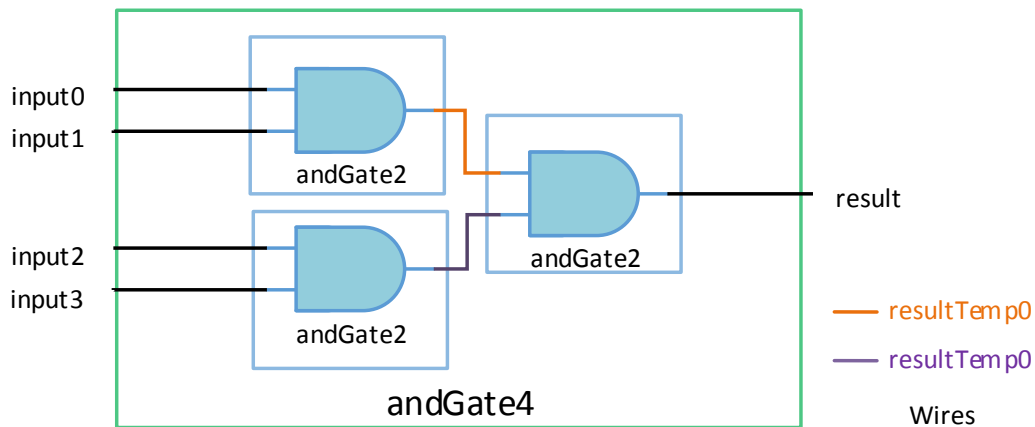


Figure 2: Gate level representation of code in Listing 8.

Wires are something very important in verilog, use of wires in Verilog is for what wires are used in real life ... to connect two things electrically! Wires will be used extensively in future assignments to connect two modules, registers and even wires together. This concept is explained using Listing 7 where wires are used to connect output of two 2-input AND gates to inputs of single 2-input AND gates. Gate level diagram of which is shown in Fig. 2.

Listing 8: Use of wires to connect output of one module to input of another

```

1  // andGate4 is a four input AND gate that uses 3 2-input AND
2  // gates to produce its result. resultTemp0 and resultTemp1 wires
3  // are used to connect output of two andGate2 to a another andGate2
4  // This module uses andGate2 module from previous listing.
5  module andGate4(input0, input1, input2, input3, result);
6      // Declare input and output
7      input input0, input1, input2, input3;
8      output result;
9
10     // Declare wire for connecting gates
11     wire resultTemp0;
12     wire resultTemp1;
13
14     // Declare instances of 2-input AND gate
15     andGate2(input0, input1, resultTemp0);
16     andGate2(input2, input3, resultTemp1);
17
18     andGate2(resultTemp0, resultTemp1, result);
19 endmodule

```

## Vectors

Verilog support declaration of wire to represent group of wires (or registers which will be explained later). Vectors are declared by specifying their type, range and then their name:

<type> <range> <name>;

Example declaration of 6 bit wide vector of type wire:

```
wire [5:0] new_wire; // Both the range specifier digits are inclusive
```

Here new\_wire[5] is MSB while new\_wire[0] is LSB.

## Operators

Verilog supports wide range of operators to represent mathematical operations, these are high level representation of what would be converted to gate level implementation later by and HDL compiler.

Table 1: List of common operators used in Verilog

Operator	Description	Functional Group
[]	bit select or part select	
()	parenthesis	
!	negation	logical
~	negation	bitwise
&	reduction AND	reduction
	reduction OR	reduction
~&	reduction NAND	reduction
~	reduction NOR	reduction
^	reduction XOR	reduction
~^ or ^~	reduction XNOR	reduction
+	Unary Plus (plus sign)	airthmetic
-	Unary minus (minus sign)	
*	multiply	airthmetic
/	divide	
%	modulus	
+	Binary Plus	airthmetic
-	Binary minus	
<<	shift left	shift
>>	shift right	
>	greater than	relational
>=	greater than or equal to	
<	less than	
<=	less than or equal to	
==	case equality	equality
!=	case inequality	
&	bitwise AND	bitwise
	bitwise OR	
~	bitwise XOR	

## Airthmetic Operators

Verilog allows use of various airthmetic operators to perform calculations on vectors (wires & reg). Following example shows its usage:

Listing 9: Functioning of airthmetic operator

```
1 module airthmeticOperators
2 (
3     output o1, o2, o3, o4, o5, o6, o7, o8
4 );
5
6 assign o1 = 1 + 2; // = 3
```

```

7  assign o2 = 1 - 2; // = -1
8  assign o3 = 10 * 5; // = 50
9  assign o4 = 10 / 5; // = 2
10
11  assign o5 = 5 / 10; // = 0 <--- NOTE
12
13  assign o6 = 10 % 3; // = 1
14  assign o7 = +7;      // = 7
15  assign o8 = -7;      // = -7
16 endmodule // airthmeticOperators

```

## Reduction Operators

Reduction operators in Verilog reduces a multibit number into a single bit by repeatedly performing a specified operation. Following example explains its usage:

Listing 10: Functioning of reduction operator

```

1  module reductionOperators
2  (
3      input [15:0] i,
4      output      r1, r2, r3, r4, r5, r6
5  );
6
7      // 16 bits of i are ANDed together and set as the value
8      // of r1
9      assign r1 = &i; // r1 = i[0] & i[1] & i[2] ... & i[15]
10     // Other reduction operator follows same logic
11     assign r2 = ~&i; // r2 = i[0] ~& i[1] ~& i[2] ... ~& i[15]
12     assign r3 = |i; // r3 = i[0] | i[1] | i[2] ... | i[15]
13     assign r4 = ~|i; // r4 = i[0] ~| i[1] ~| i[2] ... ~| i[15]
14     assign r5 = ^i; // r5 = i[0] ^ i[1] ^ i[2] ... ^ i[15]
15     assign r6 = ~^i; // r6 = i[0] ~^ i[1] ~^ i[2] ... ~^ i[15]
16 endmodule // reductionOperators

```

## Relational Operators

Relational operators in verilog are used to compare two values, usage of all four type of relational operators supported by Verilog are given in Listing 11.

Listing 11: Functioning of relational operator

```

1  module relationalOperators
2  (
3      output o1, o2, o3, o4
4  );
5
6      assign o1 = 1<2;          // = 1'b1
7      assign o2 = 1>2;          // = 1'b0
8      assign o2 = 1>=1;         // = 1'b1
9  endmodule // relationalOperators

```

## Logical Operators

Logical operators are used in conjunction with relational and equality to perform multiple comparisons within a single expression. Example usage of logical operators are provided in 12.

Listing 12: Functioning of logical operator

```

1  module logicalOperators
2  (
3      output o1, o2
4  );
5

```

```

6   assign o2 = (2'b10 & 1'b01) && (2'b00 & 1'b11);           // = 1'b0
7   assign o1 = ((1'b1 == 1'b0) || ((2'b11 && 2'b01) == 2'b01)); // = 1'b1
8 endmodule // logicalOperators

```

## Bitwise and Shift Operators

Verilog Bitwise and Shift operators works in the same way as they work in Java, except that in Verilog only left shift (<<) and right shift (>>) are supported.

## Problems

### Problem 1:

Design a 16 input AND gate using Verilog reduction operator where input to the module will be a vector of length 16 and will have a single output.

### Problem 2:

Design a 4 input AND gate using Verilog reduction operator where input to the module will be a vector of length 4 and will have a single output.

### Problem 3:

Design a 4 input AND gate using Verilog reduction operator where input to the module will be a vector of length 4 and will have a single output.

### Problem 4:

Design a 4 input AND gate using Verilog reduction operator where input to the module will be a vector of length 4 and will have a single output.

## References

- [http://cva.stanford.edu/people/davidbbs/classes/ee108a/winter0607%20labs/ee108a\\_nham\\_intro\\_to\\_verilog.pdf](http://cva.stanford.edu/people/davidbbs/classes/ee108a/winter0607%20labs/ee108a_nham_intro_to_verilog.pdf)
- Verilog HDL Samir Palnitkar
- [https://www.utdallas.edu/~akshay.sridharan/index\\_files/Page5212.htm](https://www.utdallas.edu/~akshay.sridharan/index_files/Page5212.htm)