STM32F3 Technical Training

For reference only

Refer to the latest documents for details

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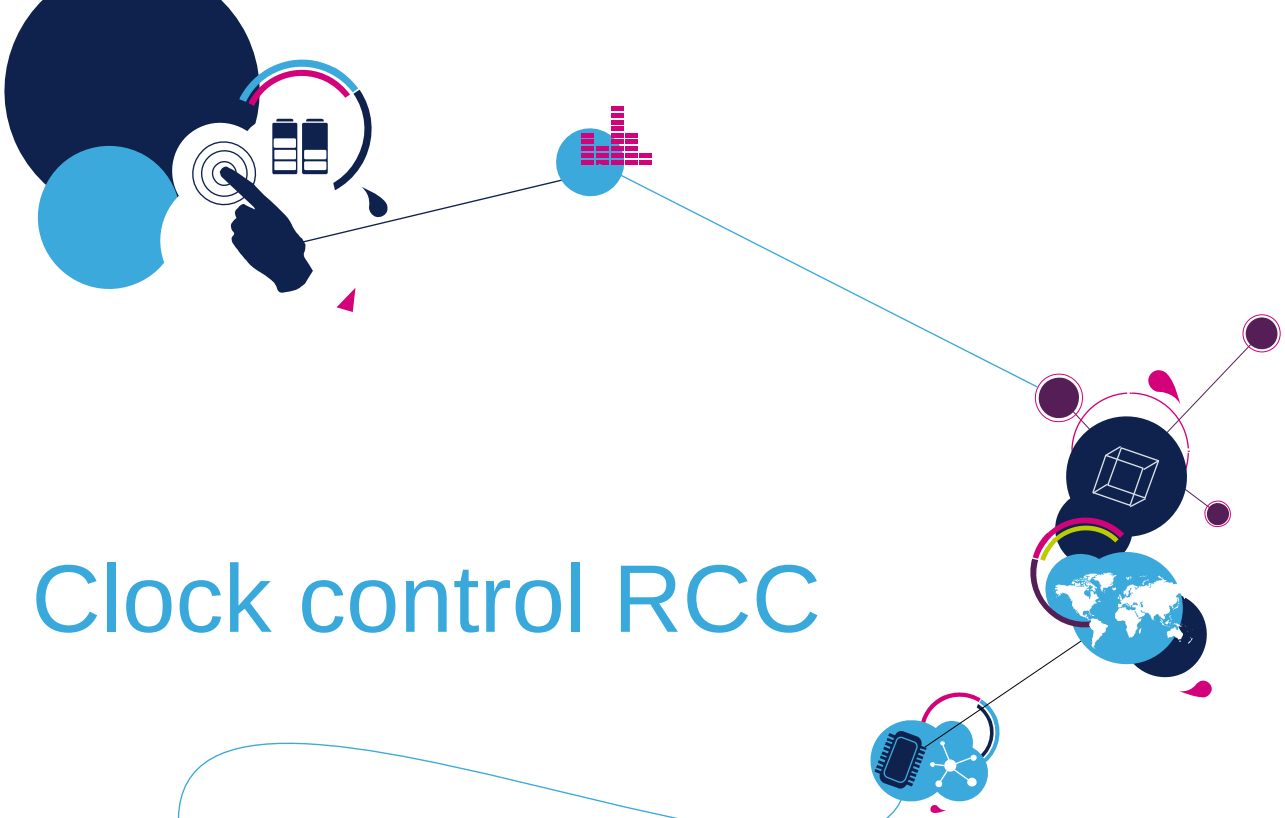

Reset and Clock control RCC

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RCC introduction

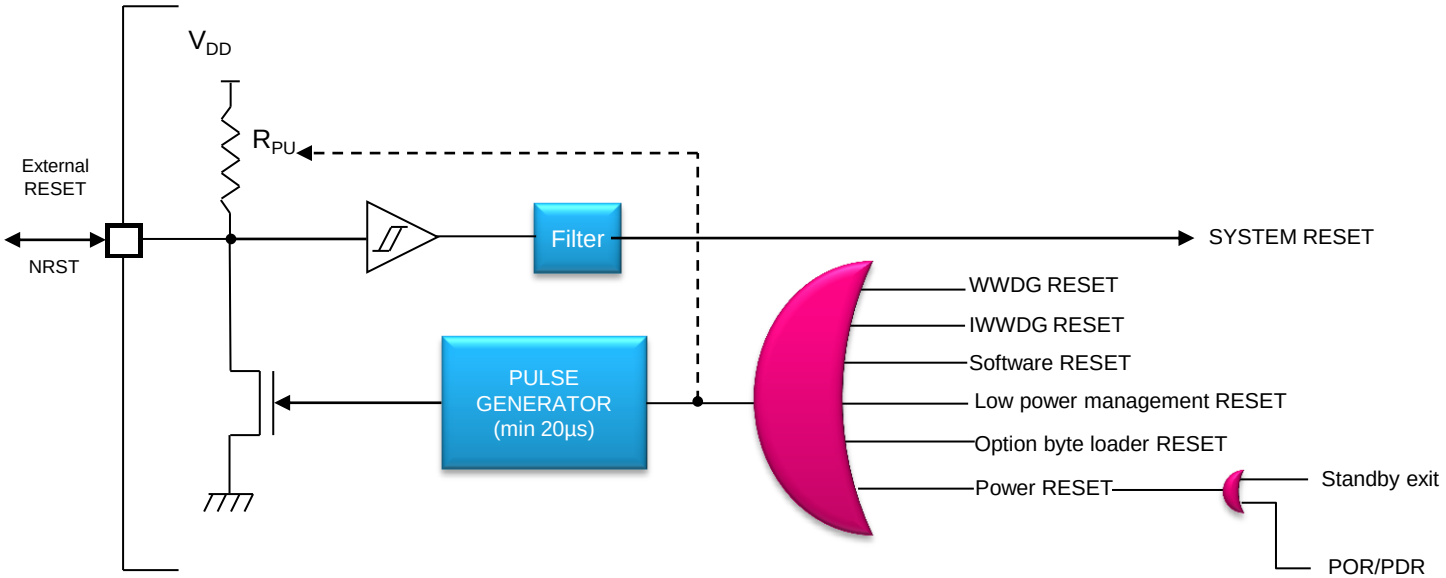
- Reset:
  - Initialize the device
  - Wakeup device
  - Safety functions (watchdog)
- Clocks:
  - Select appropriate clock source:
    - Internal
    - External
  - Select appropriate speed:
    - High speed
    - Low speed
    - Speed regulation
  - Modify clock parameters for:
    - Core
    - Peripherals
  - Security functions:
    - In case of clock source malfunction

Reset sources

- System RESET
  - Resets all registers except some RCC registers and Backup domain
  - Sources:
    - Low level on the NRST pin (External Reset)
    - WWDG & IWWDG end of count condition
    - A software reset (through NVIC)
    - Low power management reset
    - Option byte loader reset (FORCE_OBL bit)
- Power RESET
  - Resets all registers except the Backup domain
  - Sources:
    - Power On/Power down Reset (POR/PDR)
    - Exit from STANDBY
- Backup domain RESET
  - Resets in the Backup domain: RTC registers + Backup Registers + RCC_BDCR register
  - Sources:
    - BDRST bit in RCC_BDCR register
    - POWER Reset

Reset block diagram

- Reset sources in STM32F3 family and their relation to RESET pin:



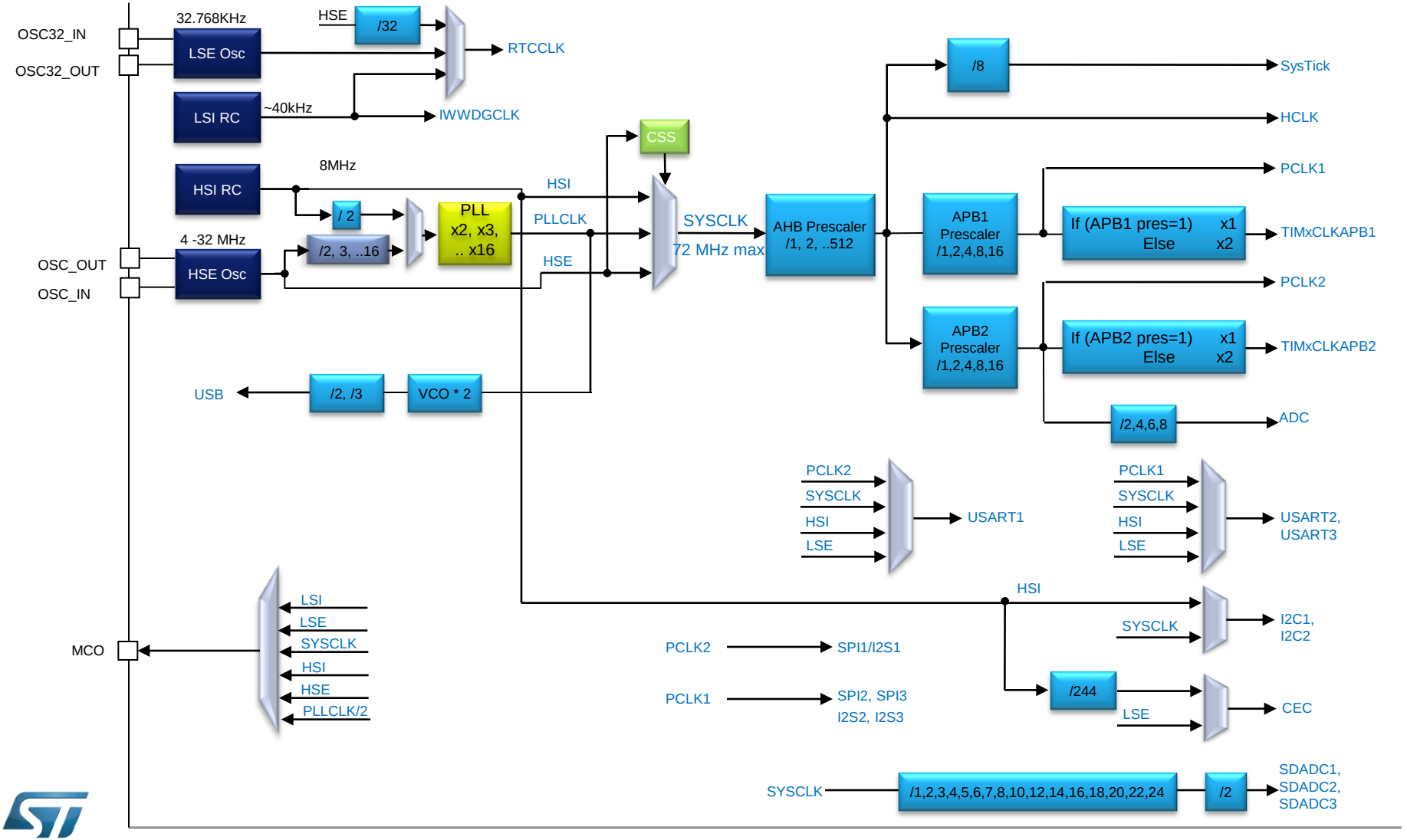
Clock features (1/2)

- System Clock (SYSCLK) sources:
  - HSE (High Speed External oscillator or crystal)
    - 4MHz to 32MHz,
    - can be bypassed by user clock
  - HSI (High Speed Internal RC):
    - factory trimmed internal RC oscillator 8MHz +/- 1%
  - PLL x2, x3, .. x16
    - From HSE or HSI/2
    - 16MHz – 72MHz output
- Additional clock sources:
  - LSI (Low Speed Internal RC):
    - ~40kHz internal RC
  - LSE (Low Speed External oscillator):
    - 32.768kHz
    - can be bypassed by user clock
    - Configurable driving strength (power/robustness compromise)

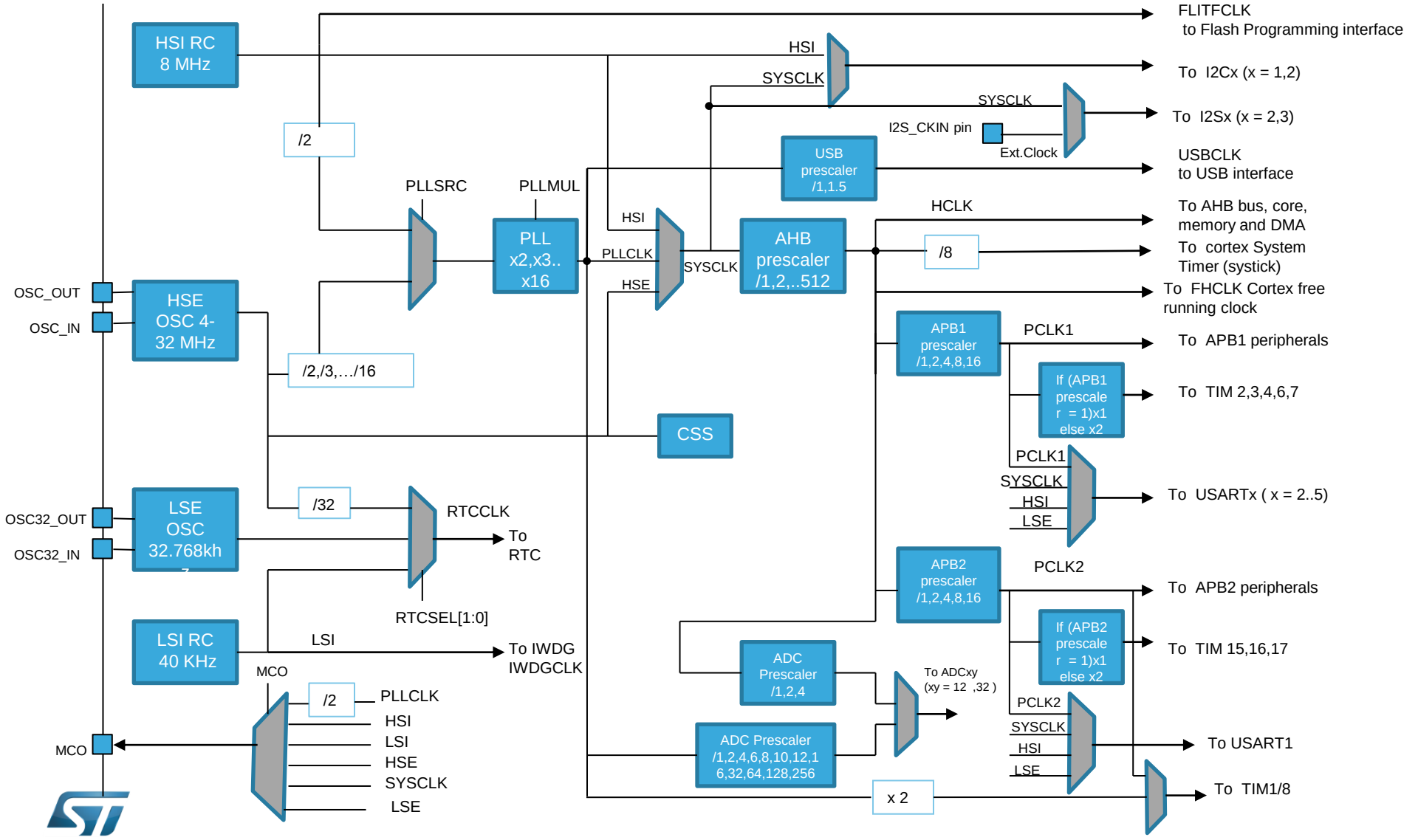
Clock features (2/2)

- Clock-out capability on the MCO:
  - LSI, LSE, SYSCLK, HSI, HSE, PLL/2
- Clock Security System (CSS) to switch to backup clock:
  - In case of HSE clock failure
  - Enabled by SW w/ interrupt capability linked to NMI
  - Could generate BREAK for Timers
- RTC Clock sources:
  - LSE, LSI and HSE/32
- USART, I2C & CEC have multiple possible clock sources:
  - Possibility to wakeup device if there is no system clock:
    - For USART: HSI, LSE
    - For I2C: HSI
    - For HDMI-CEC: LSE, HSI

Clock scheme STM32F37x



Clock scheme STM32F30x



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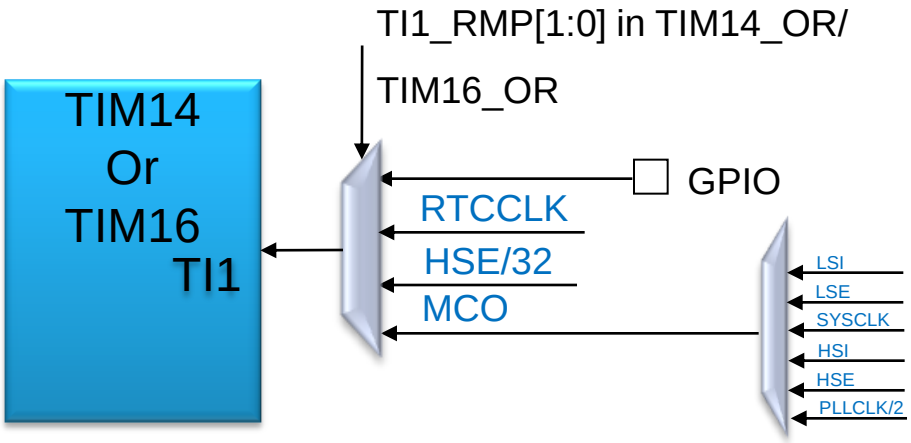
HSI/LSI/ext. clock measurement

- TIM14 (in F37x) and TIM16 (in F30x) input capture can be triggered by:
  - GPIO pin
  - RTCCLK
  - HSE/32
  - MCO output



- Purposes:
  - **Measure HSI frequency** using the precise LSE clock. HSI is used as system clock. Knowing the (more precise) LSE frequency we can determine the HSI frequency.
  - **Measure the LSI frequency** using HSE or HSI. To fine tune IWWDG and/or RTC timing (if LSI used as RTC clock).
  - Have rough indication of the **frequency of external crystal** – by comparing HSI and HSE/32

Quiz

- What is the maximum AHB and APB1 and APB2 clock frequencies ?
- What is the purpose of connecting LSE clock to TIM14/16 CH1 input capture and how it could be done?
- What is the purpose of the CSS?

Thank you !