Here's part of the case for a precision voltage reference for our emonSTM project.

First, readings when connected to the onboard 3.3V linear regulator.

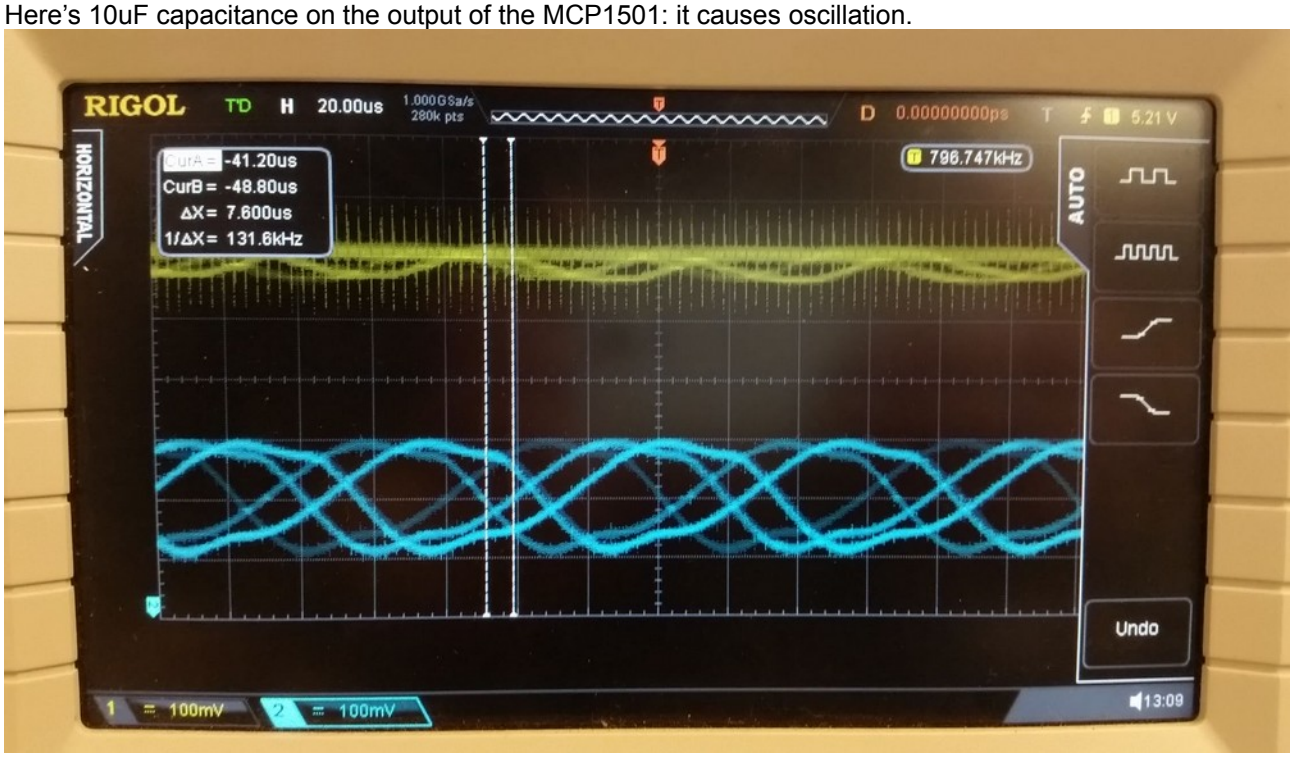
```
PC:0
V0:241.91,I0:0.078,RP0:-2.1,AP0:18.8,PF0:-0.110,C0:16156,millis:15779
V1:241.91,I1:0.109,RP1:-3.8,AP1:26.5,PF1:-0.144,C1:16156,millis:15781
V2:241.91,I2:0.102,RP2:-4.2,AP2:24.8,PF2:-0.170,C2:16156,millis:15783
V3:241.91,I3:0.105,RP3:-4.0,AP3:25.5,PF3:-0.158,C3:16156,millis:15785
V4:241.91,I4:0.070,RP4:-2.6,AP4:17.0,PF4:-0.154,C4:16156,millis:15787
V5:241.91,I5:0.090,RP5:-3.4,AP5:21.7,PF5:-0.157,C5:16156,millis:15790
V6:241.91,I6:0.105,RP6:-4.5,AP6:25.5,PF6:-0.178,C6:16155,millis:15792
V7:241.92,I7:0.076,RP7:-2.5,AP7:18.3,PF7:-0.137,C7:16155,millis:15794
V8:241.92,I8:0.107,RP8:-4.0,AP8:25.9,PF8:-0.156,C8:16155,millis:15796
PC:0
```

And then the same exact setup, but this time VREF on the stm32 is connected to the output of an MCP1501, a budget 3.3V 0.1% reference.

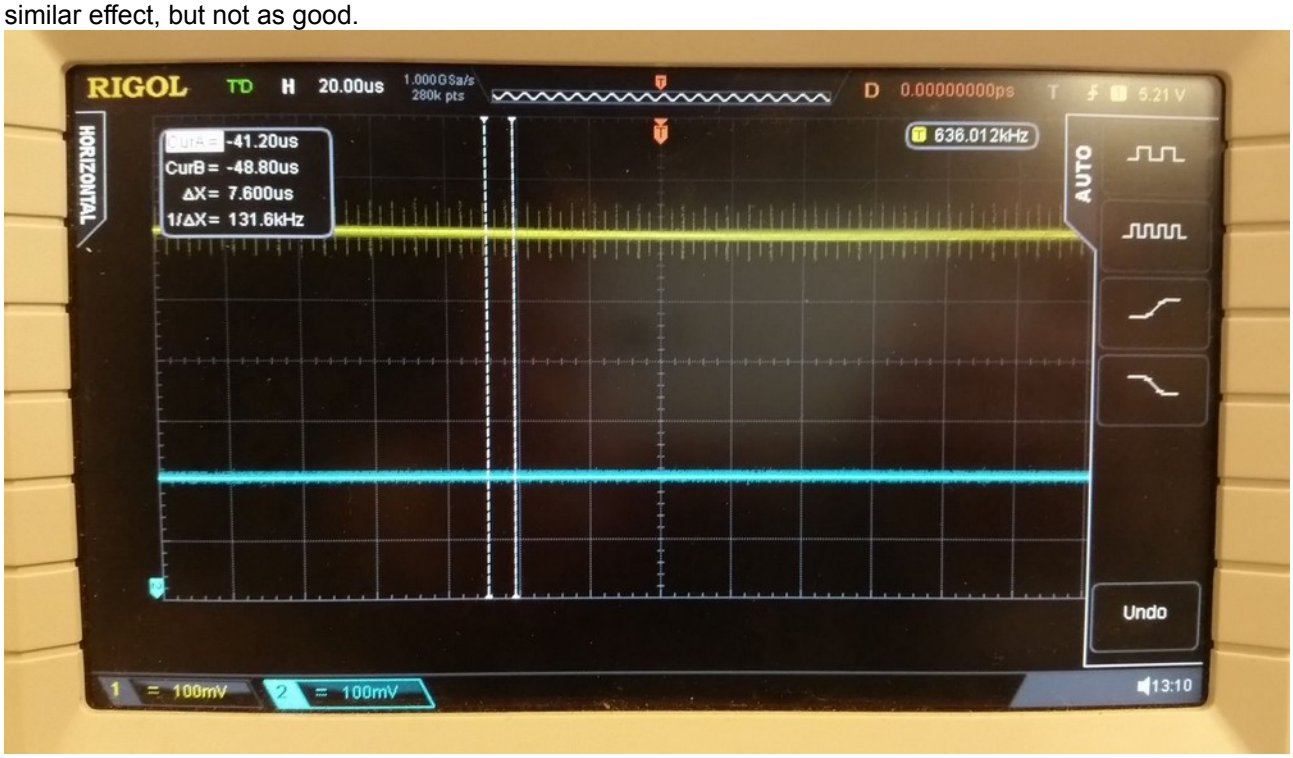
```
PC:0
V0:252.98,I0:0.044,RP0:-0.0,AP0:11.0,PF0:-0.002,C0:16165,millis:31486
V1:252.95,I1:0.018,RP1:-0.0,AP1:4.6,PF1:-0.006,C1:16165,millis:31488
V2:252.99,I2:0.023,RP2:0.0,AP2:5.9,PF2:0.003,C2:16165,millis:31490
V3:252.97,I3:0.012,RP3:0.0,AP3:3.0,PF3:0.007,C3:16165,millis:31492
V4:252.97,I4:0.025,RP4:-0.0,AP4:6.3,PF4:-0.005,C4:16165,millis:31494
V5:252.95,I5:0.022,RP5:-0.0,AP5:5.6,PF5:-0.007,C5:16165,millis:31496
V6:252.94,I6:0.021,RP6:-0.0,AP6:5.4,PF6:-0.009,C6:16164,millis:31498
V7:252.96,I7:0.008,RP7:0.0,AP7:1.9,PF7:0.004,C7:16165,millis:31500
V8:252.94,I8:0.026,RP8:-0.0,AP8:6.6,PF8:-0.007,C8:16165,millis:31502
PC:0
```

Here's 5V input coming into the MCP1501, and it's 3.3V output, noise included as it's coming from the multi-gang USB sockets in our lab. The noise is much less on the output. No capacitors on either input or output.

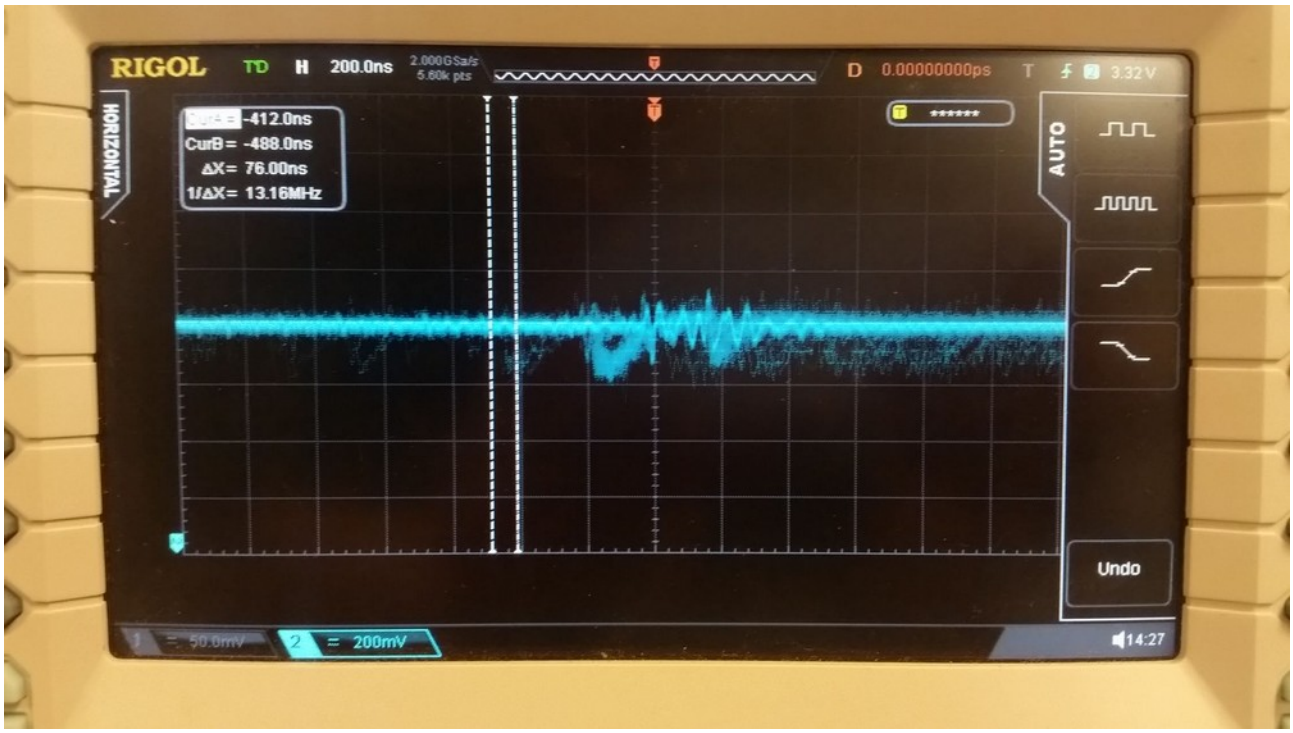
Here’s 10uF capacitance on the output of the MCP1501: it causes oscillation.



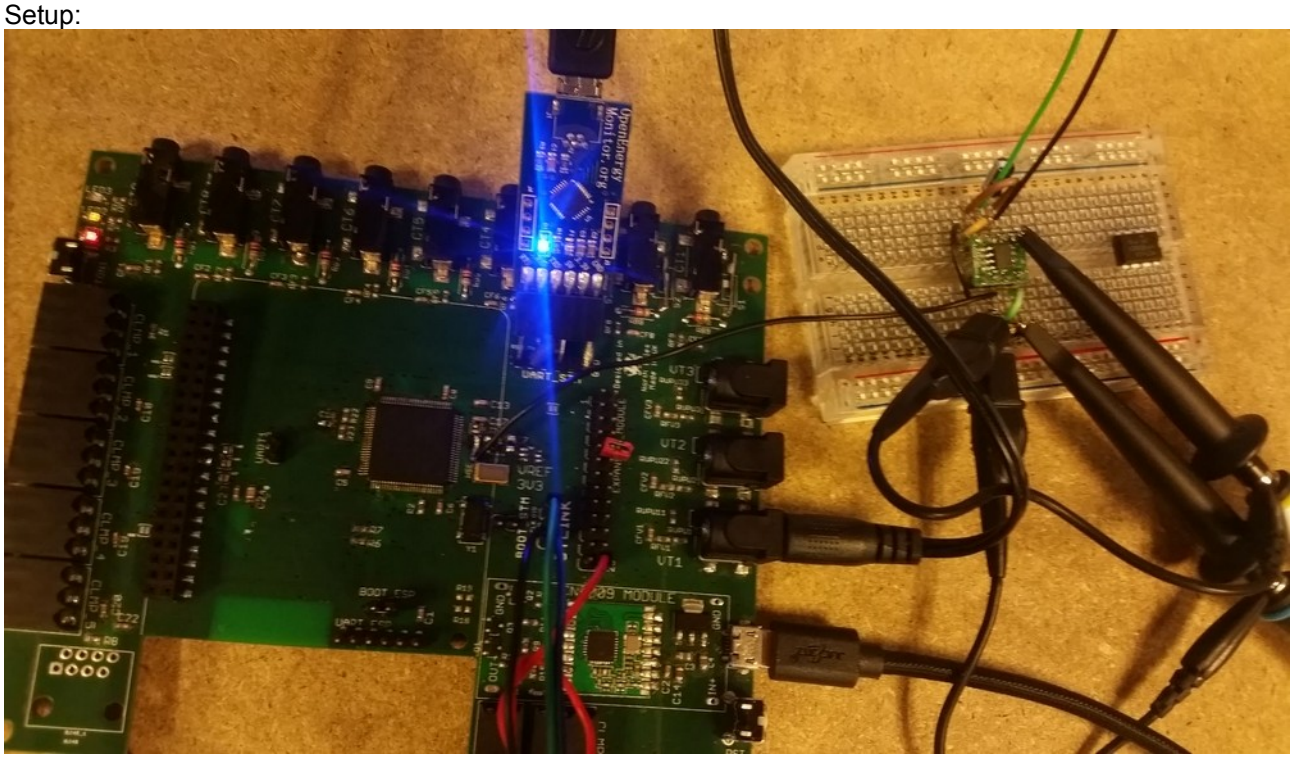
Here’s the 10uF electrolytic on the input of the MCP1501, this looks better. A 100nF ceramic cap had a similar effect, but not as good.



Here's the ADCs running causing a dip in the VREF, connected to MCP1501 reference, there seems to be ample time for the reference to recover from each ADC sampling. The picture isn't very clear, but I observed there was enough time for recovery between samples at our existing sampling speed, which is around 5kHz per CT channel. I could estimate the MCP1501 could handle a sampling speed 10 times higher.



Setup:



Notable Limitations – power supply noise, long wires.

Error from BIAS: Right now, the BIAS is created from the 3.3V linear regulator supply divided down by a 10k/10k divider, with no filtering capacitor. This will be susceptible to noise and irregular (spiky) loading of the regulator.
It might be worth connecting the output of the MCP1501 to the 10k/10k divider for the op-amp BIAS.

The unknowns in this scenario is the ADC VREF sampling dips causing a knock on error to the op-amp and BIAS line. If connected, the trace from one side of the chip to the other would also pick up noise, and add capacitance.
A capacitor on the op-amp's input, between the two 10k resistors, could be considered to mitigate noise, although could risk oscillation of the BIAS line.

Future tests:
. Look at the BIAS op-amp input and check for noise coming from 3.3V linear regulator.
. Add a capacitor to the BIAS op-amp input while connected to the 3.3V linear regulator, observe effects on the BIAS output. Values 100nF and 10uF can be tested with.
. Connect MCP1501 output to the voltage divider for the BIAS input. In this scenario, consider effects of the above capacitors on the BIAS input.