1. Description

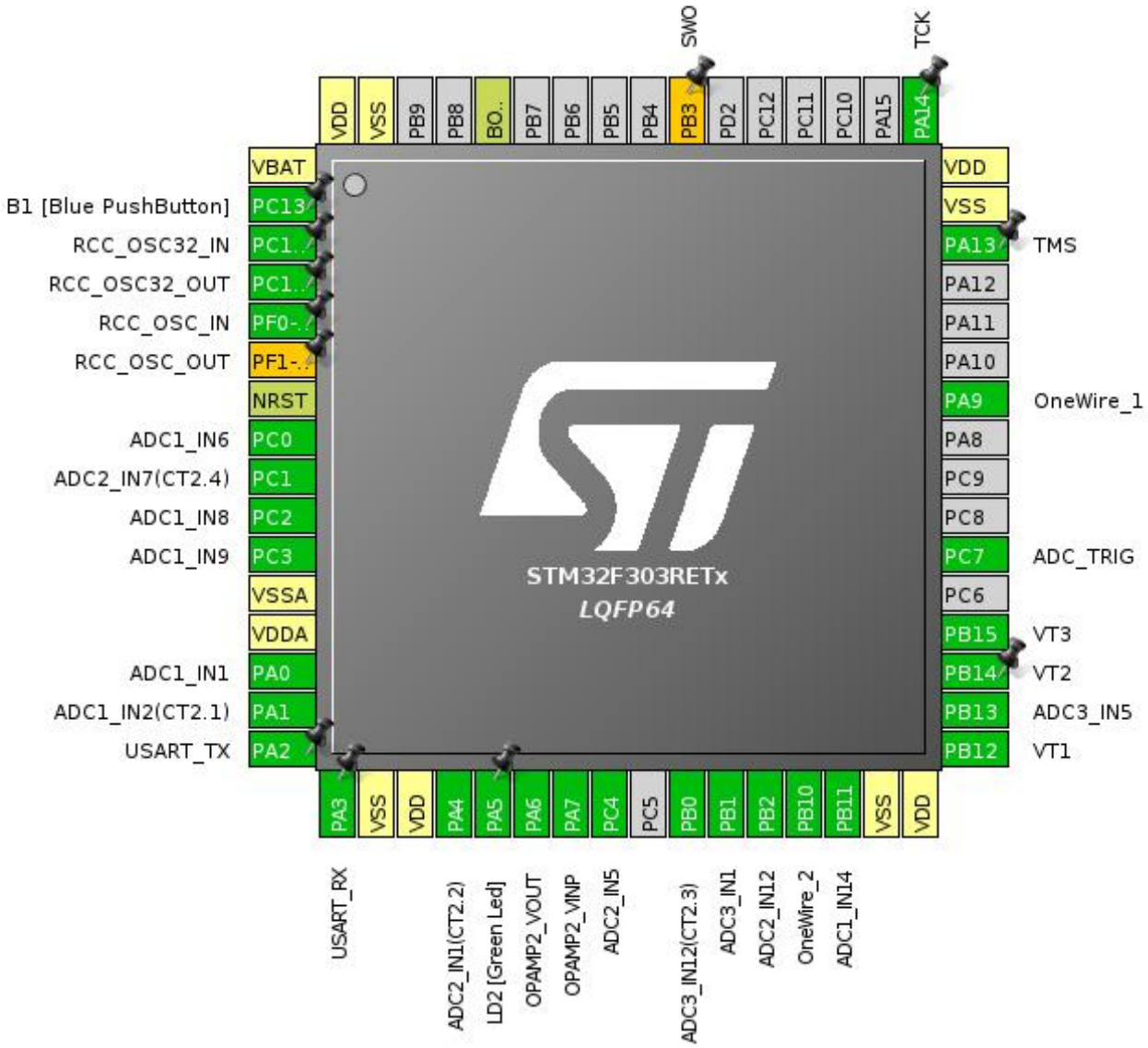
1.1. Project

Project Name	emonTxshield
Board Name	NUCLEO-F303RE
Generated with:	STM32CubeMX 4.25.1
Date	06/02/2018

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

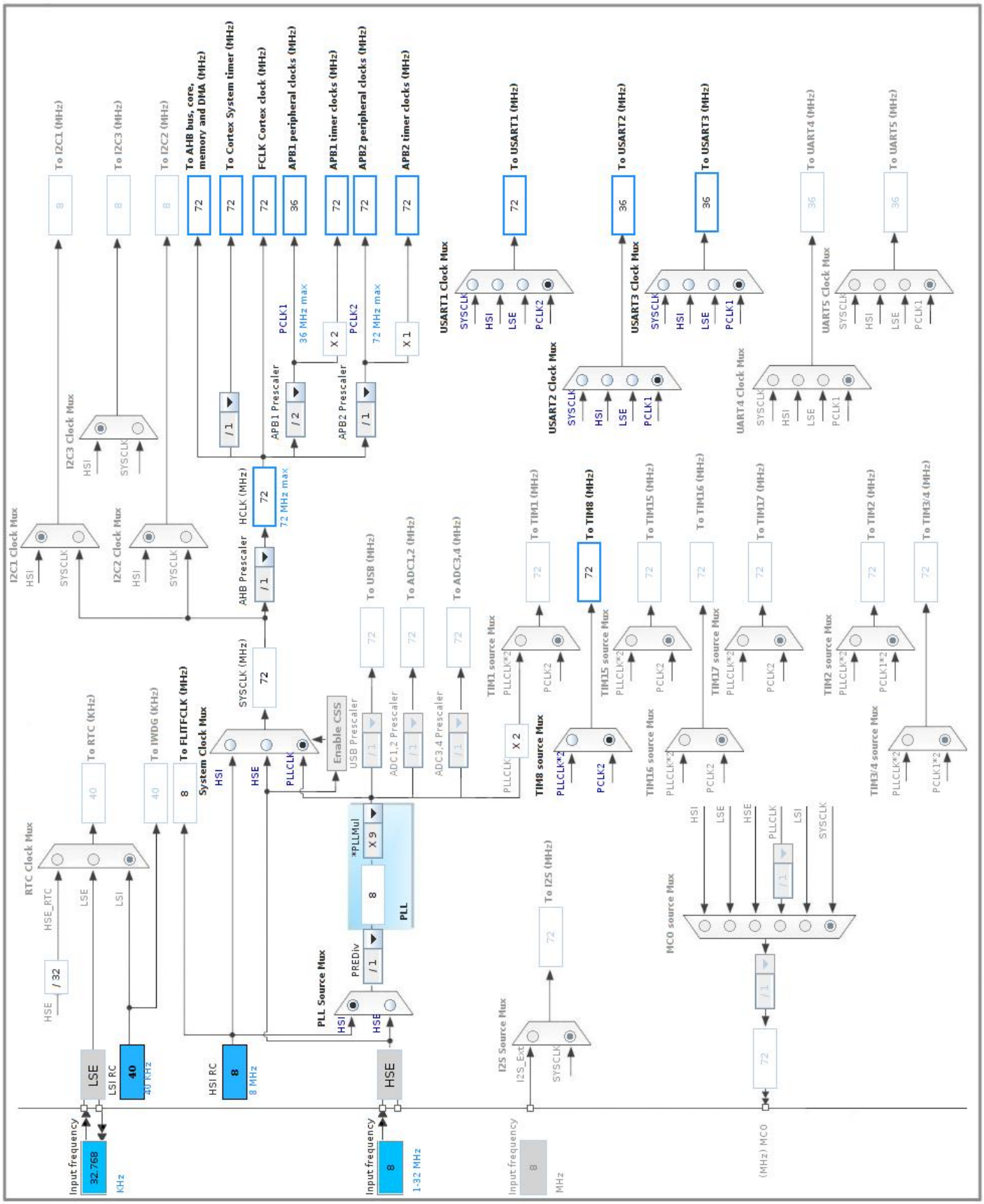
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN6	
9	PC1	I/O	ADC2_IN7	ADC2_IN7(CT2.4)
10	PC2	I/O	ADC1_IN8	
11	PC3	I/O	ADC1_IN9	
12	VSSA	Power		
13	VDDA	Power		
14	PA0	I/O	ADC1_IN1	
15	PA1	I/O	ADC1_IN2	ADC1_IN2(CT2.1)
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC2_IN1	ADC2_IN1(CT2.2)
21	PA5 **	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	OPAMP2_VOUT	
23	PA7	I/O	OPAMP2_VINP	
24	PC4	I/O	ADC2_IN5	
26	PB0	I/O	ADC3_IN12	ADC3_IN12(CT2.3)
27	PB1	I/O	ADC3_IN1	
28	PB2	I/O	ADC2_IN12	
29	PB10	I/O	USART3_TX	OneWire_2
30	PB11	I/O	ADC1_IN14	
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	ADC4_IN3	VT1
34	PB13	I/O	ADC3_IN5	
35	PB14	I/O	ADC4_IN4	VT2
36	PB15	I/O	ADC4_IN5	VT3
38	PC7	I/O	TIM8_CH2	ADC_TRIG

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PA9	I/O	USART1_TX	OneWire_1
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	SYS_JTDO-TRACESWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended
IN2: IN2 Single-ended
IN6: IN6 Single-ended
IN8: IN8 Single-ended
mode: IN9
mode: IN14
mode: Temperature Sensor Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**7 ***
External Trigger Conversion Source	**Timer 8 Trigger Out 2 event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***

Channel	**Channel 2 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 6 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 8 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 9 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 14 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	**Disable ***

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN1: IN1 Single-ended
IN5: IN5 Single-ended
IN7: IN7 Single-ended
mode: IN12
mode: VOPAMP2 Channel

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**7 ***
External Trigger Conversion Source	**Timer 8 Trigger Out 2 event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	**Channel Vopamp2 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset

Offset	0
Rank	**3 ***
Channel	**Channel Vopamp2 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 5 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 7 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 12 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel 12 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	**Disable ***

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. ADC3

IN1: IN1 Single-ended

mode: IN5

mode: IN12

mode: Vrefint Channel

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**7 ***
External Trigger Conversion Source	**Timer 8 Trigger Out 2 event ***
External Trigger Conversion Edge	**Trigger detection on the falling edge ***
Rank	1
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 12 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

Rank	**3 ***
Channel	**Channel 5 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel Vrefint ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel Vrefint ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel Vrefint ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel Vrefint ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.4. ADC4

IN3: IN3 Single-ended
IN4: IN4 Single-ended
mode: IN5

5.4.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**7 ***
External Trigger Conversion Source	**Timer 8 Trigger Out 2 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 3
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 5 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

Rank	**4 ***
Channel	Channel 3
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 4 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 5 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	Channel 3
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.5. OPAMP2

Mode: Follower

5.5.1. Parameter Settings:

Basic Parameters:

User Trimming	**Enable ***

Self Calibration	**Enable ***

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source
Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.7. SYS

Debug: Serial Wire
Timebase Source: SysTick

5.8. TIM8

Channel2: PWM Generation CH2
mode: One Pulse Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**71 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	**Output Compare (OC2REF) ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.9. USART1

Mode: Single Wire (Half-Duplex)

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.10. USART2

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.11. USART3

Mode: Single Wire (Half-Duplex)

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN6	Analog mode	No pull up pull down	n/a	
	PC2	ADC1_IN8	Analog mode	No pull up pull down	n/a	
	PC3	ADC1_IN9	Analog mode	No pull up pull down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	ADC1_IN2(CT2.1)
	PB11	ADC1_IN14	Analog mode	No pull up pull down	n/a	
ADC2	PC1	ADC2_IN7	Analog mode	No pull up pull down	n/a	ADC2_IN7(CT2.4)
	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	ADC2_IN1(CT2.2)
	PC4	ADC2_IN5	Analog mode	No pull up pull down	n/a	
	PB2	ADC2_IN12	Analog mode	No pull up pull down	n/a	
ADC3	PB0	ADC3_IN12	Analog mode	No pull up pull down	n/a	ADC3_IN12(CT2.3)
	PB1	ADC3_IN1	Analog mode	No pull up pull down	n/a	
	PB13	ADC3_IN5	Analog mode	No pull up pull down	n/a	
ADC4	PB12	ADC4_IN3	Analog mode	No pull up pull down	n/a	VT1
	PB14	ADC4_IN4	Analog mode	No pull up pull down	n/a	VT2
	PB15	ADC4_IN5	Analog mode	No pull up pull down	n/a	VT3
OPAMP2	PA6	OPAMP2_VOUT	Analog mode	No pull up pull down	n/a	
	PA7	OPAMP2_VINP	Analog mode	No pull up pull down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM8	PC7	TIM8_CH2	Alternate Function Push Pull	No pull up pull down	Low	ADC_TRIG
USART1	PA9	USART1_TX	Alternate Function Open Drain	No pull up pull down	**High ***	OneWire_1
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull up pull down	Low	USART_RX
USART3	PB10	USART3_TX	Alternate Function Open Drain	No pull up pull down	**High ***	OneWire_2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Single Mapped Signals	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull up pull down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull up pull down	Low	LD2 [Green Led]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**High ***
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low
ADC3	DMA2_Channel5	Peripheral To Memory	**High ***
ADC4	DMA2_Channel2	Peripheral To Memory	**High ***
ADC2	DMA2_Channel1	Peripheral To Memory	**High ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC4: DMA2_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	1	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	true	0	0
DMA2 channel1 global interrupt	true	1	0
DMA2 channel2 global interrupt	true	1	0
DMA2 channel5 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
EXTI line[15:10] interrupts	unused		
TIM8 break global interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupt	unused		
TIM8 capture compare interrupt	unused		
ADC3 global interrupt	unused		
ADC4 interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303RETx
Datasheet	026415_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Pack Report

9. Software Project

9.1. Project Settings

Name	Value
Project Name	emonTxshield
Project Folder	/home/dbath/STM32CubeMX/Projects/emonTxshield
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.1

9.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes