MC12G MC12T

VHF, dual-channel digital capacitive sensing chip

1. Overview

MC12G and MC12T are highly integrated dual-channel capacitive sensing chips. The chip measures the single-ended capacitance to ground and is directly connected to the measured capacitance plate. Connected, through very high frequency resonance excitation and solution to measure the micro capacitance variety. The excitation frequency is configurable in the range of 10~100MHz, and its frequency measurement output is a 16-bit digital signal, and the corresponding maximum resolution of capacitive sensing is 0.5ff. The chip adopts a fully digital design, and its functional configuration and data reading and writing support I2C communication rates up to 1MHz; it has a built-in low-noise power management module LDO, which can adapt to a wide input voltage range. In addition, the chip also integrates a temperature sensing circuit that can be used to perform temperature compensation and other temperature sensing scenarios.

Capacitive sensing realizes detection of different objects through cooperation with detection electrodes. Dielectric detection of materials is a low power consumption, low cost and high resolution non-contact detection technology. Compared with the traditional RC oscillation touch capacitor structure, MC12G and MC12T adopt the very high frequency LC resonance method, which makes the electric field intensity penetrate better. chip frequency meter. The calculation is fully digitally output through the internal digital signal processing unit, and a variety of The working mode can be flexibly configured. MC12T has a simplified SOP8 pinout for low-cost dual-channel capacitance detection. MC12G is a small QFN16 package that provides more comprehensive internal chip control.

Compared with similar products at home and abroad, MC12G and MC12T have wider capacitive excitation frequency, longer non-contact measurement performance, and wider working voltage range, more flexible reference frequency and working mode configuration set. The chip has both a temperature sensing signal for temperature compensation, independent. The dual-channel measurement circuit can compensate for each other's reference and can also be configured to automatically alarm logic. Small-sized, low-cost chips can be widely used in smart home appliance liquid level, proximity, touch and other scenarios can also be used for industrial special inspections such as automotive oil, water immersion sensing, food testing, soil moisture content, etc. test scenario.

2. Characteristics

Capacitance measurement range: 0~150pF
Temperature range: -55℃~+125℃
Frequency range: 10MHz~100MHz
Effective resolution: up to 15bit
Supply voltage range: 2.0V~5.5V
Conversion time: 1~100ms (configurable)
Measure peak current: 1.3~8.3mA (configurable)
Sleep mode current: 50nA
Shutdown mode current: 40nA

3. Application

Smart home appliance liquid level
Industrial water tank level
Car oil level
Food moisture content analysis
Soil moisture content analysis
Proximity detection
Touch sensing

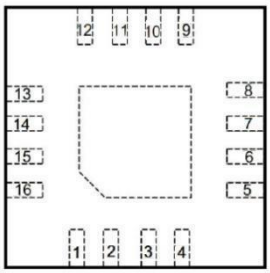
Product Information

Model	Encapsulation	Size
MC12G	QFN16	3.0*3.0*0.75mm
MC12T	SOP8	4.9*3.9*1.6mm

Contents

4. Package pin description

4.1. MC12G package pin diagram (QFN16)



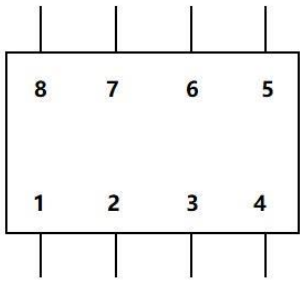
front perspective view

Pin Number	Pin Name	Type	Description
1	SCL	I	i2c clock line
2	SDA	I/O	i2c data line
3	CLKIN	I	external count clock (GND needs to be connected when selecting the internal clock)
4	ADDR	I	i2c address line
5	INTB	O	Interrupt signal output, active low level
6	SD	I	Stop mode enable signal
7	VDD	P	Power Supply
8	GND	G	Ground
9	C0A	A	Channel 0 capacitor input terminal
10	C0B	A	Channel 0 capacitor input terminal
11	C1A	A	Channel 1 capacitor input terminal
12	C1B	A	Channel 1 capacitor input terminal
13	VC	A	Internal reference voltage
14	VT	A	Negative temperature coefficient voltage
15	NC	-	Not connected
16	NC	-	Not connected

Note 1: I represents input, O represents output, P represents power supply, G represents ground, and A represents analog signal.

Note 2: During circuit design, the thermal pad can be suspended or grounded.

4.2. MC12T package pin diagram (SOP8)



top view

Pin Number	Pin Name	Type	Description
1	VT	A	negative temperature coefficient voltage
2	SCL	I	I2C clock line
3	SDA	I/O	I2C data line
4	VDD	P	power supply
5	GND	G	land
6	C0	A	Channel 0 capacitor input terminal
7	C1	A	Channel 1 capacitor input terminal
8	VC	A	Internal reference voltage

Note: I represents input, O represents output, P represents power supply, G represents ground, and A represents analog signal.

5. Electrical specifications

5.1. Absolute Maximum Ratings

	project	minimum value	maximum value	unit
VDD	Supply voltage range	- 0.3	6.0	V
Vi	Pin voltage	- 0.3	VDD	V
T_J	Junction temperature	- 55	125	℃
T_{stg}	storage temperature	- 55	125	℃

Note: The above are limit parameters. This specification does not apply to the functional operation of the device in environments beyond these limit conditions. Long-term exposure to this extreme environment can affect device reliability.

5.2. ESD Level

	project	numerical value	unit
	Human-body model(HBM)	±8000	V
V_{ESD} Electrostatic Discharge	Charged-device model(CDM)	±750	V

5.3. Electrical characteristics

Unless otherwise specified, the data conditions in the table are T=25℃, VDD=5V.

	Parameter	Test Conditions	Minimum Value	Typical value	Maximum Value	Unit
Power consumption						
VDD	voltage	T = -55℃ to 125℃	2.0		5.5	V
I_{DD}	Measure peak current(1)		1.3	3.7	8.3	mA
I_{DDCST}	Continuous conversion standby current(2)			75		uA
I_{DDSL}	Sleep mode current(3)			0.05		uA
I_{SD}	Stop mode current(3)			0.04		uA
Capacitive Sensing						
$C_{SENSORMAX}$	Maximum measured capacitance	L=150nH, f_{SENSOR}=30MHz		150		pF
$C_{C0A/C1A}$	Pin parasitic capacitance			2		pF
ENOB	Effective resolution				15	Bits
f_{cs}	Channel sampling rate		0.01		1	kSPS
Oscillator						
f_{SENSOR}	Oscillator frequency range	T = -55℃to 125℃	10		100	MHz
$I_{SENSORMAX}$	Oscillator drive current		0.5	3.0	8.0	mA
Internal clock						
f_{INTCLK}	Internal clock frequency		2.3	2.4	2.5	MHz
$T_{CF\_INT\_U}$	Internal clock temperature drift coefficient	T=20℃to 125℃		- 700		ppm/℃
		T = -55℃to 20℃		800		ppm/℃
External clock						
f_{CLKIN}	external clock frequency	T = -55℃to 125℃	0.1		50	MHz
$CLKIN_{DUTY}$	External clock duty cycle		40%		60%	
V_{CLKIN_HI}	External clock high threshold		0.7*VDD			V
V_{CLKIN_LO}	External clock low threshold				0.3*VDD	V

Note 1: Peak current is measured and represents the current during conversion when configured in single conversion and continuous conversion modes. Note 2: Continuous conversion standby current indicates the current during non-conversion when configured in continuous conversion mode. Note 3: The current flowing into the SDA and SCL pins during I2C reading and writing is not included.

5.4. i²c interface timing[1]

Parameter	Symbol	Standard Mode		Quick Mode		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	
SCL Frequency	f_{SCL}	0	400	0	1000	kHz
SCL low level time	t_{LOW}	1300	-	620	-	ns
SCL high level time	t_{HIGH}	600	-	220	-	ns
Duration of SCL high level after SDA is pulled low during start or restart	$t_{HD;STA}$	400	-	260	-	Ns
The time interval from when SCL is pulled low to when SDA data changes	$t_{HD;DAT}$	0	0.9	0	-	μs
The time interval from when SDA data becomes stable to when SCL is pulled high	$t_{SU:DAT}$	100	-	150	-	ns
The high level holding time of SCL before SDA is pulled low during restart	$t_{SU;STA}$	400	-	260	-	ns
The time interval from when SCL is pulled high to when SDA is pulled high during stop	$t_{SU:STO}$	400	-	260	-	ns
The interval between start and stop	t_{BUF}	1300	-	500	-	ns
SCL/SDA rising edge time required	t_{RC}	20+ 0.1Cb[2]	1000	20+ 0.1Cb[2]	120	ns
SCL/SDA falling edge time required	t_{FC}	20+ 0.1Cb[2]	300	20+ 0.1Cb[2]	120	ns

1 All values are based on VIHmin and VILmax
2 Cb=total capacitance of I2C bus.

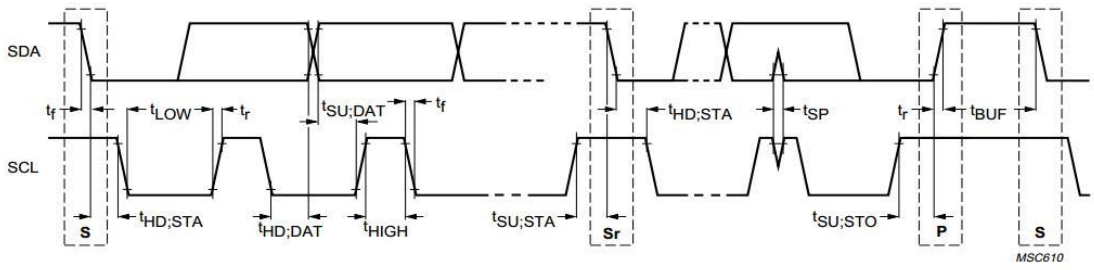


Figure 5.4 I2C timing parameters

6. Detailed description

6.1. Overview

MC12G and MC12T are high-precision, multi-channel capacitance conditioning chips suitable for a variety of capacitance sensing applications. Compared with the traditional switched capacitor structure, MC12G and MC12T adopt the LC resonance method for capacitance measurement. The narrow-band characteristics of the LC oscillator enable MC12G and MC12T to have lower noise levels and are less susceptible to external interference.

When the capacitance of the LC resonant tank changes, the resonant frequency of the circuit will also change. Based on this principle, MC12G, MC12T operate y measuring the oscillation frequency and outputting a data proportional to the frequency. From this data, the capacitance value can be calculated.

6.2. System block diagram

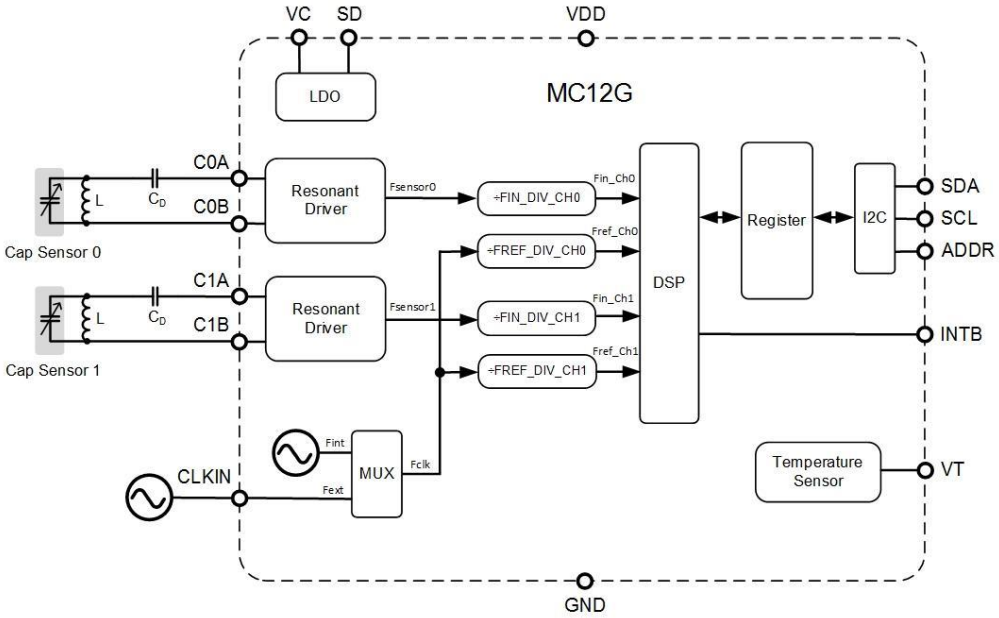


Figure 6.2-1 MC12G system block diagram

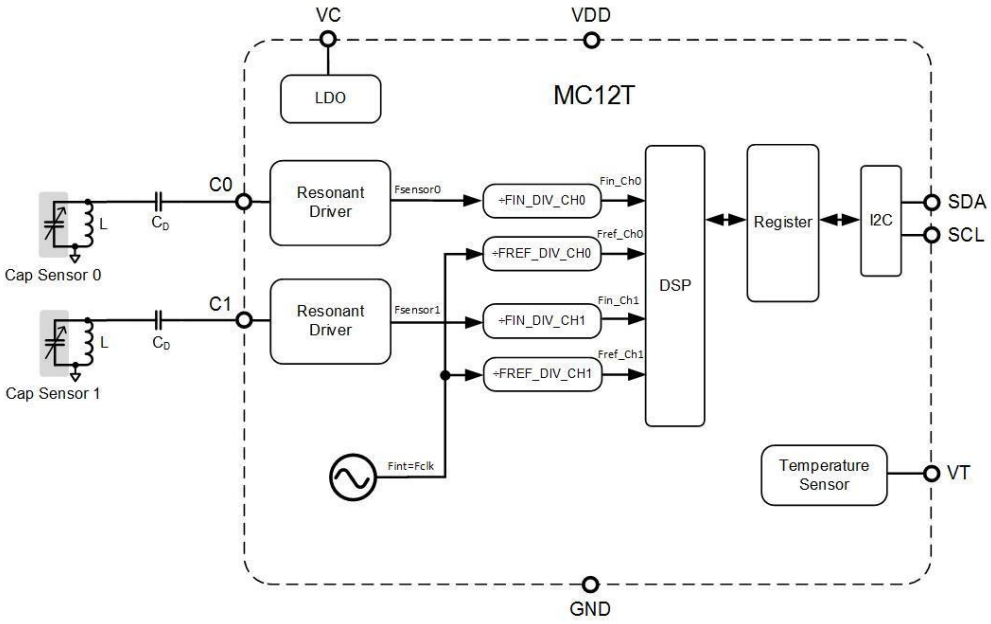


Figure 6.2-2 MC12T system block diagram

These diagrams are the system block diagrams of MC12G and MC12T respectively, including LDO power management, resonant driver circuit (Resonant Driver), and frequency divider (Divider) , internal clock (F_{int}), digital frequency calculation (DSP), register (Register), Temperature Sensor, I2C interface and other functional modules. The resonant drive circuit of MC12G and MC12T and the external LC form an active oscillation, which sends the output signal to the digital logic circuit to measure and digitize the signal frequency of the sensor rate(f_{SENSOR}) . For MC12G, the C0B/C1B pin is connected to GND internally through the sensor. Digital logic uses a reference frequency (f_{CLK}) to measure the signal frequency f of the sensor SENSOR. f_{CLK} from chip clock or external clock. The I2C interface is used for communication between the chip and the MCU. By measuring the VT pin voltage at the MCU end, the ambient temperature can be indirectly measured for temperature compensation. For MC12G, by controlling the SD pin, the chip can be shut down to reduce system power consumption; at the same time, the INTB pin can output an alarm status bit or a conversion completion flag signal according to the configuration.

6.3. Characteristic description

6.3.1.Clock system

According to the MC12G and MC12T system block diagram, f_{CLK}, f_{IN} and f_{REF} are three important clock signals. According to the register configuration, f_{CLK} can select the internal clock or the external clock (MC12T can only select the internal clock). The reference clock f_{REF} is obtained by dividing f_{CLK}. For high-precision applications, it is recommended to choose an external clock with high precision and high stability. The internal clock is more suitable for applications with low cost and moderate accuracy requirements. The measured signal clock f_{IN} is obtained by dividing the frequency of the sensor resonance signal f_{SENSOR}. In order to ensure correct measurement results, the clock frequencies of f_{REF} and f_{IN} need to meet the following conditions:

$$f_{INx} < \frac{f_{REFx}}{2.5}$$

For most effective resolution of the measurement, the ratio of f_{REF} to f_{IN} should be as close as possible to 2.5. The most significant number of digits is 15 bits. The following table is the clock configuration related register definition.

Channel	Clock	Registers and addresses	Bit	Description
0,1	f_{CLK}	CFG, 0x1F	REF_CLK_SEL	b0: Select internal clock b1: Select external clock
0	f_{REF0}	FREF_DIV_CH0, 0x12	CH0_FREF_DIV[7:0]	b00000000-b11111111 = values 0 to 255 $f_{REF0} = \frac{f_{CLK}}{CH0\_FREF\_DIV + 1}$
1	f_{REF1}	FREF_DIV_CH1, 0x14	CH1_FREF_DIV[7:0]	b00000000-b11111111 = values 0 to 255 $f_{REF1} = \frac{f_{CLK}}{CH1\_FREF\_DIV + 1}$
0	f_{IN0}	FIN_DIV_CH0, 0x11	CH0_FIN_DIV[3:0]	b0000-b0111 = value 0 to 7 b1000-b1111 = value 8 $f_{IN0} = \frac{f_{SENSOR0}}{2^{CH0\_FIN\_DIV}}$
1	f_{IN1}	FIN_DIV_CH1, 0x13	CH1_FIN_DIV[3:0]	b0000-b0111 = value 0 to 7 b1000-b1111 = value 8 $f_{IN1} = \frac{f_{SENSOR1}}{2^{CH1\_FIN\_DIV}}$

6.3.2.Channel conversion

6.3.2.1. Conversion mode

By setting the channel enable bit, you can choose to enable single-channel or multi-channel conversion. When selecting multi-channel conversion, channel 0 is started first, then channel 1, and the switching time between the two channels is ≤10us. The following table is the configuration channel related register definition.

Channel	Registers and addresses	Bit	Description
0	CH_EN, 0x20	CH0_EN	b0: Close channel 0 b1: Open channel 0
1	CH_EN, 0x20	CH1_EN	b0: Close channel 1 b1: Open channel 1

By setting the CFG register, the sensor's working mode can be configured, including single conversion, continuous conversion, stop conversion, and the measurement time interval of continuous conversion mode. The following table is the definition of registers related to working mode configuration.

Mode	Registers and addresses	Bit	illustrate
Single /Continuous	CFG, 0x1F	OS, SD	b00: Continuous conversion mode, the time interval is determined by the value of CR[2:0]. When changing the continuous conversion mode, conversion must be stopped first. b01: Stop conversion. b10: Same as b00. b11: Single conversion mode. After setting the flag, the chip will automatically stop after one conversion. After the conversion is completed, OS and SD automatically change to b01.
Collected per second Number of samples (MPS)	CFG, 0x1F	CR[2:0]	b000: Convert once every 60s b001: Convert once every 30s b010: Convert once every 10s b011: Convert once every 5 seconds b100: Convert once every 2s b101: Convert once in 1s b110: Convert once in 0.5s b111: Convert once in 0.25s

It should be noted that in order to ensure the correctness of the converted data, the following two points must be followed when modifying the register configuration:

1. To switch from continuous conversion mode to single conversion mode, you must first send a stop conversion command, and then send a single conversion command.
2. During the sensor measurement conversion process, do not modify any conversion-related register configuration. If you need to modify the configuration parameters, you need to stop the conversion first, make sure the conversion is stopped, then modify the configuration parameters and restart the conversion.

6.3.2.2. Data format and reading

The sensor measures the ratio between the divided frequency of each channel signal and the divided frequency of the reference clock, expressed in a 16-bit data format:

$$DATA_x = \frac{f_{INx}}{f_{REFx}} \times 2^{16} = \frac{f_{SENSORx}}{f_{CLK}} \times \frac{CHx\_FREF\_DIV + 1}{2^{CHx\_FIN\_DIV}} \times 2^{16}$$

The data results of channel conversion will be stored in the following corresponding registers:

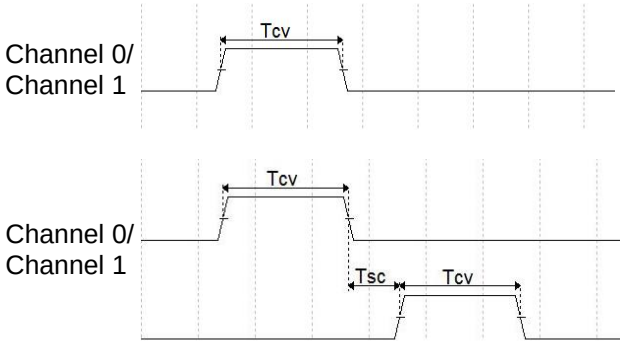
Channel	Registers and addresses	Bit	Description
0	DATA_CH0_MSB, 0x00	DATA0[15:8]	Channel 0 converts the upper 8 bits of data
	DATA_CH0_LSB, 0x01	DATA0[7:0]	Channel 0 converts the lower 8 bits of data
1	DATA_CH1_MSB, 0x02	DATA1[15:8]	Channel 1 converts the upper 8 bits of data
	DATA_CH1_LSB, 0x03	DATA1[7:0]	Channel 1 conversion data lower 8 bits

It should be noted that in order to ensure the accuracy of the converted data, the I2C reading of DATAx must be performed during the non-conversion period of the sensor. The specific method is:

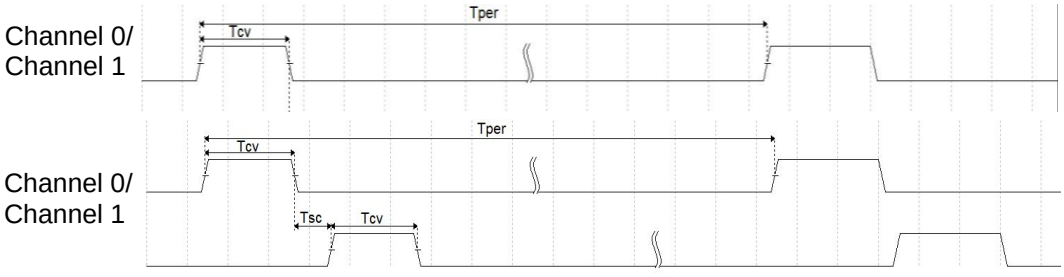
i. In single conversion mode, I2C reading of DATAx needs to be performed after the conversion is completed.
ii. In continuous conversion mode, you need to stop conversion first, execute I2C to read DATAx, and then restart continuous conversion.

6.3.2.3. Conversion time

The figure below is the timing diagram in single conversion mode when single channel and dual channel are selected. Among them, TCV is the total single-channel single conversion time, TSCIt is the channel switching time (<10us).



The figure below is the timing diagram in continuous conversion mode when single channel and dual channel are selected. Among them, T_{PER} is the measurement period of continuous conversion mode, T_{CV} is the total single-channel single conversion time, T_{SC} is the channel switching time (<10us).



To ensure that continuous conversion mode works properly, T_{PER} and T_{CV}. The following constraints need to be satisfied:

i. Single channel measurement, $T_{PER} > T_{CV}$

ii. Dual channel measurement, $T_{PER} > 2 \times T_{CV} + 10us$

T_{CV} including start-up time T_{START}, establishment time T_{SET}, counting time T_{CNT}, and the delay time T_{DELAY}.

$$T_{CV} = T_{START} + T_{SET} + T_{CNT} + T_{DELAY}$$

T_{START} indicates the stabilization time of the internal reference voltage, and is fixed at 200us. Channel establishment time T_{SET} indicates the initial stabilization time of the oscillation signal establishment, which is defined by the following registers:

Channel	Registers and addresses	Bit	Description
0	SCNT_CH0, 0x0E	SCNT0[7:0]	Channel 0 setup time
1	SCNT_CH1, 0x0F	SCNT1[7:0]	Channel 1 setup time

The calculation formula for T_{SET} is:

$$T_{SET} = \frac{SCNTx \times 16}{f_{REFx}}$$

In order to ensure sufficient time for channel signal establishment, $T_{CNT} \geq 100us$ should be set. When using the internal clock as f_{CLK}:

- Setting SCNT_CHx to 0x0F corresponds to T_{SET} being 100us and
- Setting SCNT_CHx to 0xFF corresponds to T_{SET} being 1.7ms

The counting time of the channel T_{CNT} represents the time for f_{REFx} to count pulses to f_{INx}, which is defined in the following table:

Channel	Registers and addresses	Bit	Description
0	RCNT_CH0_MSB, 0x08	RCNT0[15:8]	Channel 0 counting time high 8 bits
	RCNT_CH0_LSB, 0x09	RCNT0[7:0]	Channel 0 counting time low 8 bits
1	RCNT_CH0_MSB, 0x0A	RCNT1[15:8]	Channel 1 counting time high 8 bits
	RCNT_CH0_LSB, 0x0B	RCNT1[7:0]	Channel 1 counting time low 8 bits

The calculation formula for T_{CNT} is:

$$T_{CNT} = \frac{RCNTx}{f_{REFx}}$$

The calculation formula for T_{DELAY} is:

$$T_{DELAY} = \frac{4}{f_{REFx}}$$

Therefore, the conversion time T_{CV} is calculated by:

$$T_{CV} = \frac{200us + (SCNTx \times 16 + RCNTx + 4)}{f_{REFx}}$$

6.3.3.Capacitance calculation

The calculation formula of LC resonant frequency is:

$$f_{SENSOR} = \frac{1}{2\pi \times \sqrt{L \times (C_{SENSOR} + C_F)}}$$

Therefore, the measured capacitance C_{SENSOR} can be calculated as follows:

$$C_{SENSOR} = \frac{1}{L \times (2\pi \times f_{SENSOR})^2} - C_F$$

C_F Expressed with C_{SENSOR} the sum of the total parallel capacitances to ground, C_F can be expanded and expressed as:

$$C_F = \frac{C_D \times (C_P + C_{PCB})}{C_D + (C_P + C_{PCB})}$$

In the above formula, each capacitor represents:

C_D is an off-chip DC blocking capacitor, placed between the resonance point and the C0A/C1A pin (see section 6.2.1-2);

C_P is the total ground capacitance of the C0A/C1A pin inside the sensor, with a typical value of 52pF;

C^{PCB} is the total ground capacitance of the C0A/C1A pin on the PCB, with a typical value of 2pF.

$f_{SENSORx}$ can be calculated using DATAx as follows:

$$f_{SENSORx} = f_{CLK} \times \frac{2^{CHx\_FIN\_DIV}}{CHx\_FREF\_DIV + 1} \times \frac{DATAx}{2^{16}}$$

6.3.4.Drive current

Two-channel oscillator drive current I_{DRIVE} can be configured to different values, defined by the following registers.

Channel	Registers and addresses	Bit	illustrate
0	DRIVE_I_CH0, 0x23	I0[3:0]	Set the single channel drive current value. b0000-b1111: 0.5mA to 8mA, LSB=0.5mA
1	DRIVE_I_CH1, 0x24	I1[3:0]	

In order to ensure that the oscillator can start up successfully, the driving current I_{DRIVE} needs to be greater than a certain threshold, the threshold size is the same as C_{SENSOR}, C_D ,C_P. It is related to the capacitor network formed and the Q value of the inductor L. Generally speaking, the greater the driving current, the stronger the channel's oscillation ability and the greater the oscillation amplitude. For larger measured capacitance C_{SENSOR}, and the inductor L with a low Q value needs to increase the drive current to ensure the channel starts to oscillate.

6.3.5.Alarm function and INTB

MC12G and MC12T have alarm function. The alarm threshold includes trigger threshold TH and release threshold TL, which are defined by the following registers. Both TH and TL are 16 bits, which is the same number of bits as DATA_CHx.

Threshold	Registers and addresses	Bit	Description
Alarm trigger	TH_MSB, 0x19	TH[15:8]	When DATA_CHx > TH, ALERT_CHx in the STATUS register is set to 1
	TH_LSB, 0x1A	TH[7:0]	
Alarm stop	TL_MSB, 0x1B	TL[15:8]	When DATA_CHx<TL, ALERT_CHx in the STATUS register is set to 0
	TL_LSB, 0x1C	TL[7:0]	

When the conversion is completed, the alarm state is triggered when the following conditions are met:

$$DATA\_CHx > TH$$

After the alarm status is triggered, ALERT_CHx in the status register is set to 1, and the INTB pin output level changes from high to low (only applicable toMC12G). In order to ensure that the alarm function is turned on, when setting the TH and TL threshold parameters that TH > TL.

When the alarm status is triggered, there are 4 implementation methods to clear the alarm status:

i. Read channel conversion data through I2C, this method is limited to single conversion mode and stop mode.
ii. Perform a channel conversion and satisfy DATA_CHx < TL
iii. Enable software reset function.
iv. Pull the SD pin high.

For MC12G, the INTB pin can output the alarm status bit of channel 0 or channel 1, which is active at low level. After the alarm condition is cleared, the INTB pin returns to high level. In addition, the INTB pin can also be configured to output the conversion completion flag of channel 0 or channel 1. INTB functionality is defined by the following registers.

Channel	Registers and addresses	Bit	Description
0,1	CFG, 0x1F	INTB_EN	b0: INTB pin output enable.
			b1: INTB pin output is not enabled.
0,1	CFG, 0x1F	INTB_MODE	b0: INTB pin output alarm status bit, active low level.
			b1: INTB pin output conversion completion flag bit, active low level.
0,1	CH_EN, 0x20	INTB_CH	b0: INTB pin outputs the alarm status or conversion completion flag of channel 0.
			b1: The INTB pin outputs the alarm status or conversion completion flag of channel 1.

6.3.6.Resistance voltage

Both MC12G and MC12T can adapt to different VDD voltages. According to different VDD voltage conditions, the internal reference voltage value (VC pin voltage) is changed by configuring the VC_SEL register, so that the sensor can achieve optimal performance.

Channel	Registers and addresses	Bit	Description
0,1	VC_SEL, 0x23	VC	b00: Reference voltage 2.5V
			b01: Reference voltage 3.0V
			b10: Reference voltage 1.8V
			b11: Reference voltage 2.0V

In actual application, it is recommended to configure according to the following two points:

i. When 2.5V < VDD < 5.5V (VDD is between 2.5V and 5.5V), configure the reference voltage to 2.5V (default value).
ii. When 2V < VDD < 2.5V (VDD is between 2.0V and 2.5V), configure the reference voltage to 2.0V

6.3.7. Status Register

The status register can reflect whether the measurement data of MC12G and MC12T overflows, whether the conversion is completed, and the alarm status.

Channel	Registers and addresses	Bit	Description
0	STATUS, 0x17	OF_CH0	b0: Channel 0 data does not overflow b1: Channel 0 data overflow
1	STATUS, 0x17	OF_CH1	b0: Channel 1 data does not overflow b1: Channel 1 data overflow
0	STATUS, 0x17	DRDY_CH0	b0: Channel 0 conversion is not completed b1: Channel 0 conversion completed
1	STATUS, 0x17	DRDY_CH1	b0: Channel 1 conversion is not completed b1: Channel 1 conversion completed
0	STATUS, 0x17	ALERT_CH0	b0: Channel 0 does not trigger the alarm b1: Channel 0 triggers alarm
1	STATUS, 0x17	ALERT_CH1	b0: Channel 1 does not trigger the alarm b1: Channel 1 triggers alarm

6.3.8. Temperature Measurement

MC12G, MC12T provide a negative temperature coefficient voltage V_T, output to the V_T pin, is used to roughly evaluate the temperature. V_T Voltage measurement requires the use of an external ADC for sampling, and the conventional 10-bit precision ADC built into the MCU can meet the needs. Temperature value T can be calculated with this calculation:

$$T = K \times V_T + T_C$$

Where V_T is the voltage value measured by ADC, in mV; K is the temperature coefficient, the default value is -560.0℃/V; T_C is the temperature correction value, the default value is 386.3℃. Users can also choose to calibrate the K and T_C parameters themselves.

6.4. Functional Mode

6.4.1. Power on and start

MC12G and MC12T will automatically enter continuous conversion mode after power-on. Users can send a stop conversion command through I2C to put the chip into sleep mode, and then perform operations including parameter modification, single conversion, continuous conversion, etc.

6.4.2. Conversion Mode

The conversion modes of MC12G and MC12T are divided into single conversion mode and continuous conversion mode, which are configured through the CFG register. For details, see Chapter 6.3.2.

6.4.3. Sleep Mode

MC12G and MC12T will automatically enter sleep mode (low power consumption mode) after each execution of I2C command operation. When the host sends a valid I2C command, MC12G and MC12T will automatically wake up and perform corresponding operations. It should be noted that in continuous conversion mode, MC12G and MC12T will not enter sleep mode after each conversion is completed.

6.4.4. Shutdown Mode

The external SD pin of MC12G is used to initiate hardware shutdown (Shutdown). When the SD pin is pulled high, the chip function is completely shut down and i²c cannot be accessed. After the SD pin changes from low to high, the chip recovery time is <20us.

6.4.5. Software Reset

MC12G and MC12T provide software reset function. By writing 0x7A to the reset register, the software reset function is started, the sensor returns to the initial power-on state, all registers return to their default values, and the chip recovery time is <20us.

Channel	Registers and addresses	Bit	Description
0,1	RESET, 0x22	RESET[7:0]	b01111010 : Start the software reset and the sensor returns to the initial state after power-on, and all registers are restored to default values.

6.5. i²c Programming

The MCU accesses the control and data registers of MC12G and MC12T through the i²c interface. The SDA and SCL pins integrate spike suppression circuitry to reduce the impact of bus noise. MC12G and MC12T support i²c communication rate of 400KHz. The data SDA and clock SCL of the i²c interface are connected to the corresponding ports of the host processor respectively, and passed through the pull-up resistor RP. Connected to VDD, the read and write control of each node chip is realized through the host computer software. According to the actual application, the address of the slave device can be set through the value of pin ADDR.

6.5.1. i²c Address selection

MC12G can realize different i²c addresses through different connection methods of ADDR pin. The specific corresponding relationship is:

ADDR connection method	i²c address
Connect to GND	0x68
Connect to VDD	0x69
Connect to SDA	0x6A
Connect to SCL	0x6B

The I2C address of MC12T is fixed at 0x69. The MC12G development board PCB is also fixed at 0x69.

6.5.2. i²c Interface data format

Typical I2C bus operation is defined as follows:

Bus Idle: SDA and SCL both remain high.

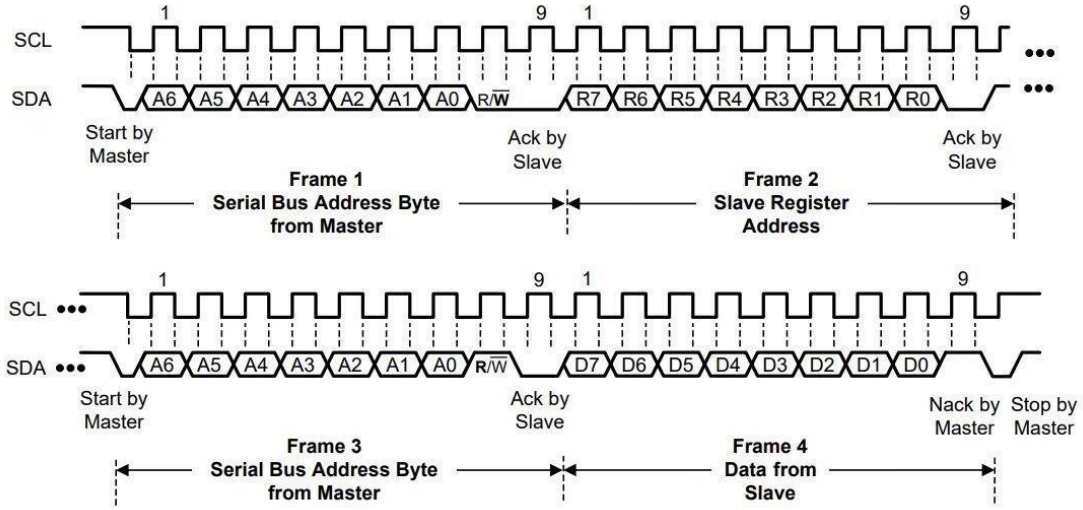
Start data transfer: When SCL is high, a change in SDA state (from high to low) indicates a start condition. Every data transfer begins with a start condition.

Stop data transfer: When SCL is high, the change of SDA state (from low level to high level) indicates the stop state. Each data transfer is terminated by a repeated start or stop condition.

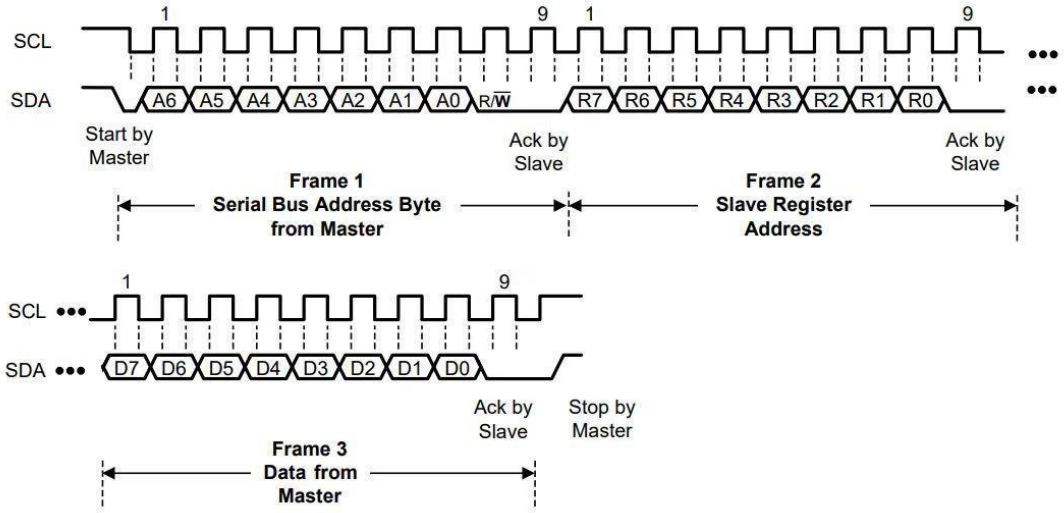
Data transfer: The number of data bytes transferred between start and stop conditions is unlimited and is determined by the master device. The receiver acknowledges the data transmission.

Response: Each receiving slave device must generate a response signal when being addressed. The slave must acknowledge by stabilizing SDA low during the high period of the acknowledge clock pulse. On the master side, the data transfer is terminated by the master not acknowledging the last byte transmitted by the slave.

For read i²c operations, the master sends the i²c slave address and write flag bit. The slave acknowledges, then the master sends the register it wishes to read. The slave acknowledges this. The master sends a bus re-start and sends the i²c slave address and the read bit. The slave acknowledges and then sends the contents of the register. Once this is complete, the master sends a negative-acknowledgement (NACK) and a bus stop.



For i²c write operations, the master will send a start bus event, then send the i²c address of the slave, accompanied by the write flag. The slave will ack this and the master will send the register address it wishes to write to. The slave will ack this and the master will send the data it wishes to put in the register. Once this is acknowledged by the slave, the master will send a bus stop event.



6.6. Register description

6.6.1. Register list

The registers of MC12G and MC12T include three categories: read-write, read-only, and write-only. The default value represents the value in the initial state of the sensor when it is powered on. Below is a list of all registers.

Address	Name	Default Value	Description
0x00	DATA_CH0_MSB	0x00	Channel 0 conversion data, read only
0x01	DATA_CH0_LSB	0x00	
0x02	DATA_CH1_MSB	0x00	Channel 1 conversion data, read only
0x03	DATA_CH1_LSB	0x00	
0x08	RCNT_CH0_MSB	0x40	Channel 0 counting time
0x09	RCNT_CH0_LSB	0x00	
0x0A	RCNT_CH1_MSB	0x40	Channel 1 counting time
0x0B	RCNT_CH1_LSB	0x00	
0x0E	SCNT_CH0	0x20	Channel 0 setup time
0x0F	SCNT_CH1	0x20	Channel 1 setup time
0x11	FIN_DIV_CH0	0x70	Channel 0 oscillation signal frequency division
0x12	FREF_DIV_CH0	0x00	Channel 0 reference clock divider
0x13	FIN_DIV_CH1	0x70	Channel 1 oscillation signal frequency division
0x14	FREF_DIV_CH1	0x00	Channel 1 reference clock divider
0x17	STATUS	0x00	Status bits, read only
0x19	TH_MSB	0x20	Single channel alarm trigger threshold
0x1A	TH_LSB	0x00	
0x1B	TL_MSB	0x10	Single channel alarm release threshold
0x1C	TL_LSB	0x00	
0x1F	CFG	0x54	Channel conversion and INTB function configuration
0x20	CH_EN	0xC0	Channel selection configuration
0x22	RESET	0x00	Reset function, write only
0x23	DRIVE_I_CH0	0x50	Channel 0 drive current
0x24	DRIVE_I_CH1	0x50	Channel 1 drive current
0x30	VC_SEL	0x00	VC voltage configuration
0x33	GLITCH_FILTER_EN	0x01	Anti-glitch filter
0x7E	CHIP_ID_MSB	0x01	Chip ID, read only
0x7F	CHIP_ID_LSB	0x20	

6.6.2. DATA_CH0_MSB, DATA_CH0_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	DATA0							
0x01	DATA0							

Bit	Scope	Operation	Default Value	Description
7:0	DATA0[15:8]	Read Only	0000 0000	The two byte registers can be used to obtain a 16 bit conversion data of channel 0
7:0	DATA0[7:0]	Read Only	0000 0000	

6.6.3. DATA_CH1_MSB, DATA_CH1_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	DATA1							
0x03	DATA1							

Bit	Scope	Operation	Default Value	Description
7:0	DATA1[15:8]	Read Write	0000 0000	The two byte registers can be used to obtain a 16 bit conversion data of channel 1
7:0	DATA1[7:0]	Read Write	0000 0000	

6.6.4. RCNT_CH0_MSB, RCNT_CH0_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	RCNT0							
0x09	RCNT0							

Bit	Scope	Operation	Default Value	Description
7:0	RCNT0[15:8]	Read Write	0000 0000	The two byte registers can be used to obtain a 16 bit counting rate of channel 0.
7:0	RCNT0[7:0]	Read Write	0000 0000	

6.6.5. RCNT_CH1_MSB, RCNT_CH1_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	RCNT1							
0x0B	RCNT1							

Bit	Scope	Operation	Default Value	Description
7:0	RCNT1[15:8]	Read Write	0000 0000	The two byte registers can be used to obtain a 16 bit counting rate of channel 1.
7:0	RCNT1[7:0]	Read Write	0000 0000	

6.6.6. SCNT_CH0

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	SCNT0							

Bit	Scope	Operation	Default Value	Description
7:0	SCNT0[7:0]	Read Write	0010 0000	Set the channel 0 settling time.

6.6.7. SCNT_CH1

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0F	SCNT1							

Bit	Scope	Operation	Default Value	Description
7:0	SCNT1[7:0]	Read Write	0010 0000	Set the channel 1 settling time.

6.6.8. FIN_DIV_CH0

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	CH0_FIN_DIV				RSV			

Bit	Scope	Operation	Default Value	Description
7:4	CH0_FIN_DIV [3:0]	Read Write	0111	Set the oscillation signal frequency division ratio of channel 0 0000: No frequency division 0001: Frequency division by 2 0010: Frequency division by 4 0011: Frequency division by 8 0100: Frequency division by 16 0101: Frequency division by 32 0110: Frequency division by 64 0111: Frequency division by 128 [Default] 1xxx: Frequency division by 256 $f_{IN0} = \frac{f_{SENSOR0}}{2^{CH0\_FIN\_DIV}}$
3:0	RSV [3:0]	Read Write	0000	Reserved bit, can only write 0

6.6.9. FREF_DIV_CH0

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	CH0_FREF_DIV							

Bit	Scope	Operation	Default Value	Description
7:0	CH0_FREF_DIV [7:0]	Read Write	0000 0000	Set the reference clock division ratio of channel 0, 8-bit value 1 to 256. $f_{REF0} = \frac{f_{CLK}}{(CH0\_FREF\_DIV + 1)}$

6.6.10. FIN_DIV_CH1

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	CH1_FIN_DIV				RSV			

Bit	Scope	Operation	Default Value	Description
7:4	CH1_FIN_DIV [3:0]	Read Write	0111	Set the oscillation signal frequency division ratio of channel 1 0000: No frequency division 0001: Frequency division by 2 0010: Frequency division by 4 0011: Frequency division by 8 0100: Frequency division by 16 0101: Frequency division by 32 0110: Frequency division by 64 0111: Frequency division by 128 [Default] 1xxx: Frequency division by 256 $f_{IN0} = \frac{f_{SENSOR0}}{2^{CH0\_FIN\_DIV}}$
3:0	RSV [3:0]	Read Write	0000	Reserved bit, can only write 0

6.6.11. FREF_DIV_CH1

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	CH1_FREF_DIV							

Bit	Scope	Operation	Default Value	Description
7:0	CH1_FREF_DIV [7:0]	Read Write	0000 0000	Set the reference clock division ratio of channel 0, 8-bit value 1 to 256. $f_{REF1} = \frac{f_{CLK}}{(CH1\_FREF\_DIV + 1)}$

6.6.12. STATUS

Register	Bit7	Bit6	Bit5	Bit4	Bit3 Bit2	Bit1	Bit0
0x17	OF_CH1	OF_CH0	DRDY_CH1	DRDY_CH0	RSV	ALERT_CH1	ALERT_CH0

Bit	Scope	Operation	Default Value	Description
7	OF_CH1	Read Only	0	DATA_CH1 overflow flag, read data is cleared.
6	OF_CH0	Read Only	0	DATA_CH0 overflow flag, read data is cleared.
5	DRDY_CH1	Read Only	0	Channel 1 conversion completed, read data cleared.
4	DRDY_CH0	Read Only	0	Channel 0 conversion completed, read data cleared.
3:2	RSV	Read Only	00	Reserved Bits
1	ALERT_CH1	Read Only	0	Channel 1 alarm trigger status bit, read register to clear.
0	ALERT_CH1	Read Only	0	Channel 0 alarm trigger status bit, read data to clear

6.6.13. TH_MSB, TH_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19	TH_MSB							
0x1A	TH_LSB							

Bit	Scope	Operation	Default Value	Description
7:0	TH[15:8]	Read Write	0100 0000	Constitute 16bit data contains the single-channel alarm triggering threshold. After the channel conversion is completed, when DATA_CHx > TH, the alarm status bit ALERT_CHx is set to 1.
7:0	TH[7:0]	Read Write	0000 0000	

6.6.14. TL_MSB, TL_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	TL_MSB							
0x1C	TL_LSB							

Bit	Scope	Operation	Default Value	Description
7:0	TH[15:8]	Read Write	0010 0000	Constitute 16bit data contains the single-channel alarm reset threshold. After the channel conversion is completed, when DATA_CHx < TL, the alarm status bit ALERT_CHx is set to 0.
7:0	TH[7:0]	Read Write	0000 0000	

6.6.15. CFG

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1F	REF_CLK_SEL	INTB_EN	INTB_MODE	CR			SD	OS

Bit	Scope	Operation	Default Value	Description
7	REF_CLK_SEL	Read Write	0	Reference Clock to use: 0: Internal Clock [Default] 1: External Clock
6	INTB_EN	Read Write	1	INTB pin is 0 (disabled) or 1 (enabled)
5	INTB_MODE	Read Write	0	Which event triggers INTB: 0: Threshold alarm triggers. 1: Conversion complete triggers.
4:2	CR	Read Write	101	The time interval between consecutive conversion modes: 000: Convert once every 60s 001: Convert once every 30 seconds 010: Convert once every 10 seconds 011: Convert once every 5 seconds 100: Convert once in 2s 101: Conversion once per 1s 110: Convert once in 0.5s 111: Convert once in 0.25s

1	OS	Read Write	0	Set channel conversion mode 00: Continuous conversion 01: Stop conversion 10: Continuous conversion (actually sets 00) 11: Single conversion
0	SD	Read Write	0	

6.6.16. Channel Enable

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	CH1_EN	CH0_EN	RSV					INTB_CH

Bit	Scope	Operation	Default Value	Description
7	CH1_EN	Read Write	1	Channel 1 is enabled (1) or disabled (0)
6	CH0_EN	Read Write	1	Channel 0 is enabled (1) or disabled (0)
5:1	RSV	Read Write	00000	Reserved (must be all zeros)
0	INTB_CH	Read Write	0	INTB port output selection 0: Output the status information of Channel 0 1: Output the status information of Channel 1

6.6.17. RESET

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	RESET							

Bit	Scope	Operation	Default Value	Description
7:0	RESET[7:0]	Write	0000 0000	0111 1010: Start software reset, the chip returns to the initial power-on state, and all registers return to their default values. Any other value: Always 0000 0000 when read.

6.6.18. DRIVE_IC_CH0, DRIVE_IC_CH1

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	I_CH0				RSV			
0x24	I_CH1				RSV			

Bit	Scope	Operation	Default Value	Description	
7:4	I_CH0[0:3] I_CH1[0:3]	Read Write	I_CH0: 0101 I_CH1: 0101	Set the drive current of channel CH0 or CH1	
				0000: 0.5mA 0001: 1.0mA 0010: 1.5mA 0011: 2.0mA 0100: 2.5mA 0101: 3.0mA 0110: 3.5mA 0111: 4.0mA	1000: 4.5mA 1001: 5.0mA 1010: 5.5mA 1011: 6.0mA 1100: 6.5mA 1101: 7.0mA 1110: 7.5mA 1111: 8.0mA
3:0	RSV	Read Write	0000	Reserved bits, must be 0.	

6.6.19. VC_SEL

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	RSV				VC		RSV	

Bit	Scope	Operation	Default Value	Description
7:4	RSV	Read Write	0000	Reserved bits, must be 0.
3:2	VC	Read Write	00	Set reference voltage 00: 2.5V [Default] 01: 3.0V 10: 1.8V 11: 2.0V
1:0	RSV	Read Write	00	Reserved bits, must be 0.

6.6.20. Glitch filter

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x33	RSV							FILTER_EN

Bit	Scope	Operation	Default Value	Description
7:1	RSV	Read Write	0000 000	Reserved bits, must be 0.
0	FILTER_EN	Read Write	1	Anti-glitch filter enabled 0: Turn off the anti-peak filter 1: Turn on the anti-peak filter [Default]

6.6.21. DEVICE_ID_MSB, DEVICE_ID_LSB

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7E	DEVICE_ID_MSB							
0x7F	DEVICE_ID_LSB							

Bit	Scope	Operation	Default Value	Description
7:0	DEVICE_ID_MSB[15:8]	Read Only	0000 0001	The two byte registers can be used to obtain a the device's chip identification number eg. 0x0120
7:0	DEVICE_ID_LSB[7:0]	Read Only	0010 0000	

7. Application and implementation

7.1. Typical application circuit

MC12G and MC12T need to build an LC resonant cavity circuit off-chip. C_{SENSOR} in the picture below is the measured capacitance, and L is the resonant inductance. After the conversion is completed, the MCU reads the chip's data DATA_CHx and calculates C_{SENSOR} according to the formula in Chapter 6.3.3. The VT signal is inversely proportional to the temperature. Referring to the formula in Chapter 6.3.8, the temperature value can be calculated. The VT value can be read using an analogue pin on the MCU.

In addition to the above application modes, the MC12G can also be used as a capacitive switch. After powering on, the sensor will automatically enter continuous conversion mode and measure once per second. When DATA_CH0 exceeds the alarm trigger threshold (TH Register), the INTB pin will automatically output the alarm flag. When the data is below the alarm reset threshold (TL Register), the INTB pin will automatically clear the alarm flag.

MC12G supports two connection methods of the capacitor under test: for double-electrode detection scenarios, one end of the capacitor under test is connected to the C0A/C1A pin, and the other end is connected to the C0B/C1B pin. The C0B/C1B pin is connected to GND through the inside of the sensor, as shown in the figure. As shown in 7.1-1.

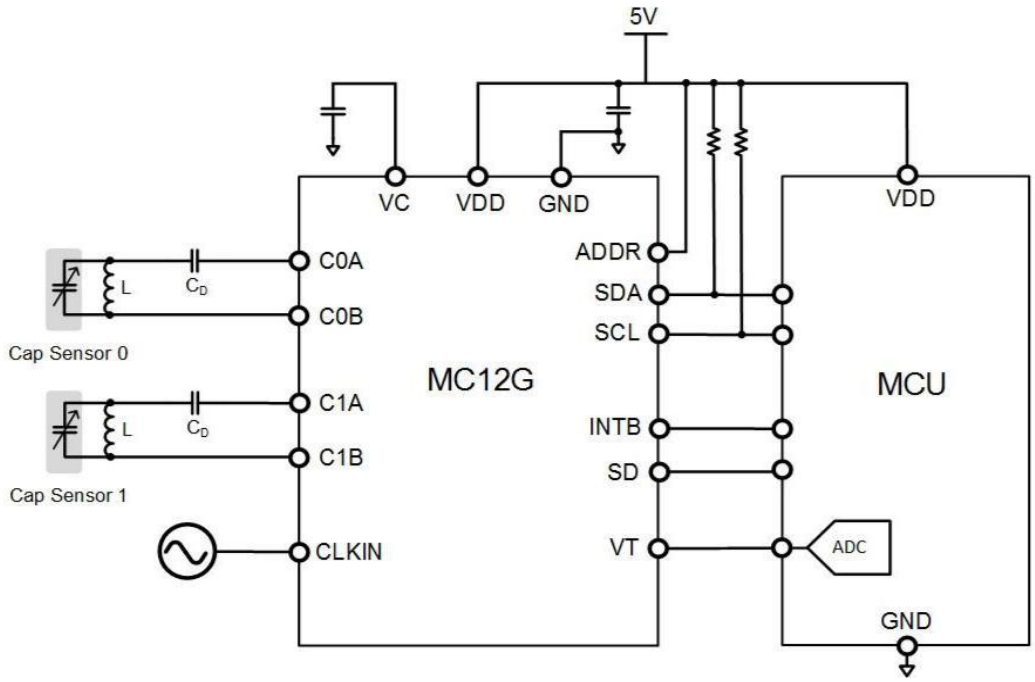


Figure 7.1-1 MC12G typical application circuit diagram: double electrode detection

For single-ended detection scenarios, the positive terminal of the capacitor under test is connected to the inductor L, and the negative terminal is connected to GND, as shown in Figure 7.1-2. In order for the sensor to enter a low-power state during non-conversion, the CLKIN pin needs to be held low.

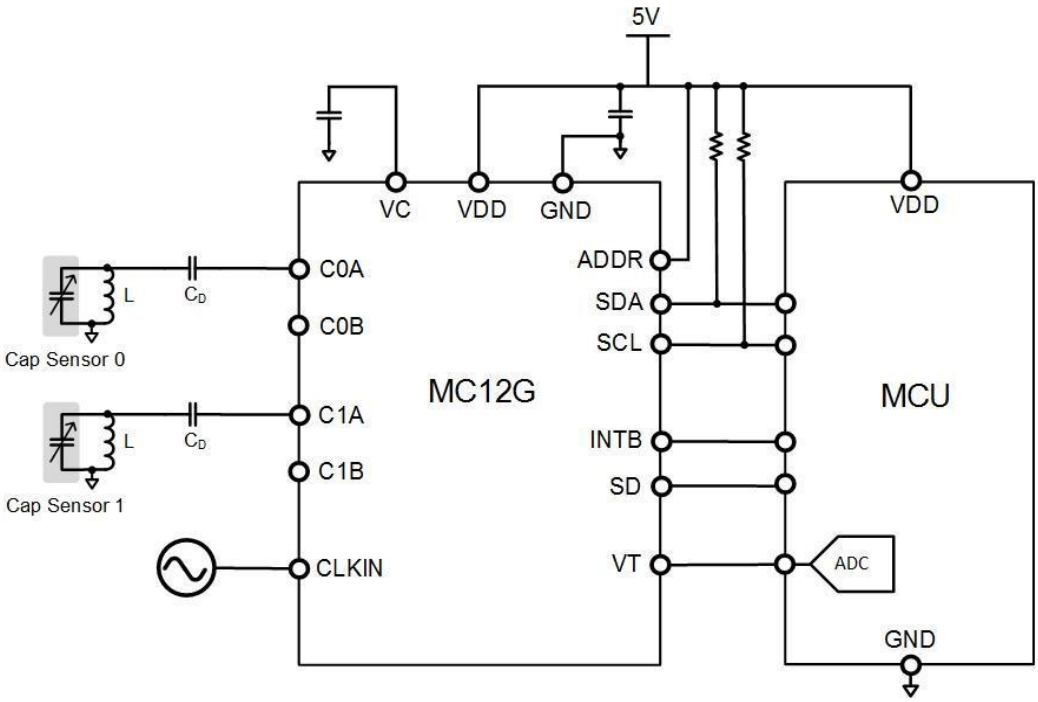


Figure 7.1-2 MC12G typical application circuit diagram: single electrode detection

MC12T only supports the positive terminal of the capacitor under test to be connected to the inductor L, and the negative terminal to GND, as shown in Figure 7.1-3.

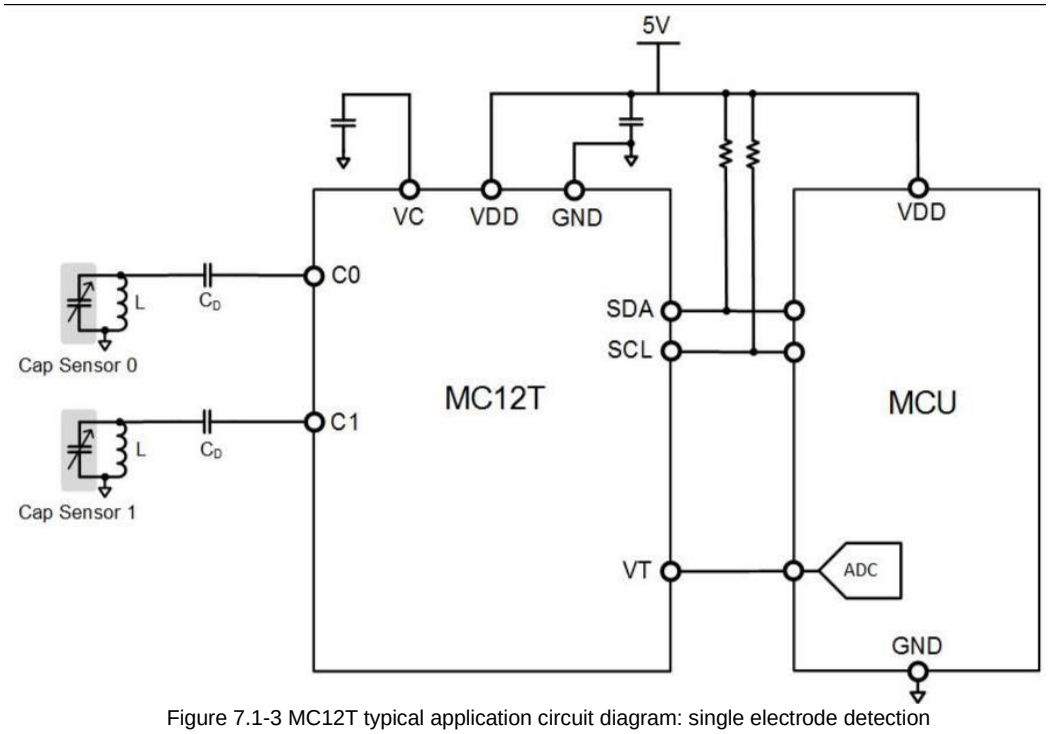


Figure 7.1-3 MC12T typical application circuit diagram: single electrode detection

For MC12G and MC12T, the recommended external capacitor value for the VC pin is 4.7nF.

7.2. Typical application examples

Scenario:

- Single-channel application requires 100 samples/second.
- Conversion time T_{CV}=10ms
- Inductor: 1uH
- C_D: 100pF.
- C0A chip internal parasitic capacitance to ground C_P = 51.5pF
- C0A PCB parasitic capacitance C_{PCB} = 2pF.

In this way, with C_{SENSOR} The sum of the total parallel capacitances to ground C_F for:

$$C_F = \frac{(C_P + C_{PCB}) \times C_D}{C_P + C_{PCB} + C_D} = 39.4pF$$

Then calculate the maximum oscillation frequency through the LC resonance formula:

$$f_{SENSOR,MAX} = \frac{1}{2\pi \times \sqrt{L \times C_F}} = 80.2MHz$$

This frequency is the maximum oscillation frequency, when using C_{SENSOR}. When connected to a circuit, the oscillation frequency will decrease. Select the internal 2.4MHz clock of the chip for counting. The configuration process of each related register is as follows:

- Configure channel 0 conversion and configure the CH_EN register to 0x40 (enable channel 0, disable channel 1, disable INTB triggering).
- Configure the chip to use the internal clock for counting: Set bit 7 of the CFG register to 0.
- To ensure accuracy, f_{REF} is recommended to meet the conditions:

$$f_{REF0} = \frac{f_{CLK}}{(CH0\_FREF\_DIV + 1)} > 2.5 \times \frac{f_{SENSOR,MAX}}{2^{CH0\_FIN\_DIV}}$$

  f_{CLK}=2.4MHz, select CH0_FREF_DIV=0, CH0_FIN_DIV=7, which can meet the above conditions. Therefore, configure the FREF_CH0_DIV register to 0x00 and the FIN_CH0_DIV register to 0x70.
  To ensure that the oscillator can start and control the oscillation amplitude, the driving current can be configured as 3mA by setting the DRIVE_I_CH0 register to 0x50. If it still fails to start, increase the drive current value and re-test.
  To ensure sufficient setup time, take T_{SET0} ≥ 100us, by configuring the SCNT_CH0 register to 0x0F, so that the actual T_{SET0}=100us.

- Calculate counting time TCNT:

$$T_{CNT0} = T_{CV0} - T_{START} - T_{SET0} - T_{DELAY} = 10000 - 200 - 100 - 1.6 = 9.7ms$$

$$T_{CNT0} = \frac{RCNT0}{f_{REF0}}$$

According to the configuration in the previous steps, f_{REF0}=2.4MHz. Therefore, R_{CNT0}=23760, the maximum resolution is >13 bit. Configure the RCNT_CH0_MSB register to 0x5A and the RCNT_CH0_LSB register to 0xF0.

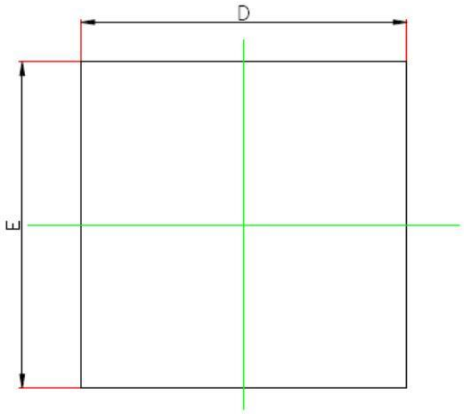
For MC12G, if you want to use the interrupt signal output by the INTB pin, you need to set bit 6 of the CFG register to 1 and bit 0 to 0, so that INTB can output the comparison result of the converted data, and the comparison thresholds are stored in the TH_MSB / TH_LSB registers. and TL_MSB/TL_LSB registers.

7.3. Inductor self-resonant frequency

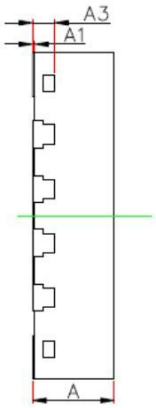
The inductor itself has parasitic capacitance, corresponding to a specific self-resonant frequency. In order to avoid entering the self-resonant state, it is recommended that the oscillation signal frequency f_{SENSOR} < 0.8 x f_{SR}.

8. Encapsulation

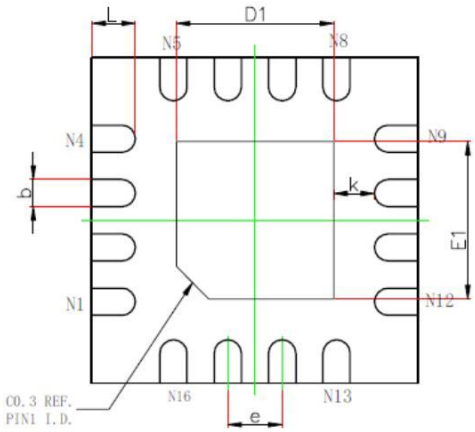
8.1. MC12G QFN16 3.0*3.0*0.75mm



TOP VIEW
[顶视图]



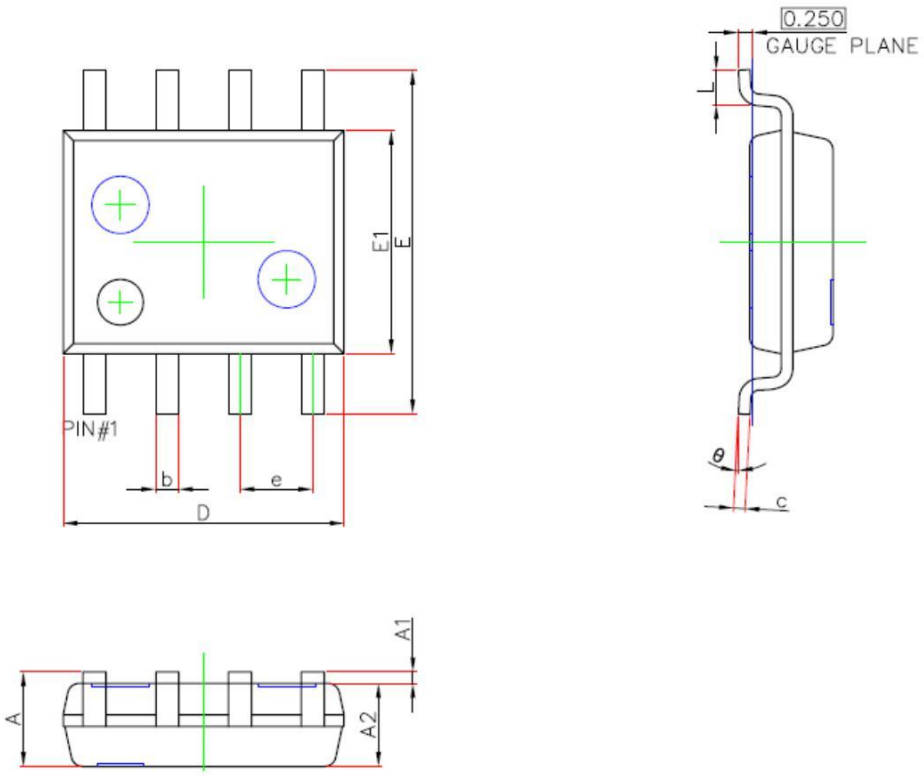
SIDE VIEW
[侧视图]



BOTTOM VIEW
[背视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.350	1.550	0.053	0.061
E1	1.350	1.550	0.053	0.061
k	0.375REF.		0.015REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020

8.2. MC12T SOP8 4.9*3.9*1.6mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°