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TWG Second Showing

Item 11-11-00001.007

Subject: DeviceID Enhancement Specification

Background: The many uses of DeviceID in future RapidIO products create a requirement for more DeviceIDs in the system. This showing proposes an extension of the maximum DeviceID size.

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Comment Expiration Date:

Distribution: RapidIO TA Technical Working Group members

Chapter 1 Introduction

All material previously related to increasing the size of device IDs has moved to showing 12-01-00000. This showing is now limitted to enhancing the routing table programming model for Dev32 device IDs.

1.1 Discussion of Routing Table Programming Model

The current standard programming model for RapidIO switches assumes sequential device ID programming. This becomes problematic when the size of a deviceID increases to 24 or 32 bits, since switches cannot incorporate the memories required to route all individual device IDs. A hierarchical routing approach is necessary, where portions of a device ID are used to route groups of device IDs. However, current hierarchical programming models are proprietary.

Gen2 IDT switches support a flexible, proprietary hierarchical programming model. It is proposed to extend this programming model to support the increase in device ID size, and incorporate it into the standard.

The proposed programming model extends the previously proposed hierarchical programming model to three levels numbered 0, 1 and 2, where 0 is the top level. Each level has an implementation specific number of routing table entries arranged in 256 entry groups. This allows switches to determine the route of a Dev32 device IDs based on the most significant or least significant three bytes simultaneously. Dev16 device IDs are routed based on a level 1 and level 2 groups. Dev8 device IDs are based on a level 2 group.

It is proposed to continue to support a flat programming model where all of the groups at all of the levels can be arranged to support a contiguous range of device IDs. It is unlikely that this routing table will expand to support any Dev32 device IDs.

Most importantly, the Dev32 routing table programming model supports routing on a per port basis. A new switch routing table register block is defined for this purpose. Each entry for all groups at all levels is memory mapped to avoid the mutual exclusion issues that an indexed register access scheme creates. Due to the number of entries, the memory mapped registers must appear in implementation specific register space. Routing table groups may be shared between multiple ports. Sharing is communicated by the registers in the new switch routing table register block.

The increased size of the device IDs breaks some limitations of the Gen2 programming model. For this reason, the Gen2 routing programming model is restricted to supporting Dev8 device IDs when Dev32 is supported.

The multicast programming model is completely changed to leverage the new per-port hierarchical programming model. The programming model is also changed to reduce/remove mutual exclusion requirements.

Chapter 2 Proposal

This showing proposes changes to the Part 3 Common Transport layer and Part 11 Multicast Support registers to support a new programming model for Dev32 device IDs.

2.1 Changes to Existing Registers

In Part 3, change the existing register definitions as identified by the underlined text below.

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2.1.1 Host Base Device ID Lock CSR (Configuration Space Offset 0x68)

The host base device ID lock CSR contains the base device ID value for the processing element in the system that is responsible for initializing this processing element. The Host_base_deviceID field is a write-once/reset-able field which provides a lock function. Once the Host_base_deviceID field is written, all subsequent writes to the field are ignored, except in the case that the value written matches the value contained in the field. In this case, the register is re-initialized to 0x0000FFFF. After writing the Host_base_deviceID field a processing element must then read the Host Base Device ID Lock CSR to verify that it owns the lock before attempting to initialize this processing element. The bit settings are shown in Table 1-1.

Table 2-1. Bit Settings for Host Base Device ID Lock CSR

Bits	Name	Reset Value	Description
0-15	Host_base_Dev32ID	0x0000	If the Processing Element Features CAR Dev32 Support bit is 0, then this field is Reserved and shall have a constant value of 0. If the Processing Element Features CAR Dev32 Support bit is 1, this field contains the most significant 16 bits of the Dev32 base device ID for the PE that is initializing this PE.
16–31	Host_base_deviceID	0xFFFF	This is the base device ID for the PE that is initializing this PE.

2.1.2 Standard Route Configuration Port Select CSR (Configuration Space Offset 0x74)

When written, the Standard Route Configuration Port Select CSR updates the switch output port configuration for packets with the destination ID selected by the Standard Route Configuration Destination ID Select CSR. When read, the Standard Route Configuration Port Select CSR returns the switch output port configuration for packets with the destination ID selected by the Standard Route Configuration Destination ID Select CSR.

If the extended route table configuration mechanism is enabled, when the Standard Route Configuration Port Select register is written the following route table configurations are carried out:

- destination ID Config_destID is routed to output port Config_output_port
- destination ID Config_destID+1 is routed to output port Config_output_port1
- destination ID Config_destID+2 is routed to output port Config_output_port2
- destination ID Config_destID+3 is routed to output port Config_output_port3

For reads of the Standard Route Configuration Port Select CSR, the configuration information is returned in the corresponding fashion.

After complete system initialization the switch output port route configuration information read may not be consistent with previously read values due to the capabilities and features of the particular switch. This register is required if bit 23 of the Processing Element Features CAR is set. The bit settings are shown in Table 1-2.

Table 2-2. Bit Settings for Standard Route Configuration Port Select CSR

Bits	Name	Reset Value	Description
0-7	Config_output_port3	0x00	Configuration output port3 - This field is reserved if extended route table mechanism is not enabled
8-15	Config_output_port2	0x00	Configuration output port2 - This field is reserved if extended route table mechanism is not enabled
16-21	Config_output_port1_msb	0x00	Most significant 6 bits of the output port 1 value if the extended route table mechanism is enabled. This field is reserved if extended route table mechanism is not enabled

Table 2-2. Bit Settings for Standard Route Configuration Port Select CSR (Continued)

Bits	Name	Reset Value	Description
22-23	Config_output_port1_lsb	0b00	Least significant 2 bits of the output port 1 value if the extended route table mechanism is enabled. Most significant 2 bits of the route value if bit 20 of the Processing Element Features CAR is set. This field is reserved if extended route table mechanism is not enabled and bit 20 of the Processing Element Features CAR is clear.
24-31	Config_output_port	see footnote*	Configuration output port. If bit 20 of the Processing Element Features CAR is set, the routing table value read and written is found in the Config_output_port1_lsb and Config_output_port fields.

*The Config_output_port reset value is implementation dependent

2.1.3 Standard Route Default Port CSR (Configuration Space Offset 0x78)

The Standard Route Default Port CSR specifies the port to which packets with destinations IDs that are greater than that specified in the Switch Route Table Destination ID Limit CAR are routed. This register is required if bit 23 of the Processing Element Features CAR is set.

.The bit settings are shown in Table 1-3.

Table 2-3. Bit Settings for Standard Route Default Port CSR

Bits	Name	Reset Value	Description
0-21	—		Reserved
22-23	Route Type	0b11	Extended value for packet routing. This field is required when bit 20 of the Processing Element Features CAR is set. If bit 20 of the Processing Element Features CAR is clear, this field is reserved.
24–31	Default_output_port	0x00	Default output port When bit 20 of the Processing Element Features CAR is set, Route Type concatenated with default_output_port shall be encoded as follows: 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF 0x200 to 0x2FF - Reserved. 0x300 - Drop Packet 0x301 to 0x3FF - Reserved. Selection of an Egress Port Number which is not supported by the device, or a Multicast Mask Number which is not supported by the device, shall result in implementation specific routing behavior.

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In Part 3, define the following new register extensions block:

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2.2 Switch Routing Table Register Block

A switch device which has bit 20 set in the Processing Element Features CAR shall implement this register block.

2.2.1 Register Map

The register map for the routing table registers shall be as specified by Table 1-4. This register map is currently only defined for devices with up to 16 RapidIO ports, but can be extended or shortened if more or less port definitions are required for a device. For example, a device with four RapidIO ports is only required to use register map space corresponding to offsets [EF_PTR+0x00] through [EF_PTR+0xBC]. Register map offset [EF_PTR+0x140] can be used for another Extended Features block.

Table 2-4. Switch Routing Table Register Map

	Block Byte Offset	Register Name
General	0x0	Routing Table Register Block Header
	0x4-0x1C	Reserved
Broadcast	0x20	Broadcast Routing Table Control CSR
	0x24-0x2C	Reserved
	0x30	Broadcast Level 0 Info CSR
	0x34	Broadcast Level 1 Info CSR
	0x38	Broadcast Level 2 Info CSR
	0x3C	Reserved
Port 0	0x40	Port 0 Routing Table Control CSR
	0x44-0x4C	Reserved
	0x50	Port 0 Level 0 Info CSR
	0x54	Port 0 Level 1 Info CSR
	0x58	Port 0 Level 2 Info CSR
	0x5C	Reserved
Port 1	0x60	Port 1 Routing Table Control CSR
	0x64-0x6C	Reserved
	0x70	Port 1 Level 0 Info CSR
	0x74	Port 1 Level 1 Info CSR
	0x78	Port 1 Level 2 Info CSR
	0x7C	Reserved

Table 2-4. Switch Routing Table Register Map

	Block Byte Offset	Register Name
Ports 2-14	0x80–21C	Assigned to Port 2-14 CSRs
Port 15	0x220	Port 15 Routing Table Control CSR
	0x224-0x22C	Reserved
	0x230	Port 15 Level 0 Info CSR
	0x234	Port 15 Level 1 Info CSR
	0x238	Port 15 Level 2 Info CSR
	0x23C	Reserved

2.2.2 Switch Routing Table Register Block Header (Block Offset 0x0)

The switch routing table register block header register contains the EF_PTR to the next EF_BLK and the EF_ID that identifies this as the switch routing table registers block header. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-5. The register shall be read-only.

Table 2-5. Bit Settings for Switch Routing Table Register Block Header

Bit	Name	Reset Value	Description
0-15	EF_PTR	see footnote*	Hard wired pointer to the next block in the data structure, if one exists
16-31	EF_ID	0x000E	Hard wired Extended Features ID

*The EF_PTR reset value is implementation dependent

2.2.3 Broadcast Routing Table Control CSR (Block Offset 0x20)

Writes to this register are broadcast to all Port n Routing Table Control CSRs. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-6. Unless otherwise specified, the bits and bit fields in this register are write only.

Table 2-6. Bit Settings for Port n Routing Table Control CSR

Bit	Name	Reset Value	Description
0	Three Levels	0b1	0 - Routing table entries support a contiguous range of device IDS, starting with device ID 0x00/0x0000/0x00000000. 1 - Routing table entries support a hierarchical routing scheme
1	Dev32 Route Control	0b0	0 - Dev32 Device IDs are routed using Byte 0 for Level 0, Byte 1 for Level 1, and Byte 2 for Level 2 1 - Dev32 Device IDs are routed using Byte 1 for Level 0, Byte 2 for Level 1, and Byte 3 for level 2 Reserved if Three Levels is clear.
2-7	___		Reserved
8-15	Dev16 Level 1 Index	0b00	Index of the routing table group used to route the most significant byte of Dev16 device IDs. Reserved if Three Levels is clear.
16-23	___	0x00	Reserved
24-31	Dev8 Level2 Index	0b00	Index of the routing table group used to route Dev8 device IDs. Reserved if Three Levels is clear.

2.2.4 Broadcast Level 0 Info CSR (Block Offset 0x30)

This register shall communicate the location of the Broadcast Level 0 routing table group. Writes to the Broadcast Level 0 routing table group affect all Port n Level 0 routing groups. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-7. This register shall be read only.

Table 2-7. Bit Settings for Broadcast Level 0 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L0_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 0. When Three Levels is 0, Num_L0_Groups shall communicate the number of groups available for routing. When Three Levels is 1, Num_L0_Groups shall be 1. Num_L0_Groups is encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L0_Group_Ptr	see footnote†	The L0_Group_Ptr value shall be the maintenance offset of the first entry in the first routing table group for level 0, divided by 1024. The maintenance offset of the first entry in the first routing group for level 0 shall be a 1024 byte aligned address. The L1_Group_Ptr value shall indicate an address in Implementation Defined register space. Writes to the broadcast routing table group entries pointed to by this register shall cause the corresponding routing table group entries for all ports to assume the value written. Implementation specific behavior shall occur for writes to routing table group entries if the contents of the Port n Routing Table Control CSRs are not the same for all ports .
22-31	___	All 0's	Reserved

*The Num_L0_Groups reset value is implementation dependent

†The L0_Group_Ptr reset value is implementation dependent

2.2.5 Broadcast Level 1 Info CSR (Block Offset 0x34)

This register shall communicate the location of the Broadcast Level 1 routing table group. When Three Levels is 0, this register is reserved. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-8. This register shall be read only.

Table 2-8. Bit Settings for Broadcast Level 1 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L1_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 1. Num_L1_Groups shall be encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L1_Group_Ptr	see footnote†	The L1_Group_Ptr value shall be the maintenance offset of the first entry in the first routing table group for level 1, divided by 1024. The maintenance offset of the first entry in the first routing group for level 1 shall be a 1024 byte aligned address. The L1_Group_Ptr value shall indicate an address in Implementation Defined register space. Writes to the broadcast routing table group entries pointed to by this register shall cause the corresponding routing table group entries for all ports to assume the value written. Implementation specific behavior shall occur for writes to routing table group entries if the contents of the Port n Routing Table Control CSRs are not the same for all ports .
22-31	___	All 0's	Reserved

*The Num_L1_Groups reset value is implementation dependent

†The L1_Group_Ptr reset value is implementation dependent

2.2.6 Broadcast Level 2 Info CSR (Block Offset 0x38)

This register shall communicate the location of the Level 2 routing table group for Port n. When Three Levels is 0, this register is reserved. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-9. This register shall be read only.

Table 2-9. Bit Settings for Broadcast Level 2 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L2_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 2. Num_L2_Groups shall be encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L2_Group_Ptr	see footnote†	The L2_Group_Ptr value shall be the maintenance offset of the first entry in the first broadcast routing table group for level 2, divided by 1024. The maintenance offset of the first entry in the first broadcast routing group for level 2 shall be a 1024 byte aligned address.The L2_Group_Ptr value shall indicate an address in Implementation Defined register space. Writes to the broadcast routing table group entries pointed to by this register shall cause the corresponding routing table group entries for all ports to assume the value written. Implementation specific behavior shall occur for writes to broadcast routing table group entries if the contents of the Port n Routing Table Control CSRs are not the same for all ports .
22-31	___	All 0's	Reserved

*The Num_L2_Groups reset value is implementation dependent

†The L2_Group_Ptr reset value is implementation dependent

2.2.7 Port n Routing Table Control CSR (Block Offset 0x40 + (0x20 * n))

This register shall control the routing mode for all ports whose Port n Level 0 Info CSR L0_Group_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-10. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-10. Bit Settings for Port n Routing Table Control CSR

Bit	Name	Reset Value	Description
0	Three Levels	0b1	0 - Routing table entries support a contiguous range of device IDS, starting with device ID 0x00/0x0000/0x00000000. 1 - Routing table entries support a hierarchical routing scheme
1	Dev32 Route Control	0b0	0 - Dev32 Device IDs are routed using Byte 0 for Level 0, Byte 1 for Level 1, and Byte 2 for Level 2 1 - Dev32 Device IDs are routed using Byte 1 for Level 0, Byte 2 for Level 1, and Byte 3 for level 2 Reserved if Three Levels is clear.

Table 2-10. Bit Settings for Port n Routing Table Control CSR

Bit	Name	Reset Value	Description
2-7	___		Reserved
8-15	Dev16 Level 1 Index	0b00	Index of the routing table group used to route the most significant byte of Dev16 device IDs. Reserved if Three Levels is clear.
16-23	___	0x00	Reserved
24-31	Dev8 Level2 Index	0b00	Index of the routing table group used to route Dev8 device IDs. Reserved if Three Levels is clear.

2.2.8 Port n Level 0 Info CSR (Block Offset 0x50 + (0x20 * n))

This register shall communicate the location of the Level 0 routing table group for Port n. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-11. This register shall be read only.

Table 2-11. Bit Settings for Port n Level 0 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L0_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 0. When Three Levels is 0, Num_L0_Groups shall communicate the number of groups available for routing. When Three Levels is 1, Num_L0_Groups shall be 1. Num_L0_Groups is encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L0_Group_Ptr	see footnote†	The L0_Group_Ptr value shall be the maintenance offset of the first entry in the first routing table group for level 0, divided by 1024. The maintenance offset of the first entry in the first routing group for level 0 shall be a 1024 byte aligned address. The L0_Group_Ptr value shall indicate an address in Implementation Defined register space. All ports with identical L0_Group_Ptr values shall have identical Level 0 routing behavior.
22-31	___	All 0's	Reserved

*The Num_L0_Groups reset value is implementation dependent

†The L0_Group_Ptr reset value is implementation dependent

2.2.9 Port n Level 1 Info CSR (Block Offset 0x54 + (0x20 * n))

This register shall communicate the location of the Level 1 routing table group for Port n. When the Three Levels of the Port n Routing Table Control CSR is 0, this register shall be reserved. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-12. This register shall be read only.

Table 2-12. Bit Settings for Port n Level 1 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L1_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 1. Num_L1_Groups shall be encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L1_Group_Ptr	see footnote†	The L0_Group_Ptr value shall be the maintenance offset of the first entry in the first routing table group for level 0, divided by 1024. The maintenance offset of the first entry in the first routing group for level 0 shall be a 1024 byte aligned address. The L1_Group_Ptr value shall indicate an address in Implementation Defined register space. All ports with identical L1_Group_Ptr values shall have identical Level 1 packet routing behavior.
22-31	___	All 0's	Reserved

*The Num_L1_Groups reset value is implementation dependent

†The L1_Group_Ptr reset value is implementation dependent

2.2.10 Port n Level 2 Info CSR (Block Offset 0x58 + (0x20 * n))

This register shall communicate the location of the Level 2 routing table group for Port n. When the Three Levels of the Port n Routing Table Control CSR is 0, this register shall be reserved. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-13. This register shall be read only.

Table 2-13. Bit Settings for Port n Level 2 Info CSR

Bit	Name	Reset Value	Description
0-7	Num_L2_Groups	see footnote*	Communicates the number of 256 entry routing table groups for Level 2. Num_L2_Groups shall be encoded as follows: 0x00 - 256 Groups 0x01 - 1 Group 0x02 - 2 Groups 0x03 - 3 Groups ... 0xFF - 255 Groups
8-21	L2_Group_Ptr	see footnote†	The L2_Group_Ptr value shall be the maintenance offset of the first entry in the first routing table group for level 2, divided by 1024. The maintenance offset of the first entry in the first routing group for level 2 shall be a 1024 byte aligned address.The L1_Group_Ptr value shall indicate an address in Implementation Defined register space. All ports with identical L2_Group_Ptr values shall have identical Level 2 routing behavior.
22-31	___	All 0's	Reserved

*The Num_L2_Groups reset value is implementation dependent

†The L2_Group_Ptr reset value is implementation dependent

2.3 Routing Table Group Register Format

A group of routing table entries consists of 256 consecutive registers. The L0_Group_Ptr, L1_Group_Ptr, and L2_Group_Ptr point to the first entry of the first group of a number of contiguous groups of register entries.

2.3.1 Broadcast Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0_Group_Ptr*0x400) + (x * 0x400) + (y*4))

Writes to the Broadcast Level 0 Group x Entry y Routing Table Entry CSRs shall cause the corresponding Port n Level 0 Group x Entry y Routing Table Entry CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-14. The bits and bit fields in this register are write only.

Table 2-14. Bit Settings for Broadcast Level 0 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Level 1 Group number 0x00 to 0xFF 0x300 - Drop Packet 0x301 - Use value found in Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number, Multicast Mask or Level 1 Group Number which does not exist in the device shall result in implementation specific behavior. When the Three Levels field of the Port n Routing Table Control CSR is clear, the values 0x200 through 0x2FF shall result in implementation specific routing behavior.

2.3.2 Broadcast Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1_Group_Ptr*0x400) + (x * 0x400) + (y*4))

Writes to the Broadcast Level 1 Group x Entry y Routing Table Entry CSRs shall cause the corresponding Port n Level 1 Group x Entry y Routing Table Entry CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-15. The bits and bit fields in this register are write only.

Table 2-15. Level 1 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Level 2 Group number 0x00 to 0xFF 0x300 - Drop Packet 0x301 - Use value found in Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number, Multicast Mask or Level 2 Group Number which does not exist in the device shall result in implementation specific behavior.

2.3.3 Broadcast Level 2 Group x Entry y Routing Table Entry CSR

(Offset = (L2_Group_Ptr*0x400) + (x * 0x400) + (y*4))

Writes to the Broadcast Level 2 Group x Entry y Routing Table Entry CSRs shall cause the corresponding Port n Level 2 Group x Entry y Routing Table Entry CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-16. The bits and bit fields in this register are write only.

Table 2-16. Bit Settings for Broadcast Level 2 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Reserved. 0x300 - Drop Packet 0x301 - Route packet using the Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number or Multicast Mask Number which does not exist in the device shall result in implementation specific behavior.

2.3.4 Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0_Group_Ptr*0x400) + (x * 0x400) + (y*4))

This register shall control the routing mode for all ports whose Port n Level 0 Info CSR L0_Group_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-17. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-17. Bit Settings for Level 0 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Level 1 Group number 0x00 to 0xFF 0x300 - Drop Packet 0x301 - Use value found in Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number, Multicast Mask or Level 1 Group Number which does not exist in the device shall result in implementation specific behavior. When the Three Levels field of the Port n Routing Table Control CSR is clear, the values 0x200 through 0x2FF shall result in implementation specific routing behavior.

2.3.5 Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1_Group_Ptr*0x400) + (x * 0x400) + (y*4))

This register shall control the routing mode for all ports whose Port n Level 1 Info CSR L1_Group_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-18. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-18. Bit Settings for Level 1 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Level 2 Group number 0x00 to 0xFF 0x300 - Drop Packet 0x301 - Use value found in Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number, Multicast Mask or Level 2 Group Number which does not exist in the device shall result in implementation specific behavior.

2.3.6 Level 2 Group x Entry y Routing Table Entry CSR

(Offset = (L2_Group_Ptr*0x400) + (x * 0x400) + (y*4))

This register shall control the routing mode for all ports whose Port n Level 2 Info CSR L2_Group_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-19. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-19. Bit Settings for Level 2 Group x Entry y Routing Table Entry CSR

Bit	Name	Reset Value	Description
0-21	___		Reserved
22-31	Routing Value	0x300	Routing table entry 0x000 to 0x0FF - Egress Port Number 0x00 to 0xFF 0x100 to 0x1FF - Multicast Mask Number 0x00 to 0xFF. Refer to Part 11. 0x200 to 0x2FF - Reserved. 0x300 - Drop Packet 0x301 - Route packet using the Standard Port Default Route CSR 0x302 to 0x3FF - Reserved. Selection of an Egress Port Number or Multicast Mask Number which does not exist in the device shall result in implementation specific behavior.

“

Add the following new section to Part 3 to illustrate the Dev32 hierarchical programming model:

“

2.4 Dev32 Configuration Examples

This chapter provides several examples of how to use the Dev32 routing table programming interface. The given examples build upon each other while proceeding through the sections. References to the order of operations within the examples run from the top of a list to the bottom unless otherwise stated.

Initially assume a switch with 16 ports which supports Dev32 device IDs. Assume that the switch must support the following routing hierarchy, where “**” means “All Values”:

- Device ID 0x00_11_20_** must be routed to port 14.
- Device IDs 0x00_11_0X_** must be routed to port X, where X is 0 to 13.
- Device IDs 0x00_ZZ_**_** must be routed to port 15 when ZZ is 0 to 0x10.
- All other packets must be dropped.

Further assume that Port 7 must be programmed to support the above hierarchy, and has

initial register values as follows:

Table 2-20. Example Port 7 Routing Table Register Block Registers

Register Name	Register Address	Register Value
Switch Routing Table Register Block Header	0x8000	N/A
Port 7 Routing Control CSR	0x8140	0x8000_0000
Port 7 Level 0 Info CSR	0x8150	0x0107_0000
Port 7 Level 1 Info CSR	0x8154	0x0107_0400
Port 7 Level 2 Info CSR	0x8158	0x0107_0C00

2.4.1 Example 1: Routing 0x00_11_20_** to Port 14

To route the Dev32 destination IDs 0x00_11_20_** to Port 14, make use of routing table group 0 for Level 0, Level 1, and Level 2. Specific entries for each level must be programmed.

Table 2-21. Example 1 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 0 Group 0 Entry 0 Routing Table Entry CSR	0x0007_0000	0x0000_0200	Map Level 0 Group 0 value 0x00 to Level 1 Group 0
Port 7 Level 1 Group 0 Entry 0x11 Routing Table Entry CSR	0x0007_0444	0x0000_0200	Map Level 1 Group 0 value 0x11 to Level 2 Group 0
Port 7 Level 2 Group 0 Entry 0x20 Routing Table Entry CSR	0x0007_0C80	0x0000_000E	Map Level 2 Group 0 value 0x20 to Port 14.

2.4.2 Example 2: Routing 0x00_11_0X_** to Port X

This example builds upon the configuration put in place by Example 1. Routing configuration is therefore complete for Level 0 and Level 1, so what remains is to complete the Level 2 programming.

Table 2-22. Example 2 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 2 Group 0 Entry 0x00 Routing Table Entry CSR	0x0007_0C00	0x0000_0000	Map Level 2 Group 0 value 0x00 to Port 0.
Port 7 Level 2 Group 0 Entry 0x01 Routing Table Entry CSR	0x0007_0C04	0x0000_0001	Map Level 2 Group 0 value 0x01 to Port 1.
Port 7 Level 2 Group 0 Entry 0x02 Routing Table Entry CSR	0x0007_0C08	0x0000_0002	Map Level 2 Group 0 value 0x02 to Port 2.
Port 7 Level 2 Group 0 Entry 0x03 Routing Table Entry CSR	0x0007_0C0C	0x0000_0003	Map Level 2 Group 0 value 0x03 to Port 3.
Port 7 Level 2 Group 0 Entry 0x04 Routing Table Entry CSR	0x0007_0C10	0x0000_0004	Map Level 2 Group 0 value 0x04 to Port 4.

Table 2-22. Example 2 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 2 Group 0 Entry 0x05 Routing Table Entry CSR	0x0007_0C14	0x0000_0005	Map Level 2 Group 0 value 0x05 to Port 5.
Port 7 Level 2 Group 0 Entry 0x06 Routing Table Entry CSR	0x0007_0C18	0x0000_0006	Map Level 2 Group 0 value 0x06 to Port 6.
Port 7 Level 2 Group 0 Entry 0x07 Routing Table Entry CSR	0x0007_0C1C	0x0000_0007	Map Level 2 Group 0 value 0x07 to Port 7.
Port 7 Level 2 Group 0 Entry 0x08 Routing Table Entry CSR	0x0007_0C20	0x0000_0008	Map Level 2 Group 0 value 0x08 to Port 8.
Port 7 Level 2 Group 0 Entry 0x09 Routing Table Entry CSR	0x0007_0C24	0x0000_0009	Map Level 2 Group 0 value 0x09 to Port 9.
Port 7 Level 2 Group 0 Entry 0x0A Routing Table Entry CSR	0x0007_0C28	0x0000_000A	Map Level 2 Group 0 value 0x0A to Port A.
Port 7 Level 2 Group 0 Entry 0x0B Routing Table Entry CSR	0x0007_0C2C	0x0000_000B	Map Level 2 Group 0 value 0x0B to Port B.
Port 7 Level 2 Group 0 Entry 0x0C Routing Table Entry CSR	0x0007_0C30	0x0000_000C	Map Level 2 Group 0 value 0x0C to Port C.
Port 7 Level 2 Group 0 Entry 0x0D Routing Table Entry CSR	0x0007_0C34	0x0000_000D	Map Level 2 Group 0 value 0x0D to Port D.

2.4.3 Example 3: Routing 0x00_ZZ_**_** to Port 15, ZZ=[0,0x10]

This example builds upon the configuration put in place by Example 1. Routing configuration is therefore complete for Level 0, so what remains is to complete the Level 1 programming.

Table 2-23. Example 3 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 1 Group 0 Entry 0x00 Routing Table Entry CSR	0x0007_0400	0x0000_000F	Map Level 1 Group 0 value 0x00 to Port 15.
Port 7 Level 1 Group 0 Entry 0x01 Routing Table Entry CSR	0x0007_0404	0x0000_000F	Map Level 1 Group 0 value 0x01 to Port 15.
Port 7 Level 1 Group 0 Entry 0x02 Routing Table Entry CSR	0x0007_0408	0x0000_000F	Map Level 1 Group 0 value 0x02 to Port 15.
Port 7 Level 1 Group 0 Entry 0x03 Routing Table Entry CSR	0x0007_040C	0x0000_000F	Map Level 1 Group 0 value 0x03 to Port 15.
Port 7 Level 1 Group 0 Entry 0x04 Routing Table Entry CSR	0x0007_0410	0x0000_000F	Map Level 1 Group 0 value 0x04 to Port 15.
Port 7 Level 1 Group 0 Entry 0x05 Routing Table Entry CSR	0x0007_0414	0x0000_000F	Map Level 1 Group 0 value 0x05 to Port 15.

Table 2-23. Example 3 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 1 Group 0 Entry 0x06 Routing Table Entry CSR	0x0007_0418	0x0000_000F	Map Level 1 Group 0 value 0x06 to Port 15.
Port 7 Level 1 Group 0 Entry 0x07 Routing Table Entry CSR	0x0007_041C	0x0000_000F	Map Level 1 Group 0 value 0x07 to Port 15.
Port 7 Level 1 Group 0 Entry 0x08 Routing Table Entry CSR	0x0007_0420	0x0000_000F	Map Level 1 Group 0 value 0x08 to Port 15.
Port 7 Level 1 Group 0 Entry 0x09 Routing Table Entry CSR	0x0007_0424	0x0000_000F	Map Level 1 Group 0 value 0x09 to Port 15.
Port 7 Level 1 Group 0 Entry 0x0A Routing Table Entry CSR	0x0007_0428	0x0000_000F	Map Level 1 Group 0 value 0x0A to Port 15.
Port 7 Level 1 Group 0 Entry 0x0B Routing Table Entry CSR	0x0007_042C	0x0000_000F	Map Level 1 Group 0 value 0x0B to Port 15.
Port 7 Level 1 Group 0 Entry 0x0C Routing Table Entry CSR	0x0007_0430	0x0000_000F	Map Level 1 Group 0 value 0x0C to Port 15.
Port 7 Level 1 Group 0 Entry 0x0D Routing Table Entry CSR	0x0007_0434	0x0000_000F	Map Level 1 Group 0 value 0x0D to Port 15.
Port 7 Level 1 Group 0 Entry 0x0E Routing Table Entry CSR	0x0007_0438	0x0000_000F	Map Level 1 Group 0 value 0x0E to Port 15.
Port 7 Level 1 Group 0 Entry 0x0F Routing Table Entry CSR	0x0007_043C	0x0000_000F	Map Level 1 Group 0 value 0x0F to Port 15.
Port 7 Level 1 Group 0 Entry 0x10 Routing Table Entry CSR	0x0007_0440	0x0000_000F	Map Level 1 Group 0 value 0x10 to Port 15.

2.4.4 Example 4: All Other Packets Must Be Dropped

This example builds upon the configuration put in place by Example 3. Routing for Dev32 device IDs has been configured. What remains is to ensure the Dev8 and Dev16 deviceIDs are dropped..

Table 2-24. Example 4 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Routing Control CSR	0x0000_8120	0x8001_0001	Map Dev16 device IDs to Level 1 Group 1. Map Dev8 device IDs to Level 2 Group 1.

2.4.5 Example 5: Flat Routing Table Operation

This example illustrates the “flat” programming model, in which device IDs are supported sequentially by the routing tables. Dev16 device IDs of the form 0x00** are treated as Dev8 device IDs.

Initially assume a switch with 16 ports which supports Dev32 device IDs. Assume that the switch must support the following routing hierarchy, where “**” means “All Values”:

- Device ID 0x01_20 must be routed to port 14.
- Device IDs 0x00_0X must be routed to port X, where X is 0 to 13.
- Device IDs 0x02_00 and 0x03_00 must be routed to port 15.
- All other packets must be dropped.

Further assume that Port 7 must be programmed to support the above hierarchy, and has initial register values as follows:

Table 2-25. Example 5 Port 7 Routing Table Register Block Registers

Register Name	Register Address	Register Value
Switch Routing Table Register Block Header	0x8000	N/A
Port 7 Routing Control CSR	0x8120	0x8000_0000
Port 7 Level 0 Info CSR	0x8130	0x0107_0000
Port 7 Level 1 Info CSR	0x8134	0x0107_0400
Port 7 Level 2 Info CSR	0x8138	0x0107_0C00

The following register accesses must be performed:

Table 2-26. Example 5 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Routing Control CSR	0x0000_8120	0x0000_0000	Change to Flat Routing Table Model
Port 7 Level 0 Info CSR	0x0000_8130	0x0407_0000	Read Level 0 Info to determine how many DeviceIDs are supported. Four groups are supported, or destIDs 0x0000 through 0x03FF.
Port 7 Level 1 Info CSR	0x0000_8134	0x0000_0000	Read Level 1 Info, confirm register is reserved
Port 7 Level 2 Info CSR	0x0000_8138	0x0000_0000	Read Level 2 Info, confirm register is reserved
Port 7 Level 0 Group 1 Entry 0x20	0x0007_0480	0x0000_000E	Route DestID 0x0120 to port 14.
Port 7 Level 0 Group 0 Entry 0x00	0x0007_0000	0x0000_0000	Route DestID 0x0000 to port 0.
Port 7 Level 0 Group 0 Entry 0x01	0x0007_0004	0x0000_0001	Route DestID 0x0001 to port 1.
Port 7 Level 0 Group 0 Entry 0x02	0x0007_0008	0x0000_0002	Route DestID 0x0002 to port 2.
Port 7 Level 0 Group 0 Entry 0x03	0x0007_000C	0x0000_0003	Route DestID 0x0003 to port 3.
Port 7 Level 0 Group 0 Entry 0x04	0x0007_0010	0x0000_0004	Route DestID 0x0004 to port 4.
Port 7 Level 0 Group 0 Entry 0x05	0x0007_0014	0x0000_0005	Route DestID 0x0005 to port 5.
Port 7 Level 0 Group 0 Entry 0x06	0x0007_0018	0x0000_0006	Route DestID 0x0006 to port 6.

Table 2-26. Example 5 Accesses

Register Name	Register Address	Register Value	Description
Port 7 Level 0 Group 0 Entry 0x07	0x0007_001C	0x0000_0007	Route DestID 0x0007 to port 7.
Port 7 Level 0 Group 0 Entry 0x08	0x0007_0020	0x0000_0008	Route DestID 0x0008 to port 8.
Port 7 Level 0 Group 0 Entry 0x09	0x0007_0024	0x0000_0009	Route DestID 0x0009 to port 9.
Port 7 Level 0 Group 0 Entry 0x0A	0x0007_0028	0x0000_000A	Route DestID 0x000A to port 10.
Port 7 Level 0 Group 0 Entry 0x0B	0x0007_002C	0x0000_000B	Route DestID 0x000B to port 11.
Port 7 Level 0 Group 0 Entry 0x0C	0x0007_0030	0x0000_000C	Route DestID 0x000C to port 12.
Port 7 Level 0 Group 0 Entry 0x0D	0x0007_0034	0x0000_000D	Route DestID 0x000D to port 13.
Port 7 Level 0 Group 2 Entry 0x00	0x0007_0800	0x0000_000F	Route DestID 0x0200 to port 15.
Port 7 Level 0 Group 3 Entry 0x00	0x0007_0C00	0x0000_000F	Route DestID 0x0300 to port 15.

“

Change the Part 11 Registers section as follows:

Add “This register shall not be implemented if Bit 20 of the Processing Element Features CAR is set.” to the start of the description of the following registers:

3.3 Switch Multicast Support CAR
3.4 Switch Multicast Information CAR
3.5 Multicast Mask Port CSR
3.6 Multicast Associate Select CSR
3.7 Multicast Associate Operation CSR

Add a new register block to Part 11 Multicast as follows:

“

2.5 Switch Routing Table Register Block

A switch device which has bits 20 and 21 set in the Processing Element Features CAR shall implement this register block. Note that this definition is a refinement of the Switch Routing Table Register block defined in Part 3 Transport Specification.

2.5.1 Register Map

The register map for the routing table registers shall be as specified by Table 1-27. This register map is currently only defined for devices with up to 16 RapidIO ports, but can be extended or shortened if more or less port definitions are required for a device. For example, a device with four RapidIO ports is only required to use register map space corresponding to offsets [EF_PTR+0x00] through [EF_PTR+0xBC]. Register map offset [EF_PTR+0x140] can be used for another Extended Features block.

Table 2-27. Switch Routing Table Register Map

	Block Byte Offset	Register Name
General	0x0	Routing Table Register Block Header
	0x4-0x1C	Reserved
Broadcast	0x20	Broadcast Routing Table Control CSR
	0x24	Reserved
	0x28	Broadcast Multicast Info CSR
	0x2C-0x3C	Reserved
Port 0	0x40	Port 0 Routing Table Control CSR
	0x44	Reserved
	0x48	Port 0 Multicast Info CSR
	0x4C-0x5C	Reserved
Port 1	0x60	Port 1 Routing Table Control CSR
	0x64	Reserved
	0x68	Port 1 Multicast Info CSR
	0x6C-0x7C	Reserved
Ports 2-14	0x80–21C	Assigned to Port 2-14 CSRs

Table 2-27. Switch Routing Table Register Map

	Block Byte Offset	Register Name
Port 15	0x220	Port 15 Routing Table Control CSR
	0x224	Reserved
	0x228	Port 15 Multicast Info CSR
	0x22C-0x23C	Reserved

2.5.2 Broadcast Routing Table Control CSR (Block Offset 0x20)

The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-28. Unless otherwise specified, the bits and bit fields in this register are write only.

Table 2-28. Bit Settings for Broadcast Routing Table Control CSR

Bit	Name	Reset Value	Description
0-5	___		Reserved
6-7	Mask_size	see footnote*	A multicast mask shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register (8 bytes) 0b01 - Two set registers, two clear registers (16 bytes) 0b10 - Four set registers, four clear registers (32 bytes) 0b11 - Eight set registers, eight clear registers (64 bytes) This bit field shall be read only.
8-31	___		Reserved

*The Mask_size reset value is implementation dependent

The following illustrates the arrangement of Multicast Mask x Set/Clear Register y CSRs for various Mask_size values.

Table 2-29. Mask 0-7 Set/Clear Registers, Mask_size = 0

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Clear Register 0	0x000004
Multicast Mask 1 Set Register 0	0x000008
Multicast Mask 1 Clear Register 0	0x00000C

Table 2-29. Mask 0-7 Set/Clear Registers, Mask_size = 0

Register Name	Offset
Multicast Mask 2 Set Register 0	0x000010
Multicast Mask 2 Clear Register 0	0x000014
Multicast Mask 3 Set Register 0	0x000018
Multicast Mask 3 Clear Register 0	0x00001C
Multicast Mask 4 Set Register 0	0x000020
Multicast Mask 4Clear Register 0	0x000024
Multicast Mask 5 Set Register 0	0x000028
Multicast Mask 5 Clear Register 0	0x00002C
Multicast Mask 6 Set Register 0	0x000030
Multicast Mask 6 Clear Register 0	0x000034
Multicast Mask 7 Set Register 0	0x000038
Multicast Mask 7 Clear Register 0	0x00003C

Table 2-30. Mask 0-3 Set/Clear Registers, Mask_size = 1

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Clear Register 0	0x000008
Multicast Mask 0 Clear Register 1	0x00000C
Multicast Mask 1 Set Register 0	0x000010
Multicast Mask 1 Set Register 1	0x000014
Multicast Mask 1 Clear Register 0	0x000018
Multicast Mask 1 Clear Register 1	0x00001C
Multicast Mask 2 Set Register 0	0x000020
Multicast Mask 2 Set Register 1	0x000024
Multicast Mask 2 Clear Register 0	0x000028
Multicast Mask 2 Clear Register 1	0x00002C
Multicast Mask 3 Set Register 0	0x000030
Multicast Mask 3 Set Register 1	0x000034
Multicast Mask 3 Clear Register 0	0x000038
Multicast Mask 3 Clear Register 1	0x00003C

Table 2-31. Mask 0-1 Set/Clear Registers, Mask_size = 2

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Set Register 2	0x000010
Multicast Mask 0 Set Register 3	0x000014
Multicast Mask 0 Clear Register 0	0x000008
Multicast Mask 0 Clear Register 1	0x00000C
Multicast Mask 0 Clear Register 2	0x000018
Multicast Mask 0 Clear Register 3	0x00001C
Multicast Mask 1 Set Register 0	0x000020
Multicast Mask 1 Set Register 1	0x000024
Multicast Mask 1 Set Register 2	0x000028
Multicast Mask 1 Set Register 3	0x00002C
Multicast Mask 1 Clear Register 0	0x000030
Multicast Mask 1 Clear Register 1	0x000034
Multicast Mask 1 Clear Register 2	0x000038
Multicast Mask 1 Clear Register 3	0x00003C

Table 2-32. Mask 0 Set/Clear Registers, Mask_size = 3

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Set Register 2	0x000010
Multicast Mask 0 Set Register 3	0x000014
Multicast Mask 0 Set Register 4	0x000008
Multicast Mask 0 Set Register 5	0x00000C
Multicast Mask 0 Set Register 6	0x000018
Multicast Mask 0 Set Register 7	0x00001C
Multicast Mask 0 Clear Register 0	0x000020
Multicast Mask 0 Clear Register 1	0x000024
Multicast Mask 0 Clear Register 2	0x000028
Multicast Mask 0 Clear Register 3	0x00002C
Multicast Mask 0 Clear Register 4	0x000030
Multicast Mask 0 Clear Register 5	0x000034
Multicast Mask 0 Clear Register 6	0x000038
Multicast Mask 0 Clear Register 7	0x00003C

2.5.3 Broadcast Multicast Info CSR (Block Offset 0x28)

This register shall communicate the location of the Broadcast Multicast Mask 0 Set Register 0 CSR. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-33. This register shall be read only.

Table 2-33. Bit Settings for Broadcast Multicast Info CSR

Bit	Name	Reset Value	Description
0-7	Num_Masks	see footnote*	Num_Masks shall indicate the number of Broadcast Multicast Masks, encoded as follows: 0x00 - 256 Masks 0x01 - 1 Masks 0x02 - 2 Masks 0x03 - 3 Masks ... 0xFF - 255 Masks
8-21	Mask_Ptr	see footnote†	The Mask_Ptr value shall be the maintenance offset of the Broadcast Multicast Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Broadcast Multicast Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The Mask_Ptr value shall indicate an address in Implementation Defined register space. Writes to the Broadcast Multicast Mask registers pointed to by this register shall cause the corresponding Port n Multicast Mask registers for all ports to assume the value written.
22-31	___	0b00	Reserved

*The Num_Masks reset value is implementation dependent

†The Mask_Ptr reset value is implementation dependent

2.5.4 Port n Routing Table Control CSR (Block Offset 0x40 + (0x20 * n))

This register shall indicate the number of registers in a multicast mask for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-34. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-34. Bit Settings for Port n Routing Table Control CSR

Bit	Name	Reset Value	Description
0-5	___		Reserved
6-7	Mask_size	see footnote*	A multicast mask shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register (8 bytes) 0b01 - Two set registers, two clear registers (16 bytes) 0b10 - Four set registers, four clear registers (32 bytes) 0b11 - Eight set registers, eight clear registers (64 bytes) This bit field shall be read only.
8-31	___		Reserved

*The Mask_size reset value is implementation dependent

2.5.5 Port n Multicast Info CSR (Block Offset 0x28 + 20 * n)

This register shall communicate the location of Port n Multicast Mask 0 Register 0 CSR. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-35. This register shall be read only.

Table 2-35. Bit Settings for Port n Multicast Info CSR

Bit	Name	Reset Value	Description
0-7	Num_Masks	see footnote*	Communicates the number of multicast masks for this port. Num_Masks is encoded as follows: 0x00 - 256 Masks 0x01 - 1 Masks 0x02 - 2 Masks 0x03 - 3 Masks ... 0xFF - 255 Masks
8-21	Mask_Ptr	see footnote†	The Mask_Ptr value shall be the maintenance offset of the Port n Multicast Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Port n Multicast Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The Mask_Ptr value shall indicate an address in Implementation Defined register space.
22-31	___	0b00	Reserved

*The Num_Masks reset value is implementation dependent

†The Mask_Ptr reset value is implementation dependent

2.5.6 Broadcast Multicast Mask x Set Register y CSR

(Offset = (Mask_Ptr * 0x400) + (x*8*2^{Mask_size}) + (y*4))

Writes to the Broadcast Multicast Mask x Set Register y CSRs shall cause the corresponding Port n Multicast Mask x Set Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-36. Unless otherwise specified, the bits and bit fields in this register are write only.

Table 2-36. Bit Settings for Broadcast Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which ports do and do not receive packets when routed according to this multicast mask. The multicast mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to ports sequentially as the port number increases. The lowest numbered port shall be assigned to Bit 31. Each bit shall be encoded as follows: 0b0 - Do not multicast to this port 0b1 - Multicast to this port Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to ports which do not exist in the device shall be reserved.

2.5.7 Broadcast Multicast Mask x Clear Register y CSR (Offset = (Mask_Ptr * 0x400) + (x * 8*2^{Mask_size}) + (4*2^{Mask_size}) + (y*4))

Writes to the Broadcast Multicast Mask x Clear Register y CSRs shall cause the corresponding Port n Multicast Mask x Clear Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-37. Unless otherwise specified, the bits and bit fields in this register are write only.

Table 2-37. Bit Settings for Broadcast Multicast Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which ports do and do not receive messages when routed according to this multicast mask. The multicast mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to ports sequentially as the port number increases. The lowest numbered port shall be assigned to Bit 31. Reading this register returns the current multicast value for the assigned ports. Each bit shall be encoded as follows: 0b0 - Do not multicast to this port 0b1 - Multicast to this port Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to ports which do not exist in the device shall be reserved.

2.5.8 Port n Multicast Mask x Set Register y CSR (Offset = (Mask_Ptr * 4) + (x * 8*2^{Mask_size}) + (y*4))

This register shall control the multicast behavior for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-38. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-38. Bit Settings for Port n Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which ports do and do not receive messages when routed according to this multicast mask. The multicast mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to ports sequentially as the port number increases. The lowest numbered port shall be assigned to Bit 31. Reading this register returns the current multicast value for the assigned ports. Each bit shall be encoded as follows: 0b0 - Do not multicast to this port 0b1 - Multicast to this port Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to ports which do not exist in the device shall be reserved.

2.5.9 Port n Multicast Mask x Clear Register y CSR (Offset = (Mask_Ptr * 4) + (x * 8*2^{Mask_size}) + (4*2^{Mask_size}) + (y*4))

This register shall control the multicast behavior for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 1-39. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 2-39. Bit Settings for Port n Multicast Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which ports do and do not receive messages when routed according to this multicast mask. The multicast mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to ports sequentially as the port number increases. The lowest numbered port shall be assigned to Bit 31. Reading this register returns the current multicast value for the assigned ports. Each bit shall be encoded as follows: 0b0 - Do not multicast to this port 0b1 - Multicast to this port Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to ports which do not exist in the device shall be reserved.