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TWG Second Showing

Item 12-08-00000.002

Subject: Revision 3.0 specification Retimer functional description

Background: This showing proposes how the description of Retimers must change for 10xN lane speeds.

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Comment Expiration Date: None

Distribution: RapidIO TA Technical Working Group members

1.0 Discussion

Retimers have always been supported by the RapidIO specification. With the specification of the 10xN lane speed and the associated PCS and PMA, retimer functionality has become more complex. This showing proposes changes to the definition of retimers to reflect this increase in complexity.

For the most part, the operation of 10xN retimers is identical to that of Gen1 and Gen2 retimers. Like Gen1 and Gen2 retimers, 10xN retimers do have a local transmit clock, and so must be aware of clock compensation. This implies that retimers can insert or remove Skip codewords from Skip ordered sequences. However, selective codeword inversion rules apply to Skip codewords. The addition or removal of a Skip control word can change the disparity for all following codewords. This implies that 10xN retimers must also be aware of selective codeword inversion, and may change the "Inverted" bit of the received bit stream based on codeword disparity.

The retimer description also does not use "shall" to identify required behavior. This proposal includes changes to use "shall" to identify required behavior.

1.1 Changes

Propose changing part 6, section 5.14.1 , on page 181 from:

"A retimer shall comply with all applicable AC specifications found in Chapter 12, "Electrical Specification for 10.3125 Gbaud LP-Serial Links". This includes resetting the jitter budget thus extending the transmission distance for the link. The retimer repeats the received codewords after performing codeword synchronization and serializes the bitstream again on transmission, based on a local clock reference.

Up to two retimers are allowed between two end nodes. A retimer is not RapidIO protocol-aware or addressable in any way. The only awareness a retimer has is to the synchronization on the /K/ code-group and the function of /R/ insertion and removal. A retimer may insert up to one /R/ code-group immediately following a /K/ code-group, or remove one /R/ code-group that immediately follows a /K/ code-group. Since the /R/ code-group is disparity neutral, its insertion or deletion does not affect the running disparity.

A N-lane retimer must perform lane synchronization and deskew, in exactly the same way a RapidIO device implementing this physical layer does when synchronizing inputs during initialization and startup. A Nx mode retimer will synchronize and align all lanes that are driven to it. Therefore, such a retimer allows for the degradation of an input Nx link to a 1x link on either lane 0 or R. If any link drops out, the retimer must merely continue to pass the active links, monitoring for the compensation sequence and otherwise passing through whatever codewords appear on its inputs. A retimer may optionally not drive any outputs whose corresponding inputs are not active.

Any insertion or removal of a Skip codewords in a N-lane retimer must be done on a full column. A retimer may retime links operating at the same width only (i.e. cannot connect a link operating at 1x to a link operating at Nx). A retimer may connect a 1x link to a Nx link that is operating in 1x mode. Retimers perform clock tolerance compensation between the receive and transmit clock. The transmit clock is usually derived from a local reference.

Retimers do not check for code violations. Codewords received on one port are transmitted on the other regardless of code violations."

to:

"A retimer shall comply with all applicable AC specifications found in Chapter 12, "Electrical Specification for 10.3125 Gbaud LP-Serial Links". Retimers shall reset the jitter budget thus extending the transmission distance for the link. A RapidIO link shall support a maximum of two retimers.

A retimer is aware of the PMA encoding of RapidIO. The retimer is otherwise unaware of the RapidIO protocol. The retimer has no registers that can be accessed from RapidIO. A retimer shall perform codeword synchronization and selective codeword inversion on the received bit stream, and shall repeat the received codewords after serializing the bitstream and performing selective codeword inversion again on transmission.

Retimers may use a transmit clock derived from a local reference. Retimers shall perform clock tolerance compensation between the received bit stream and transmitted bit stream. A retimer is aware of the Skip ordered sequence and the function of Skip codeword insertion and removal. A retimer may insert up to one Skip codeword immediately following a Skip Marker codeword, or remove one Skip codeword that immediately follows a Skip Marker codeword. Insertion or removal of a Skip codeword can affect the running disparity of the lane, so the retimer shall implement selective codeword inversion. Any insertion or removal of Skip codewords in a N-lane retimer shall be done on a full column.

A N-lane retimer shall perform lane synchronization and deskew, in exactly the same way a RapidIO device implementing this physical layer does when synchronizing inputs during initialization and startup. A Nx mode retimer shall synchronize and align all lanes that are driven to it. Therefore, such a retimer shall support the degradation of an input Nx link to a 1x link on either lane 0 or R. If any link drops out, the retimer shall continue to pass the active links, monitoring for the compensation sequence and otherwise passing through whatever codewords appear on its inputs. A retimer may optionally not drive any outputs whose corresponding inputs are not active.

A retimer shall only retime links operating at the same width (i.e. cannot connect a link operating at 1x to a link operating at Nx). A retimer may connect a 1x link to a Nx link that is operating in 1x mode.

Retimers shall not check for code violations. Codewords received on one port shall be transmitted on the other regardless of code violations."