RapidIO™ Interconnect Specification Part 11: Multicast and Port Aggregation Group Extensions Specification

4.1, 6/2017

RapidIO.org

Revision History

Revision	Description	Date
1.3	First release	06/09/2004
1.3.1	Technical changes: the following new features showings: 04-08-00015.003 Converted to ISO-friendly templates	02/23/2005
2.0	Technical changes: errata showing 06-02-00001.005	06/14/2007
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3.0	Changed RTA contact information. Technical Changes: Addition of standard register block to support Dev32 multicast programming model. Note that if Dev32 is supported, some registers are deprecated.	10/11/2013
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4.1	Addition of Port Aggregation Group behavior definition and programming model.	06/30/2017

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Chapter 1 Overview

1.1 Introduction

This chapter provides an overview of the *RapidIO Part 11: Multicast and PAG Extensions Specification*. The goal of this specification is to add a simple mechanism to the existing RapidIO specifications that provides multicast and port aggregation functionality to a system. This specification assumes that the reader has a working understanding of the other RapidIO specifications.

Implementation of this specification is optional. Devices which implement multicast functionality may optionally implement port aggregation functionality. Devices which implement port aggregation functionality shall implement multicast functionality sufficient to support port aggregation.

1.2 Overview

The concept of duplicating a single message and sending it to multiple selected destinations is known as ‘multicast’, and is found to be useful in many computing systems. This can be accomplished by a variety of means. The most efficient and highest performance method is to have hardware support for the duplication of messages.

Port aggregation is the ability to treat multiple physical ports as a single logical port. When port aggregation is used to route a packet, one physical port out of a set of physical ports is selected as the output port for a packet. Different port selection algorithms provide different user value. Commonly port aggregation employs a port selection algorithm that minimizes congestion for individual physical ports, thus balancing bandwidth utilization among multiple physical ports. Another common port aggregation use case is automatic fail over from one physical port to another in the event that the first physical port fails.

Within a RapidIO system, the ability to duplicate and/or distribute messages should scale with the number of end points in a system. Since the number of end points scales with the number of switches in the system, the multicast and port aggregation extensions are defined for switches only and end points are largely unaffected. Possible end point design considerations are described in Annex A.

The multicast specification is limited to request transactions that do not require responses, for example, *RapidIO Part 1: Input/Output Logical Specification*

SWRITE transactions. This is because implementing support for collecting the response transactions within a switch device, which are typically not aware of RapidIO logical layer protocols, is problematic and complex. Port aggregation may be used for any request or response transaction type.

The ability for a switch to send a single message to a variety of destinations can be implemented in a wide variety of ways, depending on system needs. There are two reasons, however, that motivate definition of a common interface and behavior for multicast and port aggregation in a system. Without a standard interface and behavioral definition, the wide variety of possible implementations would not allow a common multicast and port aggregation software driver to exist. The second reason is that without a standard definition for interface and behavior it is impossible to guarantee inter-interoperability of different components which support multicast and/or port aggregation.

In defining a common interface for a wide variety of implementations, it is necessary to define the standard interface with some level of abstraction in order to avoid limiting implementation flexibility. Therefore, several examples of the use of the interface have been included.

1.3 Requirements

The multicast and port aggregation mechanisms shall fulfill the following goals:

- Simple - excess complexity will not gain acceptance
- Compact - Does not cost excessive silicon area in a switch
- Robust - same level of protection and recovery as the rest of RapidIO
- Scalable - must be able to extend to multi-layer switch systems
- Compatibility with all physical layers

Chapter 2 Multicast Extensions Behavior

2.1 Introduction

This chapter describes the multicast extensions rules of operation in a RapidIO system. A RapidIO switch which does not support multicast can co-exist in a RapidIO fabric with other switches that do support multicast. The only requirement is that the switch be capable of routing the destination IDs used for multicast transactions.

2.2 Packet Replication

A RapidIO multicast operation consists of the replication of a single packet so that it can be received by multiple end points. This replication is performed by the switch devices in the fabric rather than by the end point itself, so that the capability to replicate packets expands with the number of switches (and hence possible end points) in a system. Each switch may be individually programmed to control which egress ports of the switch the replicated packets are sent to, and thus indirectly which specific set of end point devices receive the replicated packet. The packets themselves are not modified by the replication process, merely transmitted out through the appropriate ports.

This specification only addresses multicasting request packets for transactions which do not require responses. This greatly simplifies multicast support for RapidIO switches, which will therefore have no need to aggregate responses from other types of RapidIO operations. Examples of transactions which can be multicast are I/O logical specification NWRITE and SWRITE transactions. Multicasting transactions which require responses have implementation defined behavior.

2.3 Multicast Operation

Multicast operations have two control value types - **multicast masks** and **multicast groups**. The set of target end points which all receive a particular multicast packet is known as a **multicast group**. Each multicast group is associated with a unique destination ID. The destination ID of a received packet allows a RapidIO switch device to determine that a packet is to be replicated for a multicast.

A **multicast mask** is a value that controls which egress ports one or more multicast groups are associated with. Conceptually, a multicast mask is a register with one

enable bit for each possible switch egress port. There is one set of multicast masks for the entire switch. All multicast masks in a switch are assigned unique sequential ID numbers beginning with 0. Figure 2-1 shows an example of the use of multicast in a RapidIO system.

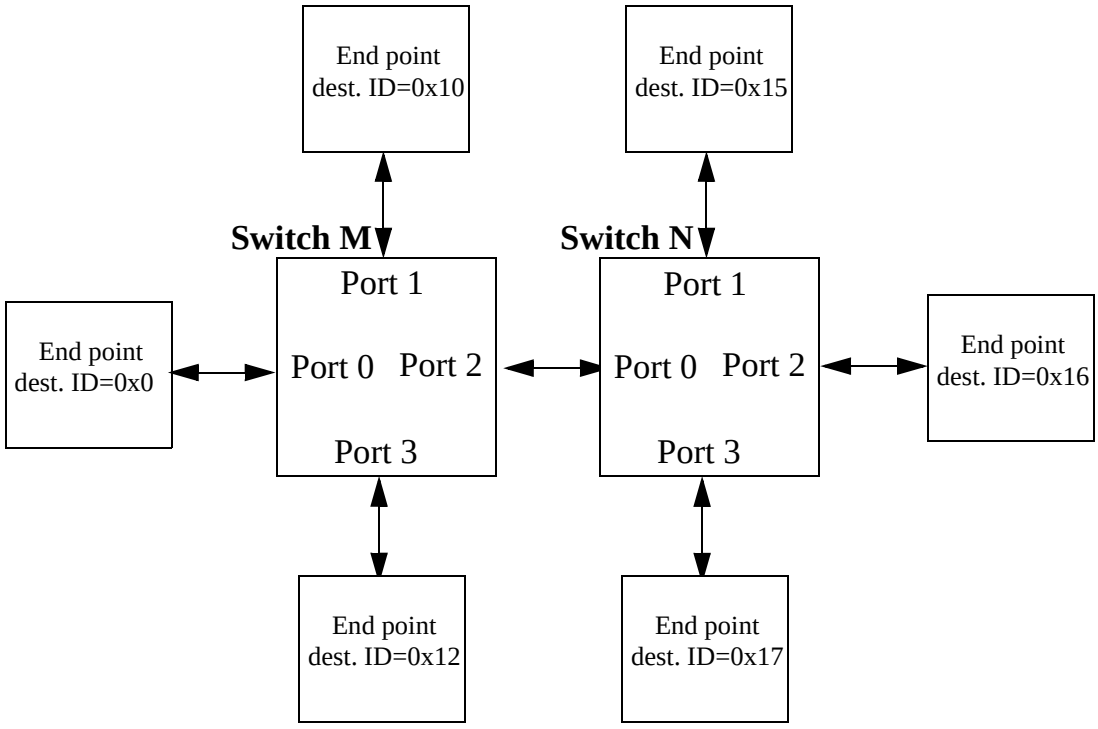

Figure 2-1. Multicast System Example

In this example, the end point assigned destination ID 0x0 uses destination ID 0x80 to perform multicast operations to the multicast group comprised of end points 0x10, 0x15, 0x16, and 0x17, arbitrarily called group A. Software configures the switch devices in the fabric to **associate** the destination IDs that represent multicast groups with multicast masks. For Figure 2-1 switch M associates destination ID 0x80 with egress ports 1 and 2, and switch N associates destination ID 0x80 with ports 1, 2, and 3. Figure 2-2 shows a possible relationship between the multicast group, the multicast masks for the switches, and the global system address map.

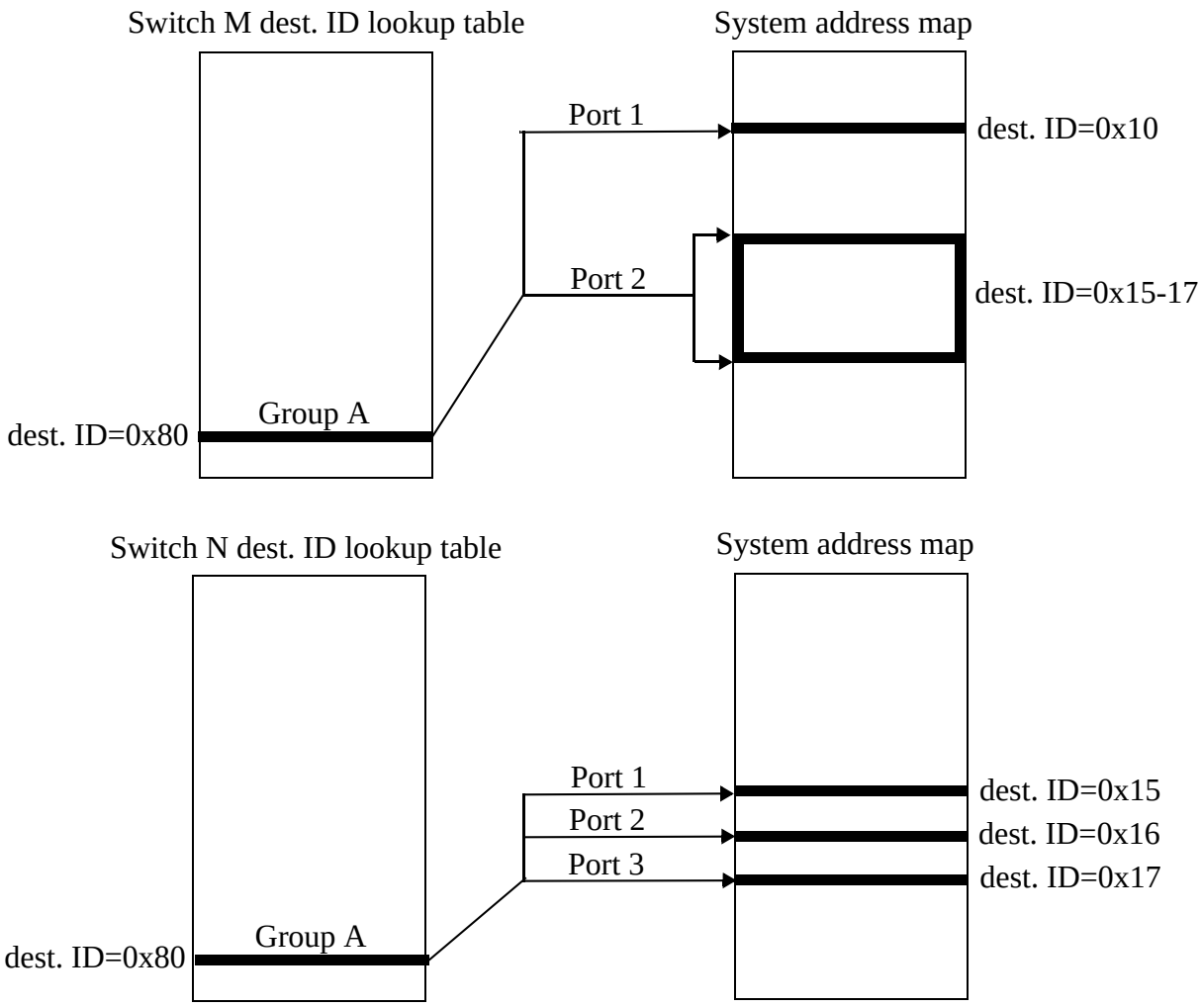

Figure 2-2. Multicast Association Example

Configuring a RapidIO switch to replicate packets for a multicast group is a two-step process. First, a list of egress ports is set in a multicast mask list. Second, one or more destination IDs which represent the multicast groups are associated with the multicast mask in the switch. During normal system operation, any time a switch receives a packet with a destination ID which has been associated with a multicast mask it will send that packet to all egress ports enabled by that multicast mask.

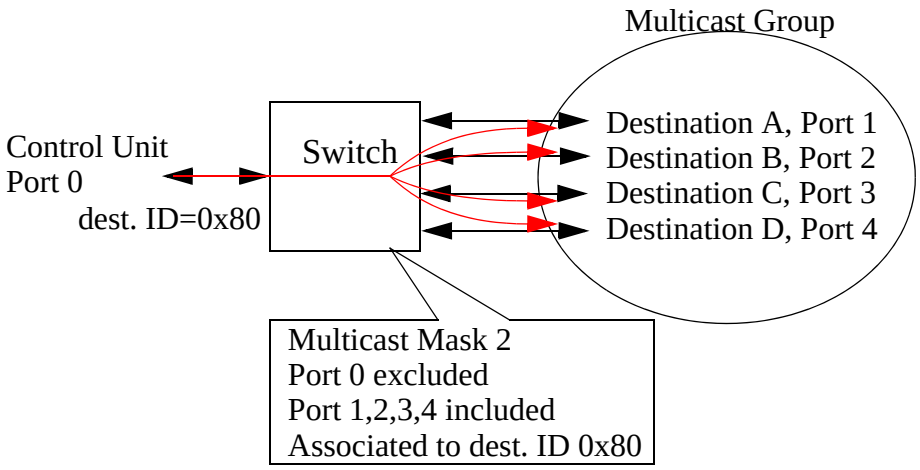

Figure 2-3. Multicast Configuration Example

Figure 2-3 shows a control unit connected to switch port 0 which needs to multicast to destinations A, B, C and D. A multicast mask, in this case arbitrarily picked as multicast mask 2, is set up to select which ports in the switch are part of the multicast group of destinations A, B, C, and D. A destination ID, in this case arbitrarily assigned 0x80, is associated with multicast mask 2 as the destination ID that the control unit should use to multicast to the multicast group. The associate operation is done using the CSRs defined in Chapter 4, “Multicast and Port Aggregation Extensions Registers”.

The defined CSRs allow a switch to associate destination IDs with multicast masks using a small number of maintenance write operations. The number of unique destination IDs that can be associated with a multicast mask is also defined in a CSR.

While each destination ID is associated with a unique multicast group, the programming model allows a destination ID to be mapped to a different multicast mask for each port on the switch. However, for each port a destination ID can be associated with at most one multicast mask. The last association operation performed for a specific port and destination ID dictates which multicast mask the destination ID is associated with. It is also possible to map a given destination ID to the same multicast mask for all ports.

A RapidIO switch may be capable of supporting large numbers of multicast groups by dedicating a sequential range of destination ID’s to an equal number of sequentially numbered multicast masks. A switch may also be designed which does not require all multicast destination IDs to be sequential. The programming model supports both of these implementations.

A packet will never be multicast back out of the port it was received on even if it is included in the multicast mask for that destination ID. This allows a group of end points which need to multicast to each other to share the same multicast mask. Packets using a multicast mask which has no egress ports selected will be dropped without error notification. A device may have implementation specific error

notification in this situation, depending on system requirements.

The default state after a reset for multicast masks is that all multicast masks have no ports selected. Additionally, after reset no associations exist between any multicast group/destination ID and the multicast masks. However, implementation specific capabilities may modify the multicast mask values and associations after reset without software intervention.

For more information and examples on the use of the programming model for multicast refer to Annex B, “Multicast Applications (Informative)”.

2.4 Multicast Transaction Ordering Requirements

RapidIO packets which are in the same multicast group (the same destination ID) with the same flowID and are received on the same ingress port must be multicast on the egress ports in the same order that they were received. There are no ordering requirements between multicast packets and non-multicast packets, or between multicast packets in different multicast groups. Maintaining ordering between transactions in the same transaction request flow for a multicast group allows an application to multicast a completion flag at the end of a potentially large data transfer which was sent to the same multicast group.

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Chapter 3 Port Aggregation Extensions Behavior

3.1 Introduction

This chapter describes the port aggregation extensions rules of operation in a RapidIO system. A RapidIO switch which does not support port aggregation can co-exist in a RapidIO fabric with other switches that do support port aggregation. The only requirement is that the switch be capable of routing the destination IDs used for port aggregation transactions.

3.2 Port Aggregation Interoperability

A RapidIO port aggregation operation consists of the selection of a physical port from a set of physical ports. There are many different possible algorithms for port selection. This specification supports two broad categories of port selection algorithms: port fail over, and load balancing.

An example of a port selection algorithm that is useful for port fail over is to always select a specific port until that port cannot transfer packets successfully, in which case another available port is selected.

Load balancing algorithms for RapidIO data streams may or may not preserve the order of packets within a flow. Packet order preservation may or may not be necessary for an application. For example, when a processing element must send a stream of writes followed by an event, the order of the writes among themselves may not matter when writing to RAM. If that same processing element is sending a sequence of data streaming transactions, however, the packets in the transaction flow must be delivered in the correct order, or the logical layer receiver will fail. In contrast, messaging packets can arrive in any order and still be successfully processed.

Load balancing port selection algorithms are therefore highly application dependent. The algorithm may make use of various packet header values. For this reason, load balancing port selection algorithms are outside the scope of this specification.

3.3 Port Aggregation Operation

Port aggregation operations are defined in terms of the following concepts: **port**

aggregation groups, port aggregation masks, virtual ports, and **virtual port masks**.

A set of physical ports that shall be treated as a single port is known as a **port aggregation group**. A **port aggregation mask** is a control value which determines which physical ports are included in a port aggregation group. Conceptually, a port aggregation mask is a register with one bit for each physical port to which a packet may routed. A set bit in a port aggregation mask shall include the associated physical port in the port aggregation group, and a clear bit shall have the opposite effect. A packet shall be forwarded to exactly one of the physical ports included in a port aggregation mask. Port aggregation groups and port aggregation masks are numbered starting at 0.

A **virtual port** is an extension of the set of physical ports on a device which is used to define additional routing behavior. The first virtual port number shall be equal to the count of the physical ports implemented on the device. For example, if a device has sixteen physical ports numbered 0 to 15, the first virtual port shall be port number 16, regardless of which physical ports are available for routing in the current configuration.

For routing purposes, each port aggregation group is identified using exactly one virtual port. Port aggregation group zero shall be mapped to the first virtual port, port aggregation group one shall be mapped to the second virtual port, and so on.

Virtual port numbers shall be treated as an extension of the number of physical ports on a device. A routing value that selects an Egress Port Number that corresponds to a valid virtual port on the device shall cause packets to be routed according to the port aggregation mask and control values for that virtual port.

A **virtual port mask** is the set of virtual ports found in a multicast mask. The physical ports and the virtual ports of the multicast mask are treated in the same manner. A packet routed according to a multicast mask shall be forwarded to each physical and virtual port asserted in the multicast mask. When a virtual port is associated with a port aggregation group, the port selection algorithm shall forward the packet out one physical port within the port aggregation group. Packets routed according to multicast masks and/or port aggregation groups shall be forwarded at most once out each physical port.

3.3.1 Fail-over Port Selection

If port aggregation is implemented in a device, the device shall support the fail-over port selection algorithm. The behavior of the fail-over port selection algorithm shall be as follows:

- The port selected from the enabled physical ports of a port aggregation mask must be capable of transferring packets successfully. The criteria for transferring packets successfully is implementation specific. If no enabled port is capable of transferring packets successfully, the fail-over port selection algorithm shall not select any port.
- The fail-over port selection algorithm shall select the physical port indicated by the PAG_Default field in the “Section 4.4.18, Port n Port Aggregation Mask x Control Register 0 CSR” on page 51, unless that physical port is not capable of transferring packets successfully.

3.4 Port Aggregation Transaction Ordering Requirements

Port aggregation implementations shall forward packets in the same transaction flow to the physical egress port(s) selected in the order in which they were received on an ingress port. Port aggregation implementations shall obey the physical layer deadlock avoidance rules defined in RapidIO Part 6: LP-Serial Physical Layer Specification.

Applications shall not assume any ordering requirements between port aggregated packets, multicast packets, and non-multicast packets.

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Chapter 4 Multicast and Port Aggregation Extensions Registers

4.1 Introduction

This section describes the Multicast and Port Aggregation Extensions CAR and CSR registers that allow an external processing element to determine if a switch supports the multicast and port aggregation extensions defined in this specification, and to manage the configuration of multicast and port aggregation for a switch processing element. This chapter only describes registers or register bits defined by this specification. Refer to the other RapidIO logical, transport, physical, and extension specifications of interest to determine a complete list of registers and bit definitions for a device. All registers are 32-bits and aligned to a 32-bit boundary. The behavior of reserved register bits and register offsets and access rules and requirements are described in the *RapidIO Part 1: Input/Output Logical Specification*.

Table 4-1. Multicast Register Map

Configuration Space Byte Offset	Register Name
0x0-C	Reserved
0x10	Processing Element Features CAR
0x14-2C	Reserved
0x30	Switch Multicast Support CAR
0x34	Reserved
0x38	Switch Multicast Information CAR
0x3C-7C	Reserved
0x80	Multicast Mask Port CSR
0x84	Multicast Associate Select CSR
0x88	Multicast Associate Operation CSR
0x8C–FC	Reserved

Table 4-1. Multicast Register Map (Continued)

Configuration Space Byte Offset	Register Name
0x100–FFFC	Extended Features Space
0x10000–FFFFFC	Implementation-defined Space

4.2 Capability Registers (CARs)

4.2.1 Processing Elements Features CAR (Configuration Space Offset 0x10)

The Processing Elements Features CAR contains 31 processing elements features bits defined in various RapidIO specifications, as well as the Multicast Support bit, defined here.

Table 4-2. Bit Settings for Processing Elements Features CAR

Bit	Name	Reset Value	Description
0-20	-		Reserved (defined elsewhere)
21	Multicast Support	*	Support for multicast extensions 0b0 - Does not support multicast extensions 0b1 - Supports multicast extensions
22-31	-		Reserved (defined elsewhere)

* Implementation dependant

4.2.2 Switch Multicast Support CAR (Configuration Space Offset 0x30)

This register shall not be implemented if Bit 19 “Dev32 Support” of the Processing Element Features CAR is set.

The Switch Multicast Support CAR defines support for a simple multicast model and the additional limits on multicast mask resources.

Table 4-3. Bit Settings for Switch Multicast Support CAR

Bit	Name	Reset Value	Description
0	Simple_Assoc	*	Support for a simple multicast association model 0b0 - Does not support simple association 0b1 - Supports simple association If this bit is set, the Block_Assoc bit in the Switch Multicast Information CAR must also be set.
1-31	-		Reserved (defined elsewhere)

* Implementation dependant

4.2.3 Switch Multicast Information CAR (Configuration Space Offset 0x38)

This register shall not be implemented if Bit 19 “Dev32 Support” of the Processing Element Features CAR is set.

The Switch Multicast Information CAR defines the methods for associating destination IDs with multicast masks supported by a RapidIO switch device. It also defines the limits on multicast mask resources.

Table 4-4. Bit Settings for Switch Multicast Information CAR

Bits	Name	Description
0	Block_Assoc	Block association support - allows equal sized blocks of destination IDs and multicast masks to be associated with each other with a single operation rather than one at a time. 0b0 - block association is not supported 0b1 - block association is supported If the Simple_Assoc bit in the Switch Multicast Support CAR is set, this bit must also be set.
1	Per_Port_Assoc	Per ingress port association support - allows a destination ID to be associated with a multicast mask on a per-ingress port basis rather than a single association for the entire switch. 0b0 - per port association is not supported 0b1 - per port association is supported
2-15	MaxDestIDAssoc	The maximum number of destination IDs associations per multicast mask 0x0000 - 1 destination ID 0x0001 - 2 destination IDs ... 0x3FFF - 16384 destination IDs
16-31	MaxMcastMasks	The number of multicast egress port masks available. This field also defines the largest block of destination IDs that can be block associated. 0x0000 - [reserved] 0x0001 - 1 multicast mask 0x0002 - 2 multicast masks ... 0xFFFF - 65535 multicast masks

4.3 Command and Status Registers (CSRs)

4.3.1 Multicast Mask Port CSR (Configuration Space Offset 0x80)

This register shall not be implemented if Bit 19 “Dev32 Support” of the Processing Element Features CAR is set.

The Multicast Mask Port CSR allows configuration of the egress port list for each of the switch’s multicast masks.

Writing the Write_to_Verify command sets up a Mcast_Mask and Egress_Port_Num pair to verify. The presence of the specified egress port in the specified multicast mask is indicated by the Port_Present bit on a subsequent read of the register.

Writing the Add_Port or Delete_Port commands adds or deletes the specified egress port to or from the specified multicast mask.

Writing the Add_All_Ports or Delete_All_Ports commands adds or deletes all of the egress ports in the specified multicast mask.

The result of illegal values or combinations for an operation is implementation dependent. For examples of how to use this register, refer to Section 5.2, “Configuring Multicast Masks”.

Table 4-5. Bit Settings for Multicast Mask Port CSR

Bits	Name	Reset Value	Description
0-15	Mcast_Mask	0x0000	Specifies the multicast mask which is to be modified or queried as determined by the Mask_Cmd field.
16-23	Egress_Port_Num	0x00	Specifies the port number to be added, deleted, or queried with the Mask_Cmd field.
24	-	0b0	Reserved
25-27	Mask_Cmd	0b000	Specifies the mask action on a write. 0b000 - Write_to_Verify 0b001 - Add_Port 0b010 - Delete_Port 0b011 - reserved 0b100 - Delete_All_Ports 0b101 - Add_All_Ports 0b110 - reserved 0b111 - reserved
28–30	-	0b000	Reserved
31	Port_Present	0b0	Indicates the existence of the egress port and multicast mask pair as a result of the last preceding Write_to_Verify command. 0b0 - Port was not enabled as an egress port in the specified multicast mask 0b1 - Port was enabled as an egress port in the specified multicast mask. This bit is reserved on a write.

4.3.2 Multicast Associate Select CSR (Configuration Space Offset 0x84)

This register shall not be implemented if Bit 19 “Dev32 Support” of the Processing Element Features CAR is set.

This register specifies the destination ID and multicast mask number for a subsequent associate operation controlled with the Multicast Associate Operation CSR. If block association is supported, this register specifies the start of the block to associate. For examples of how this register is used, refer to Section 5.4, “Configuring Associations”.

Table 4-6. Bit Settings for Multicast Associate Select CSR

Bits	Name	Reset Value	Description
0-7	Large_DestID	0x00	Selects the most significant byte of a large transport destination ID for an association operation
8-15	DestID	0x00	Selects the destination ID for an association operation
16-31	Mcast_Mask_Num	0x0000	Selects the multicast mask number for an association operation

4.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88)

This register shall not be implemented if Bit 19 “Dev32 Support” of the Processing Element Features CAR is set.

The Multicast Associate Operation CSR specifies three operations for associating destination IDs with multicast masks. The affected destination ID and multicast mask is specified in the Multicast Associate Select CSR. The specified operation is executed when this register is written. When this register is read and the Assoc_Cmd field it set to Write_to_Verify the specified operation is executed and the updated register state is returned. If this register is read and the Assoc_Cmd field is not set to Write_to_Verify the resulting behavior is implementation dependent. Block association operations assign associations sequentially starting with the destination ID and multicast mask specified in the Multicast Associate Select CSR.

Writing the Write_To_Verify command checks for an association between the destination ID and multicast mask specified in the Multicast Associate Select CSR. The result of the check is indicated by the state of the Assoc_Present bit on a read of this register. This command cannot be executed on a block.

Writing the Add_Assoc or Delete_Assoc command adds or deletes the association between the destination ID and the multicast mask (or block of associations, if block association is supported) specified in the Multicast Associate Select CSR.

The result of illegal values or field combinations for an association operation is implementation dependent. For examples of how this register is used, refer to Section 5.4, “Configuring Associations”.

Table 4-7. Bit Settings for Multicast Associate Operation CSR

Bits	Name	Reset Value	Description
0-15	Assoc_Blksize	0x0000	This field specifies the number of sequential DestinationIDs to be associated with an equal number of sequential multicast mask numbers if block association is supported. This field is ignored on a Write_to_Verify command. 0x0000 - one association 0x0001 - two sequential associations ... 0xFFFF - 65536 sequential associations
16-23	Ingress_Port	0x00	This field specifies the ingress port association to affect if per-port ingress association is supported
24	Large_Transport	0b0	0b0 - the association is for small transport destination IDs 0b1 - the association is for large transport destination IDs
25-26	Assoc_Cmd	0b00	This field specifies the command to execute when this register is written. 0b00 - Write_To_Verify 0b01 - reserved 0b10 - Delete_Assoc 0b11 - Add_Assoc

Table 4-7. Bit Settings for Multicast Associate Operation CSR (Continued)

Bits	Name	Reset Value	Description
27-30	-	0b0000	reserved
31	Assoc_Present	0b0	This bit contains the result of the last Write_to_Verify command executed. 0b0 - no association present 0b1 - association present This bit is reserved on write.

4.4 Switch Routing Table Register Block

A switch device which has bits 19 “Dev32 Support” and 21 “Multicast Support” set in the Processing Element Features CAR shall implement this register block. Note that this definition is a refinement of the Switch Routing Table Register block defined in RapidIO Part 3: Common Transport Specification.

4.4.1 Register Map

The register map for the routing table registers shall be as specified by Table 4-8. This register map is currently only defined for devices with up to 16 RapidIO ports, but can be extended or shortened if more or less port definitions are required for a device. For example, a device with four RapidIO ports is only required to use register map space corresponding to offsets [EF_PTR+0x00] through [EF_PTR+0xBC]. Register map offset [EF_PTR+0x140] can be used for another Extended Features block.

Table 4-8. Switch Routing Table Register Map

	Block Byte Offset	Register Name
General	0x0	Routing Table Register Block Header
	0x4-0x1C	Reserved
Broadcast	0x20	Broadcast Routing Table Control CSR
	0x24	Reserved
	0x28	Broadcast Multicast Info CSR
	0x2C	Broadcast Port Aggregation Info CSR
	0x30-0x3C	Reserved

Table 4-8. Switch Routing Table Register Map

	Block Byte Offset	Register Name
Port 0	0x40	Port 0 Routing Table Control CSR
	0x44	Reserved
	0x48	Port 0 Multicast Info CSR
	0x4C	Port 0 Port Aggregation Info CSR
	0x50-0x5C	Reserved
Port 1	0x60	Port 1 Routing Table Control CSR
	0x64	Reserved
	0x68	Port 1 Multicast Info CSR
	0x6C	Port 1 Port Aggregation Info CSR
	0x70-0x7C	Reserved
Ports 2-14	0x80–21C	Assigned to Port 2-14 CSRs
Port 15	0x220	Port 15 Routing Table Control CSR
	0x224	Reserved
	0x228	Port 15 Multicast Info CSR
	0x22C	Port 15 Port Aggregation Info CSR
	0x230-0x23C	Reserved

4.4.2 Broadcast Routing Table Control CSR (Block Offset 0x20)

The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-9. Unless otherwise specified, the bits and bit fields in this register are write only.

Table 4-9. Bit Settings for Broadcast Routing Table Control CSR

Bit	Name	Reset Value	Description
0-5	___		Reserved
6-7	Mask_size	see footnote[1]	A multicast mask shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register (8 bytes) 0b01 - Two set registers, two clear registers (16 bytes) 0b10 - Four set registers, four clear registers (32 bytes) 0b11 - Eight set registers, eight clear registers (64 bytes) This bit field shall be read only.
8-15	Virtual_port_count	see footnote[2]	The number of virtual ports found in the Mcast_ctl field of the Broadcast Multicast Mask x Set/Clear Register y CSRs, encoded as follows: 0x00 - No Virtual Ports 0x01 - One Virtual Port 0x02 - Two Virtual Ports 0x03 - Three Virtual Ports ... 0xFF - 255 Virtual Ports This field shall be read only. A set of port aggregation mask registers shall be implemented for each virtual port.
8-31	___		Reserved

[1]The Mask_size reset value is implementation dependent

[2]The Virtual Port_count reset value is implementation dependent

The following illustrates the arrangement of Multicast Mask x Set/Clear Register y CSRs for various Mask_size values.

Table 4-10. Mask 0-7 Set/Clear Registers, Mask_size = 0

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Clear Register 0	0x000004
Multicast Mask 1 Set Register 0	0x000008
Multicast Mask 1 Clear Register 0	0x00000C
Multicast Mask 2 Set Register 0	0x000010
Multicast Mask 2 Clear Register 0	0x000014
Multicast Mask 3 Set Register 0	0x000018
Multicast Mask 3 Clear Register 0	0x00001C
Multicast Mask 4 Set Register 0	0x000020
Multicast Mask 4Clear Register 0	0x000024
Multicast Mask 5 Set Register 0	0x000028
Multicast Mask 5 Clear Register 0	0x00002C
Multicast Mask 6 Set Register 0	0x000030
Multicast Mask 6 Clear Register 0	0x000034

Table 4-10. Mask 0-7 Set/Clear Registers, Mask_size = 0

Register Name	Offset
Multicast Mask 7 Set Register 0	0x000038
Multicast Mask 7 Clear Register 0	0x00003C

Table 4-11. Mask 0-3 Set/Clear Registers, Mask_size = 1

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Clear Register 0	0x000008
Multicast Mask 0 Clear Register 1	0x00000C
Multicast Mask 1 Set Register 0	0x000010
Multicast Mask 1 Set Register 1	0x000014
Multicast Mask 1 Clear Register 0	0x000018
Multicast Mask 1 Clear Register 1	0x00001C
Multicast Mask 2 Set Register 0	0x000020
Multicast Mask 2 Set Register 1	0x000024
Multicast Mask 2 Clear Register 0	0x000028
Multicast Mask 2 Clear Register 1	0x00002C
Multicast Mask 3 Set Register 0	0x000030
Multicast Mask 3 Set Register 1	0x000034
Multicast Mask 3 Clear Register 0	0x000038
Multicast Mask 3 Clear Register 1	0x00003C

Table 4-12. Mask 0-1 Set/Clear Registers, Mask_size = 2

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Set Register 2	0x000008
Multicast Mask 0 Set Register 3	0x00000C
Multicast Mask 0 Clear Register 0	0x000010
Multicast Mask 0 Clear Register 1	0x000014
Multicast Mask 0 Clear Register 2	0x000018
Multicast Mask 0 Clear Register 3	0x00001C
Multicast Mask 1 Set Register 0	0x000020
Multicast Mask 1 Set Register 1	0x000024
Multicast Mask 1 Set Register 2	0x000028
Multicast Mask 1 Set Register 3	0x00002C
Multicast Mask 1 Clear Register 0	0x000030

Table 4-12. Mask 0-1 Set/Clear Registers, Mask_size = 2

Register Name	Offset
Multicast Mask 1 Clear Register 1	0x000034
Multicast Mask 1 Clear Register 2	0x000038
Multicast Mask 1 Clear Register 3	0x00003C

Table 4-13. Mask 0 Set/Clear Registers, Mask_size = 3

Register Name	Offset
Multicast Mask 0 Set Register 0	0x000000
Multicast Mask 0 Set Register 1	0x000004
Multicast Mask 0 Set Register 2	0x000008
Multicast Mask 0 Set Register 3	0x00000C
Multicast Mask 0 Set Register 4	0x000010
Multicast Mask 0 Set Register 5	0x000014
Multicast Mask 0 Set Register 6	0x000018
Multicast Mask 0 Set Register 7	0x00001C
Multicast Mask 0 Clear Register 0	0x000020
Multicast Mask 0 Clear Register 1	0x000024
Multicast Mask 0 Clear Register 2	0x000028
Multicast Mask 0 Clear Register 3	0x00002C
Multicast Mask 0 Clear Register 4	0x000030
Multicast Mask 0 Clear Register 5	0x000034
Multicast Mask 0 Clear Register 6	0x000038
Multicast Mask 0 Clear Register 7	0x00003C

4.4.3 Broadcast Multicast Info CSR (Block Offset 0x28)

This register shall communicate the location of the Broadcast Multicast Mask 0 Set Register 0 CSR. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-14. This register shall be read only.

Table 4-14. Bit Settings for Broadcast Multicast Info CSR

Bit	Name	Reset Value	Description
0-7	Num_Masks	see footnote[1]	Num_Masks shall indicate the number of Broadcast Multicast Masks, encoded as follows: 0x00 - 256 Masks 0x01 - 1 Masks 0x02 - 2 Masks 0x03 - 3 Masks ... 0xFF - 255 Masks
8-21	Mask_Ptr	see footnote[2]	The Mask_Ptr value shall be the maintenance offset of the Broadcast Multicast Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Broadcast Multicast Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The Mask_Ptr value shall indicate an address in Implementation Defined register space. Writes to the Broadcast Multicast Mask registers pointed to by this register shall cause the corresponding Port n Multicast Mask registers for all ports to assume the value written.
22-31	___	0b00	Reserved

[1]The Num_Masks reset value is implementation dependent

[2]The Mask_Ptr reset value is implementation dependent

4.4.4 Broadcast Port Aggregation Mask Info CSR (Block Offset 0x2C)

This register shall be implemented if the value Virtual_port_count field of the “Section 4.4.3, Broadcast Multicast Info CSR” on page 34 is not zero. This register shall not be implemented if the Virtual_port_count field of the Section 4.4.3, “Broadcast Multicast Info CSR” on page 4-34 is zero.

This register shall communicate the location of the Broadcast Port Aggregation Mask 0 Set Register 0 CSR. The remaining registers in the block shall be implemented as illustrated in Table 4-16, Table 4-17, Table 4-18, and Table 4-19. The set mask/clear mask/control registers sequence shall repeat Virtual_port_count times. The use and meaning of the bit fields of this register shall be as specified in Table 4-15. This register shall be read only.

Table 4-15. Bit Settings for Broadcast Port Aggregation Mask Info CSR

Bit	Name	Reset Value	Description
0-5	___	0b00	Reserved
6-7	PAG_mask_size	see footnote[1]	The port aggregation masks shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register, two control registers (16 bytes) 0b01 - Two set registers, two clear registers, four control registers (32 bytes) 0b10 - Four set registers, four clear registers, eight control registers (64 bytes) 0b11 - Eight set registers, eight clear registers, sixteen control registers (128 bytes) This bit field shall be read only.
8-21	PAG_mask_ptr	see footnote[2]	The PAG_mask_ptr value shall be the maintenance offset of the Broadcast Port Aggregation Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Broadcast Port Aggregation Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The PAG_mask_ptr value shall indicate an address in Implementation Defined register space. Writes to the Broadcast Port Aggregation Mask Y registers pointed to by this register shall cause the corresponding Port n Port Aggregation Mask Y registers for all ports to be modified by the value written.
22-31	___	0b00	Reserved

[1]The PAG_mask_size reset value is implementation dependent

[2]The PAG_mask_ptr reset value is implementation dependent

The following illustrates the arrangement of Port Aggregation Mask x Set/Clear/Control 0-n Register y CSRs for various PAG_Mask_size values.

Table 4-16. Mask 0-7 Set/Clear/Control Registers, PAG_mask_size = 0

Register Name	Offset
Port Aggregation Mask 0 Set Register 0	0x000000
Port Aggregation Mask 0 Clear Register 0	0x000004
Port Aggregation Mask 0 Control Register 0	0x000008
Port Aggregation Mask 0 Control Register 1	0x00000C
Port Aggregation Mask 1 Set Register 0	0x000010
Port Aggregation Mask 1 Clear Register 0	0x000014
Port Aggregation Mask 1 Control Register 0	0x000018
Port Aggregation Mask 1 Control Register 1	0x00001C
Port Aggregation Mask 2 Set Register 0	0x000020
Port Aggregation Mask 2 Clear Register 0	0x000024
Port Aggregation Mask 2 Control Register 0	0x000028
Port Aggregation Mask 2 Control Register 1	0x00002C
Port Aggregation Mask 3 Set Register 0	0x000030
Port Aggregation Mask 3 Clear Register 0	0x000034
Port Aggregation Mask 3 Control Register 0	0x000038

Table 4-16. Mask 0-7 Set/Clear/Control Registers, PAG_mask_size = 0

Register Name	Offset
Port Aggregation Mask 3 Control Register 1	0x00003C
Port Aggregation Mask 4 Set Register 0	0x000040
Port Aggregation Mask 4 Clear Register 0	0x000044
Port Aggregation Mask 4 Control Register 0	0x000048
Port Aggregation Mask 4 Control Register 1	0x00004C
Port Aggregation Mask 5 Set Register 0	0x000050
Port Aggregation Mask 5 Clear Register 0	0x000054
Port Aggregation Mask 5 Control Register 0	0x000058
Port Aggregation Mask 5 Control Register 1	0x00005C
Port Aggregation Mask 6 Set Register 0	0x000060
Port Aggregation Mask 6 Clear Register 0	0x000064
Port Aggregation Mask 6 Control Register 0	0x000068
Port Aggregation Mask 6 Control Register 1	0x00006C
Port Aggregation Mask 7 Set Register 0	0x000070
Port Aggregation Mask 7 Clear Register 0	0x000074
Port Aggregation Mask 7 Control Register 0	0x000078
Port Aggregation Mask 7 Control Register 1	0x00007C

Table 4-17. Mask 0-3 Set/Clear/Control Registers, PAG_mask_size = 1

Register Name	Offset
Port Aggregation Mask 0 Set Register 0	0x000000
Port Aggregation Mask 0 Set Register 1	0x000004
Port Aggregation Mask 0 Clear Register 0	0x000008
Port Aggregation Mask 0 Clear Register 1	0x00000C
Port Aggregation Mask 0 Control Register 0	0x000010
Port Aggregation Mask 0 Control Register 1	0x000014
Port Aggregation Mask 0 Control Register 2	0x000018
Port Aggregation Mask 0 Control Register 3	0x00001C
Port Aggregation Mask 1 Set Register 0	0x000020
Port Aggregation Mask 1 Set Register 1	0x000024
Port Aggregation Mask 1 Clear Register 0	0x000028
Port Aggregation Mask 1 Clear Register 1	0x00002C
Port Aggregation Mask 1 Control Register 0	0x000030
Port Aggregation Mask 1 Control Register 1	0x000034
Port Aggregation Mask 1 Control Register 2	0x000038
Port Aggregation Mask 1 Control Register 3	0x00003C
Port Aggregation Mask 2 Set Register 0	0x000040

Table 4-17. Mask 0-3 Set/Clear/Control Registers, PAG_mask_size = 1

Register Name	Offset
Port Aggregation Mask 2 Set Register 1	0x000044
Port Aggregation Mask 2 Clear Register 0	0x000048
Port Aggregation Mask 2 Clear Register 1	0x00004C
Port Aggregation Mask 2 Control Register 0	0x000050
Port Aggregation Mask 2 Control Register 1	0x000054
Port Aggregation Mask 2 Control Register 2	0x000058
Port Aggregation Mask 2 Control Register 3	0x00005C
Port Aggregation Mask 3 Set Register 0	0x000060
Port Aggregation Mask 3 Set Register 1	0x000064
Port Aggregation Mask 3 Clear Register 0	0x000068
Port Aggregation Mask 3 Clear Register 1	0x00006C
Port Aggregation Mask 3 Control Register 0	0x000070
Port Aggregation Mask 3 Control Register 1	0x000074
Port Aggregation Mask 3 Control Register 2	0x000078
Port Aggregation Mask 3 Control Register 3	0x00007C

Table 4-18. Mask 0-1 Set/Clear/Control Registers, PAG_mask_size = 2

Register Name	Offset
Port Aggregation Mask 0 Set Register 0	0x000000
Port Aggregation Mask 0 Set Register 1	0x000004
Port Aggregation Mask 0 Set Register 2	0x000008
Port Aggregation Mask 0 Set Register 3	0x00000C
Port Aggregation Mask 0 Clear Register 0	0x000010
Port Aggregation Mask 0 Clear Register 1	0x000014
Port Aggregation Mask 0 Clear Register 2	0x000018
Port Aggregation Mask 0 Clear Register 3	0x00001C
Port Aggregation Mask 0 Control Register 0	0x000020
Port Aggregation Mask 0 Control Register 1	0x000024
Port Aggregation Mask 0 Control Register 2	0x000028
Port Aggregation Mask 0 Control Register 3	0x00002C
Port Aggregation Mask 0 Control Register 4	0x000030
Port Aggregation Mask 0 Control Register 5	0x000034
Port Aggregation Mask 0 Control Register 6	0x000038
Port Aggregation Mask 0 Control Register 7	0x00003C
Port Aggregation Mask 1 Set Register 0	0x000040
Port Aggregation Mask 1 Set Register 1	0x000044
Port Aggregation Mask 1 Set Register 2	0x000048

Table 4-18. Mask 0-1 Set/Clear/Control Registers, PAG_mask_size = 2

Register Name	Offset
Port Aggregation Mask 1 Set Register 3	0x00004C
Port Aggregation Mask 1 Clear Register 0	0x000050
Port Aggregation Mask 1 Clear Register 1	0x000054
Port Aggregation Mask 1 Clear Register 2	0x000058
Port Aggregation Mask 1 Clear Register 3	0x00005C
Port Aggregation Mask 1 Control Register 0	0x000060
Port Aggregation Mask 1 Control Register 1	0x000064
Port Aggregation Mask 1 Control Register 2	0x000068
Port Aggregation Mask 1 Control Register 3	0x00006C
Port Aggregation Mask 1 Control Register 4	0x000070
Port Aggregation Mask 1 Control Register 5	0x000074
Port Aggregation Mask 1 Control Register 6	0x000078
Port Aggregation Mask 1 Control Register 7	0x00007C

Table 4-19. Mask 0 Set/Clear Registers, PAG_mask_size = 3

Register Name	Offset
Port Aggregation Mask 0 Set Register 0	0x000000
Port Aggregation Mask 0 Set Register 1	0x000004
Port Aggregation Mask 0 Set Register 2	0x000008
Port Aggregation Mask 0 Set Register 3	0x00000C
Port Aggregation Mask 0 Set Register 4	0x000010
Port Aggregation Mask 0 Set Register 5	0x000014
Port Aggregation Mask 0 Set Register 6	0x000018
Port Aggregation Mask 0 Set Register 7	0x00001C
Port Aggregation Mask 0 Clear Register 0	0x000020
Port Aggregation Mask 0 Clear Register 1	0x000024
Port Aggregation Mask 0 Clear Register 2	0x000028
Port Aggregation Mask 0 Clear Register 3	0x00002C
Port Aggregation Mask 0 Clear Register 4	0x000030
Port Aggregation Mask 0 Clear Register 5	0x000034
Port Aggregation Mask 0 Clear Register 6	0x000038
Port Aggregation Mask 0 Clear Register 7	0x00003C
Port Aggregation Mask 1 Control Register 0	0x000040
Port Aggregation Mask 1 Control Register 1	0x000044
Port Aggregation Mask 1 Control Register 2	0x000048
Port Aggregation Mask 1 Control Register 3	0x00004C
Port Aggregation Mask 1 Control Register 4	0x000050

Table 4-19. Mask 0 Set/Clear Registers, PAG_mask_size = 3

Register Name	Offset
Port Aggregation Mask 1 Control Register 5	0x000054
Port Aggregation Mask 1 Control Register 6	0x000058
Port Aggregation Mask 1 Control Register 7	0x00005C
Port Aggregation Mask 1 Control Register 8	0x000060
Port Aggregation Mask 1 Control Register 9	0x000064
Port Aggregation Mask 1 Control Register 10	0x000068
Port Aggregation Mask 1 Control Register 11	0x00006C
Port Aggregation Mask 1 Control Register 12	0x000070
Port Aggregation Mask 1 Control Register 13	0x000074
Port Aggregation Mask 1 Control Register 14	0x000078
Port Aggregation Mask 1 Control Register 15	0x00007C

4.4.5 Port n Routing Table Control CSR (Block Offset 0x40 + (0x20 * n))

This register shall indicate the number of registers in a multicast mask for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-20. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 4-20. Bit Settings for Port n Routing Table Control CSR

Bit	Name	Reset Value	Description
0-5	___		Reserved
6-7	Mask_size	see footnote[1]	A multicast mask shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register (8 bytes) 0b01 - Two set registers, two clear registers (16 bytes) 0b10 - Four set registers, four clear registers (32 bytes) 0b11 - Eight set registers, eight clear registers (64 bytes) This bit field shall be read only.
8-15	Virtual_port_count	see footnote[2]	The number of virtual ports found in the Mcast_ctl field of the Port n Multicast Mask x Set/Clear Register y CSRs, encoded as follows: 0x00 - No Virtual Ports 0x01 - One Virtual Port 0x02 - Two Virtual Ports 0x03 - Three Virtual Ports ... 0xFF - 255 Virtual Ports This field shall be read only. One port aggregation mask shall be implemented for each virtual port.
8-31	___		Reserved

[1]The Mask_size reset value is implementation dependent

[2]The Virtual Port_count reset value is implementation dependent

4.4.6 Port n Multicast Info CSR (Block Offset 0x48 + 20 * n)

This register shall communicate the location of Port n Multicast Mask 0 Register 0 CSR. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-21. This register shall be read only.

Table 4-21. Bit Settings for Port n Multicast Info CSR

Bit	Name	Reset Value	Description
0-7	Num_Masks	see footnote[1]	Communicates the number of multicast masks for this port. Num_Masks is encoded as follows: 0x00 - 256 Masks 0x01 - 1 Masks 0x02 - 2 Masks 0x03 - 3 Masks ... 0xFF - 255 Masks
8-21	Mask_Ptr	see footnote[2]	The Mask_Ptr value shall be the maintenance offset of the Port n Multicast Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Port n Multicast Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The Mask_Ptr value shall indicate an address in Implementation Defined register space.
22-31	___	0b00	Reserved

[1]The Num_Masks reset value is implementation dependent

[2]The Mask_Ptr reset value is implementation dependent

4.4.7 Port n Port Aggregation Mask Info CSR (Block Offset 0x48 + 20 * n)

This register shall be implemented if the value Virtual_port_count field of the “Section 4.4.5, Port n Routing Table Control CSR” on page 40 is not zero. This register shall not be implemented if the Virtual_port_count field of the Section 4.4.5, “Port n Routing Table Control CSR” on page 4-40 is zero.

This register shall communicate the location of Port n Port Aggregation Mask 0 Set Register 0 CSR. The registers in the block shall be implemented as illustrated in Table 4-16, Table 4-17, Table 4-18, and Table 4-19. The set group/clear group/control registers sequence shall have Virtual_port_count instances. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-22. This register shall be read only.

Table 4-22. Bit Settings for Port n Port Aggregation Mask Info CSR

Bit	Name	Reset Value	Description
6-7	PAG_mask_size	see footnote[1]	A port aggregation mask shall consist of the number of registers indicated by this value, encoded as follows: 0b00 - One set register, one clear register, two control registers (16 bytes) 0b01 - Two set registers, two clear registers, four control registers (32 bytes) 0b10 - Four set registers, four clear registers, eight control registers (64 bytes) 0b11 - Eight set registers, eight clear registers, sixteen control registers (128 bytes) This bit field shall be read only.
8-21	PAG_mask_ptr	see footnote[2]	The PAG_mask_ptr value shall be the maintenance offset of the Port n Port Aggregation Mask 0 Set Register 0 CSR, divided by 1024.The maintenance offset of the Port n Port Aggregation Mask 0 Set Register 0 CSR shall be a 1024 byte aligned address. The PAG_ptr value shall indicate an address in Implementation Defined register space.
22-31	___	0b00	Reserved

[1]The PAG_mask_size reset value is implementation dependent

[2]The PAG_mask_ptr reset value is implementation dependent

4.4.8 Broadcast Multicast Mask x Set Register y CSR (Offset = (Mask_Ptr * 0x400) + (x*8*2^{Mask_size}) + (y*4))

Writes to the Broadcast Multicast Mask x Set Register y CSRs shall cause the corresponding Port n Multicast Mask x Set Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-23. This register supports both read and write. Bits are set by writing 1 to them. Bits cannot be cleared using this register.

Table 4-24 gives an example layout of a Multicast Mask x Set Register y CSR when Virtual_port_count is 8 and sixteen physical ports are present.

Table 4-23. Bit Settings for Broadcast Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which physical and/or virtual ports are enabled in this multicast mask/virtual port mask. The multicast mask/virtual port mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Multicast mask bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Bits shall be assigned to virtual ports as the port aggregation group number increases. The first virtual port bit shall be assigned to the bit immediately after the highest numbered physical port. The first virtual port bit shall control inclusion of the Port Aggregation Group 0 in the multicast mask. Each bit shall be encoded as follows: 0b0 - The corresponding port is disabled in the multicast mask 0b1 - The corresponding port is enabled in the multicast mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to physical and virtual ports which do not exist in the device shall be reserved.

Table 4-24. Example Fields for Broadcast Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-7	___	0b00	Reserved
8	Virtual Port 7	0	Set if Port Aggregation Group 7 is included in this multicast mask
9	Virtual Port 6	0	Set if Port Aggregation Group 6 is included in this multicast mask
10	Virtual Port 5	0	Set if Port Aggregation Group 5 is included in this multicast mask
11	Virtual Port 4	0	Set if Port Aggregation Group 4 is included in this multicast mask
12	Virtual Port 3	0	Set if Port Aggregation Group 3 is included in this multicast mask
13	Virtual Port 2	0	Set if Port Aggregation Group 2 is included in this multicast mask
14	Virtual Port 1	0	Set if Port Aggregation Group 1 is included in this multicast mask
15	Virtual Port 0	0	Set if Port Aggregation Group 0 is included in this multicast mask
16	Port 15	0	Set if Port 15 is included in this multicast mask
17	Port 14	0	Set if Port 14 is included in this multicast mask
18	Port 13	0	Set if Port 13 is included in this multicast mask
19	Port 12	0	Set if Port 12 is included in this multicast mask
20	Port 11	0	Set if Port 11 is included in this multicast mask
21	Port 10	0	Set if Port 10 is included in this multicast mask
22	Port 9	0	Set if Port 9 is included in this multicast mask

Table 4-24. Example Fields for Broadcast Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
23	Port 8	0	Set if Port 8 is included in this multicast mask
24	Port 7	0	Set if Port 7 is included in this multicast mask
25	Port 6	0	Set if Port 6 is included in this multicast mask
26	Port 5	0	Set if Port 5 is included in this multicast mask
27	Port 4	0	Set if Port 4 is included in this multicast mask
28	Port 3	0	Set if Port 3 is included in this multicast mask
29	Port 2	0	Set if Port 2 is included in this multicast mask
30	Port 1	0	Set if Port 1 is included in this multicast mask
31	Port 0	0	Set if Port 0 is included in this multicast mask

4.4.9 Broadcast Multicast Mask x Clear Register y CSR (Offset = (Mask_Ptr * 0x400) + (x * 8*2^{Mask_size}) + (4*2^{Mask_size}) + (y*4))

Writes to the Broadcast Multicast Mask x Clear Register y CSRs shall cause the corresponding Port n Multicast Mask x Clear Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-25. This register supports both read and write. Bits are cleared by writing 1 to them. Bits cannot be set using this register.

Table 4-25. Bit Settings for Broadcast Multicast Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which physical and/or virtual ports are enabled in this multicast mask/virtual port mask. The multicast mask/virtual port mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Multicast mask bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Bits shall be assigned to virtual ports as the port aggregation group number increases. The first virtual port bit shall be assigned to the bit immediately after the highest numbered physical port. The first virtual port bit shall control inclusion of the Port Aggregation Group 0 in the multicast mask. Each bit shall be encoded as follows: 0b0 - The corresponding port is disabled in the multicast mask 0b1 - The corresponding port is enabled in the multicast mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to physical and virtual ports which do not exist in the device shall be reserved.

4.4.10 Broadcast Port Aggregation Mask x Set Register y CSR (Offset = (Mask_Ptr * 0x400) + (x*16*2^{Mask_size}) + (y*4))

Writes to the Broadcast Port Aggregation Mask x Set Register y CSRs shall cause the corresponding Port n Port Aggregation Mask x Set Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-26. Unless otherwise specified, the bits and bit fields in this register may be write only.

Table 4-26. Bit Settings for Broadcast Port Aggregation Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	PAG_ctl	All 0's	This register controls which physical ports are enabled in a port aggregation mask. The port aggregation mask functionality for physical ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Each bit shall be encoded as follows: 0b0 - This port is disabled in the port aggregation mask 0b1 - This port is enabled in the port aggregation mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to physical ports which do not exist in the device shall be reserved.

4.4.11 Broadcast Port Aggregation Mask x Clear Register y CSR (Offset = (Mask_Ptr * 0x400) + (x * 16*2^{Mask_size}) + (4*2^{Mask_size}) + (y*4))

Writes to the Broadcast Port Aggregation Mask x Clear Register y CSRs shall cause the corresponding Port n Port Aggregation Mask x Clear Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-27. Unless otherwise specified, the bits and bit fields in this register may be write only.

Table 4-27. Bit Settings for Broadcast Port Aggregation Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	PAG_ctl	All 0's	This register controls which physical ports are enabled in a port aggregation mask. The port aggregation mask functionality for physical ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Each bit shall be encoded as follows: 0b0 - This port is disabled in the port aggregation mask 0b1 - This port is enabled in the port aggregation mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to physical ports which do not exist in the device shall be reserved.

4.4.12 Broadcast Port Aggregation Mask x Control Register 0 CSR

(Offset = (PAG_Ptr * 0x400) + (x * 16*2^{PAG_mask_size}) + (8*2^{PAG_mask_size}))

Writes to the Broadcast Port Aggregation Mask x Control Register 0 CSR shall cause the corresponding Port n Port Aggregation Mask x Control Register 0 CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-28. The bits and bit fields in this register support implementation specific functionality. Unless otherwise specified, the bits and bit fields in this register may be write only.

Table 4-28. Bit Settings for Broadcast Port Aggregation Mask x Control Register 0 CSR

Bit	Name	Reset Value	Description
0-7	___	0	Reserved
8-15	PAG_Default	0	For PAG_Control value 0, PAG_Default is the default port selected according to the algorithm specified in Chapter 3.3.1, “Fail-over Port Selection,” on page 20. This field is reserved for control values 0x01 to 0x7F. This field is implementation specific for control values 0x80 to 0xFF.
16-23	PAG_Selected	0	This field shall contain the physical port number selected for the last packet routed according to this PAG. Writes to this field are ignored.
24-31	PAG_Control	All 0’s	The value of this field determines the port selection algorithm for this port aggregation mask. A value of 0 shall cause packets to be routed according to the port selection algorithm specified in Chapter 3.3.1, “Fail-over Port Selection,” on page 20. Values 0x01 to 0x7F are reserved. Values 0x80 to 0xFF are implementation specific.

4.4.13 Broadcast Port Aggregation Mask x Control Register y CSR

(Offset = (PAG_Ptr * 0x400) + (x * 16*2^{PAG_mask_size}) + (8*2^{PAG_mask_size}) + (y*4))

‘Y’ shall not be equal to 0. Writes to the Broadcast Port Aggregation Mask x Control Register y CSRs shall cause the corresponding Port n Port Aggregation Mask x Control Register y CSRs for all ports to assume the value written. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-29. The bits and bit fields in this register support implementation specific functionality. Unless otherwise specified, the bits and bit fields in this register may be write only.

Table 4-29. Bit Settings for Broadcast Port Aggregation Mask x Control Register y CSR

Bit	Name	Reset Value	Description
0-31	Private	0	Implementation specific functionality.

4.4.14 Port n Multicast Mask x Set Register y CSR (Offset = (Mask_Ptr * 400) + (x * 8*2^{Mask_size}) + (y*4))

This register shall control the multicast behavior for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-30. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 4-30. Bit Settings for Port n Multicast Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which physical and/or virtual ports are enabled in this multicast mask/virtual port mask. The multicast mask/virtual port mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Multicast mask bits shall be assigned to physical ports sequentially as the port number increases. The lowest numbered port shall be assigned to Bit 31. Bits shall be assigned to virtual ports as the port aggregation group number increases. The first virtual port bit shall be assigned to the bit immediately after the highest numbered physical port. The first virtual port bit shall control inclusion of the Port Aggregation Group 0 in the multicast mask. Each bit shall be encoded as follows: 0b0 - The corresponding port is disabled in the multicast mask 0b1 - The corresponding port is enabled in the multicast mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to physical and virtual ports which do not exist in the device shall be reserved.

4.4.15 Port n Multicast Mask x Clear Register y CSR (Offset = (Mask_Ptr * 400) + (x * 8*2^{Mask_size}) + (4*2^{Mask_size}) + (y*4))

This register shall control the multicast behavior for all ports whose Port n Multicast Info CSR Mask_Ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-31. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 4-31. Bit Settings for Port n Multicast Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	Mcast_ctl	All 0's	This register controls which physical and/or virtual ports are enabled in this multicast mask/virtual port mask. The multicast mask/virtual port mask functionality for ports (y*32) to (y*32+31) shall be controlled by this register. Multicast mask bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Bits shall be assigned to virtual ports as the port aggregation group number increases. The first virtual port bit shall be assigned to the bit immediately after the highest numbered port. The first virtual port bit shall control inclusion of the Port Aggregation Group 0 in the multicast mask. Each bit shall be encoded as follows: 0b0 - The corresponding port is disabled in the multicast mask 0b1 - The corresponding port is enabled in the multicast mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to physical and virtual ports which do not exist in the device shall be reserved.

4.4.16 Port n Port Aggregation Mask x Set Register y CSR (Offset = (PAG_Mask_Ptr * 0x400) + (x*16*$2^{PAG\_mask\_size}$) + (y*4))

This register shall control the port aggregation group behavior for all ports whose Port n Port Aggregation Mask Info CSR PAG_mask_ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-32. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 4-32. Bit Settings for Port n Aggregation Mask x Set Register y CSR

Bit	Name	Reset Value	Description
0-31	PAG_ctl	All 0's	This register controls which physical ports are enabled in a port aggregation mask. The port aggregation mask functionality for physical ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Each bit shall be encoded as follows: 0b0 - This port is disabled in the port aggregation mask 0b1 - This port is enabled in the port aggregation mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall set the bit value. Bits corresponding to physical ports which do not exist in the device shall be reserved.

4.4.17 Port n Port Aggregation Mask x Clear Register y CSR (Offset = (Mask_Ptr * 0x400) + (x * 16*2^{PAG_mask_size}) + (4*2^{PAG_mask_size}) + (y*4))

This register shall control the port aggregation group behavior for all ports whose Port n Port Aggregation Mask Info CSR PAG_mask_ptr field value is the same. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-33. Unless otherwise specified, the bits and bit fields in this register are read/write.

Table 4-33. Bit Settings for Port n Port Aggregation Mask x Clear Register y CSR

Bit	Name	Reset Value	Description
0-31	PAG_ctl	All 0's	This register controls which physical ports are enabled in a port aggregation mask. The port aggregation mask functionality for physical ports (y*32) to (y*32+31) shall be controlled by this register. Bits shall be assigned to physical ports sequentially as the physical port number increases. The lowest numbered physical port shall be assigned to Bit 31. Each bit shall be encoded as follows: 0b0 - This port is disabled in the port aggregation mask 0b1 - This port is enabled in the port aggregation mask Writing 0 to a bit shall not change the bit value. Writing 1 to a bit shall clear the bit value. Bits corresponding to physical ports which do not exist in the device shall be reserved.

4.4.18 Port n Port Aggregation Mask x Control Register 0 CSR (Offset = (PAG_Ptr * 0x400) + (x * 16*2^{PAG_mask_size}) + (8*2^{PAG_mask_size}))

The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-34. The bits and bit fields in this register support implementation specific functionality.

Table 4-34. Bit Settings for Port n Port Aggregation Mask x Control Register 0 CSR

Bit	Name	Reset Value	Description
0-7	___	0	Reserved
8-15	PAG_Default	0	For PAG_Control value 0, PAG_Default is the default port selected according to the algorithm specified in Chapter 3.3.1, "Fail-over Port Selection," on page 20. This field is reserved for control values 0x01 to 0x7F. This field is implementation specific for control values 0x80 to 0xFF.
16-23	PAG_Selected	0	The last port successfully selected for this PAG. Writes to this field are ignored.
24-31	PAG_Control	All 0's	The value of this field determines the port selection algorithm for this port aggregation group. A value of 0 shall cause packets to be routed according to the port selection algorithm specified in Chapter 3.3.1, "Fail-over Port Selection," on page 20. Values 0x01 to 0x7F are reserved. Values 0x80 to 0xFF are implementation specific.

4.4.19 Port n Port Aggregation Mask x Control Register y CSR (Offset = (PAG_Ptr * 0x400) + (x * 16*2^{PAG_mask_size}) + (8*2^{PAG_mask_size}) + (y*4))

'Y' shall not be equal to 0. The use and meaning of the bits and bit fields of this register shall be as specified in Table 4-35. The bits and bit fields in this register support implementation specific functionality.

Table 4-35. Bit Settings for Port n Port Aggregation Mask x Control Register y CSR

Bit	Name	Reset Value	Description
0-31	Private	0	Implementation specific functionality.

Chapter 5 Configuration Examples

5.1 Introduction

This chapter provides several examples of how to use the multicast programming interface. The given examples build upon each other while proceeding through the sections. References to the order of operations within the examples run from the top of a list to the bottom unless otherwise stated.

Initially assume a switch with 8 ports which supports 4 or more multicast masks with two or more destination IDs allowed per multicast group so that a total of 8 destination IDs minimum can be associated with the multicast masks. The system has the following requirements:

- Three sources of traffic (ports 0, 1, and 2) must be multicast to two destinations (ports 6 and 7).
- Three ports (ports 3, 4 and 5) need to multicast signals between each other.
- All ports occasionally need to multicast to every other port.

Assume that the switch does not require any other multicast functions and therefore multicast masks 0, 1, and 2 will be used.

5.2 Configuring Multicast Masks

This section discusses assigning an egress port list to a multicast mask.

5.2.1 Clearing Multicast Masks

Suppose that the state of the multicast masks is unknown, and therefore the masks must be cleared before being configured. In order to clear the masks the following register accesses are made. (The accesses to the Multicast Mask Port CSR can be performed in any order.)

- Remove all ports from multicast mask 0
  - — Write the value 0x0000_0040 to the Multicast Mask Port CSR
- Remove all ports from multicast mask 1
  - — Write the value 0x0001_0040 to the Multicast Mask Port CSR
- Remove all ports from multicast mask 2
  - — Write the value 0x0002_0040 to the Multicast Mask Port CSR

5.2.2 Assigning Ports to Multicast Masks

To configure mask 0 to multicast to ports 6 and 7, mask 1 to multicast to ports 3, 4 and 5, and mask 2 to multicast to every port, requires the following series of register accesses. (The accesses to the Multicast Mask Port CSR can be performed in any order.)

- Add port 6 to multicast mask 0
  - — Write the value 0x0000_0610 to the Multicast Mask Port CSR
- Add port 7 to multicast mask 0
  - — Write the value 0x0000_0710 to the Multicast Mask Port CSR
- Add port 3 to multicast mask 1
  - — Write the value 0x0001_0310 to the Multicast Mask Port CSR
- Add port 4 to multicast mask 1
  - — Write the value 0x0001_0410 to the Multicast Mask Port CSR
- Add port 5 to multicast mask 1
  - — Write the value 0x0001_0510 to the Multicast Mask Port CSR
- Add all ports to multicast mask 2
  - — Write the value 0x0002_0050 to the Multicast Mask Port CSR

5.2.3 Removing a Port from a Multicast Mask

Suppose that the device attached to port 4 needs to be removed from the system. The following register accesses are used to modify multicast masks 1 and 2 to stop port 4 from being a multicast destination. (The accesses may be performed in any order.)

- Remove port 4 from multicast mask 1
  - — Write the value 0x0001_0420 to the Multicast Mask Port CSR
- Remove port 4 from multicast mask 2
  - — Write the value 0x0002_0420 to the Multicast Mask Port CSR

5.2.4 Querying a Multicast Mask

In this section suppose that a system designer needs to determine which of the 8 ports are included in multicast mask 2. The following accesses are to be performed to provide this information. (In each case, the write operation setting up the ‘Write to Verify’ operation must be performed before the subsequent read to check the Port Present bit status. The individual multicast masks may be queried in any order.)

- Verify that port 0 is included in mask 2
  - — Write the value 0x0002_0000 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0001 from the Multicast Mask Port CSR

- Verify that port 1 is included in mask 2
  - — Write the value 0x0002_0100 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0101 from the Multicast Mask Port CSR.
- Verify that port 2 is included in mask 2
  - — Write the value 0x0002_0200 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0201 from the Multicast Mask Port CSR
- Verify that port 3 is included in mask 2
  - — Write the value 0x0002_0300 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0301 from the Multicast Mask Port CSR
- Verify that port 4 is not included in mask 2
  - — Write the value 0x0002_0400 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0400 from the Multicast Mask Port CSR
- Verify that port 5 is included in mask 2
  - — Write the value 0x0002_0500 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0501 from the Multicast Mask Port CSR
- Verify that port 6 is included in mask 2
  - — Write the value 0x0002_0600 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0601 from the Multicast Mask Port CSR
- Verify that port 7 is included in mask 2
  - — Write the value 0x0002_0700 to the Multicast Mask Port CSR
  - — Read the value 0x0002_0701 from the Multicast Mask Port CSR

5.3 Simple Association

If the Simple_Assoc bit is set in the Switch Multicast Support CAR, the device supports the simple multicast programming model. This model allows for basic multicast support for devices with a limited number of multicast masks, and requires a fixed relationship between those masks and sequential multicast groups.

5.3.1 Restrictions on Block Size

If the Simple_Assoc bit is set the device has a limited number of masks. Therefore, the number of sequential associations equals the maximum number of masks.

The Assoc_BlkSize field in the Multicast Associate Operation CSR must be set to the value of (MaxMCastMasks - 1). The MaxMCastMasks field is in the Switch Multicast Information CAR.

5.3.2 Restrictions on Block Associate

If the Simple_Assoc bit is set, non-block associations are precluded.

5.3.3 Restrictions on Associations

If the Simple_Assoc bit is set the device requires a fixed relationship between the sequential mask numbers and sequential destination IDs. This must be taken into account when the masks are associated.

The Multicast Associate Select CSR is set with the Mcast_Mask_num value set to 0x0000 and the Large_DestID and DestID fields set to an integer multiple of the MaxMCastMasks value.

Hardware that sets the new Simple_Assoc CAR bit could implement a single block associate for all of the masks that it supports with the requirement that they all be sequential destination IDs.

5.4 Configuring Associations

This section describes how to associate destination IDs with multicast masks, including examples of how to use the block association and per-port association functions.

5.4.1 Basic Association

For the assumed system it is now necessary to associate a destination ID with each multicast mask from the preceding examples. How this can be accomplished may vary depending on the capabilities of the switch. For this section, assume that neither block association nor per-ingress-port association is supported by the switch.

Following upon the previous example, assume the following additional system requirements.

- the 16 bit destination ID 0x1234 needs to be associated with multicast mask 0.
- the 8 bit destination ID 0x44 needs to be associated with multicast mask 1.
- the 16 bit destination ID 0xFEED needs to be associated with multicast mask 2.

In order to accomplished the desired associations, the following register accesses are required. (The individual association operations can be performed in any order.)

- Set up the operation to associate destination ID 0x1234 with multicast mask 0
  - — Write the value 0x1234_0000 to the Multicast Associate Select CSR
- Associate destination ID 0x1234 with multicast mask 0
  - — Write the value 0x0000_00E0 to the Multicast Associate Operation CSR
- Set up the operation to associate destination ID 0x44 with multicast mask 1

— Write the value 0x0044_0001 to the Multicast Associate Select CSR

- Associate destination ID 0x44 with multicast mask 1

— Write the value 0x0000_0060 to the Multicast Associate Operation CSR

- Set up the operation to associate destination ID 0xFEED with multicast mask 2

— Write the value 0xFEED_0002 to the Multicast Associate Select CSR

- Associate destination ID 0xFEED with multicast mask 2

— Write the value 0x0000_00E0 to the Multicast Associate Operation CSR

5.4.2 Using Per-Ingress Port Association

For the associations discussed in the preceding section, if the switch supports per-ingress-port association (destination IDs are associated with multicast masks on a per ingress port basis), the required programming operations change. The associations for each multicast mask are grouped into a write to the Multicast Associate Select CSR, followed by a write to the Multicast Associate Operation CSR for each ingress port that must be aware of the association. (The writes to the Multicast Associate Operation CSR can occur in any order but must occur after the related writes to the Multicast Associate Select CSR. The individual association operations can be performed in any order.)

- Set up the operation to associate destination ID 0x1234 with multicast mask 0

— Write the value 0x1234_0000 to the Multicast Associate Select CSR

- Associate destination ID 0x1234 with multicast mask 0 on ingress port 0

— Write the value 0x0000_00E0 to the Multicast Associate Operation CSR

- Associate destination ID 0x1234 with multicast mask 0 on ingress port 1

— Write the value 0x0000_01E0 to the Multicast Associate Operation CSR

- Associate destination ID 0x1234 with multicast mask 0 on ingress port 2

— Write the value 0x0000_02E0 to the Multicast Associate Operation CSR

- Set up the operation to associate destination ID 0x44 with multicast mask 1

— Write the value 0x0044_0001 to the Multicast Associate Select CSR

- Associate destination ID 0x44 with multicast mask 1 on ingress port 3

— Write the value 0x0000_0360 to the Multicast Associate Operation CSR

- Associate destination ID 0x44 with multicast mask 1 on ingress port 4

— Write the value 0x0000_0460 to the Multicast Associate Operation CSR

- Associate destination ID 0x44 with multicast mask 1 on ingress port 5

— Write the value 0x0000_0560 to the Multicast Associate Operation CSR

- Set up the operation to associate destination ID 0xFEED with multicast mask 2

— Write the value 0xFEED_0002 to the Multicast Associate Select CSR

- Associate destination ID 0xFEED with multicast mask 2 on ingress port 0

— Write the value 0x0000_00E0 to the Multicast Associate Operation CSR

- Associate destination ID 0xFEED with multicast mask 2 on ingress port 1
  — Write the value 0x0000_01E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 2
  — Write the value 0x0000_02E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 3
  — Write the value 0x0000_03E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 4
  — Write the value 0x0000_04E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 5
  — Write the value 0x0000_05E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 6
  — Write the value 0x0000_06E0 to the Multicast Associate Operation CSR
- Associate destination ID 0xFEED with multicast mask 2 on ingress port 7
  — Write the value 0x0000_07E0 to the Multicast Associate Operation CSR

5.4.3 Using Block Association

In this section assume that the switch supports block association rather than per-ingress-port association. With this feature sequential destination IDs can be quickly associated to sequential multicast masks. In order to take advantage of this feature, different destination IDs assignments are required for the system than for the preceding examples. The starting destination 0xFF00 is arbitrarily selected.

- the 16 bit destination ID 0xFF00 is used to multicast from ports 0, 1 and 2 to ports 6 and 7, so destination ID 0xFF00 needs to be associated with multicast mask 0.
- the 16 bit destination ID 0xFF01 identifies the multicast group including ports 3, 4 and 5, so destination ID 0xFF01 needs to be associated with multicast mask 1.
- the 16 bit destination ID 0xFF02 identifies the multicast group that includes all ports, so destination ID 0xFF02 needs to be associated with multicast mask 2.

Note that the number of accesses needed to accomplish the desired associations is reduced to two. (The accesses must be performed in the order given.)

- Set up the associate operation starting with destination ID 0xFF00 and multicast mask 0
  — Write the value 0xFF00_0000 to the Multicast Associate Select CSR
- Associate three sequential destination IDs starting at 0xFF00 with three sequential multicast masks starting at 0
  — Write the value 0x0002_00E0 to the Multicast Associate Operation CSR

5.4.4 Using Per-Ingress Port and Block Association

Next, if both block association and per-ingress port association are supported by the switch, then the following sequence of operations is required. (The write to the Multicast Associate Select CSR must occur before the corresponding write to the Multicast Associate Operation CSR. The individual association operations can be performed in any order.)

- Set up the associate operations starting with destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF00_0000 to the Multicast Associate Select CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 0
  - — Write the value 0x0002_00E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 1
  - — Write the value 0x0002_01E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 2
  - — Write the value 0x0002_02E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 3
  - — Write the value 0x0002_03E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 4
  - — Write the value 0x0002_04E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 5
  - — Write the value 0x0002_05E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 6
  - — Write the value 0x0002_06E0 to the Multicast Associate Operation CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 7
  - — Write the value 0x0002_07E0 to the Multicast Associate Operation CSR

For this example, suppose that ingress port 4 needs a second destination ID to be mapped to each of the three multicast masks and the switch also has this capability. The second destination would be added to port 4 with the following association operation. (The write to the Multicast Associate Select CSR must occur before the write to the Multicast Associate Operation CSR.

- Set up the associate operations starting with destination ID 0xFF03 and multicast mask 0
  - — Write the value 0xFF03_0000 to the Multicast Associate Select CSR
- Associate three sequential destination IDs with three sequential multicast masks for ingress port 4
  - — Write the value 0x0002_04E0 to the Multicast Associate Operation CSR

5.4.5 Removing a Destination ID to Multicast Mask Association

Now assume that packets from destination ID 0xFF02 on port 4 should no longer be allowed to multicast to all nodes (multicast mask 2). To remove destination ID 0xFF02 from being associated with multicast mask 2 on port 4, the following register accesses need to be performed in order.

- Set up the operation to remove the association between destination ID 0xFF02 and multicast mask 2
  - — Write the value 0xFF02_0002 to the Multicast Associate Select CSR
- Remove the association between destination ID 0xFF02 and multicast mask 2 on ingress port 4
  - — Write the value 0x0000_04C0 to the Multicast Associate Operation CSR

5.4.6 Querying an Association

There are three scenarios for querying destination ID to multicast mask associations in a switch. For the first scenario assume that a system designer wants to know which multicast masks are associated with destination ID 0xFF01 on port 4. Note that since a read of the Multicast Associate Operation CSR causes the last command written to be executed, that register is only written at the beginning of the sequence. (The individual associations can be queried in any order.)

- Set up the associate operations for destination ID 0xFF01 and multicast mask 0
  - — Write the value 0xFF01_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF01 is not associated with multicast mask 0 for port 4
  - — Write the value 0x0000_0480 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF01 and multicast mask 1
  - — Write the value 0xFF01_0001 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF01 is not associated with multicast mask 1 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR

- Set up the associate operations for destination ID 0xFF01 and multicast mask 2
  - — Write the value 0xFF01_0002 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF01 is associated with multicast mask 2 for port 4
  - — Read the value 0x0000_0481 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF01 and multicast mask 3
  - — Write the value 0xFF01_0003 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF01 is not associated with multicast mask 3 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR

For the second scenario assume that the system designer wants to know which destination IDs from 0xFF00 through 0xFF07 are associated with multicast mask 0 on Port 4. (The individual associations may be queried in any order.)

- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF00_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF00 is associated with multicast mask 0 for port 4
  - — Write the value 0x0000_0480 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF01_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF01 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF02_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF02 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF03_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR

- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF04_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF04 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF05_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF05 is associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0481 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF06_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF06 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Set up the associate operations for destination ID 0xFF00 and multicast mask 0
  - — Write the value 0xFF07_0000 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF07 is not associated with multicast mask 0 for port 4
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR

For the last scenario assume that the system designer now wants to know whether or not destination ID 0xFF03 is mapped to multicast mask 3 on all ports. (The individual associations may be queried in any order.)

- Set up the associate operations for destination ID 0xFF03 and multicast mask 3
  - — Write the value 0xFF03_0003 to the Multicast Associate Select CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 0
  - — Write the value 0x0000_0080 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0080 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 1
  - — Write the value 0x0000_0180 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0180 from the Multicast Associate Operation CSR

- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 2
  - — Write the value 0x0000_0280 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0280 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is associated with multicast mask 3 for port 3
  - — Write the value 0x0000_0380 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0381 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 4
  - — Write the value 0x0000_0480 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0480 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 5
  - — Write the value 0x0000_0580 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0580 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 6
  - — Write the value 0x0000_0680 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0680 from the Multicast Associate Operation CSR
- Verify that destination ID 0xFF03 is not associated with multicast mask 3 for port 7
  - — Write the value 0x0000_0780 to the Multicast Associate Operation CSR
  - — Read the value 0x0000_0780 from the Multicast Associate Operation CSR

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Annex A End Point Considerations (Informative)

A.1 Introduction

This appendix provides implementation considerations for end points that are intended to be used in a multicast RapidIO system.

A.2 Multicast Destination ID

The transport layer requirement that processing elements be capable of accepting requests regardless of destinationID means that all end points are capable of accepting multicast traffic for all possible multicast destinationIDs. The destinationID of a multicast request may be checked by implementation-specific means.

A.3 End Point Multicast Channels

It may be valuable for an end point to have support for one or more multicast channels. Multicast channels are address ranges in RapidIO address space for which an end point may accept a multicast packet and possibly translate the RapidIO write address to another local address region. This is necessary if the recipient of a multicast transaction does not have valid address space at the address received. The size and quantity of multicast channels depend on the requirements of the application. It may also be necessary to link multicast channels to particular multicast groups.

A multicast channel valid bit can be implemented to control whether an address out-of-range error occurs for a received address which falls inside a multicast channel address range. A multicast channel enable bit can control whether an end point silently ignores the packet when an address is received which falls inside the channel address range. The enable bit allows software finer control over which end points for a particular multicast ID will actually process the multicast write without modifying switch settings in the fabric.

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Annex B Multicast Applications (Informative)

B.1 Introduction

In a multi-switch RapidIO fabric, each switch which supports multicast in the fabric will have it's own set of multicast masks. The particular multicast mask in each switch device associated with a multicast group is very likely to have a different egress port pattern enabled, depending upon where that switch is in the switch fabric topology.

As an example, refer to the following system, where data streams entering switch A1 need to be sent to a set of destinations. There are several possible approaches to implementing this system. The first example is based on the number of different multicast groups that must be supported. Destinations are linked to a destination ID which in turn is associated with static multicast mask values. In the second example, a specific multicast mask in each switch is associated with each possible destination. The destinations are linked statically to destination IDs.

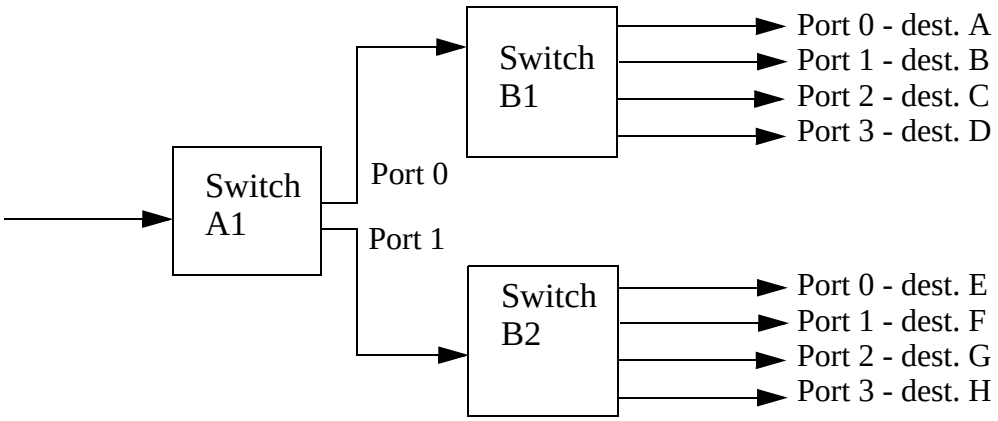

Figure 5-1. Example System using Multicast

B.2 Example 1 - Static Multicast Masks

If there are 256 combinations of destinations to receive a data stream, multicast requires 256 multicast groups, associated with 256 destination IDs. This means that an 8 bit destination ID could be used, but then there would be no destination IDs left over for control traffic in the system. As a result, this example assumes that the system needs to use 16 bit destination IDs in order to support multicast.

It is possible to use the least significant 4 bits of the 16 bit destination ID to identify which ports in Switch B1 need to be multicast to, and the next most significant 4 bits for the ports on B2. Arbitrarily selecting the value of 0x04 for the upper byte of the destination ID, then all multicast destination IDs have a format of 0x04XY, where X selects the ports in switch B2 and Y selects the ports in switch B1.

Switch A1 therefore needs two multicast masks as shown in Table 5-1.

Table 5-1. Multicast Masks for Switch A1

Multicast Mask Index	Egress Ports	Description
0	None	Associated with destination ID 0x0400, indicating that no destination is to receive this data stream. Packets multicast with destination ID of 0x0400 are dropped without notification.
1	Port 0 and port 1	Associated with destination IDs 0x04XY, where both X and Y is not 0. These represent all destination IDs which need only be multicast to both Switch B1 and switch B2.

Destination IDs of the form 0x040Y, where Y is non-zero, or 0x04X0, where X is non zero, do not have to be replicated. They can be routed directly to either port 0 (for 0x040Y) or port 1 (0x04X0) using the standard switch routing tables since there is only a single egress port.

Because Multicast Mask 1 must have 223 ((256 total) - (16 for X) - (16 for Y) - (1 for none)) destination IDs associated with it, the Switch Multicast Information CAR MaxDestIDAssociations field must contain a value of at least 222. In this particular case, the easiest internal implementation for the selection of packets to be multicast may be the use of a non-existent port in the routing table. For example, since Switch A1 has three ports, make use of a non-existent port value in the routing table to signify that the packet is subject to multicast.

Switches B1 and B2 must have 16 multicast masks, each associated with a particular combination of their egress ports 0 through 3. Each multicast mask may have 16 destination IDs associated with it, so the Switch Multicast Information CAR MaxDestIDAssociations field must contain a value of at least 15.

Table 5-2 describes which destination IDs must be associated with each multicast group for Switches B1. Note that for index 0, if the routing tables in Switch A1 are set up correctly, no packets with those multicast groups should reach switch B1.

Table 5-2. Multicast Masks for Switch B1

Multicast Mask Index	Egress Ports	Description
0	None	Associated with the following destination IDs: 0x0400 0x0410 0x0420 ... 0x04E0 0x04F0
1	Port 0	Associated with the following destination IDs: 0x0401 0x0411 0x0421 ... 0x04E1 0x04F1
2	Port 1	Associated with the following destination IDs: 0x0402 0x0412 0x0422 ... 0x04E2 0x04F2
3	Ports 1and 0	Associated with the following destination IDs: 0x0403 0x0413 ... 0x04E3 0x04F3
4	Port 2	Associated with the following destination IDs: 0x0404 0x0414 0x0424 ... 0x04E4 0x04F4
5	Ports2 and 0	Associated with the following destination IDs: 0x0405 0x0415 0x0425 ... 0x04E5 0x04F5
6	Ports2 and 1	Associated with the following destination IDs: 0x0406 0x0416 0x0426 ... 0x04E6 0x04F6

Table 5-2. Multicast Masks for Switch B1

Multicast Mask Index	Egress Ports	Description
7	Ports 2, 1 and 0	Associated with the following destination IDs: 0x0407 0x0417 0x0427 ... 0x04E7 0x04F7
8	Port 3	Associated with the following destination IDs: 0x0408 0x0418 0x0428 ... 0x04E8 0x04F8
9	Ports 3 and 0	Associated with the following destination IDs: 0x0409 0x0419 0x0429 ... 0x04E9 0x04F9
10	Ports 3 and 1	Associated with the following destination IDs: 0x040A 0x041A 0x042A ... 0x04EA 0x04FA
11	Ports 3, 1 and 0	Associated with the following destination IDs: 0x040B 0x041B 0x042B ... 0x04EB 0x04FB
12	Ports3 and2	Associated with the following destination IDs: 0x040C 0x041C 0x042C ... 0x04EC 0x04FC
13	Ports 3, 2 and 0	Associated with the following destination IDs: 0x040D 0x041D 0x042D ... 0x04ED 0x04FD

Table 5-2. Multicast Masks for Switch B1

Multicast Mask Index	Egress Ports	Description
14	Ports 3, 2 and 1	Associated with the following destination IDs: 0x040E 0x041E 0x042E ... 0x04EE 0x04FE
15	Ports 3, 2, 1 and 0	Associated with the following destination IDs: 0x040F 0x041F 0x042F ... 0x04EF 0x04FF

Table 5-2 describes which destination IDs must be associated with each multicast group for Switches B1. Note that for index 0, if the routing tables in Switch A1 are set up correctly, no packets with those multicast groups should reach switch B2.

Table 5-3. Multicast Masks for Switch B2

Multicast Mask Index	Egress Ports	Description
0	None	Associated with the following destination IDs: 0x0400 0x0401 0x0402 ... 0x040E 0x040F
1	Port 0	Associated with the following destination IDs: 0x0410 0x0411 0x0412 ... 0x041E 0x041F
2	Port 1	Associated with the following destination IDs: 0x0420 0x0421 0x0422 ... 0x042E 0x042F
3	Ports 1and 0	Associated with the following destination IDs: 0x0430 0x0431 0x0432 ... 0x043E 0x043F

Table 5-3. Multicast Masks for Switch B2

Multicast Mask Index	Egress Ports	Description
4	Port 2	Associated with the following destination IDs: 0x0440 0x0441 0x0442 ... 0x044E 0x044F
5	Ports2 and 0	Associated with the following destination IDs: 0x0450 0x0451 0x0452 ... 0x045E 0x045F
6	Ports2 and 1	Associated with the following destination IDs: 0x0460 0x0461 0x0462 ... 0x046E 0x046F
7	Ports 2, 1 and 0	Associated with the following destination IDs: 0x0470 0x0471 0x0472 ... 0x047E 0x047F
8	Port 3	Associated with the following destination IDs: 0x0480 0x0481 0x0482 ... 0x048E 0x048F
9	Ports 3 and 0	Associated with the following destination IDs: 0x0490 0x0491 0x0492 ... 0x049E 0x049F
10	Ports 3 and 1	Associated with the following destination IDs: 0x04A0 0x04A1 0x04A2 ... 0x04AE 0x04AF

Table 5-3. Multicast Masks for Switch B2

Multicast Mask Index	Egress Ports	Description
11	Ports 3, 1 and 0	Associated with the following destination IDs: 0x04B0 0x04B1 0x04B2 ... 0x04BE 0x04BF
12	Ports3 and2	Associated with the following destination IDs: 0x04C0 0x04C1 0x04C2 ... 0x04CE 0x04CF
13	Ports 3, 2 and 0	Associated with the following destination IDs: 0x04D0 0x04D1 0x04D2 ... 0x04DE 0x04DF
14	Ports 3, 2 and 1	Associated with the following destination IDs: 0x04E0 0x04E1 0x04E2 ... 0x04EE 0x04EF
15	Ports 3, 2, 1 and 0	Associated with the following destination IDs: 0x04F0 0x04F1 0x04F2 ... 0x04FE 0x04FF

It is up to the application whether either of the switch routing tables should be used for the destination IDs associated with multicast masks 1, 2, 4, and 8, as packets for these destination IDs do not have to be replicated.

Configuring each of the 16 multicast masks for switches B1 and B2 should require a maximum of 2 writes to the Multicast Mask Load CSR. Multicast masks with one or two ports require a number of register writes equal to the number of ports. Multicast masks with three egress ports to be selected should add all of the ports and then remove the port which doesn’t belong in the multicast mask, thus requiring a maximum of two register writes. The multicast mask with all ports selected requires 1 register write. Thus, to configure all 16 of the multicast masks requires a maximum of (0 + (5*1) + (10*2))=25 register write operations.

For the destination ID to multicast mask association operations for Switch B1, it

would make sense to implement block association operations since this would greatly reduce the amount of effort required to associate destination IDs with multicast masks. This feature makes possible in this example to associate a sequential block of 16 destination IDs with the 16 multicast masks with only 32 register writes. Refer to Table 5.4.3, “Using Block Association,” on page 58 for details of the pair of writes required for each block of 16 destination IDs.

For the destination ID to multicast mask association operations for Switch B2 there is no pattern that leverages the programming model to speed the association of destination IDs to multicast masks. In Switch B2, it would make sense to use the regular switch routing tables rather than a multicast mask for the destination IDs associated with multicast masks 1, 2, 4 and 8 in order to minimize the number of writes required. The remaining 12 multicast groups each require 32 register write operations to complete their associations with the appropriate destination IDs, for a total of 384 writes. Designers who prefer speed of initialization over reliability may reduce this to 352 register writes by ignoring the destination IDs associated with multicast mask 0.

For switch B2, it may make sense in some systems to implement application specific configuration registers to reduce the number of operations required for configuration.

There can be significant limitations to using static multicast masks. Assume, of the 8 destinations, destinations A, B, C, D, and E are receiving one data stream using destination ID 0x041F, and destinations F, G, and H are receiving a second data stream using destination ID 0x0420.

If destination E switches wishes to change to the second data stream, two things must happen. The destination ID for the first data stream must change from 0x041F to 0x040F in order to have the proper multicast mask for switches B1 and B2, and the destination ID for the second data stream must correspondingly change from 0x0420 to 0x0430.

Because the destination IDs have changed, the switches are now allowed to reorder packets sent to destination IDs 0x041F, 0x040F, 0x0420 and 0x0430, which may change the behavior of the system in unexpected or undesirable ways.

Another issue with static multicast masks is that the latency difference for a data stream between different destinations depends upon whether the data stream is routed using the regular switch routing table or multicast through a particular switch. The different destinations will see different performance characteristics.

These characteristics could have undesirable side effects for latency and jitter sensitive applications like Voice over Internet Protocol (VoIP).

B.3 Example 2 - Linking Multicast Masks to Destination IDs

As an alternative implementation, again suppose that there are 256 possible destinations which need to be multicast, numbered 0 through 255. Each destination has a number of data streams it can receive, up to 256, which is always associated with a 16 bit destination ID of the form 0x04<destination stream>. This requires 256 multicast masks in switches A1, B1, and B2.

When a destination changes the data stream it wants to receive, the multicast masks for that data stream need to be changed. First, the multicast mask in each switch associated with the stream currently being received needs to be modified to stop multicasting to this destination. Next, the multicast mask for the new data stream needs to be modified in each switch to enable multicast to that destination.

Depending on system requirements, there are many ways to implement the multicast capabilities in this system. For example, switch A1 could always multicast all data streams to both switch B1 and switch B2. In this case, switch A1 would require 1 multicast mask that could have all 256 destination IDs associated with it. Switch B1 and B2 may receive a lot of undesired traffic in this case.

Initial programming of the multicast masks is not a requirement as with example 1. No ports should be selected in any mask after reset. Multicast masks will be modified during system operation as destinations request to receive a particular data stream. Removing the data streams from one multicast mask and adding a data stream to a multicast mask can be performed in two register writes for each switch.

The destination ID associations with multicast masks can be done far more effectively in this example if the switch devices support block associate operations. Refer to Section 4.2.3, “Switch Multicast Information CAR”, and the programming examples in Section 5.4, “Configuring Associations” for more information and examples.

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Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book.

A

Associate, Association. A defined relationship between a destination ID and a group of end point devices, or, in a switch, a defined relationship between a destination ID and a multicast mask.

M

Multicast. The concept of sending a single message to multiple destinations in a system.

Multicast group. The group of end point devices in a system that is the target of a multicast operation.

Multicast mask. The group of egress ports in a switch that are the targets of a replicated multicast packet.

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