RapidIO™ Interconnect Specification Device Inter-operability and Certification Checklists

Rev. 1.1, 09/2005

Revision History

Revision	Description	Date
1.0	First release	07/12/2004
1.0.a	No technical changes; Converted to ISO-friendly templates	09/03/2004
1.1	Revised to support Revision 1.3 of the RapidIO specification, approved release	09/20/2005

Questions regarding the RapidIO Trade Association, specifications, or membership should be forwarded to:

Suite 325, 3925 W. Braker Lane
Austin, TX 78759
512-305-0070 Tel.
512-305-0009 FAX.

Table of Contents

Table of Contents

Table of Contents

Chapter 7 Logical Layer Optional Functionality Checklists

Chapter 8 Multicast Checklists

Table of Contents

Blank Page

List of Tables

List of Tables

Chapter 1 Overview

1.1 Introduction

The document contains the device compliance checklists adhering to revision 1.3 of the RapidIO Interconnect Specification. If an inconsistency exists between the specifications and the checklists defined by this document, the specifications take precedence.

1.2 References

- RapidIO^{TM} Interconnect Specification, Revision 1.3, 6/2005

1.3 Definitions and Acronyms

The following is a list of definitions and acronyms used in the document:

EOP	end of packet
SOP	start of packet

Blank Page

Chapter 2 8/16 LP-LVDS Physical Layer Checklists

2.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for 8/16 LP-LVDS Physical Layer devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The 8/16 LP-LVDS Physical layer inter-operability and certification checklist is broken down into a number of sub-lists.

2.2 General specification compliance list

This section specifies general requirements for a compliant device.

Reads and writes to CSRs and CARs are referenced from RapidIO transactions received by a device.

Table 2-1. General device 8/16 LP-LVDS physical layer general compliance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device assigns reserved packet fields to logic 0s. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2 Part 4, Sec. 2.3.1	Generic	
2.	Reserved packet field contents do not affect operation of the device. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
3.	Implementation-defined packet fields do not affect operation of the device unless the function is understood by the receiving device. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
4.	Received reserved packet field encodings do not affect operation of the device if it is not necessary for the field to be defined for the requested transaction. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
5.	A received reserved packet field encoding is regarded as an error if it is necessary for the field to be defined for the requested transaction. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	
6.	All registers are 32 bits in size, and aligned to 32 bit boundaries.	Part 1, Sec. 5 Part 2, Sec. 5 Part 3, Sec. 3 Part 4, Sec. 5 Part 6, Sec. 6	Generic	Inter-op
7.	Reads to reserved CAR bits return logic 0s. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	
8.	Writes to CARs do not affect operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
9.	Reads to implementation-defined CAR bits return the implementation defined value. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
10.	Writes to implementation-defined CAR bits do not affect operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
11.	Reads to reserved CARs do not cause an error. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.1	Generic	Inter-op

Table 2-1. General device 8/16 LP-LVDS physical layer general compliance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	Reads to reserved CAR return logic 0s when read. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
13.	Writes to a reserved CAR do not cause an error. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.1	Generic	Inter-op
14.	Writes to reserved CARs do not affect operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
15.	Reads to reserved CSRs and reserved Extended Features register bits return logic 0s. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2 Part 4, Sec. 5.3, Table 5-2	Generic	
16.	Writes to reserved CSRs and reserved Extended Features register bits do not affect operation of the device. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2 Part 4, Sec. 5.3, Table 5-2	Generic	Inter-op
17.	Reads to reserved CSRs and reserved Extended Features registers do not cause an error. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.1	Generic	Inter-op
18.	Reads to reserved CSRs and reserved Extended Features registers return logic 0s when read. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2 Part 4, Sec. 5.3, Table 5-2	Generic	
19.	Writes to reserved CSRs and reserved Extended Features registers do not cause an error. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.1	Generic	Inter-op
20.	Writes to reserved CSRs and reserved Extended Features registers do not affect operation of the device. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2 Part 4, Sec. 5.3, Table 5-2	Generic	Inter-op

2.3 Signal names compliance lists

The defined signals must exist, although the actual names used on a particular device may vary. The actual names used must allow an unambiguous match to the names defined in the 8/16 LP-LVDS physical specification.

2.3.1 8-bit device compliance list

Table 2-2. General device 8/16 LP-LVDS physical layer 8-bit symmetric device pins

Item no.	Signal name	I/O	Description	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	TCLK0, $\overline{\text{TCLK0}}$	O	Double data rate clock	Part 4, Sec. 8.2	Generic	
2.	TFRAME, $\overline{\text{TFRAME}}$	O	Packet and control symbol delineation signal	Part 4, Sec. 8.2	Generic	
3.	TD[0-7], $\overline{\text{TD}}$[0-7]	O	Data byte	Part 4, Sec. 8.2	Generic	
4.	RCLK0, $\overline{\text{RCLK0}}$	I	Double data rate clock	Part 4, Sec. 8.2	Generic	
5.	RFRAME, $\overline{\text{RFRAME}}$	I	Packet and control symbol delineation signal	Part 4, Sec. 8.2	Generic	
6.	RD[0-7], $\overline{\text{RD}}$[0-7]	I	Data byte	Part 4, Sec. 8.2	Generic	

2.3.2 16-bit device compliance list

Table 2-3. General device 8/16 LP-LVDS physical layer 16-bit symmetric device pins

Item no.	Signal name	I/O	Description	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	TCLK0, $\overline{\text{TCLK0}}$	O	Double data rate clock	Part 4, Sec. 8.2	Generic	
2.	TFRAME, $\overline{\text{TFRAME}}$	O	Packet and control symbol delineation signal	Part 4, Sec. 8.2	Generic	
3.	TD[0-7], $\overline{\text{TD}}$[0-7]	O	Data byte	Part 4, Sec. 8.2	Generic	
4.	TCLK1, $\overline{\text{TCLK1}}$	O	Least significant double data rate clock	Part 4, Sec. 8.2	Generic	
5.	TD[8-15], $\overline{\text{TD}}$[8-15]	O	Least significant data byte	Part 4, Sec. 8.2	Generic	
6.	RCLK0, $\overline{\text{RCLK0}}$	I	Double data rate clock	Part 4, Sec. 8.2	Generic	
7.	RFRAME, $\overline{\text{RFRAME}}$	I	Packet and control symbol delineation signal	Part 4, Sec. 8.2	Generic	
8.	RD[0-7], $\overline{\text{RD}}$[0-7]	I	Data byte	Part 4, Sec. 8.2	Generic	
9.	RCLK1, $\overline{\text{RCLK1}}$	I	Least significant double data rate clock	Part 4, Sec. 8.2	Generic	
10.	RD[8-15], $\overline{\text{RD}}$[8-15]	I	Least significant data byte	Part 4, Sec. 8.2	Generic	

2.4 Basic functionality compliance list

This is the list for basic functionality for the device.

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device meets target AC specifications	Part 4, Sec. 9	Generic	
2.	16 bit ports must be able to function as 8 bit ports	Part 4, Sec. 3.7.1.1.1	Generic	
3.	Control symbols are 16 bits followed by an inverted 16 bit copy	Part 4, Sec. 4.1	Generic	
4.	The device shall handle received undefined control symbols properly	Part 4, Sec. 4.1		
	• **4A. DETAIL:** The control symbols with reserved stype field encoding shall not affect operation of the device and no error shall be reported	Part 4, Sec. 4.1	Generic	
	• **4B. DETAIL:** The packet-control symbols with reserved sub_type field encoding shall not affect operation of the device and no error shall be reported	Part 4, Sec. 4.1	Generic	
	• **4C. DETAIL:** The link-request control symbols with reserved cmd field encoding shall cancel packet whose transmission is in progress, but itself shall not affect operation of the device and no error shall be reported	Part 4, Sec. 4.1 Part 4, Sec. 4.2.4	Generic	
5.	If the CRF bit is not supported, transaction request flow A is mapped to priority 0. If the CRF bit is supported, transaction request flow A is mapped to priority 0 if CRF=0. Otherwise, if CRF=1, transaction request flow B is mapped to priority 0.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 4, Sec. 2.3.2 Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
	• **5A. DETAIL:** Read packets are transmitted at priority level 0	Part 7, Sec. 4.5 Part 4, Sec. 2.3.2	Class 2,3	
	• **5B. DETAIL:** Write packets are transmitted at priority level 0	Part 7, Sec. 4.5 Part 4, Sec. 2.3.2	Class 2,3	
	• **5C. DETAIL:** Response packets are transmitted at priority level 1, 2, or 3	Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.2	Generic	
6.	If the CRF bit is not supported, transaction request flow B is mapped to priority 1. If the CRF bit is supported, transaction request flow C is mapped to priority 1 if CRF=0. Otherwise, if CRF=1, transaction request flow D is mapped to priority 1.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 4, Sec. 2.3.2 Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
	• **6A. DETAIL:** Read packets are transmitted at priority level 1	Part 7, Sec. 4.5 Part 4, Sec. 2.3.2	Class 2,3	
	• **6B. DETAIL:** Write packets are transmitted at priority level 1	Part 7, Sec. 3.2 Part 4, Sec. 2.3.2	Class 2,3	
	• **6C. DETAIL:** Response packets are transmitted at priority level 2 or 3	Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.2	Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
7.	If the CRF bit is not supported, transaction request flow C is mapped to priority 2. If the CRF bit is supported, transaction request flow E is mapped to priority 2 if CRF=0. Otherwise, if CRF=1, transaction request flow F is mapped to priority 2.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 4, Sec. 2.3.2 Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
	• **7A. DETAIL:** Read packets are transmitted at priority level 2	Part 7, Sec. 4.5 Part 4, Sec. 2.3.2	Class 2, Class 3	
	• **7B. DETAIL:** Write packets are transmitted at priority level 2	Part 7, Sec. 4.5 Part 4, Sec. 2.3.2	Class 2, Class 3	
	• **7C. DETAIL:** Response packets are transmitted at priority level 3	Part 4, Sec. 2.3.2	Generic	
8.	In a processing element, a higher priority packet generated before a lower priority packet with the same source ID and destination ID is always transmitted before the lower priority packet.	Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
9.	Packets received by a processing element are processed in the order they were received	Part 4, Sec. 2.3.2 Part 4, Sec. 2.3.3	Generic	
10.	Packets of the same priority level cannot pass each other in the same flow, with the following exception. A packet with the CRF bit set may pass another packet of the same priority in the same flow without the CRF bit set.	Part 4, Sec. 2.3.2 Part 4, Sec. 2.3.3	Generic	
11.	At the transmitter, packets of higher priority may pass packets of a lower priority level	Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
12.	All registers in the 8/16 LP-LVDS Physical Layer Specification Extended Features data structure can be read and/or written, as per constraints specified in Part 4, Chapter 4. The Extended Features Space is located at bytes offsets 0x0100 through 0xFFFC of the device configuration space.	Part 4, Sec. 5	Generic	
	• **12A. DETAIL:** Port Maintenance Block Header 0 CSR is read-only, and is compliant with the following:	Part 4, Sec. 5.5.2.1 Part 4, Sec. 5.6.2.1 Part 4, Sec. 5.7.2.1 Part 6, Sec. 5.8.2.1	Generic	
	• **12A1. DETAIL:** Port Maintenance Block Header 0 CSR has the proper Extended Features block ID in the EF_ID field.		Generic	
	• **12A2. DETAIL:** Port Maintenance Block Header 0 EF_PTR field reset value is implementation dependent.		Generic	
	• **12B. DETAIL:** Port Link Time-out Control CSR; reset value of time-out value field is 0xFFFFFF	Part 4, Sec. 5.5.2.2 Part 4, Sec. 5.6.2.2 Part 4, Sec. 5.7.2.2 Part 4, Sec. 5.8.2.2	Generic	
	• **12B1. DETAIL:** Port Link Time-out Control CSR Bits 0-23 are writable, and time-out value varies with value written.		Generic	
	• **12B2. DETAIL:** Port Link Time-out Control CSR Bits 24-31 cannot change value from 0.		Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12C. DETAIL:** Port Response Time-out Control CSR; reset value of the time-out value field is 0xFFFFFF (end point devices only)	Part 4, Sec. 5.5.2.3 Part 4, Sec. 5.6.2.3 Part 4, Sec. 5.8.2.3	Generic	
	• **12C1. DETAIL:** Port Response Time-out Control CSR Bits 0-23 are writable, and time-out value varies with value written.		Generic	
	• **12C2. DETAIL:** Port Response Time-out Control CSR Bits 24-31 cannot change value from 0.		Generic	
	• **12D. DETAIL:** Port General Control CSR; reset value is implementation dependent	Part 4, Sec. 5.5.2.4 Part 4, Sec. 5.6.2.4 Part 4, Sec. 5.7.2.3 Part 4, Sec. 5.8.2.4	Generic	
	• **12D1. DETAIL:** Verify Host field accurately reflects the capabilities of the device.		Generic	
	• **12D2. DETAIL:** Verify Master Enable field accurately reflects the capabilities of the device.		Generic	
	• **12D3. DETAIL:** Verify Discovered field is set to 1 as soon as a maintenance write request is received to this register bit and if Discovered bit is 0 after reset for this device.		Generic	
	• **12E. DETAIL:** Port n Error and Status CSR; reset value is 0x00000001	Part 4, Sec. 5.5.2.5 Part 4, Sec. 5.6.2.8 Part 4, Sec. 5.7.2.4 Part 4, Sec. 5.8.2.8	Generic	
	• **12E1. DETAIL:** Verify that fields in the Port n Error and Status CSR are set on the appropriate conditions.		Generic	
	• **12E2. DETAIL:** Verify that the following fields are cleared by writing 1 to them: Output Retry-encountered, Output Error-encountered, Input Error-encountered, Post-write Pending, Port Error.		Generic	
	• **12E3. DETAIL:** Verify that the following fields do not change their values when written to: Output Retried, Output Retry-stopped, Output Error-stopped, Input Retry-stopped, Input Error-stopped, Port OK, Port Un-initialized		Generic	
	• **12F. DETAIL:** Port n Control CSR is compliant with the following:	Part 4, Sec. 5.5.2.6 Part 4, Sec. 5.6.2.9 Part 4, Sec. 5.7.2.5 Part 4, Sec. 5.8.2.9	Generic	
	• **12F1. DETAIL:** Reset values of the following fields are implementation dependent: Output Port Width, Input Port Width, Output Port Enable, Input Port Enable (if applicable, also Multicast-event Participant and Enumeration Boundary).		Generic	
	• **12F2. DETAIL:** Reset value of the following fields is logic 0s: Output Port Driver Disable, Input Port Receiver Disable, Error Checking Disable (if applicable, also Re-transmit Suppression Mask).		Generic	
	• **12F3. DETAIL:** Reset value of the Port Type field is implementation defined.		Generic	
	• **12F4. DETAIL:** bits 3, 7, 10-13, 15-19, 28-30 are reserved (always logic 0s). Any bits not included in the implementation are also reserved.		Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12F5. DETAIL:** The following fields are read-only: Input Port Width, Output Port Width, Port Type. All other fields of the Port n Control CSR are read/write, if the implementation supports their existence.		Generic	
	• **12G. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Link Maintenance Request CSR register exists for each port at the correct offset.	Part 4, Sec. 5.6.2.5 Part 4, Sec. 5.8.2.5	Generic	
	• **12G1. DETAIL:** A write to the Port n Link Maintenance Request CSR results in the correct control symbol being sent.		Generic	
	• **12G2. DETAIL:** A read of the Port n Link Maintenance Request CSR returns the last command sent.		Generic	
	• **12G3. DETAIL:** The reset value of the Port n Link Maintenance Request CSR is 0.		Generic	
	• **12H. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Link Maintenance Response CSR register exists for each port at the correct offset.	Part 4, Sec. 5.6.2.6 Part 4, Sec. 5.8.2.6	Generic	
	• **12H1. DETAIL:** The first read of the Port n Link Maintenance Response CSR register will return the correct response for the last command sent by the Port n Link Maintenance Request CSR.		Generic	
	• **12H2. DETAIL:** Subsequent reads of the Port n Link Maintenance Response CSR register have the response_valid field cleared.		Generic	
	• **12H3. DETAIL:** The reset value of the Port n Link Maintenance Response CSR register is 0.		Generic	
	• **12H4. DETAIL:** All bits in the Port n Link Maintenance Response CSR register are read only.		Generic	
	• **12I. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Local ackID CSR register exists for each port at the correct offset.	Part 4, Sec. 5.6.2.7 Part 4, Sec. 5.8.2.7	Generic	
	• **12I1. DETAIL:** The Port n Local ackID CSR register always returns the correct value when read locally.		Generic	
	• **12I2. DETAIL:** Writing the Outbound_ackID field will force the retransmission of the corresponding outstanding unacknowledged packet, whose ackID=Outbound_ackID.	Part 4, Sec. 5.6.2.7 Part 4, Sec. 5.8.2.7	Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12I3. DETAIL:** When read from the RapidIO port, the Port n Local ackID CSR register always returns values as if the maintenance read request had not occurred.		Generic	
	• **12I4. DETAIL:** The reset value of the Port n Local ackID CSR register is 0.	Part 4, Sec. 5.6.2.7 Part 4, Sec. 5.8.2.7	Generic	
	• **12I5. DETAIL:** All fields of the Port n Local ackID CSR register may be written to.		Generic	
	• **12I6. DETAIL:** Bits 1-4, 8-15, and 24-26 are reserved (always logic 0s).		Generic	
	• **12J. DETAIL:** For a general end point device that supports software assisted error recovery, in the Port n Link Maintenance Request CSRs, the reset value of the command field is logic 0's.	Part 4, Sec. 5.6.2.5 Part 4, Sec. 5.8.2.5	Generic	
	• **12K. DETAIL:** For a general end point device that supports software assisted error recovery, the Port n Link Maintenance Response CSRs are read only and are compliant with the following:		Generic	
	• **12K1. DETAIL:** Reset values of the response_valid, ackID_status and link_status fields are logic 0s.		Generic	
	• **12L. DETAIL:** For a general end point device that supports software assisted error recovery, in the Port n Local ackID CSRs the reset values of the Inbound_ackID, Outstanding_ackID and Outbound_ackID fields are logic 0s.		Generic	
	• **12M. DETAIL:** Processing Elements Features CAR is read-only, and is compliant with the following:	Part 4, Sec. 5.4.1	Generic	
	• **12M1. DETAIL:** The values of Re-transmit Suppression Support and CRF Support are implementation dependent.		Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
13.	Device follows system initialization and exploration inter-operability procedure	Part 7, Sec. 2.2 Part 7, Sec. 2.3	Generic	
	• **13A. DETAIL:** End point agent device that contain a boot ROM is initially assigned base device ID=0xFE at power-up	Part 7, Sec. 2.2	Generic	
	• **13B. DETAIL:** End point agent device without a boot ROM is initially assigned base device ID=0xFF at power-up	Part 7, Sec. 2.2	Generic	
	• **13C. DETAIL:** System host device is initially assigned a non-reserved base device ID at power-up (end point device only)	Part 7, Sec. 2.2	Class 2,3	
	• **13D. DETAIL:** Host device sets the Discovered bit at power-up	Part 7, Sec. 2.3	Generic	
	• **13E. DETAIL:** Agent device resets the Discovered bit at power-up	Part 7, Sec. 2.3	Generic	
	• **13F. DETAIL:** Host device sets the Master Enable bit at power-up (end point device only)	Part 7, Sec. 2.3	Class 2,3	
	• **13G. DETAIL:** Agent device clears the Master Enable bit at power-up (end point device only)	Part 7, Sec. 2.3	Generic	
	• **13H. DETAIL:** Device with switch functionality defaults route information to allow boot ROM access by system host	Part 7, Sec. 2.2	Generic	
	• **13I. DETAIL:** Switch device must send maintenance responses that it generates to the port that the maintenance request was received on	Part 7, Sec. 2.3	Generic	
14.	A port shall time out if an acknowledgment control symbol for a packet is never received.	Part 4, Sec. 2.4.3	Generic	
	• **14A. DETAIL:** Verify that the maximum time-out value is between 3 and 6 seconds. A reasonable test procedure should be followed for simulation environments.	Part 4, Sec. 2.4.3 Part 4, Sec. 5	Generic	
15.	A request shall time out if a response packet is never received.	Part 4, Sec. 2.4.3	Generic	
	• **15A. DETAIL:** Verify that the maximum time-out value is between 3 and 6 seconds. A reasonable test procedure should be followed for simulation environments.	Part 4, Sec. 2.4.3 Part 4, Sec. 5	Generic	
16.	Training symbol is correct for port operating width.	Part 4, Sec. 3.7.1.1.3	Generic	
17.	CLK signal(s) “rising edge” is on the 32 bit boundary	Part 4, Sec. 3.2	Generic	
18.	CLK signal(s) toggle every clock (true free running clock)	Part 4, Sec. 3.2	Generic	
19.	TFRAME/RFRAME signal only toggles on the 32 bit boundary of their corresponding clock (TCLK/RCLK)	Part 4, Sec. 3.2	Generic	
20.	TFRAME/RFRAME signal only toggles to mark the first byte of a control symbol, the first byte of a new packet or during a training pattern transmission.	Part 4, Sec. 3.2 Part 4, Sec. 3.7.1.1.3	Generic	

Table 2-4. General device 8/16 LP-LVDS physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
21.	RFRAME/TFRAME signal is associated with RCLK0/TCLK0, not RCLK1/TCLK1	Part 4, Sec. 8.2	Generic	
22.	Device responds to a throttle control symbol with a pacing idle control symbol within the specified 40 interface clocks or 80 data ticks	Part 4, Sec. 3.4	Generic	

2.5 DC and AC electrical compliance list

This is the list for electrical compliance of parallel LP-LVDS RapidIO signals.

All measurements must be taken in accordance with discussions/guidance captured in Part 4, Chapter 9. All speeds quoted in Table 2-5 are clock rates.

Table 2-5. General device 8/16 LP-LVDS physical layer AC and DC electrical list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	LP-LVDS driver signals must meet DC specifications defined in Part 4 Section 9.3 Table 9-1	Part 4, Sec. 9.3, Table 9-1	Generic	
2.	LP-LVDS receiver signals must meet DC specifications defined in Part 4 Section 9.3 Table 9-2	Part 4, Sec. 9.3, Table 9-2	Generic	
3.	LP-LVDS 250 MHz drivers must meet the AC specifications defined in Part 4 Section 9.4.2 Table 9-3.	Part 4, Sec. 9.4.2, Table 9-3	Generic	
4.	LP-LVDS 375 MHz drivers must meet the AC specifications defined in Part 4 Section 9.4.2 Table 9-4.	Part 4, Sec. 9.4.2, Table 9-4	Generic	
5.	LP-LVDS 500 MHz drivers must meet the AC specifications defined in Part 4 Section 9.4.2 Table 9-5.	Part 4, Sec. 9.4.2, Table 9-5	Generic	
6.	LP-LVDS 750 MHz drivers must meet the AC specifications defined in Part 4 Section 9.4.2 Table 9-6.	Part 4, Sec. 9.4.2, Table 9-6	Generic	
7.	LP-LVDS 1000 MHz drivers must meet the AC specifications defined in Part 4 Section 9.4.2 Table 9-7.	Part 4, Sec. 9.4.2, Table 9-7	Generic	
8.	LP-LVDS 250 MHz receivers must meet the AC specifications defined in Part 4 Section 9.4.3 Table 9-8.	Part 4, Sec. 9.4.3, Table 9-8	Generic	
9.	LP-LVDS 375 MHz receivers must meet the AC specifications defined in Part 4 Section 9.4.3 Table 9-9.	Part 4, Sec. 9.4.3, Table 9-9	Generic	
10.	LP-LVDS 500 MHz receivers must meet the AC specifications defined in Part 4 Section 9.4.3 Table 9-10.	Part 4, Sec. 9.4.3, Table 9-10	Generic	
11.	LP-LVDS 750 MHz receivers must meet the AC specifications defined in Part 4 Section 9.4.3 Table 9-11.	Part 4, Sec. 9.4.3, Table 9-11	Generic	
12.	LP-LVDS 1000 MHz receivers must meet the AC specifications defined in Part 4 Section 9.4.3 Table 9-12.	Part 4, Sec. 9.4.3, Table 9-12	Generic	

2.6 Link initialization compliance list

This is the list for device link initialization.

Table 2-6. General device 8/16 LP-LVDS physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device must follow the Port and Link Initialization procedure	Part 4, Sec. 3.7.1	Generic	Inter-op
	• **1A. DETAIL:** Device port not requiring Port Initialization shall never set “Port Uninitialized” bit in its Port n Control and Status register	Part 4, Sec. 3.7.1.1.5	Generic	
	• **1B. DETAIL:** Device port requiring Port Initialization shall follow the Port Initialization Process	Part 4, Sec. 3.7.1.1.6 Part 4, Sec. 3.7.1.1.7	Generic	
	• **1C. DETAIL:** All devices shall follow Link Initialization procedure	Part 4, Sec. 3.7.1	Generic	
	• **1C1. DETAIL:** After a port has successfully trained, it will only transmit idle control symbols until it successfully receives an idle control symbol.	Part 4, Sec. 3.7.1	Generic	
	• **1D. DETAIL:** Device port being in normal operation state (transmitting/receiving packets and control symbols other than idles) shall have the “Port Uninitialized” bit clear and “Port OK” bit set in its Port n Control and Status register	Part 4, Sec. 3.7.1	Generic	
	• **1E. DETAIL:** Device in normal operation state must respond to link-request/send-training control symbol not followed by training pattern with 256 training patterns followed by one idle control symbol, and then resume normal operation.	Part 4, Sec. 3.7.1.3	Generic	
	• **1F. DETAIL:** If an unsolicited training pattern (whether or not preceded by link-request/send-training control) is received on the Device input, Device must change the “Port OK” and “Port Uninitialized” bits in the Port n Error and Status CSR to 0 and 1, respectively. The port must repeatedly transmit training pattern bursts, each followed by an idle control symbol, until an idle control is received from the connected port.	Part 4, Sec. 3.7.1.4	Generic	
	• **1G. DETAIL:** Training pattern is not embedded in a packet or used to terminate a packet.	Part 4, Sec. 3.7.1.1.4	Generic	

2.7 Link maintenance compliance list

This is the list for link maintenance functionality.

Table 2-7. General device 8/16 LP-LVDS physical layer link maintenance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Link-request/input-status control symbol causes a link-response control symbol	Part 4, Sec. 2.6.1.2	Generic	Inter-op
2.	Link-response control symbol port_status field indicates input port status prior to receiving the link-request/input-status (restart-from-error)	Part 4, Sec. 2.6.2	Generic	
	• **2A. DETAIL:** Error means unrecoverable problem encountered, won't accept any packets	Part 4, Sec. 2.6.2	Generic	
	• **2B. DETAIL:** Retry-stopped means that input port is stopped due to a retry and will not accept packets until receiving a "restart-from-retry" or a "restart-from-error" control symbol	Part 4, Sec. 2.6.2	Generic	
	• **2C. DETAIL:** Error-stopped means that input port is stopped due to a transmission error and will not accept packets until receiving a "restart-from-error" control symbol	Part 4, Sec. 2.6.2	Generic	
	• **2D. DETAIL:** OK means that the input port is operating and can communicate with the connected device	Part 4, Sec. 2.6.2	Generic	
	• **2E. DETAIL:** A link-response control symbol with a reserved port_status field value shall not affect the operation of the device.	Part 4, Sec. 2.6.2	Generic	
3.	A device receiving a reset command in a link-request control symbol shall not perform the reset function unless it has received four reset commands in a row without any other intervening packets or control symbols, except idle control symbols. Response time for reset is implementation specific.	Part 4, Sec. 2.6.1.1	Generic	
4.	Link-request/input-status, link-response control symbol pair forces completion of all preceding activity	Part 4, Sec. 2.6.1.2	Generic	
	• **4A. DETAIL:** All preceding packets have generated acknowledge control symbol if applicable	Part 4, Sec. 2.6.1.2	Generic	
	• **4B. DETAIL:** Returned link_status correctly indicates next expected ackID	Part 4, Sec. 2.6.1.2	Generic	
5.	Device doesn't issue more than one outstanding link-request control symbol (exception in case of time-out)	Part 4, Sec. 2.6	Generic	
	• **5A. DETAIL:** Must hold off another link-request control symbol until expected link-response control symbol is received	Part 4, Sec. 2.6	Generic	
6.	Link-request/send-training control symbol causes 256 training patterns to be sent followed by at least one idle control symbol. No response time is specified.	Part 4, Sec. 2.6.1.3	Generic	

2.8 Packet transmission compliance list

This is the list for the device transmitting a packet, and applies to all devices, as all generic devices are required to generate response packets.

Table 2-8. General device 8/16 LP-LVDS physical layer packet transmission list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device cannot issue more than 7 unacknowledged packets	Part 4, Sec. 2.2.2	Generic	
2.	ackIDs are always issued sequentially (exception when a retry or error causes the device to back up)	Part 4, Sec. 2.2.2	Generic	
3.	Start with ackID=0 after reset	Part 4, Sec. 5.6.2.7 Part 4, Sec. 5.8.2.7	Generic	
4.	Physical layer 2 reserved bits are set to logic 0s	Part 4, Sec. 2.4.2	Generic	
5.	A response packet for a request packet can never be transmitted before the acknowledge control symbol for the request packet	Part 4, Sec. 2.2	Generic	
6.	Embedded CRC properly inserted	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **6A. DETAIL:** Don't insert embedded CRC if packet is 80 bytes or less.	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **6B. DETAIL:** Insert embedded CRC if packet is 81 bytes or more		Generic	
7.	Packets that are not aligned to the 32-bit boundary are padded into alignment with 16 bits of logic 0	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **7A. DETAIL:** Pad data is inserted after the final CRC code for the packet.		Generic	
8.	CRC values are correctly calculated	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **8A. DETAIL:** the final CRC value is the continuation of the embedded CRC and embedded CRC is included in the running calculation (applicable only for packets greater than 80 bytes)	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **8B. DETAIL:** CRC values are computed according to the polynomial specified in Part 4, Section 2.4.7.		Generic	
	• **8C. DETAIL:** Incorrect values in Physical Layer header fields (S-bit, AckID, rsvd) do not result in CRC errors being detected.	Part 4, Sec. 2.42	Generic	
9.	Switch devices shall not allow data to be corrupted internal to the device without detection.	Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
10.	Packets are completed normally with a new packet (starting SOP control symbol) or EOP control symbol	Part 4, Sec. 3.3	Generic	
11.	Packets are canceled using stomp, restart-from-retry, or link-request control symbols	Part 4, Sec. 3.3	Generic	

Table 2-8. General device 8/16 LP-LVDS physical layer packet transmission list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	Device receiving packet-retry control symbol follows the defined retry behavior. Further discussion of this point can be found in Part 4, Sec. A.3.2.	Part 1, Sec. 2.3.2.2 Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4	Generic	
	12A. DETAIL: Set the "Output Retry-stopped" bit to 1 in the Port n Error and Status CSR when a packet-retry control symbol is received. Further discussion of this point can be found in Part 4, Sec. A.3.2.		Generic	
	12B. DETAIL: Stop transmission of any existing packet. (restart from retry will cancel packet). Further discussion of this point can be found in Part 4, Sec. A.3.2.		Generic	
	12C. DETAIL: Send a restart-from-retry control symbol to the receiving device. Further discussion of this point can be found in Part 4, Sec. A.3.2.		Generic	
	12D. DETAIL: Change the "Output Retry-stopped" bit to 0 in the Port n Error and Status CSR when the output port internal retry recovery procedure is complete. Further discussion of this point can be found in Part 4, Sec. A.3.2.		Generic	
	12E. DETAIL: Begin re-transmitting packets from the returned expected ackID value. Further discussion of this point can be found in Part 4, Sec. A.3.2.		Generic	
	• **12F. DETAIL:** Retried packet must eventually be re-transmitted	Part 4, Sec. 2.3.3	Generic	
13.	Stomp and restart-from-retry control symbols have the contents field set to all logic 0s	Part 4, Sec. 4.3	Generic	

2.9 Packet reception compliance list

This is the list for the device receiving a packet.

Table 2-9. General device 8/16 LP-LVDS physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ackIDs are only accepted sequentially	Part 4, Sec. 2.3.3	Generic	Inter-op
2.	Start with ackID=0 after reset	Part 4, Sec. 5.6.2.7 Part 4, Sec. 5.8.2.7	Generic	Inter-op
3.	Every packet causes an acknowledge control symbol with the corresponding ackID field	Part 4, Sec. 4.2	Generic	Inter-op
4.	Device must send acknowledge control symbols in same order as packets are received (ackIDs are issued sequentially)	Part 4, Sec. 2.4.5.1.2	Generic	Inter-op
5.	Device must not send a packet-accepted control symbol before the entire packet has been received and is error free (if error checking is enabled)	Part 4, Sec. 4.2.1	Generic	
6.	Physical layer 2 reserved bits do not affect operation of the device.	Part 4, Sec. 2.4.2	Generic	
7.	Packets are considered completed normally by the receiver if they are completed with a new packet (starting SOP control symbol) or EOP control symbol	Part 4, Sec. 3.3	Generic	Inter-op
8.	The contents field in stomp and restart-from-retry control symbols shall not affect operation of the device.	Part 4, Sec. 4.3	Generic	
9.	Device can accept embedded control symbols	Part 4, Sec. 3.5	Generic	Inter-op
	• **9A. DETAIL:** Packet-accepted control symbol	Part 4, Sec. 4.2	Generic	Inter-op
	• **9B. DETAIL:** Packet-retry control symbol	Part 4, Sec. 4.2	Generic	Inter-op
	• **9C. DETAIL:** Packet-not-accepted control symbol	Part 4, Sec. 4.2	Generic	Inter-op
	• **9D. DETAIL:** Idle control symbol	Part 4, Sec. 4.3	Generic	Inter-op
	• **9E. DETAIL:** Throttle control symbol	Part 4, Sec. 4.3	Generic	Inter-op
	• **9F. DETAIL:** Multicast-event control symbol	Part 4, Sec. 4.3	Generic	Inter-op
	• **9G. DETAIL:** Link-response control symbol	Part 4, Sec. 4.4	Generic	Inter-op

Table 2-9. General device 8/16 LP-LVDS physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
10.	Packets can be canceled using stomp, restart-from-retry, or link-request control symbols	Part 4, Sec. 3.3	Generic	Inter-op
	• **10A. DETAIL:** Device sends packet-retry control symbol for canceled packet, except when either the “Input Retry-stopped” or “Input Error-stopped” bits are set in the Port n Error and Status CSR.	Part 4, Sec. 3.3	Generic	Inter-op
	• **10B. DETAIL:** Cancellation of a packet during transmission/reception of the packet shall not result in any errors. Note: Cancellation by unexpected Restart-from-Retry results in input error recovery. This should not result in the detection of any other errors	Part 4, Sec. 3.3	Generic	
	• **10C. DETAIL**: Reception of valid packets after a packet has been cancelled, but before the Input Retry-Stopped Recovery Process has been completed, shall not result in any errors.	Part 4, Sec. 2.3.4.1 Part 4, Sec. 4.2.4	Generic	Inter-op
11.	Device encountering a packet retry situation follows the defined retry behavior. Further discussion of this point can be found in Part 4, Sec. A.3.1.	Part 1, Sec. 2.3.2.2 Part 4, Sec. 2.3.3 Part 4, Sec. 2.3.4 Part 4, Sec. 2.4.5.1.2	Generic	Inter-op
	• **11A. DETAIL:** A packet retry situation occurs when an internal hazard or a packet is cancelled when the “Port OK” bit is set in the Port n Error and Status CSR, with the following exception. If the packet was canceled with a link-request /input-status or (optional) restart-from-retry control symbol, this is not a packet retry situation.		Generic	Inter-op
	• **11B. DETAIL:** Change the “Input Retry-stopped” bit to 1 in the Port n Error and Status CSR when a packet retry situation has been detected.		Generic	Inter-op
	• **11C. DETAIL:** Send a packet-retry control symbol with the expected ackID value.		Generic	Inter-op
	• **11D. DETAIL:** Device silently discards packets when the “Input Retry-stopped” bit is set in the Port n Error and Status CSR.		Generic	Inter-op
	• **11E. DETAIL:** Device must detect control symbol errors when the “Input Retry-stopped” bit is set in the Port n Error and Status CSR.		Generic	Inter-op
	• **11F. DETAIL:** Change the “Input Retry-stopped” bit to 0 in the Port n Error and Status CSR when a restart-from-retry or a restart-from-error (link-request/input-status) control symbol is received.		Generic	Inter-op
12.	An end point processing element port shall accept an error-free packet of priority N if the port has enough space for the packet in the input buffer space of the port allocated for packets of priority N.	Part 1, Sec. 2.3.3 Part 4, Sec. 2.3.3.2	Generic	Inter-op
	• **12A. DETAIL:** An error free packet of priority N is rejected if insufficient buffer space exists. The receiving port sets the ‘Input Retry-stopped’ bit to 1 in the Port n Error and Status CSR.	Part 4, Sec. 2.3.3.2	Generic	Inter-op

Table 2-9. General device 8/16 LP-LVDS physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
13.	Accepting an input packet of a priority cannot be contingent on successfully transmitting a packet of a less than or equal priority from any of its ports.	Part 1, Sec. 2.3.3 Part 4, Sec. 2.3.3.2	Generic	Inter-op
14.	A generated packet-not-accepted control symbol uses a defined cause field encoding	Part 4, Sec. 4.2.3	Generic	
	• **14A. DETAIL:** “General error”(0b111) cause is used to indicate any input error situations.	Part 4, Sec. 4.2.3	Generic	
15.	A RapidIO device will accept packets of length up to 276 bytes.	Part 4, Sec. 2.5	Generic	Inter-op

2.10 Switch device specific compliance list

This list contains specific requirements for switch devices only.

Table 2-10. General device 8/16 LP-LVDS physical layer switch device specific list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device is compliant to packet delivery ordering rules.	Part 4, Sec. 2.3.3	Generic	Inter-op
	• **1A. DETAIL:** A switch shall not alter the priority of a packet.		Generic	
	• **1B. DETAIL:** Packet forwarding decisions made by a switch processing element shall provide a consistent output port selection which is based solely on the value of the destinationID field carried in the packet.		Generic	
	• **1C. DETAIL:** A switch processing element shall not change the order of packets comprising a transaction request flow (packets with the same sourceID, the same destinationID, the same priority, the same CRF value (if supported), and ftype != 8) as the packets pass through the switch.		Generic	
	• **1D. DETAIL:** A switch processing element shall not allow lower priority non-maintenance packets (ftype != 8) to pass higher priority non-maintenance packets with the same sourceID and destinationID as the packets pass through the switch.		Generic	
	• **1E. DETAIL:** A switch processing element shall not allow a priority N maintenance packet (ftype = 8) to pass another maintenance packet of priority N or greater that takes the same path through the switch (same switch input port and same switch output port) and has the same CRF value, if supported.		Generic	
2.	Device is compliant to deadlock prevention rules.	Part 4, Sec. 2.3.3.2	Generic	
	• **2A. DETAIL:** A RapidIO fabric shall be dependency cycle free for all operations that do not require a response.		Generic	
	• **2B. DETAIL:** A switch processing element port shall accept an error-free packet of priority N if there is no packet of priority greater than or equal to N that was previously received by the port and is still waiting in the switch to be forwarded.		Generic	
	• **2C. DETAIL:** A switch processing element port that transmits a priority N packet that is forced to retry by the connected device shall select a packet of priority greater than N, if one is available, for transmission.		Generic	

Table 2-10. General device 8/16 LP-LVDS physical layer switch device specific list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	Switch device provides Multicast-event processing	Part 4, 3.7.2	Generic	
	• **3A. DETAIL:** When a switch processing element receives a Multicast-Event control symbol, the switch shall forward the Multicast-Event by issuing a Multicast-Event control symbol from each port that is designated in the port's CSR as a Multicast-Event output port. The maximum value of Multicast-Event forwarding delay and delay variation shall be defined in switch device specification.		Generic	
	• **3B. DETAIL:** A switch port shall never forward a Multicast-Event control symbol back to the device from which it received a Multicast-Event control symbol regardless of whether the port is designated a Multicast-Event output or not.		Generic	
	• **3C. DETAIL:** In the event that two or more Multicast-Event control symbols are received by a switch processing element close enough in time that more than one is present in the switch at the same time, at least one of the Multicast-Event control symbols shall be forwarded. The others may be forwarded or discarded (device dependent).		Generic	

2.11 Flow control compliance list

This list defines RapidIO 8/16 LP-LVDS link level flow control.

Table 2-11. General device 8/16 LP-LVDS physical layer flow control list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device supports receiver-controlled flow control.	Part 4, Sec. 2.3.4.1	Generic	Inter-op
	• **1A. DETAIL:** Device sends buf_status=0xF in all appropriate control symbols (packet-accepted, packet-retry, status).		Generic	Inter-op
2.	Device supports transmitter-controlled flow control.	Part 4, Sec. 2.3.4.2	Generic	
	• **2A. DETAIL:** Device supports flow control mode negotiation procedure.	Part 4, Sec. 2.3.5	Generic	
	• **2A1. DETAIL:** If device supports transmitter-controlled flow control and detects that its link partner also supports transmitter-controlled flow control, it shall use transmitter-controlled flow control. Otherwise, it shall use receiver-controlled flow control.		Generic	
	• **2B. DETAIL:** Device sends the number of maximum length packet buffers currently available for packet reception (or 0xE in case this number is greater than 0xE) in buf_status field in appropriate control symbols (packet-accepted, packet-retry, status). A port may report a smaller number of buffers than it actually has available, but it shall not report a greater number.	Part 4, Sec. 2.3.4.2	Generic	
3.	When using transmitter-controlled flow control, a packet for which the receiver has indicated that it has buffers is never retried for reason of lack of resources in accordance with buffer prioritization rules.	Part 4, Sec. 2.3.4.2	Generic	

2.12 Recoverable errors compliance list

Recoverable errors are typically transmission errors or physical layer protocol violation errors and the recovery algorithm can be used to maintain communications on the link without losing any data. A compliant device must recover from a single error. Recovery from an error during the recovery from a prior error is application specific. Error detection can only be accomplished by the receiver of a packet or control symbol, never the sender.

Table 2-12. General device 8/16 LP-LVDS physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device detects the link Input errors	Part 4, Sec. 2.4	Generic	Inter-op
	• **1A DETAIL:** Requested training pattern is embedded in a packet or used to terminate a packet	Part 4, Sec. 3.7.1.1.4	Generic	
	• **1B DETAIL:** S bit parity failure	Part 4, Sec. 2.4.1	Generic	
	• **1C DETAIL:** Incorrect CRC for a packet	Part 4, Sec. 2.4.2 Part 4, Sec. 2.4.6 Part 4, Sec. 2.4.7	Generic	
	• **1C1. DETAIL:** CRC is checked against the polynomial specified in Part 4, Sec. 2.4.7		Generic	
	• **1C2. DETAIL:** CRC errors are detected at the 80 byte embedded CRC.		Generic	
	• **1C3. DETAIL:** Corruption of the ackID, S, $\overline{S}$, or rsrv fields, all resident in the first 16 bits of the packet header, shall not result in a CRC error being detected.		Generic	
	• **1C4. DETAIL:** For purposes of computing the CRC value, the ackID, S, $\overline{S}$, and rsrv fields, all resident in the first 16 bits of the packet header, shall be treated as logic 0s.		Generic	
	• **1D DETAIL:** Unexpected ackID value in a packet	Part 4, Sec. 2.4.5.1.1	Generic	
	• **1D1. DETAIL:** Device shall detect unexpected ackID error for a canceled packet (i.e. enter input error recovery instead of input retry recovery). Further discussion of this point can be found in Part 4, Sec. A.	Part 4, Sec. 2.4.5.1.1	Generic	
	• **1E DETAIL:** Received Packet exceeds the 276 byte maximum packet size limit	Part 4, Sec. 2.4.5.1.1	Generic	
	• **1F DETAIL:** Received corrupt control symbol	Part 4, Sec. 2.4.5.1.2	Generic	
	• **1G DETAIL:** Did not receive idle control symbol following requested maintenance training	Part 4, Sec. 3.7.1	Generic	
	• **1H DETAIL:** Framing signal toggles at an illegal time	Part 4, Sec. 3.2	Generic	
2.	Device encounters link Input errors as defined in point 1 above.	Part 4, Sec. 2.4	Generic	
	2A. DETAIL: Change the “Input Error-stopped” bit to 1 in the Port n Error and Status CSR. Further discussion of this point can be found in Part 4, Sec. A.4.1.	Part 4, Sec. 2.4.5.1.1	Generic	

Table 2-12. General device 8/16 LP-LVDS physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	If the Re-transmit Suppression Support bit is set (bit 25 of the Processing Elements Features CAR), suppression of error recovery on packet CRC errors is supported.	Part 4, Sec. 2.4.5.1.1 Part 4, Sec. 5.4.1 Part 4, Sec. 5.5.2.6 Part 4, Sec. 5.6.2.9 Part 4, Sec. 5.7.2.5 Part 4, Sec. 5.8.2.9	Generic	
	3A. DETAIL: The Re-transmit Suppression Mask field is only valid if bit 25 of the Processing Elements Features CAR is set. Otherwise, this field acts as reserved bits.		Generic	
	3B. DETAIL: Error recovery suppression is disabled if the entire Re-transmit Suppression Mask field is set to 0.		Generic	
	3C. DETAIL: Packets of a specific flow may have their re-transmission suppressed if the corresponding bit of the Re-transmit Suppression Mask is set in the Port n Control CSR, as defined in the version 1.3 RapidIO specification.		Generic	
4.	When the “Input Error-stopped” bit is set in the Port n Error and Status register, the port must follow the input error-recovery procedure	Part 4, Sec. 2.4.5.1.1	Generic	
	• **4A. DETAIL:** Send a packet-not-accepted control symbol to the sending device. Further discussion of this point can be found in Part 4, Sec. A.4.1.		Generic	
	• **4B. DETAIL:** Device silently discards all packets until a restart-from-error (link-request/input-status) control symbol is encountered. Further discussion of this point can be found in Part 4, Sec. A.4.1.		Generic	
	• **4C. DETAIL:** Change “Input Error-stopped” bit to 0 in the Port n Error and Status CSR. Further discussion of this point can be found in Part 4, Sec. A.4.1.		Generic	
5.	Device detects Output link errors	Part 4, Sec. 2.4.5.1.2 Part 4, Sec. 2.4.5.1.4 Part 4, Sec. 3.7.1.4	Generic	
	• **5A. DETAIL:** Received “packet-not-accepted” control symbol	Part 4, Sec. 2.4.5.1.2	Generic	
	• **5B. DETAIL:** Acknowledge control symbol time-out	Part 4, Sec. 2.4.5.1.4	Generic	
	• **5C. DETAIL:** Any acknowledge control symbol with an unexpected ackID value	Part 4, Sec. 2.4.5.1.2	Generic	
	• **5D. DETAIL:** Unexpected “packet-retry” control symbol	Part 4, Sec. 2.4.5.1.2	Generic	
	• **5E. DETAIL:** Unexpected training pattern	Part 4, Sec. 3.7.1.4	Generic	

Table 2-12. General device 8/16 LP-LVDS physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
6.	Device encounters Output link errors as defined in point 5 above.	Part 4, Sec. 2.4.5.1.2 Part 4, Sec. 2.4.5.1.4 Part 4, Sec. 3.7.1.4	Generic	
	• **6A. DETAIL:** Change the "Output Error-stopped" bit to 1 in the Port n Error and Status CSR. Further discussion of this point can be found in Part 4, Sec. A.4.2.	Part 4, Sec. 2.4.5.1.2	Generic	
7.	While the "Output Error-stopped" bit is set in the Port n Error and Status CSR the device must follow the output error-recovery procedure. Further discussion of this point can be found in Part 4, Sec. A.4.2.	Part 4, Sec. 2.4.5.1.2	Generic	
	• **7A. DETAIL:** Device stops transmitting new packets. Further discussion of this point can be found in Part 4, Sec. A.4.2.		Generic	
	• **7B. DETAIL:** Device sends link-request/input-status (restart-from-error) control symbol if no link-request control symbol is already outstanding (must wait for previous one to complete) and waits for link-response control symbol. Further discussion of this point can be found in Part 4, Sec. A.4.2.		Generic	
	• **7C. DETAIL:** Change the "Output Error-stopped" bit to 0 in the Port n Error and Status CSR. Further discussion of this point can be found in Part 4, Sec. A.4.2.		Generic	
	• **7D. DETAIL:** Start re-transmitting at the ackID value returned with the received link-response control symbol. Further discussion of this point can be found in Part 4, Sec. A.4.2.		Generic	
8.	When the 'Port OK' bit is set in the Port n Error and Status CSR, the device detects protocol violations.	Part 4, Sec. 3.7.1.4	Generic	
	• **8A. DETAIL:** Unsolicited packet-accepted or packet-retry acknowledge control symbol	Part 4, Sec. 2.4.5.1.2	Generic	
	• **8B. DETAIL:** Received packet-accepted control symbol before packet transmission has completed	Part 4, Sec. 4.2.1	Generic	
	• **8C. DETAIL:** Received link-request control symbol before sending link-response control symbol for previous link-response/input-status control symbol	Part 4, Sec. 2.6 Part 4, Sec. 2.4.5.1.2	Generic	
	• **8D. DETAIL:** Unexpected link-response control symbol	Part 4, Sec. 2.6.1	Generic	
	• **8E. DETAIL:** Unexpected restart-from-retry control symbol	Part 4, Sec. 4.3 Part 4, Sec. 2.4.5.1.2	Generic	
	• **8F DETAIL:** Unexpected stomp control symbol	Part 4, Sec. 4.3 Part 4, Sec. 2.4.5.1.2	Generic	
	• **8G. DETAIL:** Unexpected eop control symbol	Part 4, Sec. 4.3 Part 4, Sec. 2.4.5.1.2	Generic	
	• **8H. DETAIL:** Training pattern request occurs at illegal location	Part 4, Sec. 3.7.1	Generic	

Table 2-12. General device 8/16 LP-LVDS physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
9.	Device encounters a protocol violation as defined in point 8 above.	Part 4, Sec. 2.4.5.1.2	Generic	
	• **9A. DETAIL:** Change the "Output Error-stopped" or/and "Input Error-stopped" bits to 1 in the Port n Error and Status CSR, depending on conditions noted in items 1, 2, 4 and 5 of this table.		Generic	
10.	Any transmission error encountered during error recovery. Note: Some transmission errors cause subsequent protocol violations. The recovery algorithm can be used to recover from multiple transmission errors but that behavior is not required for compliance.	Part 4, Sec. 2.4.5	Generic	

2.13 Non-recoverable errors compliance list

There are a relatively small number of non-recoverable errors at the physical layer. Behavior of the interface is not defined for these events.

Table 2-13. General device 8/16 LP-LVDS physical layer non-recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device does not respond to link-request/send-training control symbol properly. No response time is specified. A reasonable test procedure should be followed to demonstrate this behavior.	Part 4, Sec. 3.7.1.1	Generic	
2.	Late or no response to throttle request	Part 4, Sec. 3.4	Generic	
3.	Device is attempting error recovery and ackID received in link-response control symbol does not make sense (device cannot complete recovery). Further discussion of this point can be found in Part 4, Sec. A.4.	Part 4, Sec. 2.4.5.1.2	Generic	
4.	Link-request control symbol to link-response control symbol time-out. Further discussion of this point can be found in Part 4, Sec. A.4.2.	Part 4, Sec. 5.5.2.2 Part 4, Sec. 5.6.2.2 Part 4, Sec. 5.7.2.2 Part 4, Sec. 5.8.2.2	Generic	
5.	Device port receives packets before device both sent and received one idle control symbol between 256 iterations of the training pattern.	Part 4, Sec. 3.7.1.1	Generic	
6.	Any transmission error encountered during error recovery. Note: Some transmission errors cause subsequent protocol violations. The recovery algorithm can be used to recover from multiple transmission errors but that behavior is not required for compliance.	Table 2-12 above	Generic	

2.14 State machines interaction compliance list

There are some rules of output error, input error, output retry, input retry state machine interaction.

Table 2-14. General device 8/16 LP-LVDS physical layer state machines interaction list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	If an input error situation was detected while the 'Input Retry-stopped' bit is 1 in the Port n Error and Status CSR, device shall change the 'Input Retry-stopped' bit to 0 and change the 'Input Error-stopped' bit to 1 in the Port n Error and Status CSR. The input retry recovery procedure stops, and the input error recovery will be followed. Further discussion of this point can be found in Part 4, Sec. A.3.1 and Part 4, Sec. A.4.1.	Part 4, Sec. 2.4.5	Generic	
2.	If an output error situation was detected while the 'Output Retry-stopped' bit is 1 in the Port n Error and Status CSR, device shall change the 'Output Retry-stopped' bit to 0 and change the 'Output Error-stopped' bit to 1 in the Port n Error and Status CSR. The output retry recover procedure stops, and the output error recovery procedure will be followed. Further discussion of this point can be found in Part 4, Sec. A.3.2 and Part 4, Sec. A.4.2.	Part 4, Sec. 2.4.5	Generic	
3.	Input state machines and output state machines shall work independently from each other. Further discussion of this point can be found in Part 4, Sec. A.	Part 4, Sec. 2.4.5	Generic	
	• **3A.DETAIL:** If the 'Input Retry-Stopped' or 'Input Error-Stopped' bits are set in the Port n Error and Status CSR, the device shall follow input retry/error recovery even if the condition causing the two previously mentioned bits to be changed to 1 was detected while the device was performing the output retry/error procedure.	Part 4, Sec. 2.4.5	Generic	
	• **3B.DETAIL:** If the 'Output Retry-Stopped' or 'Output Error-Stopped' bits are set in the Port n Error and Status CSR, the device shall follow output retry/error recovery even if the condition causing the two previously mentioned bits to be changed to 1 was detected while the device was performing input retry/error procedure.	Part 4, Sec. 2.4.5	Generic	
	• **3C.DETAIL:** If an input retry/error situation and an output retry/error situation are detected simultaneously, the device shall start both input and output recovery procedures.	Part 4, Sec. 2.4.5	Generic	
4.	If device is following input error recovery, all subsequent input port errors shall not affect operation of the device. Further discussion of this point can be found in Part 4, Sec. A.4.1.	Part 4, Sec. 2.4.5	Generic	
5.	If device is following output error recovery, all subsequent output port errors shall not affect operation of the device. Further discussion of this point can be found in Part 4, Sec. A.4.2.	Part 4, Sec. 2.4.5	Generic	

Blank Page

Chapter 3 1x/4x LP-Serial Physical Layer Checklists

3.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for 1x/4x LP-Serial Physical Layer devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The 1x/4x LP-Serial Physical layer inter-operability and certification checklist is broken down into a number of sub-lists.

3.2 General specification compliance list

This section specifies general requirements for a compliant device.

Reads and writes to CSRs and CARs are referenced from RapidIO transactions received by a device.

Table 3-1. General device 1x/4x LP-Serial physical layer general compliance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device assigns reserved packet fields to logic 0s. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2 Part 6, Sec. 2.2	Generic	
2.	Reserved packet field contents do not affect operation of the device. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
3.	Implementation-defined packet fields do not affect operation of the device unless the function is understood by the receiving device. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
4.	Received reserved packet field encodings do not affect operation of the device if it is not necessary for the field to be defined for the requested transaction. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	Inter-op
5.	A received reserved packet field encoding is regarded as an error if it is necessary for the field to be defined for the requested transaction. Applied to Physical Layer fields.	Part 1, Sec. 4.1.2	Generic	
6.	All registers are 32 bits in size, and aligned to 32 bit boundaries.	Part 1, Sec. 5 Part 2, Sec. 5 Part 3, Sec. 3 Part 4, Sec. 5 Part 6, Sec. 6	Generic	Inter-op
7.	Reads to reserved CAR bits return logic 0s. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	
8.	Writes to CARs do not affect operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
9.	Reads to implementation-defined CAR bits return the implementation defined value. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
10.	Writes to implementation-defined CAR bits do not affect operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
11.	Reads to reserved CARs do not cause an error. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.1	Generic	Inter-op

Table 3-1. General device 1x/4x LP-Serial physical layer general compliance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	Reads to reserved CARs return logic 0s when read. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
13.	Writes to reserved CARs do not cause an error. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.1	Generic	Inter-op
14.	Writes to reserved CARs do not affect the operation of the device. Applied to Physical Layer CARs. Note that no Physical Layer CARs are defined in version 1.3 of the RapidIO specification.	Part 1, Sec. 5.2	Generic	Inter-op
15.	Reads to reserved CSRs and reserved Extended Features register bits return logic 0s. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2, Part 6, Sec. 6.2, Table 6-1.	Generic	
16.	Writes to reserved CSRs and reserved Extended Features register bits do not affect operation of the device. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2, Part 6, Sec. 6,2, Table 6-1.	Generic	Inter-op
17.	Reads to reserved CSRs and reserved Extended Features registers do not cause an error. Applied to Physical CSRs and Extended Features Space.	Part 1, Sec. 5.1	Generic	Inter-op
18.	Reads to reserved CSRs and reserved Extended Features registers return logic 0s when read. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2, Part 6, Sec. 6, Table 6-1.	Generic	
19.	Writes to reserved CSRs and reserved Extended Features registers do not cause an error. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.1	Generic	Inter-op
20.	Writes to reserved CSRs and reserved Extended Features registers do not affect operation of the device. Applied to Physical Layer CSRs and Extended Features Space.	Part 1, Sec. 5.2, Part 6, Sec. 6.2, Table 6-1.	Generic	Inter-op

3.3 Signal names compliance lists

The defined signals must exist, although the actual names used on a particular device may vary. The actual names used must allow an unambiguous match to the names defined in the 8/16 LP-LVDS physical specification.

3.3.1 1x device compliance list

Table 3-2. General device 1x/4x LP-Serial physical layer 1x symmetric device pins

Item no.	Signal name	I/O	Description	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	TD[0], $\overline{\text{TD[0]}}$	O	Differential pair, lane 0	Part 6, Sec. 7.2	Generic	
2.	RD[0], $\overline{\text{RD[0]}}$	I	Differential pair, lane 0	Part 6, Sec. 7.2	Generic	

3.3.2 4x device compliance list

Table 3-3. General device 1x/4x LP-Serial physical layer 4x symmetric device pins

Item no.	Signal name	I/O	Description	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	TD[0], $\overline{\text{TD[0]}}$	O	Differential pair, lane 0	Part 6, Sec. 7.2	Generic	
2.	TD[1], $\overline{\text{TD[1]}}$	O	Differential pair, lane 1	Part 6, Sec. 7.2	Generic	
3.	TD[2], $\overline{\text{TD[2]}}$	O	Differential pair, lane 2	Part 6, Sec. 7.2	Generic	
4.	TD[3], $\overline{\text{TD[3]}}$	O	Differential pair, lane 3	Part 6, Sec. 7.2	Generic	
5.	RD[0], $\overline{\text{RD[0]}}$	I	Differential pair, lane 0	Part 6, Sec. 7.2	Generic	
6.	RD[1], $\overline{\text{RD[1]}}$	I	Differential pair, lane 1	Part 6, Sec. 7.2	Generic	
7.	RD[2], $\overline{\text{RD[2]}}$	I	Differential pair, lane 2	Part 6, Sec. 7.2	Generic	
8.	RD[3], $\overline{\text{RD[3]}}$	I	Differential pair, lane 3	Part 6, Sec. 7.2	Generic	

3.4 Basic functionality compliance list

This is the list for basic functionality for the device.

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device meets target AC specifications	Part 6, Sec. 8	Generic	
2.	1x/4x ports must be able to function as 1x ports	Part 6, Sec. 4.5.10 Part 6, Sec. 4.7.3.6	Generic	
3.	Control symbols shall follow 24-bit control symbol format.	Part 6, Sec. 3.3	Generic	
	• **3A. DETAIL:** CRC for the symbols shall be properly calculated and placed into a crc field.	Part 6, Sec. 3.6	Generic	
4.	Undefined control symbols (those having a reserved or undefined value in the stype0, stype1, or cmd field) do not affect operation of the device. Note that cmd field values of 1-7 are reserved for Start-of-packet, Stomp, End-of-Packet, Restart-from-Retry and Multicast Event. If only one part of the symbol (stype0, stype1 or cmd) is undefined then it shall not affect operation of the device and the other part shall be processed.	Part 6, Sec.3.1	Generic	
	• **4A. DETAIL:** The link-request control symbols with reserved cmd field encoding shall cancel packet whose transmission is in progress, but itself shall not affect operation of the device and no error shall be reported	Part 6, Sec. 3.5.5 Part 6, Sec. 5.11.2.3	Generic	
5.	If the CRF bit is not supported, transaction request flow A is mapped to priority 0. If the CRF bit is supported, transaction request flow A is mapped to priority 0 if CRF=0. Otherwise, if CRF=1, transaction request flow B is mapped to priority 0.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 6, Sec. 5.4.3 Part 6, Sec. 5.9 Part 6, Sec. 5.10	Generic	
	• **5A. DETAIL:** Request packets are transmitted at priority level 0	Part 7, Sec. 4.5 Part 6, Sec. 5.4.3	Class 2,3	
	• **5B. DETAIL:** Response packets are transmitted at priority level 1, 2, or 3	Part 6, Sec. 5.4.3	Generic	
6.	If the CRF bit is not supported, transaction request flow B is mapped to priority 1. If the CRF bit is supported, transaction request flow C is mapped to priority 1 if CRF=0. Otherwise, if CRF=1, transaction request flow D is mapped to priority 1.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 6, Sec. 5.4.3 Part 6, Sec. 5.9 Part 6, Sec. 5.10	Generic	
	• **6A. DETAIL:** Request packets are transmitted at priority level 1	Part 7, Sec. 4.5 Part 6, Sec. 5.4.3	Class 2,3	
	• **6B. DETAIL:** Response packets are transmitted at priority level 2, or 3	Part 6, Sec. 5.4.3	Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
7.	If the CRF bit is not supported, transaction request flow C is mapped to priority 2. If the CRF bit is supported, transaction request flow E is mapped to priority 2 if CRF=0. Otherwise, if CRF=1, transaction request flow F is mapped to priority 2.	Part 7, Sec. 4.5 Part 1, Sec. 2.3 Part 6, Sec. 5.4.3 Part 6, Sec. 5.9 Part 6, Sec. 5.10	Generic	
	• **7A. DETAIL:** Request packets are transmitted at priority level 2	Part 7, Sec. 4.5 Part 6, Sec. 5.4.3	Class 2,3	
	• **7B. DETAIL:** Response packets are transmitted at priority level 3	Part 6, Sec. 5.4.3	Generic	
8.	In a processing element, a higher priority packet generated before a lower priority packet with the same source ID and destination ID is always transmitted before the lower priority packet.	Part 6, Sec. 5.9	Generic	
9.	Packets received by a processing element are processed in the order they were received.	Part 6, Sec. 5.9	Generic	
10.	Packets with the same priority level and CRF bit setting cannot pass each other. Packets with the CRF bit set at a given priority are allowed to pass packets with the CRF bit clear at the same priority.	Part 6, Sec. 5.4.3	Generic	
11.	At the transmitter, packets of higher priority may pass packets of a lower priority level.	Part 6, Sec. 5.4.3 Part 6, Sec. 5.10	Generic	
12.	All registers in the 1x/4x/LP-Serial Physical Layer Specification Extended Features data structure can be read and/or written, as per constraints specified in Part 6, Chapter 6. The Extended Features Space is located at bytes offsets 0x0100 through 0xFFFC of the device configuration space.	Part 6, Sec. 6	Generic	
	• **12A. DETAIL:** Port Maintenance Block Header CSR is read-only, and is compliant with the following:	Part 6, Sec. 6.5.2.1 Part 6, Sec. 6.6.2.1 Part 6, Sec. 6.7.2.1 Part 6, Sec. 6.8.2.1	Generic	
	• **12A1. DETAIL:** Port Maintenance Block Header CSR has the proper Extended Features block ID in the EF_ID field.		Generic	
	• **12A2. DETAIL:** Port Maintenance Block Header EF_PTR field reset value is implementation dependant.		Generic	
	• **12B. DETAIL:** Port Link Time-out Control CSR; reset value of time-out value field is 0xFFFFFF	Part 6, Sec. 6.5.2.2 Part 6, Sec. 6.6.2.2 Part 6, Sec. 6.7.2.2 Part 6, Sec. 6.8.2.2	Generic	
	• **12B1. DETAIL:** Port Link Time-out Control CSR Bits 0-23 are writable, and time-out value varies with value written.		Generic	
	• **12B2. DETAIL:** Port Link Time-out Control CSR Bits 24-31 cannot change value from 0.		Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12C. DETAIL:** Port Response Time-out Control CSR; reset value of the time-out value field is 0xFFFFFF (end point devices only)	Part 6, Sec. 6.5.2.3 Part 6, Sec. 6.6.2.3	Generic	
	• **12C1. DETAIL:** Port Response Time-out Control CSR Bits 0-23 are writable, and time-out value varies with value written.		Generic	
	• **12C2. DETAIL:** Port Response Time-out Control CSR Bits 24-31 cannot change value from 0.		Generic	
	• **12D. DETAIL:** Port General Control CSR; reset value is implementation dependant	Part 6, Sec. 6.5.2.4 Part 6, Sec. 6.6.2.4 Part 6, Sec. 6.7.2.3 Part 6, Sec. 6.8.2.3	Generic	
	• **12D1. DETAIL:** Verify Host field accurately reflects the capabilities of the device.		Generic	
	• **12D2. DETAIL:** Verify Master Enable field accurately reflects the capabilities of the device.		Generic	
	• **12D3. DETAIL:** Verify Discovered field is set to 1 as soon as a maintenance write request is received to this register bit and if Discovered bit is 0 after reset for this device.		Generic	
	• **12E. DETAIL:** Port n Error and Status CSR; reset value is 0x00000001	Part 6, Sec. 6.5.2.5 Part 6, Sec. 6.6.2.8 Part 6, Sec. 6.7.2.4 Part 6, Sec. 6.8.2.7	Generic	
	• **12E1. DETAIL:** Verify that fields in the Port n Error and Status CSR are set on the appropriate conditions.		Generic	
	• **12E2. DETAIL:** Verify that the following fields are cleared by writing 1 to them: Output Retry-encountered, Output Error-encountered, Input Error-encountered, Post-write Pending, Port Error.		Generic	
	• **12E3. DETAIL:** Verify that the following fields do not change their values when written to: Output Retried, Output Retry-stopped, Output Error-stopped, Input Retry-stopped, Input Error-stopped, Port OK, Port Un-initialized		Generic	
	• **12F. DETAIL:** Port n Control CSR is compliant with the following:	Part 6, Sec. 6.5.2.6 Part 6, Sec. 6.6.2.9 Part 6, Sec. 6.7.2.5 Part 6, Sec. 6.8.2.8	Generic	
	• **12F1. DETAIL:** Reset value of the following fields is implementation dependant: Port Width, Initialized Port Width, Output Port Enable, Input Port Enable (if applicable, also Multicast Event Participant, Enumeration Boundary).		Generic	
	• **12F2. DETAIL:** Reset value of the following fields is logic 0s: Port Width Override, Port Disable, Error Checking Disable (if applicable, also Re-transmit Suppression Mask).		Generic	
	• **12F3. DETAIL:** Reset value of the Port Type field is implementation defined.		Generic	
	• **12F4. DETAIL:** bits 13, 15-19, 28-30 are reserved (always logic 0s). Any bits not included in the implementation are also reserved.		Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12F5. DETAIL:** The following fields are read-only: Port Width, Initialized Port Width, Port Type. All other fields of the Port n Control CSR are read/write, if the implementation supports their existence.		Generic	
	• **12F6. DETAIL:** A software write to the Port Width Override bits will cause a port to re-initialize.		Generic	
	• **12G. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Link Maintenance Request CSR register exists for each port at the correct offset.	Part 6, Sec. 6.6.2.5 Part 6, Sec. 6.8.2.4	Generic	
	• **12G1. DETAIL:** A write to the Port n Link Maintenance Request CSR results in the correct control symbol being sent.		Generic	
	• **12G2. DETAIL:** A read of the Port n Link Maintenance Request CSR returns the last command sent.		Generic	
	• **12G3. DETAIL:** The reset value of the Port n Link Maintenance Request CSR is 0.		Generic	
	• **12H. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Link Maintenance Response CSR register exists for each port at the correct offset.	Part 6, Sec. 6.6.2.6 Part 6, Sec. 6.8.2.5	Generic	
	• **12H1. DETAIL:** The first read of the Port n Link Maintenance Response CSR register will return the correct response for the last command sent by the Port n Link Maintenance Request CSR.		Generic	
	• **12H2. DETAIL:** Subsequent reads of the Port n Link Maintenance Response CSR register have the response_valid field cleared.		Generic	
	• **12H3. DETAIL:** The reset value of the Port n Link Maintenance Response CSR register is 0.		Generic	
	• **12H4. DETAIL:** All bits in the Port n Link Maintenance Response CSR register are read only.		Generic	
	• **12I. DETAIL:** For devices which support end point functionality with software assisted error recovery (EF_ID = 0x0002), the Port n Local ackID CSR register exists for each port at the correct offset.	Part 6, Sec. 6.6.2.7 Part 6, Sec. 6.8.2.6	Generic	
	• **12I1. DETAIL:** The Port n Local ackID CSR register always returns the correct value when read locally.		Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **12I2. DETAIL:** Writing the Outbound_ackID field will force the retransmission of the corresponding outstanding unacknowledged packet, whose ackID=Outbound_ackID.	Part 6, Sec. 6.6.2.7 Part 6, Sec. 6.8.2.6	Generic	
	• **12I3. DETAIL:** When read from the RapidIO port, the Port n Local ackID CSR register always returns values as if the maintenance read request had not occurred.		Generic	
	• **12I4. DETAIL:** The reset value of the Port n Local ackID CSR register is 0.		Generic	
	• **12I5. DETAIL:** All fields of the Port n Local ackID CSR registers may be written to.		Generic	
	• **12I6. DETAIL:** Bits 1-4, 8-15, and 24-26 are reserved (always logic 0s).		Generic	
	• **12J. DETAIL:** For a general end point device that supports software assisted error recovery, in the Port n Link Maintenance Request CSRs, the reset value of the command field is logic 0's.	Part 6, Sec. 6.6.2.5 Part 6, Sec. 6.8.2.4	Generic	
	• **12K. DETAIL:** For a general end point device that supports software assisted error recovery, the Port n Link Maintenance Response CSRs are read only and are compliant with the following:	Part 6, Sec. 6.6.2.6 Part 6, Sec. 6.8.2.5	Generic	
	• **12K1. DETAIL:** Reset values of the response_valid, ackID_status and link_status fields are logic 0s.		Generic	
	• **12L. DETAIL:** For a general end point device that supports software assisted error recovery, in the Port n Local ackID CSRs the reset values of the all fields are logic 0s.	Part 6, Sec. 6.6.2.7 Part 6, Sec. 6.8.2.6	Generic	
	• **12M. DETAIL:** Processing Elements Features CAR is read-only, and is compliant with the following:	Part 6, Sec. 6.4.1	Generic	
	• **12M1. DETAIL:** The values of Re-transmit Suppression Support and CRF Support are implementation dependent.		Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
13.	Device follows system initialization and exploration inter-operability procedure	Part 7, Sec. 2.2 Part 7, Sec. 2.3	Generic	
	• **13A. DETAIL:** End point agent device that contain a boot ROM is initially assigned base device ID=0xFE at power-up	Part 7, Sec. 2.2	Generic	
	• **13B. DETAIL:** End point agent device without a boot ROM is initially assigned base device ID=0xFF at power-up	Part 7, Sec. 2.2	Generic	
	• **13C. DETAIL:** System host device is initially assigned a non-reserved base device ID at power-up (end point device only)	Part 7, Sec. 2.2	Class 2,3	
	• **13D. DETAIL:** Host device sets the Discovered bit at power-up	Part 7, Sec. 2.3	Generic	
	• **13E. DETAIL:** Agent device resets the Discovered bit at power-up	Part 7, Sec. 2.3	Generic	
	• **13F. DETAIL:** Host device sets the Master Enable bit at power-up (end point device only)	Part 7, Sec. 2.3	Class 2,3	
	• **13G. DETAIL:** Agent device resets the Master Enable bit at power-up (end point device only)	Part 7, Sec. 2.3	Generic	
	• **13H. DETAIL:** Device with switch functionality defaults route information to allow boot ROM access by system host	Part 7, Sec. 2.2	Generic	
	• **13I. DETAIL:** Switch device must send maintenance responses that it generates to the port that the maintenance request was received on	Part 7, Sec. 2.3	Generic	
14.	A port shall time out if an acknowledgement control symbol for a packet is never received.	Part 6, Sec. 5.11.1	Generic	
	• **14A. DETAIL:** Verify that the maximum time-out value is between 3 and 6 seconds. A reasonable test procedure should be followed for simulation environments.		Generic	
15.	A request shall time out if a response packet is never received.	Part 6, Sec. 5.11.1	Generic	
	• **15A. DETAIL:** Verify that the maximum time-out value is between 3 and 6 seconds. A reasonable test procedure should be followed for simulation environments.		Generic	
16.	The pattern for comma detection during lane synchronization establishment shall be 0011111010/1100000101.	Part 6, Sec. 4.5.7.4	Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
17.	Device follows 8B/10B encoding rules.	Part 6, Sec. 4.5.3 Part 6, Sec. 4.5.4 Part 6, Sec. 4.5.6, Table 4-1, Part 6, Sec. 4.5.6, Table 4-2	Generic	
	• **17A. DETAIL:** Selection of code group for a given data value is dependent upon the data value and the running disparity of the code-group that has just been generated by the encoder.		Generic	
	• **17B. DETAIL:** Selection of code groups is restricted to code groups captured in Part 6, Tables 4-1 and 4-2.		Generic	
	• **17C. DETAIL:** After each character is encoded, the resulting code-group shall be used by the encoder to update the running disparity.	Part 6, Sec. 4.5.3 Part 6, Sec. 4.5.4	Generic	
18.	Device follows 8B/10B decoding rules.	Part 6, Sec. 4.5.3, Part 6, Sec. 4.5.6, Part 6, Table 4-1, Part 6, Table 4-2	Generic	
	• **18A. DETAIL:** Decoding of a code-group into a data/special character is dependent on the code-group and the running disparity of the received code-group that has just been decoded by the decoder.		Generic	
	• **18B. DETAIL:** Decoding of code groups is restricted to code groups captured in Part 6, Tables 4-1 and 4-2.		Generic	
	• **18C. DETAIL:** If a code-group can't be decoded to a defined data/special character, the code-group is decoded to a character that is flagged in some manner as invalid.	Part 6, Sec. 4.5.6	Generic	
	• **18D. DETAIL:** After each code-group is decoded, the decoded code-group shall be used by the decoder to update the decoder running disparity.	Part 6, Sec. 4.5.3	Generic	
19.	A 1x/4x port operating in 1x mode shall transmit identical character streams of delimited control symbols and packets (as well as generated idle sequence) over both lane 0 and lane 2 until such time as either lane 0 or lane 2 has been selected as the 1x lane to be received on by the initialization state machine.	Part 6, Sec. 4.5.10	Generic	
20.	A 1x/4x port operating in 1x mode must be able to allow the link partner to disable the unused lane (the lane not selected by the initialization state machine). The link partner may or may not elect to disable this lane.	Part 6, Sec. 4.5.10	Generic	Inter-op
21.	A 1x LP-Serial port (or a 1x/4x port operating in 1x mode) shall encode and transmit the character stream of delimited control symbols and packets received from the upper layers over the link in the order the characters were received from the upper layers.	Part 6, Sec. 4.5.10 Part 6, Sec.6.8.2.8	Generic	
22.	A 1x/4x port operating in 1x mode shall, on reception, select the code-group stream from either lane 0 or 2 according to the state of the 1x/4x_initialization state machine.	Part 6, Sec. 4.7	Generic	

Table 3-4. General device 1x/4x LP-Serial physical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
23.	A 1x/4x port operating in 4x mode shall follow the following transmission/reception rules:	Part 6, Sec. 4.5.11	Generic	
	• **23A. DETAIL:** On transmission the port shall stripe the character stream of delimited control symbols and packets across the four lanes before 8B/10B encoding beginning with lane 0. After striping, each of the 4 streams of characters shall be independently 8B/10B encoded and transmitted.		Generic	
	• **23B. DETAIL:** When neither delimited control symbols nor packets are available from the upper layers for transmission, the 4x idle sequence shall be transmitted. This can be achieved by feeding the 1x idle sequence in parallel to the inputs of the encoders for all four lanes for encoding and transmission on the four lanes. The 1x sequence is not striped across the four lanes.		Generic	
	• **23C. DETAIL:** On reception, each lane shall be 8B/10B decoded. After decoding, the four lanes shall be aligned. After alignment, the columns shall be destriped into a single character stream and passed to the upper protocol layers.		Generic	
	• **23D. DETAIL:** 8B/10B Encoding/Decoding shall be performed for each lane independently. Running disparity shall be calculated independently for each lane for transmission and reception.	Part 6, Sec. 4.5.11 Part 6, Sec. 4.5.3	Generic	
	• **23E. DETAIL:** The maximum lane skew that can be un-ambiguously corrected is the time it takes to transmit 7 code-groups on a lane.	Part 6, Sec. 4.5.11, Part 6, Sec. 8	Generic	
24.	On start of transmission, the transmitter shall use negative disparity.	Part 6, Sec 4.5.3	Generic	
25.	On start of transmission, the receive may use negative or positive disparity.	Part 6, Sec 4.5.3	Generic	
26.	Port follows rules for transmission bit ordering	Part 6, Sec 4.5.5	Generic	Inter-op
27.	Port detects all single bit code group errors as defined in Part 6, Section 4.5.8, Table 4-4.	Part 6, Sec 4.5.8	Generic	
	• **27A. DETAIL:** All single bit code group errors shall be treated as recoverable errors by the receiver.	Part 6, Sec 4.5.8	Generic	

3.5 AC electrical compliance list

This is the list for electrical compliance of serial RapidIO signals.

All measurements must be taken in accordance with discussions/guidance captured in Part 6, Chapter 8. All speeds quoted in Table 3-5 are clock rates.

Table 3-5. General device 1x/4x LP-Serial physical layer AC electrical list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Short run transmitter 1.25 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-1	Part 6, Sec. 8.5, Table 8-1	Generic	
2.	Short run transmitter 2.5 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-2	Part 6, Sec. 8.5, Table 8-2	Generic	
3.	Short run transmitter 3.125 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-3	Part 6, Sec. 8.5, Table 8-3	Generic	
4.	Long run transmitter 1.25 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-4.	Part 6, Sec. 8.5, Table 8-4	Generic	
5.	Long run transmitter 2.5 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-5.	Part 6, Sec. 8.5, Table 8-5	Generic	
6.	Long run transmitter 3.125 GHz baud rate signals must meet specifications defined in Part 6, Sec. 8.5, Table 8-6	Part 6, Sec. 8.5, Table 8-6	Generic	
7.	Transmitter Output Eye measurements must meet specifications defined in Part 6, Sec. 8.5, Table 8-7 for the various short/long run baud rates.	Part 6, Sec. 8.5, Table 8-7	Generic	
8.	1.25 GHz receiver signals must meet specifications as defined in Part 6, Sec. 8.6, Table 8-8.	Part 6, Sec. 8.6, Table 8-8	Generic	
9.	2.5 GHz receiver signals must meet specifications as defined in Part 6, Sec. 8.6, Table 8-9.	Part 6, Sec. 8.6, Table 8-9	Generic	
10.	3.125 GHz receiver signals must meet specifications as defined in Part 6, Sec. 8.6, Table 8-10.	Part 6, Sec. 8.6, Table 8-10	Generic	
11.	1.25 GHz receiver signals must meet the receiver eye opening diagrammed in Part 6, Sec. 8.7, Figure 8-4 and specified in Part 6, Sec. 8.7, Table 8-11.	Part 6, Sec. 8.7, Figure 8-4 Part 6, Sec. 8.7, Table 8-11	Generic	
12.	2.5 GHz receiver signals must meet the receiver eye opening diagrammed in Part 6, Sec. 8.7, Figure 8-4 and specified in Part 6, Sec. 8.7, Table 8-11.	Part 6, Sec. 8.7, Figure 8-4 Part 6, Sec. 8.7, Table 8-11	Generic	
13.	3.125 GHz receiver signals must meet the receiver eye opening diagrammed in Part 6, Sec. 8.7, Figure 8-4 and specified in Part 6, Sec. 8.7, Table 8-11.	Part 6, Sec. 8.7, Sec. 8.7, Figure 8-4 Part 6, Sec. 8.7, Table 8-11	Generic	

3.6 Link initialization compliance list

This is the list for device link initialization.

Table 3-6. General device 1x/4x LP-Serial physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device operating in 1X mode must follow the link synchronization procedure.	Part 6, Sec. 4.7.3.3 Part 6, Sec. 5.3.2	Generic	Inter-op
	• **1A. DETAIL:** In the Port n Error and Status CSR, the ’Port OK’ bit will be 0 and the ’Port Uninitialized’ bit will be 1 after device reset. This is the expected visible behavior when the link is in the ‘NO_SYNC’ state of Part 6, Figure 4-9.		Generic	
	• **1B. DETAIL:** After reset, for a device operating in 1X mode the Port n Error and Status CSR Port OK bit will be change to 1 and the ’Port Uninitialized’ bit will be set to 0 if 128 commas are received without an /INVALID/ code group for all lanes of a device, and 7 error-free status control symbols are received with no intervening errors. This is the expected visible behavior when the link transitions to the ‘SYNC’ state of Part 6, Figure 4-9.		Generic	
	• **1C. DETAIL:** When the Port n Error and Status CSR ’Port OK’ bit is 1 and the ’Port Uninitialized’ bit is 0, the ’Port OK’ bit is changed to 0 and the ’Port Uninitialized’ bit is changed to 1 if two or more /INVALID/ code groups are detected within 255 code groups on any one lane of a device. This is the expected visible behavior when the link transitions out of the ‘SYNC’ state of Part 6, Figure 4-9.		Generic	
	• **1D. DETAIL:** When the Port n Error and Status CSR ’Port OK’ bit is 0 and the ’Port Uninitialized’ bit is 1 after condition 1C is met, the ’Port OK’ bit changes to 1 and the ’Port Uninitialized’ bit is set to 0 only if 128 commas are received without an /INVALID/ code group being received, and 7 error-free status control symbols are received with no intervening errors. This is the expected visible behavior when the link transitions back to the ‘SYNC’ state of Part 6, Figure 4-9.		Generic	

Table 3-6. General device 1x/4x LP-Serial physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
2.	1x/4x device must follow the link alignment procedure.	Part 6, Sec. 4.7.3.4	Generic	Inter-op
	• **2A. DETAIL:** After the device reset, a 1x/4x device shall have the Port n Error and Status CSR 'Port OK' bit is 0 and the 'Port Uninitialized' bit is 1. This is the expected visible behavior when the link transitions to the 'NOT_ALIGNED' state of Part 6, Figure 4-10.		Generic	
	• **2B. DETAIL:** After reset, for a device operating in 1x4x mode, the Port n Error and Status CSR Port OK bit will change to 1 and the Port Uninitialized bit will be set to 0 if each lane has received 128 commas without an /INVALID/ code group, four consecutive ||A|| are achieved without an intervening alignment error, and 7 error-free status control symbols are received with no intervening errors. This is the expected visible behavior when the link transitions to the 'ALIGNED' state of Part 6, Figure 4-10.	Part 6, Sec. 4.7.3.4 Part 6, Sec. 5.3.2	Generic	
	• **2C. DETAIL:** A ||A|| condition is achieved even if the /A/ in each lane are skewed by up to 7 code groups.	Part 6, Sec. 4.5.11	Generic	
	• **2D. DETAIL:** For a device operating in 1x4x mode after achieving the condition of 2B, the Port n Error and Status CSR Port OK bit will change to 0 and the Port Uninitialized bit will be set to 1 if two alignment errors are received with less than four consecutive ||A|| between them, or if a lane reaches the condition described in 1C. This is the expected visible behavior when the link transitions out of the 'ALIGNED' state of Part 6, Figure 4-10.	Part 6, Sec. 4.7.3.4	Generic	
	• **2E. DETAIL:** After reaching the condition in 2D, the Port n Error and Status CSR Port OK bit will change to 1 and the Port Uninitialized bit will be set to 0 when all lanes reach the condition described in 2B. This is the expected visible behavior when the link transitions back to the 'ALIGNED' state of Part 6, Figure 4-10.		Generic	

Table 3-6. General device 1x/4x LP-Serial physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	1x device must follow the following initialization procedure.	Part 6, Sec. 4.7.3.5 Part 6, Sec. 4.7.1 Part 6, Sec. 5.3.2	Generic	Inter-op
	• **3A. DETAIL:** After reset, the link output driver is disabled for long enough to force initialization of the link partner. From item 1B, the time required to transmit two or more link symbols should be sufficient. This is the expected visible behavior when the link is in the 'SILENT' state of Part 6, Figure 4-11.		Generic	
	• **3B. DETAIL:** After the time accounted for in 3A has passed, the link output driver is enabled and shall transmit continuous idle packets until the condition in 1B is achieved. This is the expected visible behavior when the link is in the 'SEEK' state of Part 6, Figure 4-11.		Generic	
	• **3C. DETAIL:** After the condition in 1B is achieved, the port shall transmit the idle sequence interrupted by one status control symbol at least every 1024 transmitted code-groups until the port has received an error free status control symbol from the connected port. This is the expected visible behavior when the link enters the '1X_MODE' state of Part 6, Figure 4-11.		Generic	
	• **3D. DETAIL:** After the port achieves the condition in 3C, the port shall transmit the idle sequence and a minimum of 15 status control symbols and shall receive an additional 6 error free status control symbols with no intervening detected errors before beginning transmission of packets and other (non-status) control symbols.		Generic	

Table 3-6. General device 1x/4x LP-Serial physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	1x/4x device must follow the following initialization procedure.	Part 6, Sec. 4.7.3.6 Part 6, Sec. 4.7.2	Generic	Inter-op
	• **4A. DETAIL:** After reset, the link output drivers are disabled for long enough to force initialization of the link partner. From item 1B, the time required to transmit two or more link symbols should be sufficient. This is the expected visible behavior when the link enters the 'SILENT' state of Part 6, Figure 4-12.		Generic	
	• **4B. DETAIL:** After the time for step 4A has expired, the device shall enable lane 0 and lane 2 and transmit the idle sequence on both lanes. This is the expected visible behavior when the link enters the 'SEEK' state of Part 6, Figure 4-12.		Generic	
	• **4C. DETAIL:** Once the condition in 1B is achieved for either lane 0 or lane 2, the port shall also enable lanes 1 and 3 and begin transmission of the idle sequence on all lanes. This is the expected visible behavior when the link enters the 'DISCOVERY' state of Part 6, Figure 4-12.		Generic	
	• **4D. DETAIL:** The device shall transmit across lanes 0 through 3 in 4x mode if the condition in 3C is achieved and the device is not forced by application dependent means to work in 1x mode. This is the expected visible behavior when the link enters the '4X_MODE' state of Part 6, Figure 4-12.		Generic	
	• **4E. DETAIL:** The device shall transmit on lane 0 if the condition in 4C is not achieved and the condition in 1B is achieved for lane 0 and the device is not forced by application dependent means to work in 1x mode on lane 2. This is the expected visible behavior when the link enters the '1X_MODE_LANE0' state of Part 6, Figure 4-12.		Generic	
	• **4F. DETAIL:** The device shall transmit on lane 2 if the condition in 4C is not achieved, the condition in 1B is not achieved for lane 0 or the device is forced by application dependent means to work in 1x mode on lane 2, and the condition in 1B is achieved for lane 2 . This is the expected visible behavior when the link enters the '1X_MODE_LANE2' state of Part 6, Figure 4-12.		Generic	
	• **4G. DETAIL:** If the condition in 4E or 4F is achieved, the device shall disable output drivers on lanes 1 and 3.		Generic	
	• **4H. DETAIL:** If the conditions in 1C occur when the device is transmitting only on port 0 or only on port 2, the port will behave as per 4A.		Generic	
	• **4I. DETAIL:** If the conditions in 2D occur when the device is transmitting on all four lanes, the port will behave as per 4A.		Generic	

Table 3-6. General device 1x/4x LP-Serial physical layer link initialization list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	• **4J. DETAIL:** After an LP-Serial port is initialized, it shall transmit the idle sequence interrupted by one status control symbol at least every 1024 transmitted code-groups until the port has received an error free status control symbol from the connected port.	Part 6, Sec. 5.3.2	Generic	
	• **4K. DETAIL:** After an initialized LP-Serial port has received an error free status control symbol from the connected port, the port shall transmit the idle sequence and a minimum of 15 status control symbols and shall receive an additional 6 error free status control symbols with no intervening detected errors before entering the normal operational state. Once in the normal operational state, the port may begin the transmission of packets and other (non-status) control symbols.		Generic	

3.7 Link maintenance compliance list

This is the list for link maintenance functionality.

Table 3-7. General device 1x/4x LP-Serial physical layer link maintenance list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Link-request/input-status control symbol causes a link-response control symbol	Part 6, Sec. 5.5	Generic	Inter-op
2.	Link-response control symbol port_status field indicates input port status prior to receiving the link-request/input-status (restart-from-error)	Part 6, Sec. 3.4.5	Generic	
	• **2A.DETAIL**: Error means unrecoverable problem encountered, won't accept any packets		Generic	
	• **2B. DETAIL:** Retry-stopped means that input port is stopped due to a retry and will not accept packets until receiving a "restart-from-retry" or a "restart-from-error" control symbol		Generic	
	• **2C. DETAIL:** Error-stopped means that input port is stopped due to a transmission error and will not accept packets until receiving a "restart-from-error" control symbol		Generic	
	• **2D. DETAIL:** OK means that the input port is operating and can communicate with the connected device		Generic	
	• **2E. DETAIL:** A link-response control symbol with a reserved port_status field value shall not affect the operation of the device. Note that this may result in a device time out waiting for a non-reserved status link response.		Generic	
3.	Link-request/reset control symbol causes the device to reset after 4 link-request/reset control symbols in a row without any intervening packets or other control symbols, except status control symbols. Response time for reset is implementation specific.	Part 6, Sec. 3.5.5.1 Part 6, Sec. 5.5	Generic	
4.	Link-request/input-status, link-response control symbol pair forces completion of all preceding activity.	Part 6, Sec. 5.5	Generic	
	• **4A. DETAIL:** All preceding packets have generated acknowledge control symbol if applicable		Generic	
	• **4B. DETAIL:** Returned ackID_status correctly indicates next expected ackID.		Generic	
5.	Device doesn't issue more than one outstanding link-request control symbol.	Part 6, Sec. 5.5	Generic	
	• **5A. DETAIL:** Transmission of another link control symbol must be delayed until the reception of the expected link-response control symbol or time-out.		Generic	

3.8 Packet transmission compliance list

This is the list for the device transmitting a packet, and applies to all devices, as all generic devices are required to generate response packets.

Table 3-8. General device 1x/4x LP-Serial physical layer packet transmission list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device cannot issue more than 31 unacknowledged packets	Part 6, Sec. 5.4.2	Generic	
2.	ackIDs are always issued sequentially (exception when a retry or error causes the device to back up)	Part 6, Sec. 5.4.2 Part 6, Sec. 5.6	Generic	
3.	Start with ackID=0 after reset	Part 6, Sec. 5.4.2	Generic	
4.	The 2 physical layer reserved bits are set to logic 0s when a request or response packet is created.	Part 6, Sec. 2.3	Generic	
5.	A response packet for a request packet can never be transmitted before the acknowledge control symbol for the request packet	Part 6, Sec. 5.2	Generic	
6.	Embedded CRC properly inserted	Part 6, Sec. 2.4.1	Generic	
	• **6A. DETAIL:** Don't insert embedded CRC if packet is 80 bytes or less.		Generic	
	• **6B. DETAIL:** Insert embedded CRC if packet is 81 bytes or more		Generic	
7.	Packets that are not aligned to the 32-bit boundary are padded into alignment with 16 bits of logic 0	Part 6, Sec. 2.4.1	Generic	
	• **7A. DETAIL:** Pad data is inserted after the final CRC code for the packet.	Part 6, Sec 2.4.1	Generic	
8.	Packet CRC values are correctly calculated	Part 6, Sec. 2.4.2	Generic	
	• **8A. DETAIL:** the final CRC value is the continuation of the embedded CRC and embedded CRC is included in the running calculation (applicable only for packets greater than 80 bytes)	Part 6, Sec. 2.4.1	Generic	
	• **8B. DETAIL:** CRC values are computed according to the polynomial specified in Part 6, Section 2.4.2.	Part 6, Sec. 2.4.2	Generic	
	• **8C. DETAIL:** Incorrect values in Physical Layer header fields (AckID, bit 0 of rsvd) do not result in CRC errors being detected.	Part 6, Sec 2.4	Generic	
9.	Switch devices shall not allow data to be corrupted internal to the device without detection.	Part 6, Sec. 5.6	Generic	
10.	Packets are completed normally with a new packet (starting SOP control symbol) or EOP control symbol	Part 6, Sec. 5.4.1.2	Generic	
11.	Packets are canceled using stomp, restart-from-retry, or link-request control symbols	Part 6, Sec. 5.4.1.2 Part 6, Sec. 3.5.2 Part 6, Sec. 3.5.4 Part 6, Sec. 3.5.5	Generic	

Table 3-8. General device 1x/4x LP-Serial physical layer packet transmission list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	Device receiving packet-retry control symbol follows the defined retry behavior. Further discussion of this point can be found in Part 6, Sec. A.2.2.	Part 1, Sec. 2.32.2 Part 6, Sec. 5.7.2.2	Generic	
	• **12A. DETAIL:** Change the "Output Retry-stopped" bit to 1 in the Port n Error and Status CSR when a packet-retry control symbol is received. Further discussion of this point can be found in Part 6, Sec. A.2.2.		Generic	
	• **12B. DETAIL:** Complete transmission of current packet if applicable, don't transmit new packets. Further discussion of this point can be found in Part 6, Sec. A.2.2.		Generic	
	• **12C. DETAIL:** Send a restart-from-retry control symbol to the receiving device. Further discussion of this point can be found in Part 6, Sec. A.2.2.		Generic	
	• **12D. DETAIL:** Change the "Output Retry-stopped" bit to 0 in the Port n Error and Status CSR when the output port internal retry recovery procedure is complete. Further discussion of this point can be found in Part 6, Sec. A.2.2.		Generic	
	• **12E. DETAIL:** Begin re-transmitting packets from the returned expected ackID value. Further discussion of this point can be found in Part 6, Sec. A.2.2.		Generic	
	• **12F. DETAIL:** Retried packet must eventually be re-transmitted	Part 6, Sec. 3.4.2 Part 6, Sec. 5.7.1	Generic	
13.	Control symbols are inserted only a multiple of 4 character boundary within a packet.	Part 6, Sec. 5.3.3	Generic	
14.	/PD/ character is used to delimit a control symbol which contains packet delimiter, /SC/ is used for other control symbols	Part 6, Sec. 4.5.7.1 Part 6, Sec. 4.5.7.2 Part 6, Sec. 5.3.1	Generic	
	• **14A DETAIL**: Restart-from-retry and link-request may only be packet delimiters if a packet is in progress.	Part 6, Sec. 3.5.4 Part 6, Sec. 3.5.5	Generic	
15.	Stype1 control symbols are transmitted using the correct format and encodings, as per Part 6 Table 3-6.	Part 6, Sec. 3.5	Generic	

3.9 Packet reception compliance list

This is the list for the device receiving a packet or control symbol.

Table 3-9. General device 1x/4x LP-Serial physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ackIDs are only accepted sequentially	Part 6, Sec. 5.6	Generic	Inter-op
2.	Start with ackID=0 after reset	Part 6, Sec. 5.4.2	Generic	Inter-op
3.	Every packet causes an acknowledge control symbol with the corresponding ackID field	Part 6, Sec. 5.6	Generic	Inter-op
4.	Device sends Stype0 control symbols with correct parameter0 and parameter1 values	Part 6, Sec. 3.4	Generic	Inter-op
	• **4A. DETAIL:** Packet Accepted control symbols contain the AckID of the packet being accepted as parameter 0, and the buf_status as parameter 1. Buf_status is encoded as per the definition in Part 6, Table 3-3.	Part 6, Sec. 3.4.1	Generic	Inter-op
	• **4B. DETAIL:** Packet Retry control symbols contain the AckID of the packet being retried as parameter 0, and the buf_status as parameter 1. Buf_status is encoded as per the definition in Part 6, Table 3-3.	Part 6, Sec. 3.4.2	Generic	Inter-op
	• **4C. DETAIL:** Packet-Not-Accepted control symbols contain an undefined value as parameter 0. The cause for not accepting the packet is contained in parameter 1. Cause is encoded as per the definition in Part 6, Table 3-4. Buf_status is encoded as per the definition in Part 6, Table 3-3.	Part 6, Sec. 3.4.3	Generic	Inter-op
	• **4D. DETAIL:** Status control symbols contain the ackID of the next expected packet as parameter 0, and the buf_status as parameter 1. Buf_status is encoded as per the definition in Part 6, Table 3-3.	Part 6, Sec 3.4.4	Generic	
	• **4E. DETAIL:** Link Response symbols contain the ackID of the next expected packet as parameter 0, and the port status as parameter 1. Port Status is encoded as per the definition in Part 6, Table 3-5.	Part 6, Sec 3.4.5	Generic	Inter-op
	• **4F. DETAIL:** Successful reception of 32 packets results in linear progression though all possible ackID_status/packet_ackID values. ackID_status after receipt of packet n is n+1.	Part 6, Sec. 5.4.2 Part 6, Sec. 5.6	Generic	Inter-op
5.	Device must send acknowledge control symbols in same order as packets are received (ackIDs are issued sequentially)	Part 6, Sec. 5.6	Generic	
6.	Device must not send a packet-accepted control symbol before the entire packet has been received and is error free (if error checking is enabled)	Part 6, Sec. 3.4.1	Generic	
7.	Physical layer reserved bits do not affect operation of the device.	Part 6, Sec. 2.4	Generic	Inter-op
8.	Packets are considered completed normally by the receiver if they are completed with a new packet (starting SOP control symbol) or EOP control symbol.	Part 6, Sec. 5.4.1.2	Generic	Inter-op

Table 3-9. General device 1x/4x LP-Serial physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
9.	Device can accept embedded control symbols with any combination of the encodings of stype1 and stype0 captured in items 9A through 9G below.	Part 6, Sec. 5.3.3	Generic	Inter-op
	• **9A. DETAIL:** STYPE1 - Multicast-event control symbol		Generic	Inter-op
	• **9B. DETAIL:** STYPE 1 - NOP control symbol		Generic	Inter-op
	• **9C. DETAIL:** STYPE 0 - Packet-accepted control symbol		Generic	Inter-op
	• **9D. DETAIL:** STYPE 0 - Packet-retry control symbol		Generic	Inter-op
	• **9E. DETAIL:** STYPE 0 - Packet-not-accepted control symbol		Generic	Inter-op
	• **9F. DETAIL:** STYPE 0 - Status control symbol		Generic	Inter-op
	• **9G. DETAIL:** STYPE 0 - Link-response control symbol		Generic	Inter-op
	• **9H. DETAIL:** All embedded control symbols must begin on a 4-character boundary of the packet.		Generic	Inter-op
10.	Packets can be canceled using stomp, restart-from-retry, or link-request control symbols	Part 6, Sec. 5.8	Generic	Inter-op
	• **10A. DETAIL**: Device sends packet-retry control symbol for canceled packet, except when either the “Input Retry-stopped” or “Input Error-stopped” bits are set in the Port n Error and Status CSR.	Part 6, Sec. 5.8	Generic	Inter-op
	• **10B. DETAIL:** Cancellation of a packet during transmission/reception of the packet shall not result in any errors. Note: Cancellation by unexpected Restart-from-Retry results in input error recovery. This should not result in the detection of any other errors	Part 6, Sec. 5.8	Generic	
	• **10C. DETAIL**: Reception of valid packets after a packet has been cancelled, but before the Input Retry-Stopped Recovery Process has been completed, shall not result in any errors.	Part 6, Sec. 5.8	Generic	Inter-op

Table 3-9. General device 1x/4x LP-Serial physical layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
11.	Device encountering a packet retry situation follows the defined retry behavior. Further discussion of this point can be found in Part 6, Sec. A.2.1.	Part 6, Sec. 5.7.2.1	Generic	Inter-op
	• **11A. DETAIL:** Packet retry situation is an internal hazard or a packet is cancelled when the "Port OK" bit is set in the Port n Error and Status CSR, with the following exception. If the packet was canceled with a link-request/input-status control symbol or Restart-From-Retry control symbol, this is not a packet retry situation.		Generic	Inter-op
	• **11B. DETAIL:** Change the "Input Retry-stopped" bit to 1 in the Port n Error and Status CSR when a packet retry situation has been detected. If packet has been canceled with unexpected restart-from-retry (i.e. input port received restart-from-retry canceling the packet while the "Port OK" bit is set to 1 in the Port n Error and Status CSR), also trigger output error recovery.		Generic	Inter-op
	• **11C. DETAIL:** Send a packet-retry control symbol with the expected ackID value		Generic	Inter-op
	• **11D. DETAIL:** Device silently discards packets when the "Input Retry-stopped" bit is set in the Port n Error and Status CSR.		Generic	Inter-op
	• **11E. DETAIL:** Device must detect control symbol errors when the "Input Retry-stopped" bit is set in the Port n Error and Status CSR.		Generic	Inter-op
	• **11F. DETAIL:** Change the "Input Retry-stopped" bit to 0 in the Port n Error and Status CSR when a restart-from-retry or a restart-from-error (link-request/input-status) control symbol is received		Generic	Inter-op
12.	An end point processing element port shall accept an error-free packet of priority N if the port has enough space for the packet in the input buffer space of the port allocated for packets of priority N.	Part 1, Sec. 2.3.3 Part 6, Sec. 5.10	Generic	Inter-op
	• **12A. DETAIL:** An error free packet of priority N is rejected if insufficient buffer space exists. The receiving port sets the 'Input Retry-stopped' bit to 1 in the Port n Error and Status CSR.	Part 6, Sec. 5.7.1	Generic	Inter-op
13.	Accepting an input packet of a priority cannot be contingent on successfully transmitting a packet of a less than or equal priority from any of its ports.	Part 1, Sec. 2.3.3 Part 6, Sec. 5.10	Generic	Inter-op
14.	A generated packet-not-accepted control symbol uses a defined cause field encoding	Part 6, Sec. 3.4.3	Generic	
	• **14A. DETAIL:** "General error"(0b11111) cause is used to indicate any input error situations.	Part 6, Sec. 3.4.3 Part 6, Sec. 5.11.2.4	Generic	
15.	A RapidIO device will accept packets of length up to 276 bytes.	Part 6, Sec. 2.5	Generic	Inter-op

3.10 Switch device specific compliance list

This list contains specific requirements for switch devices only.

Table 3-10. General device 1x/4x LP-Serial physical layer switch device specific list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device is compliant to packet delivery ordering rules.	Part 6, Sec. 5.9	Generic	Inter-op
	• **1A. DETAIL:** A switch shall not alter the priority of a packet.		Generic	
	• **1B. DETAIL:** Packet forwarding decisions made by a switch processing element shall provide a consistent output port selection which is based solely on the value of the destinationID field carried in the packet.		Generic	
	• **1C. DETAIL:** A switch processing element shall not change the order of packets comprising a transaction request flow (packets with the same sourceID, the same destinationID, the same priority, the same CRF value (if supported), and ftype != 8) as the packets pass through the switch.		Generic	
	• **1D. DETAIL:** A switch processing element shall not allow lower priority non-maintenance packets (ftype != 8) to pass higher priority non-maintenance packets with the same sourceID and destinationID as the packets pass through the switch.		Generic	
	• **1E. DETAIL:** A switch processing element shall not allow a priority N maintenance packet (ftype = 8) to pass another maintenance packet of priority N or greater that takes the same path through the switch (same switch input port and same switch output port) and has the same CRF value, if supported.		Generic	
2.	Device is compliant to deadlock prevention rules.	Part 6, Sec. 5.10	Generic	
	• **2A. DETAIL:** A RapidIO fabric shall be dependency cycle free for all operations that do not require a response.		Generic	
	• **2B. DETAIL:** A switch processing element port shall accept an error-free packet of priority N if there is no packet of priority greater than or equal to N that was previously received by the port and is still waiting in the switch to be forwarded.		Generic	
	• **2C. DETAIL:** A switch processing element port that transmits a priority N packet that is forced to retry by the connected device shall select a packet of priority greater than N, if one is available, for transmission.		Generic	

Table 3-10. General device 1x/4x LP-Serial physical layer switch device specific list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	Switch device provides Multicast-event processing	Part 6, Sec. 5.3.4	Generic	
	• **3A. DETAIL:** When a switch processing element receives a Multicast-Event control symbol, the switch shall forward the Multicast-Event by issuing a Multicast-Event control symbol from each port that is designated in the port's CSR as a Multicast-Event output port. The maximum value of Multicast-Event forwarding delay and delay variation shall be defined in switch device specification.		Generic	
	• **3B. DETAIL:** A switch port shall never forward a Multicast-Event control symbol back to the device from which it received a Multicast-Event control symbol regardless of whether the port is designated a Multicast-Event output or not.		Generic	
	• **3C. DETAIL:** In the event that two or more Multicast-Event control symbols are received by a switch processing element close enough in time that more than one is present in the switch at the same time, at least one of the Multicast-Event control symbols shall be forwarded. The others may be forwarded or discarded (device dependent).		Generic	

3.11 Flow control compliance list

This list defines RapidIO 1x/4x LP-Serial link level flow control.

Table 3-11. General device 1x/4x LP-Serial physical layer flow control list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device supports receiver-controlled flow control.	Part 6, Sec. 5.7.1	Generic	Inter-op
	• **1A. DETAIL:** Device sends buf_status=0x1F in all appropriate control symbols (packet-accepted, packet-retry, status).		Generic	Inter-op
2.	Device supports transmitter-controlled flow control.	Part 6, Sec. 5.7.2	Generic	
	• **2A. DETAIL:** Device supports flow control mode negotiation procedure.	Part 6, Sec. 5.7.3	Generic	
	• **2A1. DETAIL:** If device supports transmitter-controlled flow control and detects that its link partner also supports transmitter-controlled flow control, it shall use transmitter-controlled flow control. Otherwise, it shall use receiver-controlled flow control.		Generic	
	• **2B. DETAIL:** Device sends the number of maximum length packet buffers currently available for packet reception (or 0x1E in case this number is greater than 0x1E) in buf_status field in appropriate control symbols (packet-accepted, packet-retry, status). A port may report a smaller number of buffers than it actually has available, but it shall not report a greater number.	Part 6, Sec. 5.7.2	Generic	
3.	When using transmitter-controlled flow control, a packet for which the receiver has indicated that it has buffers is never retried for reason of lack of resources in accordance with buffer prioritization rules.	Part 6, Sec. 5.7.2	Generic	
4.	Device shall send a control symbol containing the buf_status field to its link partner at least once every 1024 code groups after an 1x/4x LP-Serial link is initialized.	Part 6, Sec. 5.7.2 Part 6, Sec. 5.3.2	Generic	

3.12 Recoverable errors compliance list

Recoverable errors are typically transmission errors or physical layer protocol violation errors and the recovery algorithm can be used to maintain communications on the link without losing any data. A compliant device must recover from a single error. Recovery from an error during the recovery from a prior error is application specific. Error detection can only be accomplished by the receiver of a packet or control symbol, never the sender.

Table 3-12. General device 1x/4x LP-Serial physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device detects the link Input errors	Part 6, Sec. 5.11.2	Generic	Inter-op
	• **1A. DETAIL:** invalid code-group	Part 6, Sec. 5.11.2.2 Part 6, Sec. 5.10.2.3.2 Part 6, Sec. 5.11.2.4	Generic	
	• **1B. DETAIL:** valid but illegal character (non-data character inside packet or control symbol, or any valid character other than A, K, or R in an idle sequence)	Part 6, Sec. 5.11.2.2 Part 6, Sec. 5.10.2.3.2 Part 6, Sec. 5.11.2.4	Generic	
	• **1C. DETAIL:** Incorrect CRC for a packet	Part 6, Sec. 2.4	Generic	
	• **1C1. DETAIL:** CRC is checked against the polynomial specified in Part 6, Sec. 2.3.2		Generic	
	• **1C2. DETAIL:** CRC errors are detected at the 80 byte embedded CRC.		Generic	
	• **1C3. DETAIL:** Corruption of the ackID field or the most significant bit in the rsvd field, both resident in the first 16 bits of the packet header, shall not result in a CRC error being detected.		Generic	
	• **1C4. DETAIL:** For purposes of computing the CRC value, the ackID field and the most significant bit in the rsvd field, both resident in the first 16 bits of the packet header, shall be treated as logic 0s.		Generic	
	• **1D. DETAIL:** Unexpected ackID value in a packet	Part 6, Sec. 5.11.2.4	Generic	
	• **1D1. DETAIL:** Device shall detect unexpected ackID error for a canceled packet (i.e. enter input error recovery instead of input retry recovery). Further discussion of this point can be found in Part 6, Sec. A.	Part 6, Sec. 5.11.2.4	Generic	
	• **1E. DETAIL:** Device shall detect reception of a packet greater than 276 bytes in length.	Part 6, Sec. 5.11.2.4	Generic	
	• **1F. DETAIL:** Incorrect CRC for a control symbol	Part 6, Sec. 5.11.2.3.2	Generic	
2.	Device encounters link Input errors as defined in point 1 above.	Part 6, Sec. 5.11.2	Generic	
	• **2A. DETAIL:** Change the “Input Error-stopped” bit to 1 in the Port n Error and Status CSR. Further discussion of this point can be found in Part 6, Sec. A.3.1.	Part 6, Sec. 5.11.2.6	Generic	

Table 3-12. General device 1x/4x LP-Serial physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	If the Re-transmit Suppression Support bit is set (bit 25 of the Processing Elements Features CAR), suppression of error recovery on packet CRC errors is supported.	Part 6, Sec. 5.11.2.4 Part 6, Sec. 6.4.1 Part 6, Sec. 6.5.2.6 Part 6, Sec. 6.5.2.6 Part 6, Sec. 6.5.2.6 Part 6, Sec. 6.5.2.6	Generic	
	• **3A. DETAIL:** The Re-transmit Suppression Mask field is only valid if bit 25 of the Processing Elements Features CAR is set. Otherwise, this field acts as reserved bits.		Generic	
	• **3B. DETAIL:** Error recovery suppression is disabled if the entire Re-transmit Suppression Mask field is set to 0.		Generic	
	• **3C. DETAIL:** Packets of a specific flow may have their re-transmission suppressed if the corresponding bit of the Re-transmit Suppression Mask is set in the Port n Control CSR, as defined in the version 1.3 RapidIO specification.		Generic	
4.	When the “Input Error-stopped” bit is set in the Port n Error and Status CSR, the port must follow the input error-recovery procedure. Further discussion of this point can be found in Part 6, Sec. A.3.1.	Part 6, Sec. 5.11.2.6	Generic	
	• **4A. DETAIL:** Send a packet-not-accepted control symbol to the sending device		Generic	
	• **4B. DETAIL:** Device silently discards all packets until a restart-from-error (link-request/input-status) control symbol is encountered		Generic	
	• **4C. DETAIL:** Change the “Input Error-stopped” bit to 0 in the Port n Error and Status CSR.		Generic	
5.	Device detects Output link errors	Part 6, Sec. 5.11.2 Part 6, Sec. 5.6	Generic	
	• **5A. DETAIL:** Received “packet-not-accepted” control symbol	Part 6, Sec. 5.11.2 Part 6, Sec. 5.6	Generic	
	• **5B. DETAIL:** Acknowledge control symbol time-out		Generic	
	• **5C. DETAIL:** Any acknowledge control symbol with an unexpected ackID value		Generic	
	• **5D. DETAIL:** Unexpected Retry Control Symbol		Generic	
6.	Device encounters Output link errors as defined in point 5 above. Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.7	Generic	
	• **6A. DETAIL:** Change the “Output Error-stopped” bit to 1 in the Port n Error and Status CSR.		Generic	

Table 3-12. General device 1x/4x LP-Serial physical layer recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
7.	While the "Output Error-stopped" bit is set in the Port n Error and Status CSR, the device must follow the output error-recovery procedure. Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.7	Generic	
	• **7A.DETAIL:** Device stops transmitting new packets		Generic	
	• **7B. DETAIL:** Device sends link-request/input-status (restart-from-error) control symbol if no link-request control symbol is already outstanding (must wait for previous one to complete) and waits for link-response control symbol		Generic	
	• **7C. DETAIL:** Change the "Output Error-stopped" bit to 0 in the Port n Error and Status CSR.		Generic	
	• **7D. DETAIL:** Start re-transmitting at the ackID value returned with the received link-response control symbol		Generic	
8.	When the 'Port OK' bit is set in the Port n Error and Status CSR, the device detects protocol violations	Part 6, Sec. 5.11.2.3.1	Generic	
	• **8A. DETAIL:** Any acknowledge control symbol with an unexpected ackID value		Generic	
	• **8B. DETAIL:** Unsolicited (unexpected) acknowledge control symbol		Generic	
	• **8C. DETAIL:** Received link-request control symbol before sending link-response control symbol for previous link-response/input-status control symbol		Generic	
	• **8D. DETAIL:** Unexpected link-response control symbol		Generic	
	• **8E. DETAIL:** Unexpected restart-from-retry control symbol		Generic	
	• **8F DETAIL:** Unexpected stomp control symbol		Generic	
	• **8G. DETAIL:** Unexpected eop control symbol		Generic	
9.	Device encounters a protocol violation as defined in item 8 above. Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.3.1 Part 6, Sec. 5.11.2.7	Generic	
	• **9A. DETAIL:** Change the "Output Error-stopped" bit to 1 or/and "Input Error-stopped" bit to 1 in the Port n Error and Status CSR.		Generic	
10.	Any transmission error encountered during error recovery. Note: Some transmission errors cause subsequent protocol violations. The recovery algorithm can be used to recover from multiple transmission errors but that behavior is not required for compliance.	Part 6, Sec. 5.11.2	Generic	

3.13 Non-recoverable errors compliance list

There is a number of non-recoverable errors at the physical layer. Behavior of the interface is not defined for these events.

Table 3-13. General device 1x/4x LP-Serial physical layer non-recoverable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Device does not respond to the initialization sequence. No response time is specified. A reasonable test procedure should be followed to demonstrate this behavior.	Part 6, Sec. 4.7	Generic	
2.	Device is attempting error recovery and ackID received in link-response control symbol does not make sense (device cannot complete recovery). Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.3.1	Generic	
3.	Link-request control symbol to link-response control symbol time-out. Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 6.5.2.2 Part 6, Sec. 6.6.2.2 Part 6, Sec. 6.7.2.2 Part 6, Sec. 6.8.2.2	Generic	
4.	Any transmission error encountered during error recovery. Note: Some transmission errors cause subsequent protocol violations. The recovery algorithm can be used to recover from multiple transmission errors but that behavior is not required for compliance.	Table 3-12 above	Generic	

3.14 State machines interaction compliance list

There are some rules of output error, input error, output retry, input retry state machine interactions.

Table 3-14. General device 1x/4x LP-Serial physical layer state machines interaction list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	If an input error situation was detected while the 'Input Retry-stopped' bit is 1 in the Port n Error and Status CSR, the device shall change the 'Input Retry-stopped' bit to 0 and change the 'Input Error-stopped' bit to 1 in the Port n Error and Status CSR. The input retry recovery procedure stops, and the input error recovery will be followed. Further discussion of this point can be found in Part 6, Sec. A.2.1 and Part 6, Sec. A.3.1.	Part 6, Sec. 5.11.2.6 Part 6, Sec. 5.11.2.7	Generic	
2.	If an output error situation was detected while the 'Output Retry-stopped' bit is 1 in the Port n Error and Status CSR, the device shall change the 'Output Retry-stopped' bit to 0 and change the 'Output Error-stopped' bit to 1 in the Port n Error and Status CSR. The output retry recover procedure stops, and the output error recovery procedure will be followed. Further discussion of this point can be found in Part 6, Sec. A.2.2 and Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.6 Part 6, Sec. 5.11.2.7	Generic	
3.	Input state machines and output state machines shall work independently from each other. Further discussion of this point can be found in Part 6, Sec. A.	Part 6, Sec. 5.11.2.6 Part 6, Sec. 5.11.2.7	Generic	
	• **3A. DETAIL:** If the 'Input Retry-Stopped' or 'Input Error-Stopped' bits are set in the Port n Error and Status CSR, the device shall follow input retry/error recovery even if the condition causing the two previously mentioned bits to be changed to 1 was detected while the device was performing the output retry/error procedure.		Generic	
	• **3B. DETAIL:** If the 'Output Retry-Stopped' or 'Output Error-Stopped' bits are set in the Port n Error and Status CSR, the device shall follow output retry/error recovery even if the condition causing the two previously mentioned bits to be changed to 1 was detected while the device was performing input retry/error procedure.		Generic	
	• **3C. DETAIL:** If an input retry/error situation and an output retry/error situation were detected simultaneously, the device shall start both input and output recovery procedures.		Generic	
4.	If device is following input error recovery, all subsequent input port errors shall not affect operation of the device. Further discussion of this point can be found in Part 6, Sec. A.3.1.	Part 6, Sec. 5.11.2.6 Part 6, Sec. 5.11.2.7	Generic	
5.	If device is following output error recovery, all subsequent output port errors shall not affect operation of the device. Further discussion of this point can be found in Part 6, Sec. A.3.2.	Part 6, Sec. 5.11.2.6 Part 6, Sec. 5.11.2.7	Generic	

3.15 Retimer and repeater compliance list

This is a list for retimer and repeater devices.

Table 3-15. General device 1x/4x LP-Serial physical layer retimer and repeater device specific list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-operability Item
1.	Up to two retimers are allowed between 2 end nodes	Part 6, Sec. 4.6.1	Generic	Inter-op
2.	A retimer may insert up to one /R/ code-group immediately following a /K/ code-group sequence, or remove one /R/ code-group that immediately follows a /K/ code-group sequence.		Generic	Inter-op
3.	A retimer may retime links operating at the same width only (i.e. cannot connect a link operating at 1x to a link operating at 4x).		Generic	Inter-op
4.	Repeaters do not interpret or alter the bit stream in any way.	Part 6, Sec. 4.6.2	Generic	

3.16 Sequence generation compliance list

This is the list for idle and compensation sequences and status symbol generation functionality.

Table 3-16. General device 1x/4x LP-Serial physical layer sequence generation list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	At least once per 5000 code-groups a port operating in 1x mode (4x mode) shall transmit a compensation sequence of /K/R/R/R/ codegroup sequence (||K||R||R||R|| column sequence). The compensation sequence shall be transmitted with this rate even when there are packets or control symbols available to transmit to allow clock rate compensation.	Part 6, Sec. 4.5.9	Generic	Inter-op
2.	The idle sequence shall be transmitted continuously over each lane whenever neither packets nor control symbols are being transmitted.		Generic	Inter-op
3.	Idle sequence may not be inserted in a packet or delimited control symbol.		Generic	Inter-op
	• **3A. DETAIL:** No more than 5000 code-groups should be transmitted between compensation sequences.		Generic	Inter-op
4.	The idle sequence shall be transmitted over each lane as part of the port initialization process.	Part 6, Sec. 4.7.3.5 Part 6, Sec. 4.7.3.6	Generic	Inter-op

Table 3-16. General device 1x/4x LP-Serial physical layer sequence generation list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
5.	The 1x idle sequence shall consist of a sequence of the code-groups /K/, /A/, /R/ and shall be used by ports operating in 1x mode. The 4x idle sequence shall consist of a sequence of the columns ||K||, ||A||, ||R|| and shall be used by ports operating in 4x mode.	Part 6, Sec. 4.5.9 Part 6, Sec. 4.5.7.4 Part 6, Sec. 4.5.7.6	Generic	Inter-op
	• **5A. DETAIL:** The /K/ code-group provides the receiver with the information it requires to achieve and maintain bit and 10-bit code-group boundary synchronization.		Generic	
	• **5B. DETAIL:** The ||A|| columns are used for lane alignment on 4x links.		Generic	
6.	The idle sequence shall comply with the following rules:		Generic	Inter-op
	• **6A. DETAIL:** The first code-group (column) of an idle sequence generated by a port operating in 1x mode (4x mode) shall be /K/ (||K||). The first code-group (column) shall be transmitted immediately following the last code-group (column) of a packet or delimited control symbol.		Generic	Inter-op
	• **6B. DETAIL:** When not transmitting the compensation sequence, all code-groups (columns) following the first code-group (column) of an idle sequence generated by a port operating in 1x mode (4x mode) shall be a pseudo-randomly selected sequence of /A/, /K/, and /R/ (||A||, ||K||, and ||R||) based on a pseudo-random sequence generator of 7th order or greater. The number of non /A/ code-groups (non ||A|| columns) between /A/ code-groups (||A|| columns) in the idle sequence of a port operating in 1x mode (4x mode) shall be not less than 16 and no more than 32. The number of code groups shall be pseudo-randomly selected based on a pseudo-random sequence generator of 7th order or greater.		Generic	

Chapter 4 Common Transport Layer Checklists

4.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for devices supporting common transport functionality for 8/16 LP-LVDS and 1x/4x LP-Serial compliant devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The Common Transport layer inter-operability and certification checklist is broken down into a number of sub-lists.

4.2 Generic functionality compliance list

This is the list for generic functionality for the device.

Table 4-1. General device common transport layer generic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Items 1 through 20 of Table 2-1, “General device 8/16 LP-LVDS physical layer general compliance list,” on page 12. Applied to Transport Layer fields, CARs and CSRs.	Chapter 2, Table 2-1	Generic	Inter-op
2.	All necessary CSRs (command and status registers) exist and can be read	Part 3, Sec. 3.5	Generic	Inter-op
	• **2A. DETAIL:** Base Device ID CSR; reset value is application and implementation dependant (end point devices only)	Part 3, Sec. 3.5.1	Generic	
	• **2B. DETAIL:** Host Base Device ID Lock CSR; Host_base_deviceID field reset value is 0xFFFF	Part 3, Sec. 3.5.2	Generic	Inter-op
	• **2C. DETAIL:** Component Tag CSR; reset value is 0x00000000	Part 3, Sec. 3.5.3	Generic	Inter-op
	• **2D. DETAIL:** Standard Route Configuration Destination ID Select CSR; reset values of the following fields are all 0: Ext_config_en, Config_destID_msb, and Config_destID	Part 3, Sec. 3.5.4	Generic	Inter-op
	• **2E. DETAIL:** Standard Route Configuration Port Select CSR; reset values are defined as follows:	Part 3, Sec. 3.5.5	Generic	Inter-op
	• **2E1. DETAIL:** Reset value of Config_output_port is implementation defined.		Generic	Inter-op
	• **2E2. DETAIL:** Reset values of Config_output_port1, Config_output_port2, and Config_output_port3 are 0x00. However, if the extended route table mechanism is not enabled, these fields are these fields are reserved (still a reset value of 0x00).		Generic	Inter-op
	• **2F. DETAIL:** Standard Route Default Port CSR; Default_output_port field reset value is 0x00	Part 3, Sec. 3.5.6	Generic	Inter-op
	• **2G. DETAIL:** Processing Element Features CAR, bit 27 accurately reflects device’s ability to support common transport large systems.	Part 3, Sec 2.3.1	Generic	Inter-op
	• **2H. DETAIL:** Processing Element Features CAR, bit 23 accurately reflects device’s ability to support the standard route table mechanism.	Part 3, Sec 3.4.1	Generic	Inter-op
	• **2I. DETAIL:** Processing Element Features CAR, bit 22 accurately reflects device’s ability to support the extended route table mechanism.	Part 3, Sec 3.4.1	Generic	Inter-op
	• **2J. DETAIL:** Switch Route Table Destination ID Limit CAR, bits 16-31 accurately reflects the device’s maximum configurable destination ID value.	Part 3, Sec 3.4.2	Generic	Inter-op

Table 4-1. General device common transport layer generic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
3.	Writable CSR fields can be written	Part 3, Sec. 3.5	Generic	Inter-op
	• **3A. DETAIL:** Host Base Device ID CSR Host_base_deviceID field reset value is 0xFFFF	Part 3, Sec 3.5.2	Generic	Inter-op
	• **3B. DETAIL:** When Host Base Device ID CSR Host_base_deviceID field value is 0xFFFF, the field value can be changed to any value.	Part 3, Sec 3.5.2	Generic	Inter-op
	• **3C. DETAIL:** When Host Base Device ID CSR Host_base_deviceID field value is not 0xFFFF, the field value will change to 0xFFFF when a value equal to the current field value is written.	Part 3, Sec 3.5.2	Generic	Inter-op
	• **3D. DETAIL:** When Host Base Device ID CSR Host_base_deviceID field value is not 0xFFFF, the field value does not change when a value not equal to the current field value is written.	Part 3, Sec 3.5.2	Generic	Inter-op
	• **3E. DETAIL:** When the Host Base Device ID CSR Host_base_deviceID field value is equal to 0xFFFF, and 0xFFFF is written to the field, subsequent writes of values not equal to 0xFFFF behave as per 3B, 3C and 3D above.	Part 3, Sec 3.5.2	Generic	Inter-op
	• **3F. DETAIL:** The Component Tag CSR component_tag field can be written to any value.	Part 3, Sec 3.5.3	Generic	Inter-op
	• **3G. DETAIL:** The Standard Route Configuration Destination ID Select CSR fields are writable when this function is supported by the implementation. Otherwise, this register acts as a reserved register and cannot be written.	Part 3, Sec 3.5.4	Generic	Inter-op
	• **3H. DETAIL:** The Standard Route Configuration Port Select CSR fields are writable when this function is supported by the implementation. Otherwise, this register acts as a reserved register and cannot be written.	Part 3, Sec 3.5.5	Generic	Inter-op
	• **3I. DETAIL:** The Standard Route Default Port CSR Default_output_port field can be written to any value when this function is supported by the implementation. Otherwise, this register acts as a reserved register and cannot be written.	Part 3, Sec 3.5.6	Generic	Inter-op

Table 4-1. General device common transport layer generic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	Standard and extended route table configuration mechanisms function as described.	Part 3, Sec. 3.5.4 Part 3, Sec. 3.5.5	Generic	Inter-op
	• **4A. DETAIL:** When read, the Standard Route Configuration Port Select CSR returns the switch output port configurations when this function is supported by the implementation. Otherwise, this register acts as a reserved register and returns all 0's.	Part 3, Sec 3.5.5	Generic	Inter-op
	• **4B. DETAIL:** When written, the Standard Route Configuration Port Select CSR updates the switch output port configurations when this function is supported by the implementation. Otherwise, this register acts as a reserved register and returns all 0's.	Part 3, Sec 3.5.5	Generic	Inter-op
	• **4C. DETAIL:** Ext_config_en bit enables/disables extended configuration support when this function is supported by the implementation. Otherwise, this register acts as a reserved register and returns all 0's.	Part 3, Sec 3.5.4	Generic	Inter-op

4.3 Packet transmission compliance list

This is the list for the device transmitting a packet (a slave device is required to generate response packets).

Table 4-2. General device common transport layer packet transmission list

Item no.	Compliance item	Specification reference	Comment	Inter-op Item
1.	tt field matches the size of the destID/sourceID fields. Certification requires small (8-bit) device ID fields; 16-bit device ID support optional.	Part 3, Sec. 2.4	Generic	Inter-op
	• **1A. DETAIL:** tt field is always 0 if Processing Element Features CAR Common Transport Large System Support field value is 0.	Part 3, sec. 3.4.1 Part 3, sec. 2.4	Generic	Inter-op
2.	small transport type (tt=0) is supported (8-bit device ID fields)	Part 3, Sec. 2.4	Generic	Inter-op
3.	large transport type (tt=1) is supported (16-bit device ID fields)	Part 3, Sec. 2.4	Generic	
4.	tt most significant bit is reserved (always logic 0)	Part 3, Sec. 2.4	Generic	
5.	End point-free switch responds to maintenance requests with the hop_count=0 when received, otherwise decrement hop_count, recompute CRC and route to proper output port	Part 3, Sec. 2.5	Generic	Inter-op
	• **5A. DETAIL:** The response to a maintenance packet has hop_count field set to 0xFF	Part 3, Sec 2.5	Generic	Inter-op
6.	Switches retransmit all packets not destined for them without altering the packet, other than detailed in point 5 above.	Part 3, Sec 2.4	Generic	Inter-op
7.	Response packets are sent with the source and destination ID fields reversed from the corresponding request packet	Part 3, Sec. 2.3	Generic	Inter-op

4.4 Packet reception compliance list

This is the list for the device receiving a packet.

Table 4-3. General device common transport layer packet reception list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	End point-free switch responds to maintenance requests with the hop_count=0 when received	Part 3, Sec. 2.5	Generic	Inter-op

4.5 Detectable errors compliance list

Transport layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 4-4. General device common transport layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Received reserved tt field encoding.	Part 3, Sec. 2.4	Generic	
2.	For switch devices, if the destination ID has no valid output port set.	Part 3, Sec. 2.4	Generic	

Blank Page

Chapter 5 I/O Logical Layer Checklists

5.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for devices supporting I/O logical functionality for 8/16 LP-LVDS and 1x/4x LP-Serial compliant devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The I/O Logical layer inter-operability and certification checklist is broken down into a number of sub-lists.

5.2 Basic functionality compliance list

This is the list for basic functionality for RapidIO devices.

Table 5-1. General device I/O logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Items 1 through 20 of Table 2-1, “General device 8/16 LP-LVDS physical layer general compliance list,” on page 12 and/or items 1 through 20 of Table 3-1, “General device 1x/4x LP-Serial physical layer general compliance list,” on page 42, depending on the physical layer(s) supported by the device. Note that these requirements are applied to the Logical Layer fields of CARs & CSRs.	Chapter 2, Table 2-1 Chapter 3, Table 3-1	Generic	Inter-op
2.	The address field of a packet is a double-word (8 byte) aligned address	Part 1, Sec. 4.1.1	Generic	Inter-op
3.	Multiple double-word data payloads are linear starting at the specified address	Part 1, Sec. 4.1.1	Generic	Inter-op
4.	Multiple double-word data payloads are aligned to a double-word boundary	Part 1, Sec. 4.1.1	Generic	Inter-op
5.	Multiple double-word data payloads must be less than or equal to the transfer size as indicated by the wrsize/rdsize and wdptr fields.	Part 1, Sec. 4.1.1	Generic	
6.	Sub-double-word data payloads have a defined data payload, properly aligned and padded to a double-word boundary	Part 1, Sec. 3.3 Part 1, Sec. 3.4 Part 1, Sec. 4.1.1	Generic	
7.	Response packets have the transaction ID of the associated request packet	Part 1, Chp. 3.1	Generic	Inter-op
8.	Responses that are not expected to have a data payload must not have a data payload	Part 1, Sec. 4.2.3	Generic	
9.	Responses shall not contain a data payload if the response status is “ERROR”	Part 1, Sec. 4.2.3	Generic	

Table 5-1. General device I/O logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
10.	All necessary CARs (capabilities registers) exist and can be read	Part 1, Sec. 5.4	Generic	Inter-op
	• **10A. DETAIL:** Device Identity CAR; bits 0-15: value is implementation dependant • bits 16-31: value is vendor specific as assigned by the RapidIO Trade Association.	Part 1, Sec. 5.4.1	Generic	
	• **10B. DETAIL:** Device Information CAR; value is vendor and implementation dependant	Part 1, Sec. 5.4.2	Generic	
	• **10C. DETAIL:** Assembly Identity CAR; bits 0-15: value is implementation dependant bits 16-31: value is vendor specific as assigned by the RapidIO Trade Association	Part 1, Sec. 5.4.3	Generic	
	• **10D. DETAIL:** Assembly Information CAR; value is vendor and implementation dependant	Part 1, Sec. 5.4.4	Generic	
	• **10E. DETAIL:** Processing Element Features CAR; value is implementation dependant; must indicate support for 34-bit address format packets. Only check 10F is bit 3 is set.	Part 1, Sec. 5.4.5	Generic	
	• **10F. DETAIL:** Switch Port Information CAR; value is implementation dependant (switch devices only)	Part 1, Sec. 5.4.6	Generic	
	• **10G. DETAIL:** Source Operations CAR; value is implementation dependant	Part 1, Sec. 5.4.7	Generic	
	• **10H. DETAIL:** Destination Operations CAR; value is implementation dependant (end point devices only)	Part 1, Sec. 5.4.8	Generic	
11.	All necessary CSRs (command and status registers) exist and can be read	Part 1, Sec. 5.5	Generic	Inter-op
	• **11A. DETAIL:** Processing Element Logical Layer Control CSR: reset value of the Extended addressing control field is 0b001 (end point devices only)	Part 1, Sec. 5.5.1	Generic	
	• **11B: DETAIL:** Local Configuration Space Base Address 0 CSR: value dependant on addressing mode supported. Bit 0 - reserved for all addressing modes. Bits 1-16 reserved for 34-bit and 50-bit addressing modes only. Bit 17-31 reserved for 34-bit addressing mode.	Part 1, Sec. 5.5.2	Generic	
	• **11C: DETAIL:** Local Configuration Space Base Address 1 CSR: value is implementation dependant. Bit0 - reserved for 34 bit addressing mode only.	Part 1, Sec 5.5.3	Generic	
12.	Writable CSR fields can be written	Part 1, Sec. 5.5	Generic	
13.	All registers in the Extended Features data structure are double-word (8 byte) aligned.	Part 1, Sec. 5.3	Generic	
14.	All Extended Features blocks lie completely within the Extended Features Space in the register address map	Part 1, Sec. 5.3	Generic	

Table 5-1. General device I/O logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
15.	Extended Features list is terminated with an Extended Features pointer value of logic 0s	Part 1, Sec. 5.3	Generic	
16.	The response to a maintenance packet has the logical transaction, status, and TID fields and data payload (if applicable) set according to the request.	Part 1, Sec. 4.1.10	Generic	Inter-op

5.3 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 5-2. General device I/O logical layer target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MAINTENANCE read transaction	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	Inter-op
	• **1A. DETAIL:** MAINTENANCE read request size of 4 bytes must be supported	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1B. DETAIL:** MAINTENANCE read request generates a MAINTENANCE read response	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1C. DETAIL:** MAINTENANCE read response payload size matches requested size	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1D. DETAIL:** Response data for a MAINTENANCE packet consists of one or more double words, although sub-double-word data may have been requested.	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
2.	MAINTENANCE write transaction	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	Inter-op
	• **2A. DETAIL:** MAINTENANCE write request size of 4 bytes must be supported	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **2B. DETAIL:** MAINTENANCE write request generates a MAINTENANCE write responses	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **2C. DETAIL:** MAINTENANCE write response does not contain a data payload	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	

5.4 Source transaction support compliance list

General compliance does not require a device to initiate any operations.

5.5 Detectable errors compliance list

I/O logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 5-3. General device I/O logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MAINTENANCE write packet data payload length is not 4B, 8B, or multiple double-word quantity up to 64B.	Part 1, Sec. 4.1.10	Generic	
2.	Received MAINTENANCE read packet has a data payload	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
3.	Received MAINTENANCE write packet has no data payload	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
4.	Received MAINTENANCE packet uses a reserved field encoding for a required field	Part 1, Sec. 4.1.2	Generic	
5.	Received MAINTENANCE packet uses illegal combinations of field encodings, for example a 128 byte data payload.	Part 1, Sec. 4.1.10	Generic	

5.6 Class 1 compliance lists

A Class 1 device must meet all requirements specified in the General device compliance checklists. The only difference between Class 1 compliance and general device compliance is in logical layer transaction support.

5.6.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 5-4. Class 1 device logical layer target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	
	• **1A. DETAIL:** NREAD operations	Part 1, Sec. 5.4.8	Class 1, 2, 3	
	• **1B. DETAIL:** NWRITE operations	Part 1, Sec. 5.4.8	Class 1, 2, 3	
	• **1C. DETAIL:** SWRITE operations	Part 1, Sec. 5.4.8	Class 1, 2, 3	
	• **1D. DETAIL:** NWRITE_R operations	Part 1, Sec. 5.4.8	Class 1, 2, 3	
2.	NREAD transaction	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 1, 2, 3	Inter-op
	• **2A. DETAIL:** NREAD request generates a response packet which always contain data payloads of one or more double-words, although sub-double-word data may have been requested	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 1, 2, 3	
	• **2B. DETAIL:** NREAD response data payload is of the requested size and alignment	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 1, 2, 3	
	• **2C. DETAIL:** Maximum NREAD request can be 256 bytes.	Part 1, Sec. 4.1.2, Table 4-3	Class 1, 2, 3	
3.	NWRITE transaction	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 1, 2, 3	Inter-op
	• **3A. DETAIL:** NWRITE request does not generate a response packet	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 1, 2, 3	
	• **3B. DETAIL:** Maximum NWRITE data payload can be 256 bytes	Part 1, Sec. 4.1.2, Table 4-4	Class 1, 2, 3	
	• **3C. DETAIL:** All NWRITE requests containing a data payload smaller than 8 bytes must be padded to 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.7	Class 1, 2, 3	
	• **3D. DETAIL:** NWRITE request payload is a multiple of 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.7	Class 1, 2, 3	

Table 5-4. Class 1 device logical layer target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	SWRITE transaction	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.8	Class 1, 2, 3	Inter-op
	• **4A. DETAIL:** SWRITE request does not generate a response packet	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.8	Class 1, 2, 3	
	• **4B. DETAIL:** Maximum SWRITE data payload can be 256 bytes	Part 1, Sec. 4.1.2, Table 4-4	Class 1, 2, 3	
	• **4C. DETAIL:** SWRITE request payload is a minimum of 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.8		
	• **4D. DETAIL:** SWRITE request payload is a multiple of 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.8	Class 1, 2, 3	
5.	NWRITE_R transaction	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 1, 2, 3	Inter-op
	• **5A. DETAIL:** NWRITE_R request generates a response packet	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 1, 2, 3	
	• **5B. DETAIL:** Maximum NWRITE_R data payload can be 256 bytes	Part 1, Sec. 4.1.2, Table 4-4	Class 1, 2, 3	
	• **5C. DETAIL:** NWRITE_R response packet has no payload.	Part 1, Sec. 4.1.2, Table 4-4	Class 1, 2, 3	
	• **5D. DETAIL:** All NWRITE_R requests containing a data payload smaller than 8 bytes must be padded to 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.7	Class 1, 2, 3	
	• **5E. DETAIL:** NWRITE_R request payload is a multiple of 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5 Part 1, Sec. 4.1.7	Class 1, 2, 3	
6.	NREAD, NWRITE and SWRITE transactions operate on memory regardless of system wide cache/coherence mechanism.	Part 1, Sec. 3.3.1 Part 1, Sec. 3.3.2	Generic	

5.6.2 Source transaction support compliance list

I/O device class 1 compliance does not require the device to initiate any operations.

5.6.3 Detectable errors compliance list

I/O logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 5-5. Class 1 device logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	NWRITE, SWRITE and NWRITE_R request packet data payload exceeds size specified in wrsize field	Part 1, Sec. 4.1.7 Part 1, Sec. 4.1.8	Class 1, 2, 3	
2.	NWRITE, SWRITE and NWRITE_R request packet data payload exceeds 256 bytes	Part 1, Sec. 4.1.7 Part 1, Sec. 4.1.8	Class 1, 2, 3	
3.	Received read request packet has a data payload	Part 1, Sec. 4.1.5 Part 1, Sec. 4.1.10	Class 1, 2, 3	
4.	Received NWRITE, SWRITE or NWRITE_R request packet has no data payload	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7 Part 1, Sec. 4.1.8	Class 1, 2, 3	
5.	Received request packet uses a reserved field encoding for a required field	Part 1, Sec. 4.1.2	Class 1, 2, 3	
6.	Received request packet uses illegal combinations of field encodings. For example, any ATOMIC transaction of more than 4 bytes.	Part 1, Sec. 4.1.7	Class 1, 2, 3	
7.	Unsupported transaction requested	Part 1, Sec. 5.4.8	Class 1, 2, 3	
8.	Received NWRITE, NWRITE_R, SWRITE request data payload is not padded to a multiple of 8 bytes.	Part 1, Sec. 3.4 Part 1, Sec. 3.5	Class 1, 2, 3	

5.7 Class 2 compliance lists

A Class 2 device must meet all requirements specified in the General device and Class 1 compliance checklists. The only difference between Class 2 compliance and Class 1 compliance is in logical layer transaction support.

5.7.1 Basic functionality compliance list

A class 2 device is the source as well as the target of transactions.

Table 5-6. Class 2 device logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Outstanding transaction IDs are unique for each outstanding request transaction between a particular transaction source and destination pair.	Part 1, Sec. 3.1	Class 2	

5.7.2 Target transaction support compliance list

There are no additional transaction types for the device as a transaction target.

5.7.3 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 5-7. Class 2 device logical layer source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	
	• **1A. DETAIL:** NREAD operations	Part 1, Sec. 5.4.7	Class 2, 3	
	• **1B. DETAIL:** NWRITE operations	Part 1, Sec. 5.4.7	Class 2, 3	
	• **1C. DETAIL:** NWRITE_R operations	Part 1, Sec. 5.4.7	Class 2, 3	
	• **1D. DETAIL:** SWRITE operations	Part 1, Sec. 5.4.7	Class 2, 3	
2.	NREAD transaction	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 2, 3	Inter-op
	• **2A. DETAIL:** NREAD packet never has a data payload	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 2, 3	
	• **2B. DETAIL:** NREAD packet must properly specify the requested size and alignment	Part 1, Sec. 3.3.1 Part 1, Sec. 4.1.5	Class 2, 3	
3.	NWRITE transaction	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 2, 3	Inter-op
	• **3A. DETAIL:** NWRITE packets always contain data payloads of one or more double-words, although sub-double-word data may be specified	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 2, 3	
	• **3B. DETAIL:** NWRITE packet must properly specify the data payload size and alignment	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 2, 3	
	• **3C. DETAIL:** NWRITE packet actual data payload size may be less than the specified size (multiple double-word only)	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.7	Class 2, 3	
4.	NWRITE_R transaction	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	Inter-op
	• **4A. DETAIL:** NWRITE_R packets always contain data payloads of one or more double-words, although sub-double-word data may be specified	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	
	• **4B. DETAIL:** NWRITE_R packet must properly specify the data payload size and alignment	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	
	• **4C. DETAIL:** NWRITE_R packet actual data payload size may be less than the specified size (multiple double-word only)	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	
5.	SWRITE transaction	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.8	Class 2, 3	Inter-op
	• **5A. DETAIL:** SWRITE packets always contain data payloads of one or more double-words	Part 1, Sec. 3.3.2 Part 1, Sec. 4.1.8	Class 2, 3	

5.7.4 Detectable errors compliance list

I/O logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 5-8. Class 2 device logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Received unsolicited response packet	Part 1, Sec. 3.1	Class 2, 3	
2.	NREAD “DONE” response packet data payload is more or less than requested data quantity	Part 1, Sec. 3.3.1	Class 2, 3	
3.	NREAD “DONE” response packet has no data payload	Part 1, Sec. 3.3.1	Class 2, 3	
4.	NREAD “DONE” response packet data payload is not a multiple of 8 bytes.	Part 1, Sec. 3.3.1 Part 1, Sec. 3.4 Part 1, Sec. 3.5	Class 2, 3	
5.	NWRITE_R response has a data payload.	Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	
6.	Response packet time-out	Part 4, Sec. 2.4.3 Part 6, Sec. 5.11.1	Class 2, 3	
7.	Received “ERROR” response status	Part 1, Sec. 3.1	Class 2, 3	
8.	“ERROR” response packet has a data payload	Part 1, Sec. 4.2.3	Class 2, 3	
9.	Received response packet has reserved field encoding	Part 1, Sec. 4.1.2	Class 2, 3	
10.	NWRITE/NWRITE_R packet data size exceeds specified size.	Part 1, Sec. 3.3.2 Part 1, Sec. 3.3.3 Part 1, Sec. 4.1.7	Class 2, 3	

5.8 Class 3 compliance lists

An I/O Class 3 device must meet all requirements specified in the General device and I/O Class 2 compliance checklists. The only difference between I/O Class 3 compliance and I/O Class 2 compliance is in logical layer transaction support.

5.8.1 Basic functionality compliance list

An I/O class 3 device is the source as well as the target of transactions.

Table 5-9. Class 3 device logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Response packets have the letter/mbox/msgseg fields of the associated request packet	Part 2, Sec. 4.2.5	Class 3	
2.	Outstanding letter/mbox/msgseg/xmbox fields are unique for a particular transaction source and destination pair and the values cannot be reused by the sending device until the entire message operation has completed	Part 2, Sec. 4.2.5	Class 3	

5.8.2 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 5-10. Class 3 device logical layer target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	
	• **1A. DETAIL:** Atomic set operations	Part 1, Sec. 5.4.8	Class 3	
2.	MAINTENANCE port-write transaction	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Class 3	Inter-op
	• **2A. DETAIL:** MAINTENANCE port-write does not cause a MAINTENANCE response	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Class 3	
	• **2B. DETAIL:** MAINTENANCE port-write is discarded if the receiver does not have the resources to accept the port-write.	Part 1, Sec. 4.1.10	Class 3	
3.	ATOMIC set transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **3A. DETAIL:** ATOMIC set response returns the unmodified data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **3B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **3C. DETAIL:** Logic 1s are written after the data is read	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
4.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.2	Class 3	Inter-op
	• **4A. DETAIL:** Receive • msglen = 0 • ssize = 8B • mbox = 0 • letter = 0 • Above parameters are the minimum required for a device to indicate that it supports messages.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.2	Class 3	
	• **4B. DETAIL:** Verify correct receipt of out of order message segments.	Part 2, Sec. 3.3.2	Class 3	
	• **4C. DETAIL:** Response to a MESSAGE request never has a data payload	Part 2, Sec. 4.3.1 Part 2, Sec. 4.3.3	Class 3	

5.8.3 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 5-11. Class 3 device logical layer source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	
	• **1A. DETAIL:** Atomic set operations	Part 1, Sec. 5.4.7	Class 3	
2.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.1	Class 3	Inter-op
	• **2A. DETAIL:** Send • msglen = 0 • ssize = 8B • mbox = 0 • letter = 0 • Above parameters are the minimum required for a device to indicate that it supports messages.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.1	Class 3	
	• **2B. DETAIL:** MESSAGE packets always have data payloads	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2C. DETAIL:** MESSAGE transaction payload is a multiple of 8 bytes in size.	Part 2, Sec. 3.3.2	Class 3	
	• **2D. DETAIL:** Up to 16 individual MESSAGE transactions are allowed in one data message operation	Part 2, Sec. 3.3.2	Class 3	
	• **2E. DETAIL:** A “RETRY” response may cause the MESSAGE packet to be re-issued. A transaction request that is retried must be transmitted in order to complete.	Part 2, Sec. 3.1	Class 3	
	• **2F. DETAIL:** A response status of “ERROR” on any message packet causes termination of the message.	Part 2, Sec. 3.1	Class 3	
	• **2G. DETAIL:** Device generates the number of packets specified in the msglen field for a message operation	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2H. DETAIL:** All packets for a message operation must be of the same size and of the size specified in the ssize field (exception: data payload for the last packet in a message operation can be less than the size specified in the ssize field)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2I. DETAIL:** Send multiple outstanding messages to common mbox & letter but different msgseg/xmbox. Responses must be associated with the correct message target_info.	Part 2, Sec. 4.3.3 Part 2, Sec. 4.2.5	Class 3	
	• **2J. DETAIL:** All transactions for the same message must have the same (xmbox, if applicable) mbox and letter field values	Part 2, Sec. 3.3.2	Class 3	

5.8.4 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 5-12. Class 3 device logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ATOMIC set request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
2.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2A. DETAIL:** Received MESSAGE packet has no data payload	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2B. DETAIL:** MESSAGE transaction payload is not a multiple of 8 bytes in size	Part 2, Sec. 3.3.2	Class 3	
	• **2C. DETAIL:** For multiple packet data message operations, msgseg value is greater than msglen value for the same sender, mailbox and letter.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2D. DETAIL:** For multiple packet data message operations, msgseg or xmbox value is repeated and there was not a “RETRY” response for the previous usage for the same sender, mailbox and letter.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2E. DETAIL:** Received MESSAGE packet data payload is not of the size specified in the ssize field (exception for last packet which may be less)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2F. DETAIL:** Logical timeout on a message transaction is detected by the transmitter.	Part 4, Sec. 2.4.3 Part 6, Sec. 5.11.1	Class 3	
	• **2G. DETAIL:** Received MESSAGE response for destID/mailbox/letter/msgseg/xmbox that is not in use.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **2H. DETAIL:** Received MESSAGE response with ERROR status.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
3.	Illegal response for given request type	Part 2, Sec. 3.1	Class 3	

Blank Page

Chapter 6 Message Passing Logical Layer Checklists

6.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for devices supporting only Message Passing logical functionality for 8/16 LP-LVDS and 1x/4x LP-Serial compliant devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The Message Passing Logical layer inter-operability and certification checklist is broken down into a number of sub-lists.

6.2 Basic functionality compliance list

This is the list for basic functionality for RapidIO devices which only support message passing logical functionality.

Table 6-1. General device message passing logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Items 1 through 20 of Table 2-1, "General device 8/16 LP-LVDS physical layer general compliance list," on page 12 and/or items 1 through 20 of Table 3-1, "General device 1x/4x LP-Serial physical layer general compliance list," on page 42, depending on the physical layer(s) supported by the device. Note that these requirements are applied to the Logical Layer fields of CARs & CSRs.	Chapter 2, Table 2-1 Chapter 3, Table 3-1	Generic	Inter-op
2.	MESSAGE request payloads are always a multiple of double words in size.	Part 2, Sec. 3.4	Generic	
3.	DOORBELL requests always have a 2 byte 'Info' field instead of a payload.	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4	Generic	
4.	Response packets have the transaction ID of the associated request packet	Part 2, Sec. 3.1	Generic	Inter-op
5.	Responses to DOORBELL and MESSAGE requests never have data.	Part 2, Sec. 4.3.3	Generic	
6.	All necessary CARs (capabilities registers) exist and can be read	Part 1, Sec. 5.4	Generic	Inter-op
	• **6A. DETAIL:** Device Identity CAR; bits 0-15: value is implementation dependant • bits 16-31: value is vendor specific as assigned by the RapidIO Trade Association.	Part 1, Sec. 5.4.1 Part 7, Sec. 3.2.1.1	Generic	
	• **6B. DETAIL:** Device Information CAR; value is vendor and implementation dependant	Part 1, Sec. 5.4.2 Part 7, Sec. 3.2.1.1	Generic	
	• **6C. DETAIL:** Assembly Identity CAR; bits 0-15: value is implementation dependant bits 16-31: value is vendor specific as assigned by the RapidIO Trade Association	Part 1, Sec. 5.4.3 Part 7, Sec. 3.2.1.1	Generic	
	• **6D. DETAIL:** Assembly Information CAR; value is vendor and implementation dependant	Part 1, Sec. 5.4.4 Part 7, Sec. 3.2.1.1	Generic	
	• **6E. DETAIL:** Source Operations CAR; value is implementation dependant	Part 2, Sec. 5.4.1 Part 1, Sec. 5.4.7 Part 7, Sec. 3.2.1.1	Generic	
	• **6F. DETAIL:** Destination Operations CAR; value is implementation dependant	Part 2, Sec. 5.4.2 Part 1, Sec. 5.4.8 Part 7, Sec. 3.2.1.1	Generic	
7.	The response to a maintenance packet has the logical transaction, status, and TID fields and data payload (if applicable) set according to the request.	Part 1, Sec. 4.1.10	Generic	Inter-op

Table 6-1. General device message passing logical layer basic functionality list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
8.	For MESSAGEs, response packets have the letter/mbox/msgseg fields of the associated request packet	Part 2, Sec. 4.3.3	Generic	
9.	For MESSAGEs, outstanding letter/mbox/mseg fields are unique for a particular transaction source and destination pair and the values cannot be reused by the sending device until the entire message operation has completed	Part 2, Sec. 3.1 Part 2, Sec. 4.2.5	Generic	

6.3 Message passing target transaction support compliance list

This is the list for the device as a target of message passing logical layer transactions.

Table 6-2. General device message passing logical layer target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MAINTENANCE read transaction	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	Inter-op
	• **1A. DETAIL:** MAINTENANCE read request size of 4 bytes must be supported	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1B. DETAIL:** MAINTENANCE read request generates a MAINTENANCE read response	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1C. DETAIL:** MAINTENANCE read response payload size matches requested size	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **1D. DETAIL:** Response data for a MAINTENANCE packet consists of one or more double words, although sub-double-word data may have been requested.	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
2.	MAINTENANCE write transaction	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	Inter-op
	• **2A. DETAIL:** MAINTENANCE write request may be for 4 bytes	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **2B. DETAIL:** MAINTENANCE write request generates a MAINTENANCE write responses	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
	• **2C. DETAIL:** MAINTENANCE write response does not contain a data payload	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
3.	MESSAGE transaction (if device supports MESSAGEs)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.2	Generic	Inter-op
	• **3A. DETAIL:** Receive msglen = 0 ssize = 8B mbox = 0 letter = 0 Above parameters are the minimum required for a device to indicate that it supports messages.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.2	Generic	
	• **3B. DETAIL:** Verify correct receipt of out of order message segments.	Part 2, Sec. 3.3.2	Generic	
	• **3C. DETAIL:** Response to a MESSAGE request never has a data payload	Part 2, Sec. 4.3.1 Part 2, Sec. 4.3.3	Generic	
4.	DOORBELL transaction (if device supports DOORBELLs)	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4 Part 2, Sec. 4.3.3 Part 2, Sec. 5.4.2	Generic	Inter-op
	• **4A. DETAIL:** Receive a DOORBELL transaction		Generic	
	• **4B. DETAIL:** Response to a DOORBELL transaction never has a data payload.		Generic	
	• **4C. DETAIL:** Response to a DOORBELL transaction is DONE, RETRY or ERROR.		Generic	

6.4 Message passing source transaction support compliance list

This is the list for the device as a source of message passing logical layer transactions.

Table 6-3. General device message passing logical layer source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	DOORBELL transaction (if supported by device)	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4 Part 2, Sec. 4.3.3 Part 2, Sec. 5.4.1	Generic	Inter-op
	• **1A. DETAIL:** Send DOORBELL transaction, verify correct management of TID.		Generic	
	• **1B. DETAIL:** Receive DONE, RETRY or ERROR response transaction, verify correct matching to DOORBELL request transaction.		Generic	
	• **1C. DETAIL:** Receive DONE, RETRY or ERROR response transaction, verify correct matching to DOORBELL request transaction.		Generic	

Table 6-3. General device message passing logical layer source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
2.	MESSAGE transaction (if supported by device)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.1	Generic	Inter-op
	• **2A. DETAIL:** Send msglen = 0 ssize = 8B mbox = 0 letter = 0 Above parameters are the minimum required for a device to indicate that it supports messages.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 5.4.1	Generic	
	• **2B. DETAIL:** MESSAGE packets always have data payloads	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **2C. DETAIL:** MESSAGE transaction payload is a multiple of 8 bytes in size.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **2D. DETAIL:** Up to 16 individual MESSAGE transactions are allowed in one data message operation	Part 2, Sec. 3.3.2	Generic	
	• **2E. DETAIL:** A “RETRY” response may cause the MESSAGE packet to be re-issued. A transaction request that is retried must be transmitted in order to complete.	Part 2, Sec. 3.1	Generic	
	• **2F. DETAIL:** Device generates the number of packets specified in the msglen field for a message operation	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **2G. DETAIL:** All packets for a message operation must be of the same size and of the size specified in the ssize field (exception: data payload for the last packet in a message operation can be less than the size specified in the ssize field)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **2H. DETAIL:** Send multiple outstanding messages to common mbox & letter but different msgseg/xmbox. Responses must be associated with the correct message target_info.	Part 2, Sec. 4.3.3 Part 2, Sec 4.2.5	Generic	
	• **2I. DETAIL:** All transactions for the same message must have the same mbox, letter, msglen or xmbox, and size field values	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
3.	For devices which support both DOORBELL and MESSAGE transactions, verify that the TID values for DOORBELL and MESSAGE responses are managed correctly.	Part 2, Sec. 4.3.3	Generic	

6.5 Message passing detectable errors compliance list

Message passing logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the receiver of a packet for error detection.

Table 6-4. General device message passing logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MAINTENANCE write packet data payload length is not 4B, 8B, or multiple double-word quantity up to 64B.	Part 1, Sec. 4.1.10 Part 1, Sec. 3.4 Part 1, Sec. 3.5	Generic	
2.	Received MAINTENANCE read packet has a data payload	Part 1, Sec. 3.4.1 Part 1, Sec. 4.1.10	Generic	
3.	Received MAINTENANCE write packet has no data payload	Part 1, Sec. 3.41 Part 1, Sec. 4.1.10	Generic	
4.	Received MAINTENANCE packet uses a reserved field encoding for a required field	Part 1, Sec. 4.1.2	Generic	
5.	Received MAINTENANCE packet uses illegal combinations of field encodings, for example a 128 byte data payload.	Part 1, Sec. 4.1.10	Generic	
6.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **6A. DETAIL:** Received MESSAGE packet has no data payload	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **6B. DETAIL:** MESSAGE transaction payload is not a multiple of 8 bytes in size	Part 2, Sec. 3.3.2	Generic	
	• **6C. DETAIL:** For multiple packet data message operations, msgseg value is greater than msglen value for the same sender, mailbox and letter.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **6D. DETAIL:** For multiple packet data message operations, msgseg or xmbox value is repeated and there was not a “RETRY” response for the previous usage for the same sender, mailbox and letter.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Generic	
	• **6E. DETAIL:** Received MESSAGE packet data payload is not of the size specified in the ssize field (exception for last packet which may be less)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Generic	
	• **6F. DETAIL:** Logical timeout on a message transaction is detected by the transmitter.	Part 4, Sec. 2.4.3 Part 6, Sec. 5.11.1	Generic	
	• **6G. DETAIL:** Received MESSAGE response for destID/mailbox/letter/msgseg/xmbox that is not in use.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Generic	
	• **6H. DETAIL:** Received MESSAGE response with ERROR status.	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.1 Part 2, Sec. 4.3.3	Generic	

Table 6-4. General device message passing logical layer detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
7.	DOORBELL transaction	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4 Part 2, Sec. 4.3.3	Generic	
	• **7A. DETAIL:** Received DOORBELL packet is longer than allowed.		Generic	
	• **7B. DETAIL:** Received DONE response using a TID that is not in use.		Generic	
8.	Illegal response for given request type	Part 2, Sec. 3.1	Generic	

Chapter 7 Logical Layer Optional Functionality Checklists

7.1 Introduction

This chapter contains the optional I/O and Message Passing logical functionality inter-operability and certification checklists for 8/16 LP-LVDS and 1x/4x LP-Serial compliant devices.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The optional I/O and Message Passing layer inter-operability and certification checklist is broken down into a number of sub-lists.

7.2 Atomic clear compliance lists

A device supporting the atomic clear operation must meet these additional Logical Layer specification compliance requirements.

7.2.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-1. Atomic clear target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	Inter-op
	• **1A. DETAIL:** Atomic clear operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC clear transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC clear response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** Logic 0s are written after the data is read	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.2.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-2. Atomic clear source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic clear operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC clear can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.2.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-3. Atomic clear detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ATOMIC clear request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.3 Atomic increment compliance lists

A device supporting the atomic increment operation must meet these additional Logical layer specification compliance requirements.

7.3.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-4. Atomic increment target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Class 3	Inter-op
	• **1A. DETAIL:** Atomic increment operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC increment transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC increment response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** Read data is incremented then written to memory	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.3.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-5. Atomic increment source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic increment operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC increment can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.3.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-6. Atomic increment detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ATOMIC increment request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.4 Atomic decrement compliance lists

A device supporting the atomic decrement operation must meet these additional Logical layer specification compliance requirements.

7.4.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-7. Atomic decrement target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	Inter-op
	• **1A. DETAIL:** Atomic decrement operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC decrement transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC decrement response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** Read data is decremented then written to memory	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.4.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-8. Atomic decrement source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic decrement operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC decrement can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.4.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-9. Atomic decrement detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	ATOMIC decrement request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.5 Atomic test-and-swap compliance lists

A device supporting the atomic test-and-swap operation must meet these additional Logical layer specification compliance requirements.

7.5.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-10. Atomic test-and-swap target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	Inter-op
	• **1A. DETAIL:** Atomic test-and-swap operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC test-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC test-and-swap response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** ATOMIC test-and-swap compares read data to 0 and writes with supplied data if compare is true	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.5.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-11. Atomic test-and-swap source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic test-and-swap operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC test-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC test-and-swap can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** ATOMIC test-and-swap transaction must have a data payload	Part 1, Sec. 3.3.4	Class 3	

7.5.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-12. Atomic test-and-swap detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Atomic test-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **1A. DETAIL:** ATOMIC test-and-swap request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **1B. DETAIL:** ATOMIC test-and-swap transaction does not have a data payload	Part 1, Sec. 3.3.4	Class 3	
	• **1C. DETAIL:** Response to ATOMIC test-and-swap transaction does not have a data payload	Part 1, Sec. 4.1.7	Class 3	

7.6 Atomic swap compliance lists

A device supporting the atomic swap operation must meet these additional Logical layer specification compliance requirements.

7.6.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-13. Atomic swap target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	Inter-op
	• **1A. DETAIL:** Atomic swap operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC swap response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** ATOMIC swap unconditionally writes with supplied data.	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.6.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-14. Atomic swap source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic swap operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC swap can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** ATOMIC swap transaction must have a data payload	Part 1, Sec. 3.3.4	Class 3	

7.6.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-15. Atomic swap detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Atomic swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **1A. DETAIL:** ATOMIC swap request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **1B. DETAIL:** ATOMIC swap transaction does not have a data payload	Part 1, Sec. 3.3.4	Class 3	
	• **1C. DETAIL:** Response to ATOMIC swap transaction does not have a data payload	Part 1, Sec. 4.1.7	Class 3	

7.7 Atomic compare-and-swap compliance lists

A device supporting the atomic compare-and-swap operation must meet these additional Logical layer specification compliance requirements.

7.7.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-16. Atomic compare-and-swap target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Destination Operations CAR must indicate target support for	Part 1, Sec. 5.4.8	Generic	Inter-op
	• **1A. DETAIL:** Atomic compare-and-swap operations	Part 1, Sec. 5.4.8	Class 3	
2.	ATOMIC compare-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC compare-and-swap response returns unmodified read data	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** Read-modify-write operation is never interrupted by another operation to the same address	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2C. DETAIL:** ATOMIC compare-and-swap compares read data to the first 8 bytes of the payload. If they are equal, it writes the second 8 bytes of payload to the memory location.	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	

7.7.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-17. Atomic compare-and-swap source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Source Operations CAR must indicate source support for	Part 1, Sec. 5.4.7	Generic	Inter-op
	• **1A. DETAIL:** Atomic compare-and-swap operations	Part 1, Sec. 5.4.7	Class 3	
2.	ATOMIC compare-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **2A. DETAIL:** ATOMIC compare-and-swap can only request 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **2B. DETAIL:** ATOMIC compare-and-swap transaction must have a data payload	Part 1, Sec. 3.3.4	Class 3	
	• **2C. DETAIL:** ATOMIC compare-and-swap transaction data payload must be two double words (16-bytes). This is different than other ATOMIC transactions.	Part 1, Sec. 4.1.7	Class 3	

7.7.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-18. Atomic compare-and-swap detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Atomic compare-and-swap transaction	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	Inter-op
	• **1A. DETAIL:** ATOMIC compare-and-swap request is for other than 1, 2, or 4 bytes	Part 1, Sec. 3.3.4 Part 1, Sec. 4.1.5	Class 3	
	• **1B. DETAIL:** ATOMIC compare-and-swap transaction does not have a data payload	Part 1, Sec. 3.3.4	Class 3	
	• **1C. DETAIL:** Response to ATOMIC compare-and-swap transaction does not have a data payload	Part 1, Sec. 4.1.7	Class 3	
	• **1D. DETAIL:** Response to ATOMIC compare-and-swap transaction data payload must be two double words (16-bytes).	Part 1, Sec. 4.1.7	Class 3	

7.8 Doorbell compliance lists

A device supporting the doorbell operation must meet these additional Logical layer specification compliance requirements.

7.8.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-19. Doorbell target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	DOORBELL transaction	Part 2, Sec. 3.3.1 Part 2, Sec. 4.3.3	Class 3	Inter-op
	• **1A. DETAIL:** Response to a DOORBELL transaction packet never has a data payload	Part 2, Sec. 4.3.3	Class 3	
2.	DOORBELL transaction packets are placed in the doorbell message queue within the processing element	Part 2, Sec. 3.3.1	Class 3	

7.8.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-20. Doorbell source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	DOORBELL transaction	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4	Class 3	Inter-op
	• **1A. DETAIL:** Send srcTID = 0-255, info field - 16 bytes	Part 2, Sec. 4.2.4	Class 3	
	• **1B. DETAIL:** DOORBELL transaction packets never have data payloads	Part 2, Sec. 4.2.4	Class 3	
	• **1C. DETAIL:** A “RETRY” response may cause the DOORBELL packet to be re-issued. A transaction request that is retried must be transmitted in order to complete.	Part 2, Sec. 3.1	Class 3	
	• **1D. DETAIL:** Send multiple outstanding doorbells to different Transaction ID’s. Responses must be associated with the correct doorbell (targetTID).	Part 2, Sec. 4.3.3	Class 3	

7.8.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-21. Doorbell detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	DOORBELL transaction	Part 2, Sec. 3.3.1 Part 2, Sec. 4.2.4 Part 2, Sec. 4.3.3	Class 3	Inter-op
	• **1A. DETAIL:** DOORBELL transaction packet has a data payload	Part 2, Sec. 4.2.4	Class 3	
	• **1B. DETAIL:** Response to DOORBELL transaction packets has a data payload	Part 2, Sec. 4.3.3	Class 3	
2.	DOORBELL transaction packets are not placed in the doorbell message queue	Part 2, Sec. 3.3.1	Class 3	

7.9 Data message compliance lists

A device supporting data message operations to mailboxes 1, 2, or 3 or containing mailboxes 1, 2, or 3 must meet these additional Logical layer specification compliance requirements.

7.9.1 Target transaction support compliance list

This is the list for the device as a transaction target.

Table 7-22. Data message target transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Class 3	Inter-op
	• **1A. DETAIL:** Receive msglen = 0-15 = 1-16 packets ssize = 8,16,32,64,128,256B mbox = 0-3 letter = 0-3 msgseg <= msglen (or xmbox 0-15)	Part 2, Sec. 4.2.5	Class 3	
	• **1B. DETAIL:** Verify correct receipt of out of order message segments.	Part 2, Sec. 3.3.2	Class 3	
	• **1C. DETAIL:** Response to a MESSAGE transaction packet never has a data payload	Part 2, Sec. 4.3.3	Class 3	
2.	MESSAGE transaction packets are placed in the targeted mailbox within the processing element	Part 2, Sec. 3.3.1	Class 3	

7.9.2 Source transaction support compliance list

This is the list for the device as a transaction source.

Table 7-23. Data message source transaction support list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Class 3	Inter-op
	• **1A. DETAIL:** Send msglen = 0-15 = 1-16 packets ssize = 8,16,32,64,128,256B mbox = 0-3 letter = 0-3 msg_seg <= msglen (or xmbox 0-15)	Part 2, Sec. 4.2.5	Class 3	
	• **1B. DETAIL:** MESSAGE packets always have data payloads	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1C. DETAIL:** MESSAGE data payload is a multiple of 8 bytes in size.	Part 2, Sec. 4.2.5	Class 3	
	• **1D. DETAIL:** Up to 16 individual MESSAGE transactions are allowed in one data message operation	Part 2, Sec. 3.3.2	Class 3	
	• **1E. DETAIL:** A “RETRY” response may cause the MESSAGE packet to be re-issued. A transaction request that is retried must be transmitted in order to complete.	Part 2, Sec. 3.1	Class 3	
	• **1F. DETAIL:** All packets for a message operation have the same mbox and letter field values	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Class 3	
	• **1G. DETAIL:** Device generates the number of packets specified in the msglen field for a message operation	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1H. DETAIL:** All packets for a message operation must be of the same size and of the size specified in the ssize field (exception: data payload for the last packet in a message operation can be less than the size specified in the ssize field)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1I. DETAIL:** Send multiple outstanding messages to common mbox & letter but different msgseg/xmbox. Responses must be associated with the correct message (target_info).	Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Class 3	

7.9.3 Detectable errors compliance list

Logical layer errors are generally not recoverable in hardware. They may be recoverable in software. The device is always the target of a packet for error detection.

Table 7-24. Data message detectable errors list

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	MESSAGE transaction	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5 Part 2, Sec. 4.3.3	Class 3	Inter-op
	• **1A. DETAIL:** Received MESSAGE packet has no data payload	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1B. DETAIL:** MESSAGE transaction data payload is not a multiple of 8 bytes in size	Part 2, Sec. 4.2.5	Class 3	
	• **1C. DETAIL:** More than 16 individual MESSAGE transactions are used in one data message operation	Part 2, Sec. 3.3.2	Class 3	
	• **1D. DETAIL:** msgseg value is greater than msglen value	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1E. DETAIL:** msgseg value is repeated and there was not a “RETRY” response for the previous usage	Part 2, Sec. 3.3.2 Part 2, Sec. 3.1	Class 3	
	• **1F. DETAIL:** Received MESSAGE packet data payload is not of the size specified in the ssize field (exception for last packet which may be less)	Part 2, Sec. 3.3.2 Part 2, Sec. 4.2.5	Class 3	
	• **1G. DETAIL:** Logical timeout on message transaction causes retransmission	Part 2, Sec. 3.1	Class 3	Inter-op

Blank Page

Chapter 8 Multicast Checklists

8.1 Introduction

This chapter contains the device inter-operability and certification checklists adhering to the RapidIO Interconnect Specification for devices supporting the *RapidIO Interconnect Specification Part 11: Multicast Extensions Specification, Revision 1.3.1*.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in Part 7: System and Device Inter-operability Specification, Rev. 1.3.

The last column, 'Inter-op Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-op Item' column with the word 'Inter-op' can be made to work between two devices. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite. A standard test suite does not yet exist.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The multicast inter-operability and certification checklist is broken down into a number of sub-lists.

8.2 Behavioral Certification List

This section specifies general requirements for a compliant device which supports multicast functionality.

Reads and writes to CSRs and CARs are reference from RapidIO transactions received by a device.

Table 8-1. Multicast Packet Behavior Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Packets multicast are not modified by the multicasting device.	Part 11, Sec. 2.2	Generic	Interop
2.	The destination ID of a packet is used to determine if the packet will be multicast.	Part 11, Sec. 2.1	Generic	Interop
3.	There is one set of multicast masks for the entire switch.	Part 11, Sec. 2.3	Generic	
4.	When the destination ID of a packet matches that of a destination ID associated with a multicast mask, the packet is multicast to all egress ports configured in the multicast mask, except that a packet is never multicast out of the port that it was received on.	Part 11, Sec. 2.3	Generic	
5.	The defined CSRs allow multicast masks to be configured.	Part 11, Sec. 2.3	Generic	
6.	The implementation of the defined CSRs allow a destination ID to be associated with at most one multicast mask per port.	Part 11, Sec. 2.3	Generic	
7.	The last association operation performed for a destination ID dictates which multicast mask is associated with that destination ID.	Part 11, Sec. 2.3	Generic	
8.	Packets to be multicast using a multicast mask with no egress ports selected are dropped without error notification.	Part 11, Sec. 2.3	Generic	
9.	The state of multicast masks after reset is that no egress ports are selected.	Part 11, Sec. 2.3	Generic	
10.	After reset, no destination IDs are associated with multicast masks.	Part 11, Sec. 2.3	Generic	
11.	Multicast packets in the same multicast group with the same flowID received on the same ingress port are multicast on egress ports in the same order they were received on the ingress port.	Part 11, Sec. 2.4	Generic	Interop
12.	Packets which do not require a response can be multicast. Packets which do require a response result in implementation specific behavior.	Part 11, Sec. 2.2	Generic	

8.3 Multicast Programming Model Certification Lists

This is the list of requirements for the multicast registers and programming model.

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	Processing Element Features CAR	Part 11, Sec. 3.2	Generic	
	• **1A. DETAIL:** If the device supports the multicast extensions, bit 21 of the Processing Element Features CAR has a value of 1.	Part 11, Sec. 3.2	Generic	
	• **1B. DETAIL:** Bit 21 of the Processing Element Features CAR is read only.	Part 11, Sec. 3.2	Generic	
2.	Switch Multicast Support CAR is read only, and is compliant with the following:	Part 11, Sec. 3.3	Generic	
	• **2A. DETAIL:** If device supports the 'simple association' model, bit 0 has a value of 1. If the device does not support the 'simple association' model, bit 0 has a value of 0.	Part 11, Sec. 3.3	Generic	
	• **2B. DETAIL:** If device supports the 'simple association' model, the Switch Multicast Information CAR must indicate support for block association operations.	Part 11, Sec. 3.3	Generic	
3.	Switch Multicast Information CAR is read only, and compliant with the following:	Part 11, Sec. 3.4	Generic	
	• **3A. DETAIL:** If the device supports block association operations, bit 0 has a value of 1. If block association operations are not supported, bit 0 has a value of 0.	Part 11, Sec. 3.4	Generic	
	• **3B. DETAIL:** If the device supports per port association operations, bit 1 has a value of 1. If per port association operations are not supported, bit 1 has a value of 0.	Part 11, Sec. 3.4	Generic	
	• **3C. DETAIL:** The maximum number of destination IDs that can be associated with a single multicast mask is contained in bits 2 through 15.	Part 11, Sec. 3.4	Generic	
	• **3D. DETAIL:** The number of multicast masks that exist in the device is contained in bits 16 through 31.	Part 11, Sec. 3.4	Generic	
	• **3E. DETAIL:** The maximum number of destination IDs/multicast masks that can be programmed using a block association operation is contained in bits 16 through 31.	Part 11, Sec. 3.4	Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	The Multicast Mask Port CSR operates correctly.	Part 11, Sec. 3.5 Part 11, Sec. 4.2	Generic	
	• **4A. DETAIL:** Associations between destination IDs and multicast masks are not affected by any read or write operation performed on the Multicast Mask Port CSR.		Generic	
	• **4B. DETAIL:** The index of the multicast mask that is the subject of the register operations is contained in bits 0 through 15 (Mcast_Mask).		Generic	
	• **4C. DETAIL:** The egress port that is the subject of the multicast mask operations is contained in bits 16 through 23 (Egress_Port_Num).		Generic	
	• **4D. DETAIL:** The command value that indicates which multicast mask operation to perform is contained in bits 25-27 (Mask_Cmd).		Generic	
	• **4E. DETAIL:** All multicast Mask_Cmd commands operate correctly when the value in the Mcast_Mask field is less than the value of the MaxMcastMasks field in the Switch Multicast Information CAR.	Part 11, Sec. 3.4 Part 11, Sec. 3.5 Part 11, Sec. 4.2	Generic	
	• **4F. DETAIL:** All multicast Mask_Cmd commands operate correctly when the value in the Egress_Port_Num field is less than the value of the Port_Total field in the Switch Port Information CAR.	Part 11, Sec. 3.4 Part 11, Sec. 3.5 Part 11, Sec. 4.2	Generic	
	• **4G. DETAIL:** All multicast Mask_Cmd commands operate correctly when the value in the Mask_Cmd field is that of a defined command (0b000, 0b001, 0b010, 0b100, 0b101).	Part 11, Sec. 3.5	Generic	
	• **4H. DETAIL:** The capability to perform Write-to-Verify commands must be present.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.4	Generic	Interop
	• **4H1. DETAIL:** When the Multicast Mask Port CSR is written with a Mask_Cmd field value of 0b000, the set of egress ports enabled for each multicast masks is not affected.		Generic	
	• **4H2. DETAIL:** The value of Port_Present after a Write_to_Verify command is unchanged until the next Write_to_Verify command is written to the Multicast Mask Port CSR.		Generic	
	• **4H3. DETAIL:** Bit 31 is read as 1 after a Write_to_Verify command is written to the Multicast Mask Port CSR only when the specified egress port in the specified multicast mask is enabled.		Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **4I. DETAIL:** The capability to perform Add_Port commands must be present.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.2	Generic	Interop
	• **4I1. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b001 in the Mask_Cmd field, the egress port identified by the value in the Egress_Port_Num field is enabled in the multicast mask identified by the value in the Mcast_Mask field.		Generic	
	• **4J. DETAIL:** The capability to perform Delete_Port commands must be present.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.3	Generic	Interop
	• **4J1. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b010 in the Mask_Cmd field, the egress port identified by the value in the Egress_Port_Num field is disabled in the multicast mask identified by the value in the Mcast_Mask field.		Generic	
	• **4K. DETAIL:** The capability perform Delete_All_Ports commands must be present.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.1	Generic	
	• **4K1. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b100 in the Mask_Cmd field, all egress ports are disabled in the multicast mask identified by the value in the Mcast_Mask field.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.1	Generic	
	• **4K2. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b100 in the Mask_Cmd field, the value in the Egress_Port_Num field does not affect the operation of the command.		Generic	
	• **4L. DETAIL:** The capability to perform Add_All_Ports commands must be present.	Part 11, Sec. 3.5 Part 11, Sec. 4.2.2	Generic	
	• **4L1. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b101 in the Mask_Cmd field, all egress ports are enabled in the multicast mask identified by the value in the Mcast_Mask field.		Generic	
	• **4L2. DETAIL:** When a register write to the Multicast Mask Port CSR occurs with a value of 0b101 in the Mask_Cmd field, the value in the Egress_Port_Num field does not affect the operation of the command.		Generic	
	• **4M. DETAIL:** After reset, the Multicast Mask Port CSR value is 0x00000000.	Part 11, Sec. 3.5	Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
5.	The Multicast Associate Select CSR operates correctly.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 4.3	Generic	
	• **5A. DETAIL:** The egress ports selected in each multicast mask are not affected by any read or write operation performed on the Multicast Associate Select CSR.		Generic	
	• **5B. DETAIL:** The associations between destination IDs and multicast masks are not affected by any read or write operation performed on the Multicast Associate Select CSR.		Generic	
	• **5C. DETAIL:** The most significant 8 bits of the large (16 bit) destination ID that is the subject of associate operations is contained in bits 0 through 7 (Large_DestID).		Generic	
	• **5D. DETAIL:** The least significant 8 bits of the destination ID that is the subject of associate operations is contained in bits 8 through 15 (DestID).		Generic	
	• **5E. DETAIL:** The index of the multicast mask that is the subject of associate operations is contained in bits 16 through 31 (Mcast_Mask_Num).		Generic	
	• **5G. DETAIL:** Multicast Assoc_Cmd commands operate correctly when the value in the Mcast_Mask_Num field is less than the value of the MaxMcastMasks field in the Switch Multicast Information CAR.		Generic	
	• **5H. DETAIL:** After a reset, the value of the Multicast Associate Select CSR is 0x00000000.	Part 11, Sec. 3.6	Generic	
6.	The Multicast Associate Operation CSR operates correctly.	Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6A. DETAIL:** The egress ports selected in each multicast mask are not affected by any read or write operation performed on the Multicast Associate Operation CSR.	Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6B. DETAIL:** The number of sequential destination IDs and multicast masks to be affected by an associate operation can be controlled by the value in bits 0 to 15 (Assoc_Blksize) of the Multicast Associate Operation CSR only if bit 0 in the Switch Multicast Information CAR has a value of 1.	Part 11, Sec. 3.5 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6C. DETAIL:** The ingress port for an associate operation can be controlled by the value in bits 16 to 23 (Ingress_Port) of the Multicast Associate Operation CSR only if bit 1 in the Switch Multicast Information CAR has a value of 1.	Part 11, Sec. 3.5 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **6D. DETAIL:** The Large_DestID field in the Multicast Associate Select CSR is used to select the destination ID for an associate operation only when bit 24 (Large_Transport) in the Multicast Associate Operation CSR has a value of 1.	Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6E. DETAIL:** Selection of the specific associate operation is controlled by bits 25 and 26 (Assoc_Cmd) in the Multicast Associate Operation CSR.	Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6F. DETAIL:** Multicast Assoc_Cmd commands operate correctly when bit 1 in the Switch Multicast Information CAR has a value of 1 and the value in the Ingress_Port field is less than the value of the Port_Total field in the Switch Port Information CAR.	Part 11, Sec. 3.4 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6G. DETAIL:** Multicast Assoc_Cmd commands operate correctly when bit 0 in the Switch Multicast Information CAR has: a value of 1 AND the value in the Mcast_Mask_Num field of the Switch Multicast Select CSR added to the value of the Assoc_Blksize field in the Multicast Associate Operation CSR is less than the value of the MaxMcastMasks field in the Switch Multicast Information CAR.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4	Generic	
	• **6H. DETAIL:** Multicast Assoc_Cmd commands operate correctly when bit 0 in the Switch Multicast Information CAR has: a value of 1 AND the Large_DestID/DestID fields added to the value of Assoc_Blksize is not greater than the maximum destination ID, as indicated by the Large_Transport field in the Switch Multicast Operation CSR.		Generic	
	• **6I. DETAIL:** When the Assoc_Cmd value is written to a value defined in the specification (0b00, 0b10, 0b11), the function defined in the specification is performed correctly.	Part 11, Sec. 3.7	Generic	
	• **6J. DETAIL:** The capability to perform Write_To_Verify commands must be present.	Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.6	Generic	Interop
	• **6J1. DETAIL:** When the Multicast Associate Operation CSR is written with an Assoc_Cmd field value of 0b00, associations between any destination ID and any multicast mask are not affected.		Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **6J2. DETAIL:** After a write to the Multicast Associate Operation CSR when the Assoc_Cmd field value is 0b00, a read of the Multicast Associate Operation CSR has a value of 1 in bit 31 only if an association exists between the destination ID and multicast mask specified by the values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport and Ingress Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.6	Generic	
	• **6J3. DETAIL:** A read of the Multicast Associate Operation CSR returns 1 in bit 31 to indicate an association exists between the destination ID and multicast mask specified by the current values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport and Ingress Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR only if the Assoc_Cmd field value is 0b00.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.6	Generic	
	• **6K. DETAIL:** The capability to perform Delete_Assoc commands must be present.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.5	Generic	Interop
	• **6K1. DETAIL:** WHEN the Block_Assoc field in the Switch Multicast Information CAR has a value of 0 AND the Multicast Associate Operation CSR is written with an Assoc_Cmd field value of 0b10, THEN any association is removed between the destination ID and multicast mask specified by the current values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport and Ingress Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR.		Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **6K2. DETAIL:** WHEN • the Block_Assoc field in the Switch Multicast Information CAR has a value of 1 • the Multicast Associate Operation CSR is written with an Assoc_Cmd field value of 0b10 • AND the Large_DestID/DestID fields added to the value of Assoc_Blksize is not greater than the maximum destination ID, as indicated by the Large_Transport field in the Switch Multicast Operation CSR • THEN any association is removed between the block of destination IDs and multicast masks specified by the current values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport, Assoc_Blksize and Ingress_Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.5	Generic	
	• **6K3. DETAIL:** The associations deleted in 6K2 are between the first destination ID and the first multicast mask, the second destination ID and the second multicast mask, the third destination ID and the third multicast mask, and so on.		Generic	
	• **6K4. DETAIL:** If bit 1 in the Switch Multicast Information CAR has a value of 1, the associations in 6K1 and 6K2 are removed only on the ingress port selected by the Ingress_Port field value.		Generic	
	• **6K5. DETAIL:** WHEN • the Delete_Assoc command is written to the Multicast Associate Operation CSR • bit 0 of the Switch Multicast Information CAR has a value of 1, • bit 0 in the Switch Multicast Support CAR has a value of 1, • the Assoc_Blksize field in the Multicast Associate Operation CSR has a value of MaxMCastMasks - 1 • the Mcast_Mask_Num field value is 0 • AND the Large_DestID/DestID fields added to the value of Assoc_Blksize is not greater than the maximum destination ID, as indicated by the Large_Transport field in the Switch Multicast Operation CSR • THEN the associations specified in 6K3 will be removed.	Part 11, Sec. 3.3 Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4.5	Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **6L. DETAIL:** The capability to perform Add_Assoc commands must be present.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.1	Generic	Interop
	• **6L1. DETAIL:** WHEN • the Block_Assoc field in the Switch Multicast Information CAR has a value of 0 • AND the Multicast Associate Operation CSR is written with an Assoc_Cmd field value of 0b11, • THEN an association is created between the destination ID and multicast mask specified by the current values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport and Ingress Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR.		Generic	
	• **6L2. DETAIL:** WHEN • the Block_Assoc field in the Switch Multicast Information CAR has a value of 1 • the Multicast Associate Operation CSR is written with an Assoc_Cmd field value of 0b11 • AND the Large_DestID/DestID fields added to the value of Assoc_Blksize is not greater than the maximum destination ID controlled by the Large_Transport field in the Switch Multicast Operation CSR • THEN associations are created between the block of destination IDs and multicast masks specified by the current values of the Large_DestID, DestID and Mcast_Mask_Num fields in the Multicast Associate Select CSR and the value of the Large_Transport, Assoc_Blksize and Ingress Port (if bit 1 in the Switch Multicast Information CAR has a value of 1) fields in the Multicast Associate Operation CSR.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.3	Generic	
	• **6L3. DETAIL:** The associations created in 6L2 are between the first destination ID and the first multicast mask, the second destination ID and the second multicast mask, the third destination ID and the third multicast mask, and so on.	Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.4.2 Part 11, Sec. 4.4.3	Generic	
	• **6L4. DETAIL:** If bit 1 in the Switch Multicast Information CAR has a value of 1, the associations in 6L1 and 6L2 are created only on the ingress port selected by the Ingress_Port field value.		Generic	

Table 8-2. Multicast Programming Model Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
	• **6M. DETAIL:** WHEN • the Add_Assoc command is written to the Multicast Associate Operation CSR • bit 0 in the Switch Multicast Support CAR has a value of 1 • the Mcast_Mask_Num field in the Multicast Associate Select CSR has a value of 0 • the Assoc_Blksize field in the Multicast Associate Operation CSR has a value of MaxMCastMasks - 1 • AND the Large_DestID/DestID fields added to the value of Assoc_Blksize is not greater than the maximum destination ID, as indicated by the Large_Transport field in the Switch Multicast Operation CSR • THEN the multicast associations specified in 6L3 are added.	Part 11, Sec. 3.3 Part 11, Sec. 3.4 Part 11, Sec. 3.6 Part 11, Sec. 3.7 Part 11, Sec. 4.3 Part 11, Sec. 4.4.3		
	• **6N. DETAIL:** After a reset, the Multicast Associate Operation CSR has a value of 0x00000000.	Part 11, Sec. 3.7	Generic	

Blank Page

Blank Page

Blank Page