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Subject: Error Management Extensions Certification checklist

Background: Certification and interoperability checklist for the RapidIO specification Revision 1.3, part 8 ‘Error Management Extensions Specification’.

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Error Management Certification Checklist

This document contains the device inter-operability and certification checklists

adhering to the RapidIO Interconnect Specification for devices supporting the *RapidIO Interconnect Specification Part 8: Error Management Specification, Revision 1.3*.

Each checklist is contained within a table having 5 columns. The item number, 'Item No.' contains a number/letter combination which uniquely identifies the checklist item. A text description of the aspect of the RapidIO specification checked is kept in the 'Compliance Item' column. A reference to the specific section of the specification which contains the requirement occurs in the 'Specification Reference' column. The 'Device Class' column contains the list of device classes, as defined in the multicast extensions specification.

The last column, 'Inter-operability Item', requires further explanation. This document defines three levels to which devices can be considered to meet the RapidIO specification. Inter-operability is the least stringent, requiring only that vendors demonstrate in some fashion that the functionality identified in the 'Inter-operability Item' column with the word 'Inter-op' can be made to work between two devices. An 'Inter-op' function does not need to be precisely compliant to the specification. Only those items marked as 'Inter-op' are required to claim interoperability. The next level, compliance, requires that all items in the checklist be demonstrated by the vendor, using a vendor developed test suite. The last level, certification, requires that all items in the checklist be demonstrated using a standard test suite.

Some parts of the specification are optional, but still require check list items to be assigned to them. Those checklist items which pertain to optional portions of the specification are highlighted with a grey background.

The data streaming inter-operability and certification checklist is broken down into sub-lists.

1 Error Management Behavioral Requirements List

This section specifies behavioral requirements for a compliant device which supports Error Management functionality.

Table 1. Error Management Behavioral Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	The occurrence of a transmission error shall be logged by hardware by setting the appropriate error indication bit in the Port n Error Detect CSR. For more detail on which errors cause which bits to be set, refer to Table 2, item 12 in this document.	Part 8, Sec. 1.2.1	Generic	Interop
2.	When the bit corresponding to an error is set in the Port n Error Rate Enable CSR, that error is enabled for error capture and error counting.	Part 8, Sec. 1.2.1	Generic	Interop
3.	When the Capture Valid Info status bit is not set in the Port n Error Capture Attributes CSR, and the error detected is enabled in the Port n Error Rate Enable CSR, then up to the first 16 bytes of a packet header or the 4 bytes of the control symbol that have a detected error shall be saved to the Port n Error Capture CSRs, and the Capture Valid Info bit is set to 1.	Part 8, Sec. 1.2.1	Generic	Interop
4.	Port n Error Capture CSRs are not overwritten by error capture information when the Capture Valid Info bit is 1.	Part 8, Sec. 1.2.1	Generic	
5.	No action shall be taken if the Error Rate Counter continues to exceed either the Error Rate Failed Threshold or Error Rate Degraded Threshold.	Part 8, Sec. 1.2.2	Generic	
6.	No action shall be taken if the Error Rate Counter drops below either the Error Rate Failed Threshold or Error Rate Degraded threshold.	Part 8, Sec. 1.2.2	Generic	
7.	The Error Rate Bias field determines the rate at which the Error Rate Counter is decremented.	Part 8, Sec. 1.2.3	Generic	
8.	If the Error Rate Counter is less than the Error Rate Recovery value added to the Error Rate Failed Threshold Trigger, the Error Rate Counter shall increment when a physical layer error is detected whose associated enable bit is set in the Port n Error Rate Enable register.	Part 8, Sec. 1.2.3 Part 8, Sec. 2.3.2.17	Generic	Interop
9.	The Error Rate Counter shall not underflow or overflow.	Part 8, Sec. 1.2.3	Generic	Interop
10.	The Error Rate Counter can be reset at any time by software.	Part 8, Sec. 1.2.3	Generic	
11.	When a logical or transport layer error is detected, the appropriate bit is set by the hardware in the Logical/Transport Layer Error Detect CSR. For more information, refer to table 2 item 4 of this document.	Part 8, Sec. 1.3.1	Generic	Interop

Table 1. Error Management Behavioral Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	An endpoint shall detect that, within a message transfer operation, following transmission of a response, a request is not received before a timeout period equal to the Port Response Time-out Control CSR expires.	Part 8, Sec. 1.3.2	Class 3	Interop
13.	If an interrupt is not issued to the local system, then a Maintenance port-write operation is sent to a predetermined system host to notify software that an error has occurred.	Part 8, Sec. 1.4	Generic	
14.	Clearing the Port-write pending status bit indicates that the port-write has been received.	Part 8, Sec. 1.4	Generic	
15.	The port write contains information as defined in Part 8, Table 1-2	Part 8, Sec. 1.4	Generic	Interop
16.	To create events for software test and debug, software must write to Logical/Transport Layer Error capture registers and then write the Logical/Transport Layer Error detect Register to trigger the error reporting mechanism.	Part 8, Sec. 1.5	Generic	Interop
17.	Writing a ‘1’ to an enabled event in the Logical/Transport Layer Error Detect Register will cause the standard reporting mechanism to be triggered.	Part 8, Sec. 1.5	Generic	Interop
18.	To create events for software test and debug, software must write the Port n Attributes Error Capture CSR to set the Capture Valid Info bit and then the packet/control symbol information in the other capture registers to trigger the error reporting mechanism.	Part 8, Sec. 1.5	Generic	Interop
19.	Each write of a non-zero value to the Port n Error Detect CSR shall cause the Error Rate Counter to increment if the corresponding bit is enabled in the Port n Error Rate Enable CSR.	Part 8, Sec. 1.5	Generic	Interop
20.	When a port-write is generated, it is sent to the destination ID programmed in the Port-write Target Device ID CSR.	Part 8, Sec. 2.3.2.8	Generic	Interop

2 Register Checklist

The register checklist describes the behavioral requirements for the Error Management Extensions register block.

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
1.	When a device has an Error Management Extensions Block Header, the following bits are available in the Port n Control CSRs:	Part 8, Sec. 2.2	Generic	Interop
	1A: Detail: Stop on Port Failed Encountered, Drop Packet Enable, and Port Lockout bits are bits 28, 29, and 30 in the Port n Control CSRs:	Part 8, Sec. 2.2	Generic	
	1B: Detail: Bits 28, 29, 30 are writable	Part 8, Sec. 2.2	Generic	
	1C: Detail: Bits 28 and 29 control behavior as described in section 1.2.4	Part 8, Sec. 1.2.4 Part 8, Sec. 2.2	Generic	
	1D: Detail: When Port Lockout is cleared, the packets that may be received and issued are controlled by the state of the Output Port Enable and Input Port Enable bits in the Port n Control CSR.	Part 8, Sec. 2.2	Generic	
	1E: Detail: When Port Lockout is set, this port is stopped and is not enabled to issue or receive any packets; the input port can still follow the training procedure and can still send and respond to link requests, all received packets return packet-not-accepted control symbols to force an error condition to be signalled by the sending device.	Part 8, Sec. 2.2	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
2.	When a device has an Error Management Extensions Block Header, the following bits are available in the Port n Error and Status CSRs:	Part 8, Sec. 2.2	Generic	Interop
	2A: Detail: Output-Packet Dropped, Output Failed-encountered, and Output Degraded-encountered bits are bits 5, 6 and 7 in the Port n Error and Status CSRs:	Part 8, Sec. 2.2	Generic	
	2B: Detail: Bits 5, 6 and 7 may be individually written with 1 to clear the bit 0.	Part 8, Sec. 2.2	Generic	
	2C: Detail: Bits 5, 6 and 7, once set, remain set until cleared as described in 2B above.	Part 8, Sec. 2.2	Generic	
	2D: Detail: If the output port in a switch has discarded a packet due to expiry of the Time-to-Live counter, the 'Output Packet-dropped' bit is set to 1.	Part 8, Sec. 1.2.5 Part 8, Sec. 2.2	Generic	
	2E: Detail: When the Error Rate Counter in the Port n Error Rate register exceeds the value of the Error Rate Degraded Threshold Trigger, the Output Degraded-encountered bit in the Port n Error and Status CSR shall be set.	Part 8, Sec. 1.2.2 Part 8, Sec. 2.2	Generic	
	2F: Detail: When the Error Rate Counter in the Port n Error Rate register exceeds the value of the Error Rate Failed Threshold Trigger, the Output Failed-encountered bit in the Port n Error and Status CSR shall be set.	Part 8, Sec. 1.2.2 Part 8, Sec. 2.2	Generic	
	2G: Detail: Transmission of a port write causes the port-write Pending status bit in the Port n Error and Status CSR to be set to 1.	Part 8, Sec. 1.4 Part 6, Sec. 6.5.2.5 Part 6, Sec. 6.6.2.8 Part 6, Sec. 6.7.2.4 Part 6, Sec. 6.8.2.7 Part 4, Sec. 5.5.2.5 Part 4, Sec. 5.6.2.8 Part 4, Sec. 5.7.2.4 Part 4, Sec. 5.8.2.8	Generic	
	2H: Detail: Output Packet-Dropped bit in the Port n Error and Status CSR is set upon discard of a packet.	Part 8, Sec. 2.2	Generic	
3.	Error Management Extensions Block Header	Part 8, Sec. 2.3.2.1	Generic	Interop
	3A: Detail: The Error Management Extensions Block Header register is read only.	Part 8, Sec. 2.3.2.1	Generic	
	3B: Detail: The Error Management Extensions Block Header register EF_ID field value is 0x0007.	Part 8, Sec. 2.3.2.1	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	Logical/Transport Layer Error Detect CSR	Part 8, Sec. 2.3.2.2	Generic	Interop
	4A: Detail: The Logical/Transport Layer Error Detect CSR is writable	Part 8, Sec. 2.3.2.2	Generic	
	4B: Detail: The Logical/Transport Layer Error Detect CSR has a reset value of 0	Part 8, Sec. 2.3.2.2	Generic	
	4C: Detail: When an Error Response is received for an IO Logical Layer Request, the IO Error Response bit is set to 1	Part 8, Sec. 2.3.2.2	Generic	
	4D: Detail: When an Error Response is received for an MS Logical Layer Request, the Message Error Response bit is set to 1	Part 8, Sec. 2.3.2.2	Class 3	
	4E: Detail: When an Error Response is received for a GSM Logical Layer Request, the GSM Error Response bit is set to 1	Part 8, Sec. 2.3.2.2	Class 3	
	4F: Detail: When an MESSAGE packet data payload has an invalid size or segment, the Message Error Response bit is set to 1	Part 8, Sec. 2.3.2.2	Class 3	
	4G: Detail: When a packet has illegal field values, but is otherwise supported, the Illegal Transaction Decode bit is set to 1	Part 8, Sec. 2.3.2.2	Generic	
	4H: Detail: When a packet has a destination ID that cannot be accepted by an endpoint, the Illegal Transaction Target Error bit is set to 1	Part 8, Sec. 2.3.2.2	Generic	
	4I: Detail: When a required message request has not been received within the specified time-out interval, the Message Request Time-out bit is set to 1	Part 8, Sec. 1.3.2 Part 8, Sec. 2.3.2.2 Part 6, Sec. 6.5.2.3 Part 6, Sec. 6.6.2.3 Part 4, Sec. 5.5.2.3 Part 4, Sec. 5.6.2.3	Class 3	
	4J: Detail: When a required response has not been received within the specified time-out interval, the Packet Response Time-out bit is set to 1	Part 8, Sec. 2.3.2.2	Class 1, 2, 3	
	4K: Detail: When an unsolicited/unexpected response has been received, the Unsolicited Response bit is set to 1	Part 8, Sec. 2.3.2.2	Generic	
	4L: Detail: When an transaction is received that is not supported in the Destination Operations CAR, the Unsupported Transaction bit is set to 1	Part 8, Sec. 2.3.2.2	Generic	
	4M: Detail: To clear the Logical/Transport Layer Error Detect CSR, write all 0's to the register.	Part 8, Sec. 2.3.2.2	Generic	
	4N: Detail: If all bits are 0 no information is latched in the Logical/Transport Layer Error information registers.	Part 8, Sec. 2.3.2.2	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
4.	**4O: Detail:** If any bit is set in the Logical/Transport Layer Error Detect CSR, and enabled in the Logical/Transport Layer Error Enable CSR, detection of other events will not cause new information to be latched in the Logical/Transport Layer Error information registers.	Part 8, Sec. 1.3.1 Part 8, Sec. 2.3.2.2 Part 8, Sec. 2.3.2.3	Generic	
	4P: Detail: If multiple enabled errors occur during the same clock cycle, multiple bits will be set in the detect register. The contents of the Logical/Transport Layer Capture registers are implementation dependent in this case.	Part 8, Sec. 1.3.1	Generic	
	4Q: Detail: The contents of the Logical/Transport Capture CSRs are valid if the bitwise AND of the Logical/Transport Layer Error Detect CSR and the Logical/Transport Layer Error Detect Enable CSR is not equal to 0.	Part 8, Sec. 1.3.1	Generic	
	4R: Detail: Writing 0 to the Logical/Transport Detect CSR will clear the error detect bits and unlock the register and the Logical/Transport Error Capture CSRs.	Part 8, Sec. 1.3.1	Generic	
5.	Logical/Transport Layer Error Enable CSR	Part 8, Sec. 2.3.2.3	Generic	Interop
	5A: Detail: The Logical/Transport Layer Error Enable CSR is writable	Part 8, Sec. 2.3.2.3	Generic	
	5B: Detail: The Logical/Transport Layer Error Enable CSR has a reset value of 0	Part 8, Sec. 2.3.2.3	Generic	
	5C: Detail: When a bit in the Logical/Transport Layer Error Enable CSR is set to 1, detection of the corresponding event in the Logical/Transport Layer Error Detect CSR will cause the Logical/Transport Layer Error information registers to lock, and all resources held by the transaction are freed.	Part 8, Sec. 1.3.1 Part 8, Sec. 2.3.2.3	Generic	
6.	Logical/Transport Layer High Address Capture CSR	Part 8, Sec. 2.3.2.4	Generic	Interop
	6A: Detail: The Logical/Transport Layer High Address Capture CSR is writable	Part 8, Sec. 2.3.2.4	Generic	
	6B: Detail: The Logical/Transport Layer High Address Capture CSR has a reset value of 0	Part 8, Sec. 2.3.2.4	Generic	
	6C: Detail: When an error is detected in a request packet which is enabled in the Logical/Transport Layer Error Enable CSR, the Logical/Transport Layer High Address Capture CSR is locked with the most significant 32 bits of the address in the erroneous request, for 66 or 50 bit addresses.	Part 8, Sec. 2.3.2.4	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
7.	Logical/Transport Layer Address Capture CSR	Part 8, Sec.2.3.2.5	Generic	Interop
	7A: Detail: The Logical/Transport Layer Address Capture CSR is writable	Part 8, Sec.2.3.2.5	Generic	
	7B: Detail: The Logical/Transport Layer Address Capture CSR has a reset value of 0	Part 8, Sec.2.3.2.5	Generic	
	7C: Detail: When an error in a request packet which is enabled in the Logical/Transport Layer Error Enable CSR is detected, the Logical/Transport Layer Address Capture CSR is locked with the least significant 29 bits of the address and the extended address bits of the address in the erroneous request.	Part 8, Sec.2.3.2.5	Generic	
8.	Logical/Transport Layer Device ID Capture CSR	Part 8, Sec.2.3.2.6	Generic	Interop
	8A: Detail: The Logical/Transport Layer Device ID Capture CSR is writable	Part 8, Sec.2.3.2.6	Generic	
	8B: Detail: The Logical/Transport Layer Device ID Capture CSR has a reset value of 0	Part 8, Sec.2.3.2.6	Generic	
	8C: Detail: When an error which is enabled in the Logical/Transport Layer Error Enable CSR is detected, the Logical/Transport Layer Device ID Capture CSR is locked with the source and destination ID of the erroneous packet.	Part 8, Sec.2.3.2.6	Generic	
9.	Logical/Transport Layer Control Capture CSR	Part 8, Sec.2.3.2.7	Generic	Interop
	9A: Detail: The Logical/Transport Layer Control Capture CSR is writable	Part 8, Sec.2.3.2.7	Generic	
	9B: Detail: The Logical/Transport Layer Control Capture CSR has a reset value of 0	Part 8, Sec.2.3.2.7	Generic	
	9C: Detail: When an error is detected which is enabled in the Logical/Transport Layer Error Enable CSR, the Logical/Transport Layer Control Capture CSR is locked with the FTYPE and Transaction Type of the erroneous packet.	Part 8, Sec.2.3.2.7	Generic	
	9D: Detail: When an error is detected in a Message packet which is enabled in the Logical/Transport Layer Error Enable CSR, the Logical/Transport Layer Control Capture CSR is locked with the Letter, MBox and msgseg of the last Message request packet received for the mailbox which had an error.	Part 8, Sec.2.3.2.7	Class 3	
	9E: Detail: If the situation in the Error Management Checklist Table 1, Item 12 is detected, the Logical/Transport Layer Control Capture CSR contains the 'msg info' field to capture the critical information of the last received (or sent) message segment before the timeout occurred. NOTE: No behavior specified as a response to the timeout.	Part 8, Sec. 1.3.2 Part 8, Sec.2.3.2.7	Class 3	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
10.	Port-write Target deviceID CSR	Part 8, Sec.2.3.2.8	Generic	Interop
	10A: Detail: The Port-write Target deviceID CSR is writable	Part 8, Sec.2.3.2.8	Generic	
	10B: Detail: The Port-write Target deviceID CSR has a reset value of 0	Part 8, Sec.2.3.2.8	Generic	
	10C: Detail: When a port-write is generated due to an enabled error in the Logical/Transport Layer Error Enable CSR or the Port n Error Detect CSR the destination ID in the port-write packet is controlled by the port-write target device-ID CSR.	Part 8, Sec.2.3.2.8	Generic	
	10D: Detail: When a port-write is generated due to an enabled error in the Logical/Transport Layer Error Enable CSR or the Port n Error Detect CSR the TT code in the port-write packet is controlled by the large-transport bit in the Port-write Target device-ID CSR	Part 8, Sec.2.3.2.8	Generic	
11.	Packet time-to-live CSR (Required for Switches, optional for other devices)	Part 8, Sec. 2.3.2.9	Generic	Interop
	11A: Detail: The Packet time-to-live CSR is writable	Part 8, Sec. 2.3.2.9	Generic	
	11B: Detail: The Packet Time-to-Live CSR has a reset value of 0	Part 8, Sec. 2.3.2.9	Generic	
	11C: Detail: The timeout corresponding to the maximum value of the Packet Time-to-Live CSR shall correspond to 100 msec +/- 34 msec.	Part 8, Sec. 2.3.2.9	Generic	
	11D: Detail: No packet will time out when the time-to-live value is 0.	Part 8, Sec. 2.3.2.9	Generic	
	11E: Detail: If a packet is buffered within a switch for longer than the time-to-live value, the packet is dropped.	Part 8, Sec. 2.3.2.9	Generic	
	11F: Detail: When a packet is dropped due to time-to-live expiry, the Output Packet-dropped bit is sent in the Port n Error and Status CSR.	Part 8, Sec. 2.3.2.9	Generic	
	11G: Detail: If a packet remains in a switch longer than the Time-to-Live time specified by the Time-to-Live field of the Packet Time-to-Live CSR, the packet shall be discarded.	Part 8, Sec. 1.2.5 Part 8, Sec. 2.3.2.9	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
12.	Port n Error Detect CSR	Part 8, Sec. 2.3.2.10	Generic	Interop
	12A: Detail: The Port n Error Detect CSR is writable	Part 8, Sec. 2.3.2.10	Generic	
	12B: Detail: The Port n Error Detect CSR has a reset value of 0	Part 8, Sec. 2.3.2.10	Generic	
	12C: Detail: When an S-bit error is detected, the 'Received S-bit error' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12D: Detail: When a control symbol with a bad CRC value (serial) or a true complement mismatch (parallel) is received, the 'Received corrupt control symbol' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12E: Detail: When an acknowledge control symbol with an unexpected ackID is received, the 'Received acknowledge control symbol with unexpected ackID' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12F: Detail: When an packet-not-accepted control symbol is received, the 'Received packet-not-accepted control symbol' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12G: Detail: When an packet with an unexpected ackID is received, the 'Received packet with unexpected ackID' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12H: Detail: When a packet with incorrect CRC is received, the 'Received packet with bad CRC' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12I: Detail: When an packet longer than 276 bytes is received, the 'Received packet exceeds 276 bytes' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12J: Detail: When a link-response is received with an ackID value that is not outstanding, the 'Non-outstanding ackID' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12K: Detail: When an unexpected packet or control symbol was received, the 'Protocol Error' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12L: Detail: Parallel: When the FRAME signal is toggled on a non-32-bit boundary, the 'Delineation Error' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12M: Detail: Serial: When the port receives an unaligned /SC/ or /PD/ or undefined code-group, the 'Delineation Error' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12N: Detail: When an unexpected acknowledge control symbol is received, the 'Unsolicited Acknowledge Control Symbol' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12O: Detail: When an acknowledge or link-response control symbol is not received in the period controlled by the Port Link Timeout Control CSR, the 'Link Timeout' bit field is set to 1	Part 8, Sec. 2.3.2.10	Generic	
	12P: Detail: Bits in the Port n Error Detect CSR are cleared by writing 0 to them.	Part 8, Sec. 2.3.2.10	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
13.	Port n Error Rate Enable CSR	Part 8, Sec. 2.3.2.11	Generic	Interop
	13A: Detail: The Port n Error Rate Enable CSR is writable	Part 8, Sec. 2.3.2.11	Generic	
	13B: Detail: The Port n Error Rate Enable CSR has a reset value of 0	Part 8, Sec. 2.3.2.11	Generic	
	13C: Detail: Error conditions are enabled in the Port n Error Rate Enable CSR by setting the bit corresponding to the specific error condition to 1.	Part 8, Sec. 2.3.2.11	Generic	
	13D: Detail: When an error condition that is enabled in the Port n Error Rate Enable CSR occurs, the error rate counter in the Port n Error Rate Threshold Register increments.	Part 8, Sec. 2.3.2.11	Generic	
14.	Port n Attributes Capture CSR	Part 8, Sec. 2.3.2.12	Generic	Interop
	14A: Detail: The Port n Attributes Capture CSR is writable	Part 8, Sec. 2.3.2.12	Generic	
	14B: Detail: The Port n Attributes Capture CSR has a reset value of 0	Part 8, Sec. 2.3.2.12	Generic	
	14C: Detail: When a packet related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the info type field has a value of 0b00	Part 8, Sec. 2.3.2.12	Generic	
	14D: Detail: When a control symbol related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the info type field has a value of 0b01	Part 8, Sec. 2.3.2.12	Generic	
	14E: Detail: When an implementation specific error condition that is enabled in the Port n Error Rate Enable CSR occurs, the info type field has a value of 0b10	Part 8, Sec. 2.3.2.12	Generic	
	14F: Detail: When an error condition that is enabled in the Port n Error Rate Enable CSR occurs, the ‘error type’ field is set to the bit number in the Port n Error Detect CSR which corresponds to the error condition	Part 8, Sec. 2.3.2.12	Generic	
	14G: Detail: When an error condition that is enabled in the Port n Error Rate Enable CSR occurs, the Port n Error Capture Registers are locked and the Capture Valid Info bit is set in the Port n Error Capture Attributes CSR. In case of multiple detected errors during the same clock cycle one of the errors is reflected in the Error Type field of the Port n Attributes Capture CSR.	Part 8, Sec. 2.3.2.12	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
15.	Port n Packet/Control Symbol Capture 0 CSR	Part 8, Sec. 2.3.2.13	Generic	Interop
	15A: Detail: The Port n Packet/Control Symbol Capture 0 CSR is writable	Part 8, Sec. 2.3.2.13	Generic	
	15B: Detail: The Port n Packet/Control Symbol Capture 0 CSR has a reset value of 0	Part 8, Sec. 2.3.2.13	Generic	
	15C: Detail: When a packet related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the Port n Packet/Control Symbol Capture 0 CSR contains the first 4 bytes of the packet header.	Part 8, Sec. 2.3.2.13	Generic	
	15D: Detail: When a control symbol related error condition that is enabled in the Port n Error Rate Enable CSR occurs, Port n Packet/Control Symbol Capture 0 CSR contains the complete control symbol information.	Part 8, Sec. 2.3.2.13	Generic	
16.	Port n Packet Capture 1 CSR	Part 8, Sec. 2.3.2.14	Generic	Interop
	16A: Detail: The Port n Packet Capture 1 CSR is writable	Part 8, Sec. 2.3.2.14	Generic	
	16B: Detail: The Port n Packet Capture 1 CSR has a reset value of 0	Part 8, Sec. 2.3.2.14	Generic	
	16C: Detail: When a packet related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the Port n Packet Capture 1 CSR contains bytes 4 through 7 of the packet.	Part 8, Sec. 2.3.2.14	Generic	
17.	Port n Packet Capture 2 CSR	Part 8, Sec. 2.3.2.15	Generic	Interop
	17A: Detail: The Port n Packet Capture 2 CSR is writable	Part 8, Sec. 2.3.2.15	Generic	
	17B: Detail: The Port n Packet Capture 2 CSR has a reset value of 0	Part 8, Sec. 2.3.2.15	Generic	
	17C: Detail: When a packet related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the Port n Packet Capture 2 CSR contains bytes 8 through 11 of the packet.	Part 8, Sec. 2.3.2.15	Generic	
18.	Port n Packet Capture 3 CSR	Part 8, Sec. 2.3.2.16	Generic	Interop
	18A: Detail: The Port n Packet Capture 3 CSR is writable	Part 8, Sec. 2.3.2.16	Generic	
	18B: Detail: The Port n Packet Capture 3 CSR has a reset value of 0	Part 8, Sec. 2.3.2.16	Generic	
	18C: Detail: When a packet related error condition that is enabled in the Port n Error Rate Enable CSR occurs, the Port n Packet Capture 3 CSR contains bytes 12 through 15 of the packet.	Part 8, Sec. 2.3.2.16	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
19.	Port n Error Rate CSR	Part 8, Sec. 2.3.2.17	Generic	Interop
	19A: Detail: The Port n Error Rate CSR is writable	Part 8, Sec. 2.3.2.17	Generic	
	19B: Detail: The Port n Error Rate CSR has a reset value of 0x8000_0000	Part 8, Sec. 2.3.2.17	Generic	
	19C: Detail: The Error Rate Bias field in the Port n Error Rate CSR causes the Error Rate Counter field in the Port n Error Rate CSR to decrement at the rate specified in Part 8, Table 2-21	Part 8, Sec. 2.3.2.17	Generic	
	19D: Detail: The Error Rate Counter field in the Port n Error Rate CSR does not warp around to 0 once it achieves its maximum value.	Part 8, Sec. 2.3.2.17	Generic	
	19E: Detail: In the Port n Error Rate CSR, the Error Rate Counter will not reach a value greater than the Error Rate Recovery Field added to the Error Rate Failed Threshold Trigger in the Port n Error Rate Threshold CSR	Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	19F: Detail: The maximum value that the Error Rate Counter field in the Port n Error Rate CSR has attained is captured in the Peak Error Rate field of the Port n Error Rate CSR on the same clock cycle that the Error Rate Counter field achieved the maximum value.	Part 8, Sec. 2.3.2.17	Generic	
	19G: Detail: The Error Rate Counter in the Port n Error Rate CSR increments by 1 for every error which is both detected and enabled in the Port n Error Rate Enable CSR	Part 8, Sec. 2.3.2.11 Part 8, Sec. 2.3.2.17	Generic	

Table 2. Error Management Register Requirements Certification List

Item no.	Compliance item	Specification reference	Device Class (Generic, 1, 2, 3)	Inter-op Item
20.	Port n Error Rate Threshold CSR	Part 8, Sec.2.3.2.18	Generic	Interop
	20A: Detail: The Port n Error Rate Threshold CSR is writable	Part 8, Sec.2.3.2.18	Generic	
	20B: Detail: The Port n Error Rate Threshold CSR has a reset value of 0xFFFF_0000	Part 8, Sec.2.3.2.18	Generic	
	20C: Detail: When the Error Rate Count field in the Port n Error Rate CSR reaches the value programmed in the Error Rate Failed Threshold Trigger field in the Port n Error Rate Threshold CSR, the port behaves as defined in Part 8, Table 1-1 and the Output Failed-encountered bit in the Port n Error and Status CSR shall be set. APort-Failed Event is detected.	Part 8, Sec. 1.2.2 Part 8, Sec. 1.2.3 Part 8, Sec. 1.2.4 Part 8, Sec. 1.4 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	20D: Detail: The Error Rate Count field in the Port n Error Rate CSR reaches the value programmed in the Error Rate Degraded Threshold Trigger field in the Port n Error Rate Threshold CSR, a Port-degraded Event is detected.	Part 8, Sec. 1.2.2 Part 8, Sec. 1.2.3 Part 8, Sec. 1.4 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	20E: Detail: If the Stop-on-Port-Failed-Encountered Enable bit is 0, and the Drop Packet Enable bit is 0, when the Port Failed Threshold is reached the port shall continue to attempt to transmit packets to the connected device.	Part 8, Sec. 1.2.4 Part 8, Sec. 2.2 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	20F: Detail: For switch devices, if the Stop-on-Port-Failed-Encountered Enable bit is 0, and the Drop Packet Enable bit is 1, when the Port Failed Threshold is reached the port shall drop packets which receive a Packet-not-Accepted control symbol.	Part 8, Sec. 1.2.4 Part 8, Sec. 2.2 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	20G: Detail: If the Stop-on-Port-Failed-Encountered Enable bit is 1, and the Drop Packet Enable bit is 0, when the Port Failed Threshold is reached the port shall stop attempting to transmit packets to the connected device. The output port will congest.	Part 8, Sec. 1.2.4 Part 8, Sec. 2.2 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	
	20H: Detail: If the Stop-on-Port-Failed-Encountered Enable bit is 1, and the Drop Packet Enable bit is 1, when the Port Failed Threshold is reached the port shall discard all output packets.	Part 8, Sec. 1.2.4 Part 8, Sec. 2.2 Part 8, Sec. 2.3.2.17 Part 8, Sec. 2.3.2.18	Generic	