RapidIO Trade Association

Suite 325, 3925 W. Baker Lane

Austin, TX 78759

512-305-0070 Tel.

512-305-0009 FAX.

TWG First Showing

Item 12-08-00002.000

Subject: Revision 3.0 specification Register Changes Proposal

Background: After working with the D3.0.8 spec for a while, there have been some suggestions for improvements/modifications to the registers.

Contributors: Barry Wood, IDT

Comment Expiration Date: None

Distribution: RapidIO TA Technical Working Group members

1.0 Discussion

The per-lane registers are currently a bit complicated, as the Lane n Status 1 register has different formats depending on the IDLE sequence in use. To simplify this situation a new register format is proposed which combines the two register formats.

The Lane n Status 2 CSR and Lane n Status 3 CSR need to be updated to reflect the current definition of the Status Control codeword/ordered sequence. It is further proposed that the Lane n Status 3 CSR capture the 9 "reserved" bits in the Status/Control Ordered Sequence for future proofing.

1.1 Proposed Change to Lane n Status 1 CSR Definition

Change the definition of the Lane N Status 1 CSR from:

"

1.1.0.1 Lane *n* Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4)

These registers shall be implemented if the lane supports the IDLE2 or IDLE3 sequence.

When the lane is operating with IDLE2, these registers contain information about the connected port that is collected from the CS markers and CS fields of the IDLE2 sequence received by the local lane *n* receiver. Only information from error free CS markers and CS fields shall be reported in these registers. When IDLE2 information is received, the bits and bit fields of this registers shall be as defined in Table 1-1.

When the lane is operating with IDLE3, these registers contain information regarding the lanes' initialization and electrical status. Only information from error-free Control/Status ordered sequences shall be reported in this register. When IDLE3 information is received, the bits and bit fields of these registers shall be as defined in Table 1-2.

Unless otherwise specified, all bits in these registers are read-only.

Table 1-1. Bit Settings for Lane *n* Status 1 CSRs For IDLE2

Bit	Name	Reset Value	Description
0	IDLE2 received	0b0	This bit indicates whether an IDLE2 has been received by the lane since the bit was last reset. The bit is R/W. This bit can be reset by writing the bit with the value 0b1. Writing the bit with the value 0b0 does not change the value of the bit. 0b0 - No IDLE2 sequence has been received since the bit was last reset 0b1 - An IDLE2 sequence has been received at some time since the bit was last reset
1	IDLE2 information current	0b0	This bit indicates whether the information in this register that is collected from the received IDLE2 sequence is current. When asserted, this bit indicates that the information is from the last IDLE2 CS Marker and CS Field that were received by the lane without detected errors, and that the lane's lane_sync signal has remained asserted since the last CS Marker and CS Field were received. 0b0 - The IDLE2 information is not current 0b1 - The IDLE2 information is current
2	Values changed	0b1	This bit indicates whether the values of any of the other 31 bits in this register have changed since the register was last read. This bit is reset when the register is read. 0b0 - The values have not changed 0b1 - One or more values have changed
3	Implementation defined		Implementation defined
4	Connected port lane receiver trained		Connected port lane receiver trained 0b0 - Receiver not trained 0b1 - Receiver trained
5-7	Received port width		Received port width 0b000 - 1 lane 0b001 - 2 lanes 0b010 - 4 lanes 0b011 - 8 lanes 0b100 - 16 lanes 0b101-0b111 - Reserved
8-11	Lane number in connected port		The number of the lane (0-15) within the connected port 0b0000 - Lane 0 0b0001 - Lane 1 ... 0b1111 - Lane 15
12-13	Connected port transmit emphasis Tap(-1) status		Tap(-1) status 0b00 - Tap(-1) not implemented 0b01 - Tap(-1) at minimum emphasis 0b10 - Tap(-1) at maximum emphasis 0b11 - Tap(-1) at intermediate emphasis setting
14-15	Connected port transmit emphasis Tap(+1) status		Tap(+1) status 0b00 - Tap(+1) not implemented 0b01 - Tap(+1) at minimum emphasis 0b10 - Tap(+1) at maximum emphasis 0b11 - Tap(+1) at intermediate emphasis setting

Bit	Name	Reset Value	Description
16	Connected port scrambling/descrambling enabled		Connected port scrambling/descrambling 0b0 - Scrambling/descrambling not enabled 0b1 - Scrambling/descrambling enabled
17-31	—		Reserved

Table 1-2. Bit Settings for Lane *n* Status 1 CSRs for IDLE3

Bit	Name	Reset Value	Description
0	Lane Info received	0b0	This bit indicates whether a valid Status/Control Ordered Sequence has been received by the lane since the bit was last reset. The bit is R/W. This bit can be reset by writing the bit with the value 0b1. Writing the bit with 0b0 does not change its value. 0b0 - No Status/Control Ordered Sequence has been received since the bit was last reset 0b1 - A Status/Control Ordered Sequence has been received since the bit was last reset
1	Lane Info current	0b0	This bit indicates whether the information in this register that is collected from the received Status/Control Ordered Sequence is current. When asserted, this bit indicates that the information is from the last Status/Control Ordered Sequence that was received by the lane without detected errors, and that the lane's lane_sync signal has remained asserted since the last Status/Control Ordered Sequence was received. 0b0 - The Status/Control Ordered Sequence information is not current 0b1 - The Status/Control Ordered Sequence information is current
2	Values changed	0b1	This bit indicates whether the values of any of the status bits in the Lane n Status 2 or 3 registers have changed since this register was last read. This bit is reset when the register is read. 0b0 - The values have not changed 0b1 - One or more values have changed
3	Loss of lane sync	0b0	This bit indicates that the receiver is unable to track the !Type and Type bits at the beginning of each codeword. 0b0 - The lane is receiving valid code groups 0b1 - The lane is not receiving valid code groups
4	Loss of signal	0b0	When set, this bit shall indicate that at least one of the following has occurred: • The receiver has not received a valid control symbol in 2048 columns • The "signal_detected" indication is de-asserted • A Status/Control codeword was received that indicates the link partner's transmitter is entering the silent state, or that the transmitter for this lane is disabled • Lane synchronization was lost • ?? UPDATE when lane sync showing is concluded 0b0 - The lane is receiving valid Status/Control codewords b01 - The lane is not receiving valid Status/Control codewords

Bit	Name	Reset Value	Description
5-6	DME Training State	0b00	For Baud Rate Class 1 and 2 operation, this field is reserved. For Baud Rate Class 3 operation, this field shall indicate the status of DME training for this lane. This field shall be encoded as follows: 0b00 - Lane is untrained, or is in the process of training 0b01 - Training has failed 0b10 - Training completed successfully 0b11 - Reserved For Baud Rate Class 1 and 2 operation, this field is reserved.
7-8	SC Training State	0b00	For Baud Rate Class 1 and 2 operation, this field is reserved. For Baud Rate Class 3 operation, this field shall indicate the status of SC training for this lane. This field shall be encoded as follows: 0b00 - Lane is untrained, or in the process of training 0b01 - Training has failed 0b10 - Training completed successfully 0b11 - Lane has detected degraded operation and is retraining
9-31	—		Reserved

“

to:

“

1.1.0.2 “Lane *n* Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4)

The Lane n Status 1 CSRs shall be implemented if the lane supports the IDLE2 or IDLE3 sequence.

When the lane is operating with IDLE2, this register contains information about the connected port that is collected from the CS markers and CS fields of the IDLE2 sequence received by the local lane *n* receiver. Only information from error free CS markers and CS fields shall be reported in these registers.

When the lane is operating with IDLE3, this register contains information regarding the lanes’ initialization and electrical status. Only information from error-free Status/Control ordered sequences shall be reported in this register.

Unless otherwise specified, all bits in these registers are read-only.

Table 1-3. Bit Settings for Lane *n* Status 1 CSRs

Bit	Name	Reset Value	Description
0	IDLE received	0b0	This bit indicates whether valid information has been received by the lane since the bit was last reset. Information is accepted from a IDLE2 Control and Status Field or Field Marker, or a valid IDLE3 Status Control Ordered Sequences. The bit is R/W. This bit can be reset by writing the bit with the value 0b1. Writing the bit with the value 0b0 does not change the value of the bit. 0b0 - No information has been received since the bit was last reset 0b1 - New information has been received at some time since the bit was last reset
1	IDLE information current	0b0	This bit indicates whether the information in this register that is collected from the received IDLE sequence is current. When asserted, this bit indicates that the information is from the last IDLE2 CS Marker and CS Field, or from an IDLE3 Status Control Ordered Sequence that was received by the lane without detected errors, and that the lane's lane_sync signal has remained asserted since the last information was received. 0b0 - The IDLE information is not current 0b1 - The IDLE information is current
2	Values changed	0b1	When the lane is operating using IDLE2, this bit indicates whether the values of any of the other 31 bits in this register have changed since the register was last read. When the lane is operating using IDLE3, this bit indicates whether the values of the IDLE3 fields in this register, or if any fields in the Lane n Status 2 CSR and the Lane n Status 3 CSR have changed. This bit is reset when the Lane n Status 1 CSR is read. 0b0 - The values have not changed 0b1 - One or more values have changed
3	Implementation defined	0b0	Implementation defined
4	IDLE2 Connected port lane receiver trained	0b0	IDLE2 Connected port lane receiver trained 0b0 - Receiver not trained 0b1 - Receiver trained Captured from the IDLE2 Command and Status Field "Receiver Trained" bit.
5-7	IDLE2 Received port width		IDLE2 Received port width 0b000 - 1 lane 0b001 - 2 lanes 0b010 - 4 lanes 0b011 - 8 lanes 0b100 - 16 lanes 0b101-0b111 - Reserved Captured from the IDLE2 Command and Status Marker "Active Port Width Field"
8-11	IDLE2 Lane number in connected port		The number of the lane (0-15) within the connected port 0b0000 - Lane 0 0b0001 - Lane 1 ... 0b1111 - Lane 15 Captured from the IDLE2 Command and Status Marker "Lane Number Field"

Bit	Name	Reset Value	Description
12-13	IDLE2 Connected port transmit emphasis Tap(-1) status		Tap(-1) status 0b00 - Tap(-1) not implemented 0b01 - Tap(-1) at minimum emphasis 0b10 - Tap(-1) at maximum emphasis 0b11 - Tap(-1) at intermediate emphasis setting Captured from the IDLE2 Command and Status Field "Tap(-1) Status" bit.
14-15	IDLE2 Connected port transmit emphasis Tap(+1) status		Tap(+1) status 0b00 - Tap(+1) not implemented 0b01 - Tap(+1) at minimum emphasis 0b10 - Tap(+1) at maximum emphasis 0b11 - Tap(+1) at intermediate emphasis setting Captured from the IDLE2 Command and Status Field "Tap(+1) Status" bit.
16	IDLE2 Connected port scrambling/descrambling enabled		IDLE2 Connected port scrambling/descrambling 0b0 - Scrambling/descrambling not enabled 0b1 - Scrambling/descrambling enabled Captured from the IDLE2 Command and Status Field "Data scrambling/descrambling enabled" bit.
17	IDLE3 Loss of Signal		When set, this bit shall indicate that at least one of the following has occurred: • The receiver has not received a valid control symbol in 2048 columns • The "signal_detected" indication is de-asserted • A Status/Control codeword was received that indicates the link partner's transmitter is entering the silent state, or that the transmitter for this lane is disabled • Lane synchronization was lost 0b0 - The lane is receiving valid Status/Control codewords b01 - The lane is not receiving valid Status/Control codewords
18-19	IDLE3 Training Type	0b00	This field indicates the type of adaptive equalization being performed by the lane 0b00 = DME training 0b01 = CW training 0b10 = CW retraining 0b11 = training completed
20-21	IDLE3 DME Training State	0b00	For Baud Rate Class 1 and 2 operation, this field is reserved. For Baud Rate Class 3 operation, this field shall indicate the status of DME training for this lane. This field shall be encoded as follows: 0b00 - Lane is untrained, or is in the process of training 0b01 - Training has failed 0b10 - Training completed successfully 0b11 - Reserved For Baud Rate Class 1 and 2 operation, this field is reserved.
22-23	IDLE3 SC Training State	0b00	For Baud Rate Class 1 and 2 operation, this field is reserved. For Baud Rate Class 3 operation, this field shall indicate the status of SC training for this lane. This field shall be encoded as follows: 0b00 - Lane is untrained, or in the process of training 0b01 - Training has failed 0b10 - Training completed successfully 0b11 - Lane has detected degraded operation and is retraining

Bit	Name	Reset Value	Description
24-25	IDLE3 SC Retraining State	0b00	For Baud Rate Class 1 and 2 operation, this field is reserved. For Baud Rate Class 3 operation, this field shall indicate the status of SC retraining for this lane. This field shall be encoded as follows: 0b00 - Retraining is not active 0b01 - Retraining has failed 0b10 - Retraining completed successfully 0b11 - Lane is retraining
26-31	—		Reserved

“

1.2 Proposed Change to Lane n Status 2 CSR Definition

Change the definition of the Lane N Status 2 CSR from:

“

1.2.0.1 Lane *n* Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8)

These registers shall be implemented if the lane supports IDLE3. These registers contain information from received Status/Control ordered sequences. The bits and bit fields of these registers shall be as defined in Table 1-4. Only information from error-free Status/Control ordered sequences, shall be reported in these registers. Unless otherwise specified, all bits in these registers are read-only.

Table 1-4. Bit Settings for Lane *n* Status 2 CSRs

Bit	Name	Reset Value	Description
0-7	LP Port Number	All 0’s	Number of the link partner’s port that is connected to this lane. It should match what is in the Lane n Status 0 CSR [Port Number] field on the link partner.
8-11	LP Lane Number	All 0’s	Number of the link partner’s lane connected to this lane. It should match what is in the Lane n Status 0 CSR [Lane Number] field on the link partner.
12	LP Port Initialized	0b0	Indicates whether the link partner’s port has completed initialization. Matches the port_initialized state machine signal. 0b0 - Port in not initialized 0b1 - Port is initialized
13	LP Asymmetric Mode Enabled	0b0	The status of support for Asymmetric Operation in the link partner. 0b0 - Asymmetric mode disabled 0b1 - Asymmetric mode enabled

Bit	Name	Reset Value	Description
14-17	LP Receive width	0b000	The width at which the Link Partner port is currently receiving control symbols and packets. 0b0000 - none 0b0001 - 1x mode 0b0010 - 2x mode 0b0011 - 4x mode 0b0100 - 8x mode 0b0101 - 16x mode 0b0110 - 0b1101 - reserved 0b1110 - 1x mode, lane 1 0b1111 - 1x mode, lane 2
18-20	LP Receive lanes ready	0b000	Indicates the lanes being received by the port for which lane_ready is asserted. 0b000 - No lanes ready 0b001 - lane_ready[0] 0b010 - lane_ready[0] & lane_ready[1] 0b011 - lane_ready[0] & lane_ready[1] &... & lane_ready[3] 0b100 - lane_ready[0] & lane_ready[1] &... & lane_ready[7] 0b101 - lane_ready[0] & lane_ready[1] &... & lane_ready[15] 0b110–0b111 - reserved
21-23	Change receiver width command	0b000	The port receiving the command shall attempt to switch to the receive width specified in the command. 0b000 - hold current receive width 0b001 - receive in 1x mode 0b010 - receive in 2x mode 0b011 - receive in 4x mode 0b100 - receive in 8x mode 0b101 - receive in 16x mode 0b110–0b111 - reserved
24	LP change receiver width command acknowledge		Receive width command ACK 0b0 - No command status 0b1 - Command executed
25	LP change receiver width command negative acknowledge		Receive width command NACK 0b0 - No command status 0b1 - Command not executed
26-28	Transmit width request		A request that the port receiving this field change its transmit width to the width specified in the request. 0b000 - no request (hold current transmit width) 0b001 - request transmit 1x mode 0b010 - request transmit 2x mod 0b011 - request transmit 4x mode 0b100 - request transmit 8x mode 0b101 - request transmit 16x mode 0b110–0b111 - reserved
29	LP Transmit width request pending	0b0	Indicates that the link partner has received the transmitter width request sent by this device and is processing it. 0b0 - No request pending 0b1 - Request pending

Bit	Name	Reset Value	Description
30	Transmit SC-sequences	0b0	Request to transmit SC-sequence at least every 128 codewords per lane. 0b0 - no additional SC-sequence transmission rate requirement 0b1 - required minimum SC-sequences transmission rate is once every 128 codewords per lane.
31	—		Reserved

“

to:

“

1.2.0.2 “Lane *n* Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8)

These registers shall be implemented if the lane supports IDLE3. These registers contain information from received Status/Control ordered sequences. The bits and bit fields of these registers shall be as defined in Table 1-5. Only information from error-free Status/Control ordered sequences, shall be reported in these registers. Unless otherwise specified, all bits in these registers are read-only.

Table 1-5. Bit Settings for Lane *n* Status 2 CSRs

Bit	Name	Reset Value	Description
0-7	LP Port Number	All 0’s	Number of the link partner’s port that is connected to this lane. It should match what is in the Lane n Status 0 CSR [Port Number] field on the link partner.
8-11	LP Lane Number	All 0’s	Number of the link partner’s lane connected to this lane. It should match what is in the Lane n Status 0 CSR [Lane Number] field on the link partner.
12	Remote training support	0	Indicates whether the port supports control of its per lane transmit equalization by the lane receivers in the connected port. 0b0 - The port does not support control of its transmit equalization by the connected port. 0b1 - The port supports control of its transmit equalization by the connected port.
13	Retraining enabled	0	Indicates whether the port is allowed to enter retraining mode, based on the register value of the “10G Retraining Enable” field described in Section 7.6.10. The value of this bit shall be the same as the state variable retrain_en.
14	Asymmetric mode enabled	0	Indicates whether the port is allowed to enter asymmetric mode, based on the register value of the “Asymmetric modes enabled” field described in Section 7.6.8. 0b0 - Asymmetric mode is not enabled 0b1 - Asymmetric mode is enabled

Bit	Name	Reset Value	Description
15	LP Port Initialized	0b0	Indicates whether the link partner's port has completed initialization. Matches the port_initialized state machine signal. 0b0 - Port in not initialized 0b1 - Port is initialized
16	Transmit 1x mode	0b0	Transmit 1x mode Indicates when the port is transmitting in 1x symmetric mode. 0b0 - The port is not transmitting in 1x mode. The state machine variable max_width != 1x. 0b1 - The port is transmitting in 1x symmetric mode. The state machine variable max_width = 1x.
17-19	LP Receive width	0b000	The width at which the Link Partner port is currently receiving control symbols and packets. 0b0000 - none 0b0001 - 1x mode 0b0010 - 2x mode 0b0011 - 4x mode 0b0100 - 8x mode 0b0101 - 16x mode 0b0110 - 0b1101 - reserved 0b1110 - 1x mode, lane 1 0b1111 - 1x mode, lane 2
20-22	LP Receive lanes ready	0b000	Indicates the lanes being received by the port for which lane_ready is asserted. 0b000 - No lanes ready 0b001 - lane_ready[0] 0b010 - lane_ready[0] & lane_ready[1] 0b011 - lane_ready[0] & lane_ready[1] &... & lane_ready[3] 0b100 - lane_ready[0] & lane_ready[1] &... & lane_ready[7] 0b101 - lane_ready[0] & lane_ready[1] &... & lane_ready[15] 0b110–0b111 - reserved
23	Lane trained	0b0	Lane trained Indicates the training status of the lane. The value and meaning of this bit transmitted on lane k shall be the same as that of the port's state machine variable lane_trained[k]
24-26	Change receiver width command	0b000	The port receiving the command shall attempt to switch to the receive width specified in the command. 0b000 - hold current receive width 0b001 - receive in 1x mode 0b010 - receive in 2x mode 0b011 - receive in 4x mode 0b100 - receive in 8x mode 0b101 - receive in 16x mode 0b110–0b111 - reserved
27	LP change receiver width command acknowledge		Receive width command ACK 0b0 - No command status 0b1 - Command executed

Bit	Name	Reset Value	Description
28	LP change receiver width command negative acknowledge		Receive width command NACK 0b0 - No command status 0b1 - Command not executed
29-31	Transmit width request		A request that the port receiving this field change its transmit width to the width specified in the request. 0b000 - no request (hold current transmit width) 0b001 - request transmit 1x mode 0b010 - request transmit 2x mod 0b011 - request transmit 4x mode 0b100 - request transmit 8x mode 0b101 - request transmit 16x mode 0b110–0b111 - reserved

“

1.3 Proposed Change to Lane n Status 3 CSR Definition

Change the definition of the Lane N Status 3 CSR from:

1.3.0.1 “Lane *n* Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC)

These registers shall be implemented if the lane supports the IDLE3 sequence. These registers contain information from received Status/Control ordered sequences. The bits and bit fields of these registers shall be as defined in Table 1-6. Only information from error free Status/Control ordered sequences shall be reported in these registers. Unless otherwise specified, all bits in these registers are read-only. ?? FIXME: Update when IDLE3 SC ordered sequence content are finalized.

Table 1-6. Bit Settings for Lane *n* Status 3 CSRs

Bit	Name	Reset Value	Description
0-4	Transmit FIR filter tap number	0b00000	When the transmit-emphasis update command is FIR tap specific, this field contains the FIR tap number to which the tap specific command shall be applied. The tap number is encoded as a signed 2's complement 5-bit integer. 0b00000 - Tap 0 0b00001 - Tap +1 0b00010 - Tap +2 ------ 0b01110 - Tap +14 0b01111 - Tap +15 0b10000 - Tap -16 0b10001 - Tap -15 ------ 0b11110 - Tap -2 0b11111 - Tap -1
5-6	Transmit emphasis update command	0b00	Command to change or retain the emphasis setting the tap indicated by the "Transmit FIR filter tap number" of the specified tap. 0b00 - hold 0b01 - decrease emphasis by one step 0b10 - increase emphasis by one step 0b11 - reserved
7-8	LP Transmit emphasis status	0b00	Transmit emphasis status for the tap encoded as: 0b00 - not implemented 0b01 - at minimum emphasis 0b10 - at maximum emphasis 0b11 - at intermediate emphasis
9-31	Reserved	---	

"

to:

1.3.0.2 "Lane *n* Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC)

These registers shall be implemented if the lane supports the IDLE3 sequence. These registers contain information from received Status/Control ordered sequences. The bit fields of these registers shall be as defined in Table 1-7. Only information from error free Status/Control ordered sequences shall be reported in these registers. Unless otherwise specified, all bits in these registers are read-only.

Table 1-7. Bit Settings for Lane *n* Status 3 CSRs

Bit	Name	Reset Value	Description
0	LP Transmit width request pending	0b0	Indicates that the link partner has received the transmitter width request sent by this device and is processing it. 0b0 - No request pending 0b1 - Request pending
1	Transmit SC-sequences	0b0	Request to transmit SC-sequence at least every 128 codewords per lane. 0b0 - no additional SC-sequence transmission rate requirement 0b1 - required minimum SC-sequences transmission rate is once every 128 codewords per lane.
2-5	Transmit equalizer tap	0b0000	When the transmit equalizer command is tap specific, this field contains the number of the equalizer tap to which the tap specific command shall be applied. The tap number is encoded as a signed 2's complement 4-bit integer. 0b0000 - Tap 0 0b0001 - Tap +1 0b0010 - Tap +2 0b0011 - Tap +3 0b0100 - Tap +4 0b0101 - Tap +5 0b0110 - Tap +6 0b0111 - Tap +7 0b1000 - Tap -8 0b1001 - Tap -7 0b1010 - Tap -6 0b1011 - Tap -5 0b1100 - Tap -8 0b1101 - Tap -3 0b1110 - Tap -2 0b1111 - Tap -1
6-8	Transmit equalizer command	0b000	Transmit equalizer command 0b000 - Hold/No command 0b001 - Decrement (make more negative by one step) the coefficient of the specified tap. 0b010 - Increment (make more positive by one step) the coefficient of the specified tap. 0b011-0b100 - Reserved 0b101- Initialize - Set the tap coefficients to their INITIALIZE state as defined Clause 72.6.10.4.2 of IEEE Standard 802.3-2008 (part 5) 0b110 - Preset coefficients - Set the coefficient of tap 0 to its maximum value and the coefficients of all other taps to 0 as specified in Clause 72.6.10.4.1 of IEEE Standard 802.3-2008 (part 5). 0b111 - Indicate specified tap implementation status

Bit	Name	Reset Value	Description
9-11	Transmit equalizer status	0b000	Transmit equalizer status 0b000 - Not updated - No command is pending or the status of the current command has not been determined. 0b001 - Updated - The tap specific command has been executed and the tap is at neither its minimum nor maximum value. 0b010 - Minimum - Either the tap specified tap decrement command has been executed and the tap is now at its minimum value or the specified tap was already at its minimum value. 0b011 - Maximum - Either the tap specific tap increment command has been executed and the tap is now at its maximum value or the specified tap was already at it maximum value. 0b100 - Preset or Initialize command executed. 0b101 - Reserved 0b110 - Specified tap not implemented 0b111 - Specified tap implemented
12	Retrain grant	0b0	When the Status/Control control codeword is formed, the value of this bit shall be the same as the value of the port's state machine variable retrain_grnt.
13	Retrain ready	0b0	When the Status/Control control codeword is formed, the value of this bit shall be the same as the value of the port's state machine variable retrain_ready.
14	Retraining	0b0	When the Status/Control control codeword is formed, the value of this bit shall be the same as the value of the port's state machine variable retraining.
15	Port Entering Silence	0b0	0b0 - The port is transmitting normally 0b1 - All lanes of the port are going to enter the Silence state
16	Lane Entering Silence	0b0	0b0 - The lane is transmitting normally 0b1 - The lane is going to enter the Silence state based on asymmetric mode operation
17-25	Status Control Ordered Sequence Reserved Bits	0b0_0000_0000	Captures bit 49-57 of the Status_control field content. This information is currently reserved in the RapidIO Interconnect Specification (Revision 3.0)
26-31	Reserved	---	

"