RapidIO™ Interconnect Specification Foreword

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Chapter 1 Foreword

1.1 Introduction

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1.2 Definitions

The RapidIO specification was developed to allow different, in some cases competing, vendors to develop RapidIO technology that can be integrated into an efficient, robust, high-performance system. The RapidIO specification uses specific terms for the behaviors required to reach and maintain that objective:

- **“Compliant”:** A correct implementation of the implemented features of the RapidIO specification.
- **“Required”:** Behavior that must be present for a device to be compliant to the RapidIO specification.
- **“Optional”:** An implementation may or may not implement optional functionality. If the optional functionality is implemented, it shall be implemented per specification.
- **“Shall”, “Must”:** Occur in definitions of requirements.
- **“Shall not”, “must not”:** Occur in definitions of requirements phrased such that conditions or behaviors never occur.
- **“Should”, “should not”:** Occur in definitions of recommended behavior that maintains the quality of the ecosystem.
- **“May”:** Defines an allowable, possibly optional, behavior. Compliant devices must handle all allowable behaviors.
- **“Reserved”:** Generally applies to bits within packet formats and registers. Compliant implementations shall transmit reserved bits as 0. Reserved bits shall not affect compliant implementations behavior. Reserved bits may be defined in future versions of the RapidIO specification.

- **“Implementation Specific bit(s)/value(s)”:** The bit(s)/values may be used in an implementation specific manner by a vendor. Other vendors must treat these values as “Reserved”. System integrators shall not assume that these bits/values control the same functionality on different devices. Transmitting and receiving implementation specific bits/values shall be disabled after reset.
- **“Implementation specific behavior”:** Members agree that the behavior does not affect the quality of the ecosystem, and so there are no requirements for this behavior.

Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this specification.

A

AC Coupling. A method of connecting two devices together that does not pass DC.

Address collision. An address based conflict between two or more cache coherence operations when referencing the same coherence granule.

Agent. A processing element that provides services to a processor.

ANSI. American National Standards Institute.

Application programming interface (API.). A standard software interface that promotes portability of application programs across multiple devices.

Associate, Association. A defined relationship between a destination ID and a group of end point devices, or, in a switch, a defined relationship between a destination ID and a multicast mask.

Asychronous transfer mode (ATM). A standard networking protocol which dynamically allocates bandwidth using a fixed-size packet.

B

Big-endian. A byte-ordering method in memory where the address n of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

Block flush. An operation that returns the latest copy of a block of data from caches within the system to memory.

Bridge. A processing element that connects one computer bus to another, allowing a processing element on one bus to access an processing element on the other.

Broadcast. The concept of sending a packet to all processing elements in a system.

Bus-based snoopy protocol. A broadcast cache coherence protocol that assumes that all caches in the system are on a common bus.

Byte. An 8-bit unit of information. Each bit of a byte has the value 0 or 1.

C

Cache coherence. TBD KENT.

Cache coherent-non uniform memory access (CC-NUMA). A cache coherent system in which memory accesses have different latencies depending upon the physical location of the accessed address.

Cache line. A contiguous block of data that is the standard memory access size for a processor within a system.

Cache paradox. A circumstance in which the caches in a system have an undefined or disallowed state for a coherence granule, for example, two caches have the same coherence granule marked “modified”.

Cache. High-speed memory containing recently accessed data and/or instructions (subset of main memory) associated with a processor

Capability registers (CARs). A set of read-only registers that allows a processing element to determine another processing element’s capabilities.

Castout operation. An operation used by a processing element to relinquish its ownership of a coherence granule and return it to home memory.

CCITT. Consultive Communication for International Telegraph and Telephone.

CCP. (Congestion Control Packet). A packet sent from the point of congestion in the fabric back to the source endpoint of particular flows instructing the source to either turn on or off the flow.

Class of service (cos) a term used to describe different treatment (quality of service) for different data streams. Support for class of service is provided by a class of service field in the data streaming protocol. The class of service field is used in the virtual stream ID and in identifying a virtual queue.

Code-group. A 10-bit entity produced by the 8b/10b encoding process and the input to the 8b/10b decoding process.

Codeword. A 67-bit entity produced by the 64b/67b encoding process and the input to the 64b/67b decoding process.

Coherence domain. A logically associated group of processing elements that participate in the globally shared memory protocol and are able to maintain cache coherence among themselves.

Coherence granule. A contiguous block of data associated with an address for the purpose of guaranteeing cache coherence.

Command and status registers (CSRs). A set of registers that allow a processing element to control and determine the status of another processing element's internal hardware.

Command and status registers (CSRs). A set of registers that allows a processing element to control and determine the status of another processing element's internal hardware.

Conduit. A bidirectional data transfer mechanism consisting of two streams or virtual streams, one for communication in each direction.

Congestion. A condition found in output ports of switch and bridge elements characterized by excessive packet buildup in the buffer, when packet entry rate into the buffer exceeds packet exit rate for a long enough period of time.

Continuous Transmission (CT). A mode of packet transmission that allows some packet loss to minimize latency by not retransmitting packets.

Control symbol. A quantum of information transmitted between two linked devices to manage packet flow between the devices.

Controlled Flow List. A memory structure associated with controlling elements which holds a list of currently controlled flows, used by the element to turn back on controlled flows.

Conveyance. A communication channel, e.g. mailbox, stream, shared memory mechanism, etc.

CRC. Cyclic redundancy code

CRF. Critical Request Flow. TBD KENT.

D

Deadlock. A situation in which two processing elements that are sharing resources prevent each other from accessing the resources, resulting in a halt of system operation.

Deferred or delayed transaction. The process of the target of a transaction capturing the transaction and completing it after responding to the source with a retry.

Degraded threshold. Bits 8-15 of the Port n Error Rate Threshold CSR. An application-specific level that indicates an unacceptable error rate resulting in degraded throughput, when equal to the error rate count.

Delayed transaction. The process of the target of a transaction capturing the transaction and completing it after responding to the source with a retry.

Destination. The termination point of a packet on the RapidIO interconnect, also referred to as a target.

Device ID. The identifier of a processing element connected to the RapidIO interconnect.

Device. A generic participant on the RapidIO interconnect that sends or receives RapidIO transactions, also called a processing element.

Direct Memory Access (DMA). The process of accessing the address space of a processing element by specifying the address directly.

Discovery. The passive exploration of a RapidIO network fabric. This process involves walking an already enumerated RapidIO fabric to determine network topology and resource allocations.

Distributed memory. System memory that is distributed throughout the system, as opposed to being centrally located.

Domain. A logically associated group of processing elements.

Doorbell. A port on a device that is capable of generating an interrupt to a processor.

Double word. An eight-byte quantity.

Egress. Egress is the device or node where traffic exits the system. The egress node also becomes the destination for traffic out of the RapidIO fabric. The terms egress and destination may or may not be used interchangeably when considering a single end to end connection.

EMI. Electromagnetic Interference.

End point device. A processing element that contains end point functionality.

End point free device. A processing element that does not contain end point functionality.

End point/Endpoint. A processing element that is the source or destination of transactions through a RapidIO fabric.

Enumeration. The active exploration of a RapidIO network fabric. This process involves configuring device identifiers and maintaining proper host locking.

Ethernet. A common local area network (LAN) technology

Exclusive. A processing element has the only cached copy of a sharable coherence granule. The exclusive state allows the processing element to modify the coherence granule without notifying the rest of the system.

External processing element. A processing element other than the processing element in question.

Fabric. A series of interconnected switch devices, typically used in reference to a switch fabric.

Failed threshold. Bits 0-7 of the Port n Error Rate Threshold CSR. An application-specific level that indicates an error rate due to a broken link, when equal to the error rate count.

Field or Field name. A sub-unit of a register, where bits in the register are named and defined.

FIFO. First in, first out.

FlowID. TBD KENT.

Flush operation. An operation used by a processing element to return the ownership and current data of a coherence granule to home memory

Full-duplex. Data can be transmitted in both directions between connected processing elements at the same time.

Globally shared memory (GSM). Cache coherent system memory that can be shared between multiple processors in a system.

Half-word. A two-byte quantity.

Hardware abstraction layer (HAL). A a standard software interface to device-specific hardware resources.

Header. Typically the first few bytes of a packet, containing control information.

Home memory. The physical memory corresponding to the physical address of a coherence granule

Host. A processing element responsible for exploring and initializing all or a portion of a RapidIO based system

Hot-extraction. Hot-extraction is the removal of a processing element from a powered-up system.

Hot-insertion. Hot-insertion is the insertion of a processing element into a powered-up system.

I/O read operation. An operation used by an I/O processing element to obtain a globally shared copy of a coherence granule without disturbing the coherence state of the granule

I/O. Input-output.

I2O. Intelligent I/O architecture specification.

Ingress. Ingress is the device or node where traffic enters the system. The ingress node also becomes the source for traffic into the RapidIO fabric. The terms ingress and source may or may not be used interchangeably when considering a single end to end connection.

Initiator. The origin of a packet on the RapidIO interconnect, also referred to as a source.

Instruction cache invalidate operation. An operation that is used if the instruction cache coherence must be maintained by software.

Instruction cache. High-speed memory containing recently accessed instructions (subset of main memory) associated with a processor.

Instruction read operation. An operation used to obtain a globally shared copy of a coherence granule specifically for an instruction cache.

Instruction set architecture (ISA). The instruction set for a certain processor or family of processors.

Intervention. A data transfer between two processing elements that does not go through the coherence granule's home memory, but directly between the requestor of the coherence granule and the current owner.

Invalidate operation. An operation used to remove a coherence granule from caches within the coherence domain

IP. Intellectual Property

ITU. International Telecommunication Union.

Little-endian. A byte-ordering method in memory where the address n of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte

Local memory. Memory associated with the processing element in question.

Logical/Transport error. A logical/transport error is one that cannot be resolved using the defined transmission error recovery sequence, results in permanent loss of data or causes system corruption. Recovery may possible under software control.

Long Term Congestion. A severe congestion event in which a system does not have the raw capacity to handle the demands placed upon it in actual use.

LP. Link Protocol

LSB. Least significant byte.

LVDS. Low voltage differential signaling.

Mailbox. Dedicated hardware that receives messages.

Medium Term Congestion. A congestion event in which a frequent series of short term congestion events occur over a long period of time such as seconds or minutes, handled in RapidIO systems by reconfiguration of the fabric by system-level software.

Memory coherence. Memory is coherent if a processor performing a read from its cache is supplied with data corresponding to the most recent value written to memory or to another processor's cache. In other words, a write operation to an address in the system is visible to all other caches in the system. Also referred to as cache coherence

Memory controller. The point through which home memory is accessed.

Memory directory. A table of information associated with home memory that is used to track the location and state of coherence granules cached by coherence domain participants.

Message passing. An application programming model that allows processing elements to communicate via messages to mailboxes instead of via DMA or GSM. Message senders do not write to a memory address in the receiver.

MFA. Message frame address.

MFD. Message frame descriptor.

Modified exclusive shared invalid (MESI). A standard 4 state cache coherence definition.

Modified shared invalid (MSI). A standard 3 state cache coherence definition.

Modified shared local (MSL). A standard 3 state cache coherence definition.

Modified. A processing element has written to a locally cached coherence granule and so has the only valid copy of the coherence granule in the system.

MSB. Most significant byte.

Multicast group. The group of end point devices in a system that is the target of a multicast operation.

Multicast mask. The group of egress ports in a switch that are the targets of a replicated multicast packet.

Multicast. The concept of sending a single packet to multiple destinations in a system.

Non-coherent. A transaction that does not participate in any system globally shared memory cache coherence mechanism.

Non-reporting processing element. A non-reporting processing element depends upon an attached device (usually a switch) to report its logged errors to the system host on its behalf.

Operation. A set of transactions between end point devices in a RapidIO system (requests and associated responses) such as a read or a write

Orphaned XOFF Mechanism. A mechanism in an end point which is used to restart the oldest controlled flow within the end point after a certain period of time has elapsed without the flow being XON'd.

Ownership. A processing element has the only valid copy of a coherence granule and is responsible for returning it to home memory.

Packet. A set of information transmitted between devices in a RapidIO system.

Payload. The user data embedded in the RapidIO packet.

PCB. Printed circuit board.

PCS. Physical Coding Sublayer.

PDU. Protocol Data Unit, the OSI term for a packet.

Performance Collapse. Non-linear behavior found in non-congestion controlled fabrics, whereby reduced aggregate throughput is exhibited with increased load.

Peripheral component interface (PCI). A bus commonly used for connecting I/O devices in a system.

Physical error. A physical error occurs only in the physical layer.

PMA. Physical Media Attachment.

Port healing. The process whereby software resets the error rate count, or allows it to decrement as required by the error rate bias field of the Port n Error Rate CSR.

Port-write. An address-less maintenance write operation.

Priority. The relative importance of a packet. In most cases, a higher priority packet will be serviced or transmitted before one of lower priority.

Processing Element (PE). A generic participant on the RapidIO interconnect that sends or receives RapidIO transactions, also called a device.

Processor. The logic circuitry that responds to and processes the basic instructions that drive a computer.

Protocol Attributes. Information relevant to communication using a particular protocol, or to data transferred within the context of a connection using that protocol.

Read operation. An operation used to obtain a globally shared copy of a coherence granule.

Read-for-ownership operation. An operation used to obtain ownership of a coherence granule for the purposes of performing a write operation.

Receiver. The RapidIO interface input port on a processing element.

Reliable Transmission (RT). A mode of operation that guarantees packet delivery by retransmitting packets when an error occurs.

Remote access. An access by a processing element to memory located in another processing element.

Remote memory. Memory associated with a processing element other than the processing element in question.

Reporting processing element. A reporting processing element is capable of reporting its logged errors to the system host.

ROM. Read-only memory.

SAR. Segmentation and Reassembly, a mechanism for encapsulating a PDU within multiple packets.

Saturation Tree. A pattern of congestion identified within the fabric which grows backward from the root buffer overflow towards the sources of all transaction request flows passing through this buffer.

Segmentation Context. Information that allows a receiver to associate a particular packet with the correct PDU.

Segmentation. A process by which a PDU is transferred as a series of smaller segments.

Semaphore. A technique for coordinating activities in which multiple processing elements compete for the same resource.

Sender. The RapidIO interface output port on a processing element.

Sequence. Sequentially ordered, uni-directional group of messages that constitute the basic unit of data delivered from one end point to another.

Serializer. A device which converts parallel data (such as 8-bit data) to a single bit-wide datastream.

Session Management Protocol. The protocol specified in this document, used for negotiation of communication sessions and optionally for data transfers.

Shared. A processing element has a cached copy of a coherence granule that may be cached by other processing elements and is consistent with the copy in home memory

Sharing mask. The state associated with a coherence granule in the memory directory that tracks the processing elements that are sharing the coherence granule.

Short Term Congestion. A congestion event lasting up into the dozens or hundreds of microseconds, handled in RapidIO by Logical Layer Flow Control

Source. The origin of a packet on the RapidIO interconnect, also referred to as an initiator.

SRAM. Static random access memory.

StreamID. A specific field in the data streaming protocol that is combined with the data stream's transaction request flow ID and the sourceID or destinationID from the underlying packet transport fabric to form the virtual stream ID.

Sub-double-word. Aligned on eight byte boundaries.

Suspect. A communication partner, which may not fully conform to the session management protocol.

Switch processing element. One of three processing elements, a switch processing element, or switch, is capable of logging and reporting errors to the host system.

Switch. A multiple port processing element that directs a packet received on one of its input ports to one of its output ports.

Symbol. A 16-bit quantity.

Target. The termination point of a packet on the RapidIO interconnect, also referred to as a destination.

Topology. The structure represented by the physical interconnections of a switch fabric.

Transaction request flow. TBD KENT.

Transaction. A specific request or response packet transmitted between end point devices in a RapidIO system.

Translation look-aside buffer (TLB). Part of a processor's memory management unit; a TLB contains a set of virtual to physical page address translations, along with a set of attributes that describe access behavior for that portion of physical memory.

Transmission error. A transmission error is one that can be resolved using the defined transmission error recovery sequence, results in no permanent loss of data and does not cause system corruption. Recovery may also be possible under software control using mechanisms outside of the scope of this specification.

Ultra Short Term Congestion. A congestion event lasting from dozens to hundreds of nanoseconds, handled in RapidIO by Link Level Flow Control.

Underflow. A condition within output buffers of switches in which the buffer runs dry.

Virtual input Queue (ViQ). Virtual output Queue (VoQ). An intermediate point in the system where one or more virtual streams may be concentrated

Virtual Stream ID (VSID). TBD KENT.

Watermark. A predetermined buffer occupancy level indicating either congestion (high watermark) or abatement of congestion (low watermark).

Word. A four-byte quantity.

Write port. Hardware within a processing element that is the target of a port-write operation.

Write-through. A cache policy that passes all write operations through the caching hierarchy directly to home memory.

XOFF (Transmit Off). A congestion control packet sent from the point of congestion back to the source of a particular flow, telling the source endpoint to shut off the flow.

XON (Transmit On). A congestion control packet sent from the point of congestion back to the source of a particular flow, telling the source endpoint to restart a controlled flow.