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TWG Second Showing

Item 12-08-00001.003

Subject: Revision 3.0 specification Timer Control Proposal

Background: This showing proposes a change to the definition of the programmable timeouts for 10xN operation

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Comment Expiration Date: None

Distribution: RapidIO TA Technical Working Group members

1.0 Discussion

During the development of the revision 3.0 specification, members came to a concensus that it would be wise to make the timers related to link initialization and dynamic width management programmable. However, a complete list of timers was not agreed upon before the 3.0 draft was published for ballot. This showing proposes a more complete list of timeouts and controls, and a programming model for these timeouts.

1.1 Timeouts and Controls for DME Training

1.1.1 List of Timeouts/Controls

The most basic timeout for DME training is the DME completion timeout, which controls the total time allowed for training. The IEEE specification requires this timer to be 0.5 seconds +/- 1%.

Another timer value is the “wait_timer”, which is the number of frames to send after the link partner indicates that it has achieved receiver_ready. The IEEE states that this should be 100-300 training frames.

Lastly, there should be a timeout for Transmit Emphasis command processing and acknowledgement. Nothing is specified by IEEE for this timeout.

1.1.2 Discussion and Basis of Proposal

While the IEEE requires the DME completion timeout to be 0.5 seconds +/- 1%, it is possible that a longer interval would be required for RapidIO. It is proposed that the RapidIO DME completion timeout should be a default of 0.5 seconds +/- 34%, with a maximum value of 1.0 second +/- 34%. This allows the timeout counter to make use of the same clock source as the Port Link Timeout Control CSR. A programmed value of 0 disables the DME training completion timeout, allowing DME training to operate forever.

The wait_timeout similarly is increased in size compared to IEEE, allowing a range of 4 to 1020 frames with a default value of 252. A value of “0” will cause the training frames to continue until the DME completion timeout expires.

The transmit emphasis command timeout timer should be consistent with the timeouts for CW training and retraining, and ideally would be the same as those for IDLE2. It is proposed that the timeout for acknowledging a DME transmit emphasis command is a maximum of 250 usec +/- 34%.

1.2 Codeword Training Timeouts

1.2.1 List of Timeouts

Similar to DME training, CW training requires a CW training completion timeout to govern the maximum amount of time allowed to complete CW training.

Additionally, CW training requires timeouts on Transmit Emphasis command acknowledgement.

1.2.2 Discussion and Basis of Proposal

The CW training completion timeout should have the same range as that for DME training completion. It is proposed that the CW training completion timeout should default to 0.5 seconds +/- 34%, with a maximum value of 1.0 second +/- 34%. A programmed value of 0 disables the CW training completion timeout, allowing CW training to operate forever.

The transmit emphasis command timeout timer should be consistent with the timeouts for DME training and retraining, and ideally would be the same as those for IDLE2. It is proposed that the timeout for acknowledging a CW training transmit emphasis command is a maximum of 250 usec +/- 34%.

1.3 Asymmetric Mode Timeouts

1.3.1 List of Timeouts

There are two timeouts associated with Asymmetric Mode operation which already appear in the D.3.0.8 draft specification. The first is the timeout for a Receive Width Command, and the second is the timeout for the Transmit Width Command. Since a Receive Width Command is issued in response to a Transmit Width Command, the timeout for a Receive Width Command should be shorter than that of the Transmit Width Command.

Additionally, there is a “keep alive” behavior that should be programmable in two dimensions: How often the lane transmits, and how long the lane transmits.

1.3.2 Discussion and Basis of Proposal

Both the Transmit Width Command and Receive Width Command timeouts are currently specified to be 64 msec +/- 10%.

To keep the basis of timeouts consistent with DME and CW training, it is proposed that the Transmit Width Command timeout shall be 250 microseconds +/- 34%, and the Receive Width Command timeout shall be 62.5 microseconds +/- 34%. This ensures that the Receive Width Command timeout will be less than the Transmit Command Timeout, and that the same clock source can be used for both timeouts.

It is proposed that the "keep alive" period be programmable in a manner consistent with the Interlaken specification. A period ranging from 10 msec to 10 seconds is required between transmission periods. The transmission period should be programmable up to 100 usec in 1 usec increments. Since 10 bits are required for the keep-alive period, the granularity of the transmission period is reduced to ~2 usec to allow the two values to fit in 16 bits.

1.4 Retraining Timeouts

1.4.1 List of Timeouts

Similar to DME and CW training, Retraining requires a Retraining completion timeout. This is currently in the specification as 64 msec +/- 10%.

1.4.2 Discussion and Basis of Proposal

To make the Retraining timeout consistent with other timeouts, it is proposed that the Retraining timeout be changed to 62.5 msec +/- 34%.

1.5 Other Timeouts

1.5.1 List of Timeouts

The Discovery timeout must be slightly longer than the CW training timeout, and so should be made programmable.

The Recovery timer found int the D3.0.8 draft is used to determine when 1x, 2x and Nx recovery modes should transition to a new states.

1.5.2 Discussion and Basis of Proposal

The Discovery timer is proposed to have a maximum period of 1 second +/- 34% to be consistent with the CW training timeout. The Discovery timer has a default value which is one greater than the CW training timeout.

The Recovery timer controls the length of time to stay in 1x_RECOVERY, 2x_RECOVERY and Nx_RECOVERY states. The Recovery timer is currently specified to by 64 msec +/- 10%. To be consistent with the other timers, it is proposed that the Recovery timer should have an interval of 62.5 msec +/- 34%.

1.6 Programming Model Discussion

Each of the timeouts needs to be programmable. However, the number of bits dedicated to the programmability should be minimized.

It is proposed that each of the timers listed be programable to a granularity of 1/256, with a value of 0 used to disable the timers.

Note that it is impossible for all of the timers to be in use simultaneously. A gate-efficient implementation may therefore reuse the same counter for several different timeouts.

1.7 Changes to D3.0.8

Multiple changes to the text are implied by the changes to the registers defined below. These changes will be added to the showing once concensus is reached on the list of timers and the programming model.

It is proposed to change the Port n Timeout Control CSR from a single register into three registers, as follows. The original Port n Timeout Control CSR is changed from: “

1.7.1 Port *n* Timer Control CSRs (Block Offsets 0x50, 90, ... , 430)

The Port n Timer Control CSRs are used to control timers related to 10.3125 Gbaud operation. All bit fields in this register shall be as defined in Table 1-1. Unless otherwise specified, the bits and bit fields of this register shall be readable and writable.

Table 1-1. Bit Settings for Port *n* Timer Control CSRs

Bit	Name	Reset Value	Description
0-15	Retraining Timer	0xFFFF	Controls the length of time allowed for retraining a lane once the lane is determined to be operating in a degraded state. Maximum time is 64 milliseconds, +/- 10%. A value of 0 shall disable this timer.
16-31	Recovery Timer	0xFFFF	Controls the length of time allowed for a width change to complete. Maximum time is 64 milliseconds, +/- 10% A value of 0 shall disable this timer.

“

to: “

1.7.2 Port *n* Training Timer Control CSRs (Block Offsets 0x70, 0xB0, ... , 0x430)

The Port n Training Timer Control CSRs are used to control timers related to Baud Rate Class 3 operation. All bit fields in this register shall be as defined in Table 1-2. Unless otherwise specified, the bits of this register shall be readable and writable.

Table 1-2. Bit Settings for Port *n* Timer Control CSRs

Bit	Name	Reset Value	Description
0-7	DME Training Completion Timer	See Description	Controls the length of time allowed for DME training to complete. The Maximum Period for this timeout shall be one second +/- 34%. The programmed period for this timeout is computed by: (DME Training Completion Timer) * (Maximum Period/256). The reset value of this field shall result in a DME Training Completion timeout period that is - at least 500 milliseconds and - is as close to 500 milliseconds as possible A value of 0 shall disable this timer.
8-15	DME Wait_Timer	0x3F	Controls the number of DME training frames transmitted after the link partner has indicated that its receiver is trained. This value is encoded as the number of training frames to send, divided by 4. The default value shall cause transmission of 252 training frames. The maximum value shall cause transmission of 1020 training frames. A value of 0 shall cause DME training frames to be transmitted continuously until the DME Training Completion Timer expires.
16:23	CW Training Completion Timer	See Description	Controls the length of time allowed for Codeword training to complete. The Maximum Period for this timeout shall be one second +/- 34%. The programmed period for this timeout is computed by: (CW Training Completion Timer) * (Maximum Period/256). The reset value of this field shall result in a CW training completion timeout period that is - at least 500 milliseconds and - is as close to 500 milliseconds as possible A value of 0 shall disable this timer.
24:31	Emphasis Command Timeout	0xFF	Controls the length of time allowed for transmit emphasis command to be acknowledged during DME training, CW training, and retraining. The Maximum Period for this timeout shall be 250 microseconds +/- 34%. The programmed period for this timeout is computed by: (Emphasis Command Timeout) * (Maximum Period/256). A value of 0 shall disable this timer.

1.7.3 Port *n* Training Timer Control 2 CSRs (Block Offsets 0x74, 0xB4, ... , 0x434)

The Port n Training Timer Control 2 CSRs are used to control timers related to Baud Rate Class 3 operation. All bit fields in this register shall be as defined in Table 1-3. Unless otherwise specified, the bits of this register shall be readable and writable.

Table 1-3. Bit Settings for Port *n* Timer Control 2 CSRs

Bit	Name	Reset Value	Description
0-7	Retraining Completion Timer	0xFF	Controls the length of time allowed for retraining a lane once the lane is determined to be operating in a degraded state. The Maximum Period for this timeout is 62.5 milliseconds, +/- 34%. The programmed period for this timeout is computed by: (Retraining Completion Timer) * (Maximum Period/256). A value of 0 shall disable this timer.
8-15	Discovery Completion Timer	See Description	Controls the length of time allowed for Discovery for multi-lane ports. The Maximum Period for this timeout is 1 second, +/- 34%. The programmed period for this timeout is computed by: (Discovery Completion Timer) * (Maximum Period/256). The reset value of this field shall be computed by adding 1 to the reset value of the CW Training Completion Timer. A value of 0 shall disable this timer.
16-23	Recovery Timer	0xFF	Controls the length of time the Port_Initialization state machines and the Receive_Width state machine are allowed to remain in the 1x_RECOVERY, 2x_RECOVERY, or Nx_RECOVERY states. The Maximum Period for this timeout is 62.5 milliseconds, +/- 34%. The programmed period for this timeout is computed by: (Recovery Timer) * (Maximum Period/256). A value of 0 shall disable this timer.
24-31	—		Reserved

1.7.4 Port *n* Training Timer Control 3 CSRs (Block Offsets 0x78, 0xB8, ... , 0x438)

The Port n Training Timer Control 3 CSRs are used to control timers related to Baud Rate Class 3 asymmetric mode operation. All bit fields in this register shall be as defined in Table 1-4. Unless otherwise specified, the bits of this register shall be readable and writable.

Table 1-4. Bit Settings for Port *n* Timer Control 3 CSRs

Bit	Name	Reset Value	Description
0-7	Transmit Width Command Timeout	0xFF	Controls the length of time allowed for a Transmit Width Command change to complete. The Maximum Period for this timeout is 250 microseconds, +/- 34%. The programmed period for this timeout is computed by: (Transmit Width Command Timeout) * (Maximum Period/256). A value of 0 shall disable this timer.
8-15	Receive Width Command Timeout	0xFF	Controls the length of time allowed for a Receive Width Command change to complete. The Maximum Period for this timeout is 250 microseconds, +/- 34%. The programmed period for this timeout is computed by: (Receive Width Command Timeout) * (Maximum Period/256). A value of 0 shall disable this timer.

Table 1-4. Bit Settings for Port *n* Timer Control 3 CSRs (Continued)

Bit	Name	Reset Value	Description
16-21	Keep-alive Transmission Period	0x01	Controls the length of time a lane shall transmit to keep the link partner SerDes alive on lanes that are not in use in asymmetric mode. The Maximum Period for transmission is 125 microseconds, +/- 34%. The programmed period for transmission is computed by: (Keep-alive Transmission Period) * (Maximum Period/64). A value of 0 results in implementation specific behavior.
22-31	Keep-alive Transmission Interval	0x3FF	Controls the length of time between Keep-alive Transmission Periods for lanes that are not in use when a port is operating in asymmetric mode. The Maximum Period for this timeout is 10 seconds, +/- 34%. The programmed period for this timeout is computed by: (Keep-alive Transmission Interval) * (Maximum Period/1024). A value of 0 shall disable this timeout. When the timeout is disabled, no Keep-Alive transmissions are performed.