Registers Summary First Cut

Autogenerated register summary from file **Register\_Summaries/register\_summary\_4.0.txt. Generated** 2020-12-16 09:14:57

Note that registers are defined using big endian notation. Bit 0 is the most significant bit!

# Block: 0x0001 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 6C, ... , 22C) | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234) | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238) | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C) | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |

# Block: 0x0002 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 60, ... , 220) | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 7.6.5 Port n Link Maintenance Request CSRs (RM-I Block Offsets 0x40, 60, ... , 220) (RM-II Block Offsets 0x40, 80, ... , 400) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 64, ... , 224) | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 1:2 | Reserved | | |
| 3:14 | port\_status\_cs64 | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 15:26 | ackID\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 27:31 | port\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| Name: Port n Local ackID CSRs Offset: 0x48, 68, ... , 228 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 1 | Reserved | | |
| 2:7 | Inbound\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 8:17 | Reserved | | |
| 18:23 | Outstanding\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 24:25 | Reserved | | |
| 26:31 | Outbound\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 6C, ... , 22C) | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234) | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238) | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C) | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |

# Block: 0x0003 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 6C, ... , 22C) | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234) | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238) | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C) | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |

# Block: 0x0007 : Error Management Extensions Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Error Management Extensions Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 8 | 2.5.1 Error Management Extensions Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 8 | 2.5.1 Error Management Extensions Block Header (Block Offset 0x0) |
| Name: Error Management/Hot Swap Extension Block CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0 | Error Management Extensions Not Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 1 | Hot Swap Extensions Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 2 | Physical Layer Error Capture FIFO Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 3 | Logical/Transport Layer Error Capture FIFO Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 4:31 | Reserved | | |
| Name: Logical/Transport Layer Error Detect CSR Offset: 0x08 | | | |
| Bits | Name | Part | Section |
| 0 | IO error response | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 1 | Message error response | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 2 | GSM error response | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 3 | Message Format Error | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 4 | Illegal transaction decode | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 5 | Illegal transaction target error | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 6 | Message Request Timeout | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 7 | Packet Response Timeout | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 8 | Unsolicited Response | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 9 | Unsupported Transaction | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 10 | Missing data streaming context | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 11 | Open existing data streaming context | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 12 | Long data streaming segment | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 13 | Short data streaming segment | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 14 | Data streaming PDU length error | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 15:21 | Reserved | | |
| 22 | Lost Tick Error Status | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 23 | Lost TSG Sync Error Status | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 24:31 | Implementation Specific error | Part 8 | 2.5.3 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| Name: Logical/Transport Layer Error Enable CSR Offset: 0x0C | | | |
| Bits | Name | Part | Section |
| 0 | IO error response enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 1 | Message error response enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 2 | GSM error response enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 3 | Message Format Error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 4 | Illegal transaction decode enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 5 | Illegal transaction target error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 6 | Message Request timeout error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 7 | Packet Response Timeout error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 8 | Unsolicited Response error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 9 | Unsupported Transaction error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 10 | Missing data streaming context error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 11 | Open existing data streaming context error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 12 | Long data streaming segment error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 13 | Short data streaming segment error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 14 | Data streaming PDU length error error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 15:21 | Reserved | | |
| 22 | Lost Tick Error Enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 23 | Lost TSG Sync Error Enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 24:31 | Implementation Specific error enable | Part 8 | 2.5.4 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| Name: Logical/Transport Layer High Address Capture CSR Offset: 0x10 | | | |
| Bits | Name | Part | Section |
| 0:31 | address[0-31] | Part 8 | 2.5.5 Logical/Transport Layer High Address Capture CSR (Block Offset 0x10) |
| Name: Logical/Transport Layer Address Capture CSR Offset: 0x14 | | | |
| Bits | Name | Part | Section |
| 0:28 | address[32-60] | Part 8 | 2.5.6 Logical/Transport Layer Address Capture CSR (Block Offset 0x14) |
| 29 | Implementation Specific | Part 8 | 2.5.6 Logical/Transport Layer Address Capture CSR (Block Offset 0x14) |
| 30:31 | xamsbs | Part 8 | 2.5.6 Logical/Transport Layer Address Capture CSR (Block Offset 0x14) |
| Name: Logical/Transport Layer Device ID Capture CSR Offset: 0x18 | | | |
| Bits | Name | Part | Section |
| 0:7 | MSB destinationID | Part 8 | 2.5.7 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 8:15 | destinationID | Part 8 | 2.5.7 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 16:23 | MSB sourceID | Part 8 | 2.5.7 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 24:31 | sourceID | Part 8 | 2.5.7 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| Name: Logical/Transport Layer Control Capture CSR Offset: 0x1C | | | |
| Bits | Name | Part | Section |
| 0:3 | ftype | Part 8 | 2.5.8 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 4:7 | ttype | Part 8 | 2.5.8 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 8:15 | msg info | Part 8 | 2.5.8 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 16:31 | Implementation specific | Part 8 | 2.5.8 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| Name: Logical/Transport Layer Dev32 Destination ID Capture CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:31 | Dev32 DestID | Part 8 | 2.5.9 Logical/Transport Layer Dev32 Destination ID Capture CSR (Block Offset 0x20) |
| Name: Logical/Transport Layer Dev32 Source ID Capture CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:31 | Dev32 SrcID | Part 8 | 2.5.10 Logical/Transport Layer Dev32 Source ID Capture CSR (Block Offset 0x24) |
| Name: Port-Write Target deviceID CSR Offset: 0x28 | | | |
| Bits | Name | Part | Section |
| 0:7 | Dev16\_deviceID\_msb | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 8:15 | Dev8\_deviceID | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 16 | Dev8\_or\_16 | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 17 | Dev32\_PW | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 18:31 | Reserved | | |
| Name: Packet Time-to-live CSR Offset: 0x2C | | | |
| Bits | Name | Part | Section |
| 0:15 | Time-to-live value | Part 8 | 2.5.12 Packet Time-to-live CSR (Block Offset 0x2C) |
| 16:31 | Reserved | | |
| Name: Port-write Dev32 Target deviceID CSR Offset: 0x30 | | | |
| Bits | Name | Part | Section |
| 0:31 | Dev32\_deviceID | Part 8 | 2.5.13 Port-write Dev32 Target deviceID CSR (Block Offset 0x30) |
| Name: Port-Write Transmission Control CSR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:30 | Reserved | | |
| 31 | Port-write Transmission Disable | Part 8 | 2.5.14 Port-Write Transmission Control CSR (Block Offset 0x34) |
| Name: Port n Error Detect CSR Offset: 0x40, 80,..., 400 | | | |
| Bits | Name | Part | Section |
| 0 | Implementation specific error | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 1 | Link OK to Uninit Transition | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 2 | Link Uninit Packet Discard Active | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 3 | Link Uninit to OK Transition | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 4:7 | Reserved | | |
| 8 | Deprecated | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 9 | Received corrupt control symbol | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 10 | Received acknowledge control symbol with unexpected ackID | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 11 | Received packet-not-accepted control symbol | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 12 | Received packet with unexpected ackID | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 13 | Received packet with bad CRC | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 14 | Received packet exceeds maximum allowed size | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 15 | Received illegal or invalid character | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 16 | Received data character in IDLE1 sequence | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 17 | Loss of descrambler synchronization | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 18 | Invalid Ordered Sequence | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 19:25 | Reserved | | |
| 26 | Non-outstanding ackID | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 27 | Protocol error | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 28 | Deprecated | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 29 | Delineation error | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 30 | Unsolicited acknowledgement control symbol | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 31 | Link timeout | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| Name: Port n Error Rate Enable CSR Offset: 0x44, 84,..., 404 | | | |
| Bits | Name | Part | Section |
| 0 | Implementation specific error enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 1 | Link OK to Uninit Transition Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 2 | Link Uninit Packet Discard Active Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 3 | Link Uninit to OK Transition Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 4:7 | Reserved | | |
| 8 | Deprecated | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 9 | Received corrupt control symbol enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 10 | Received acknowledge control symbol with unexpected ackID enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 11 | Received packet-not-accepted control symbol enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 12 | Received packet with unexpected ackID enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 13 | Received packet with bad CRC enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 14 | Received packet exceeds maximum allowed size enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 15 | Received illegal or invalid character enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 16 | Received data character in an IDLE1 sequence enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 17 | Loss of descrambler synchronization enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 18 | Invalid ordered sequence enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 19:25 | Reserved | | |
| 26 | Non-outstanding ackID enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 27 | Protocol error enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 28 | Deprecated | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 29 | Delineation error enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 30 | Unsolicited acknowledgement control symbol enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 31 | Link timeout enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| Name: Port n Attributes Capture CSR Offset: 0x48, 88,..., 408 | | | |
| Bits | Name | Part | Section |
| 0:2 | Info type | Part 8 | 2.5.17 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 3:7 | Error type | Part 8 | 2.5.17 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 8:27 | Implementation Dependent | Part 8 | 2.5.17 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 28:30 | Reserved | | |
| 31 | Capture valid info | Part 8 | 2.5.17 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| Name: Port n Capture 0 CSR Offset: 0x4C, 8C,..., 40C | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 0 | Part 8 | 2.5.18 Port n Capture 0 CSR (Block Offset 0x4C, 8C,..., 40C) |
| Name: Port n Capture 1 CSR Offset: 0x50, 90,..., 410 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 1 | Part 8 | 2.5.19 Port n Capture 1 CSR (Block Offset 0x50, 90,..., 410) |
| Name: Port n Capture 2 CSR Offset: 0x54, 94,..., 414 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 2 | Part 8 | 2.5.20 Port n Capture 2 CSR (Block Offset 0x54, 94,..., 414) |
| Name: Port n Capture 3 CSR Offset: 0x58, 98,..., 418 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 3 | Part 8 | 2.5.21 Port n Capture 3 CSR (Block Offset 0x58, 98,..., 418) |
| Name: Port n Capture 4 CSR Offset: 0x5C, 9C,..., 41C | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 4 | Part 8 | 2.5.22 Port n Capture 4 CSR (Block Offset 0x5C, 9C,..., 41C) |
| Name: Port n Error Rate CSR Offset: 0x68, A8,..., 428 | | | |
| Bits | Name | Part | Section |
| 0:7 | Error Rate Bias | Part 8 | 2.5.23 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 8:13 | Reserved | | |
| 14:15 | Error Rate Recovery | Part 8 | 2.5.23 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 16:23 | Peak Error Rate | Part 8 | 2.5.23 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 24:31 | Error Rate Counter | Part 8 | 2.5.23 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| Name: Port n Error Rate Threshold CSR Offset: 0x6C, AC, ..., 42C | | | |
| Bits | Name | Part | Section |
| 0:7 | Error Rate Failed Threshold Trigger | Part 8 | 2.5.24 Port n Error Rate Threshold CSR (Block Offset 0x6C, AC, ..., 42C) |
| 8:15 | Error Rate Degraded Threshold Trigger | Part 8 | 2.5.24 Port n Error Rate Threshold CSR (Block Offset 0x6C, AC, ..., 42C) |
| 16:31 | Reserved | | |
| Name: Port n Link Uninit Discard Timer CSR Offset: 0x70, 0xB0, ..., 0x430 | | | |
| Bits | Name | Part | Section |
| 0:23 | Link Uninit Timeout | Part 8 | 2.5.25 Port n Link Uninit Discard Timer CSR (Block Offset 0x70, 0xB0, ..., 0x430) |
| 24:31 | Reserved | | |
| Name: Port n FIFO Error Detect CSR Offset: 0x7C, BC,..., 43C | | | |
| Bits | Name | Part | Section |
| 0 | Implementation specific error | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 1 | Link OK to Uninit Transition | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 2 | Link Uninit Packet Discard Active | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 3 | Link Uninit to OK Transition | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 4:7 | Reserved | | |
| 8 | Deprecated | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 9 | Received corrupt control symbol | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 10 | Received acknowledge control symbol with unexpected ackID | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 11 | Received packet-not-accepted control symbol | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 12 | Received packet with unexpected ackID | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 13 | Received packet with bad CRC | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 14 | Received packet exceeds maximum allowed size | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 15 | Received illegal or invalid character | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 16 | Received data character in IDLE1 sequence | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 17 | Loss of descrambler synchronization | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 18 | Invalid Ordered Sequence | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 19:25 | Reserved | | |
| 26 | Non-outstanding ackID | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 27 | Protocol error | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 28 | Deprecated | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 29 | Delineation error | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 30 | Unsolicited acknowledgement control symbol | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |
| 31 | Link timeout | Part 8 | 2.5.26 Port n FIFO Error Detect CSR (Block Offset 0x7C, BC,..., 43C) |

# Block: 0x0009 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 60, ... , 220) | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 7.6.5 Port n Link Maintenance Request CSRs (RM-I Block Offsets 0x40, 60, ... , 220) (RM-II Block Offsets 0x40, 80, ... , 400) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 64, ... , 224) | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 1:2 | Reserved | | |
| 3:14 | port\_status\_cs64 | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 15:26 | ackID\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 27:31 | port\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| Name: Port n Local ackID CSRs Offset: 0x48, 68, ... , 228 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 1 | Reserved | | |
| 2:7 | Inbound\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 8:17 | Reserved | | |
| 18:23 | Outstanding\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| 24:25 | Reserved | | |
| 26:31 | Outbound\_ackID | Part 6 | 7.6.7 Port n Local ackID CSRs (RM-I Block Offsets 0x48, 68, ... , 228) |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 6C, ... , 22C) | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234) | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238) | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C) | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |

# Block: 0x000A : VC Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: VC Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.8.2.1 VC Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.8.2.1 VC Register Block Header (Block Offset 0x0) |
| Name: Port n VCx BW Allocation Registers Offset: ((((port number) + 1) \* 0x20) + (offset based on . VC #, see Table 7-31)) | | | |
| Bits | Name | Part | Section |
| 0:15 | Bandwidth Allocation | Part 6 | 7.8.2.4 Port n VCx BW Allocation Registers (Block Offset ((((port number) + 1) \* 0x20) + (offset based on . VC #, see Table 7-31))) |
| 16:31 | Bandwidth Allocation | Part 6 | 7.8.2.4 Port n VCx BW Allocation Registers (Block Offset ((((port number) + 1) \* 0x20) + (offset based on . VC #, see Table 7-31))) |
| Name: Port n VC0 BW Allocation Registers Offset: (((port number) + 1) \* 0x20) + 0x04) | | | |
| Bits | Name | Part | Section |
| 0 | VC0 Bandwidth Reservation Capable | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 1 | VC0 BW Res Enable | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 2 | VC0 Supports VC bit for Priority | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 3 | VC0 Enable VC Bit for Priority | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 4:7 | Reserved | | |
| 8:15 | Bandwidth Reservation Precision | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 16:31 | Bandwidth Allocation | Part 6 | 7.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| Name: Port n VC Control and Status Registers Offset: ((port number) + 1) \* 0x20) | | | |
| Bits | Name | Part | Section |
| 0:7 | VC Refresh Interval | Part 6 | 7.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 8:15 | CT Mode | Part 6 | 7.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 16:23 | VCs Support | Part 6 | 7.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 24:31 | VCs Enable | Part 6 | 7.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |

# Block: 0x000B : LP-Serial VC Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial VC Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 12 | 5.1.2.1 LP-Serial VC Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 12 | 5.1.2.1 LP-Serial VC Register Block Header (Block Offset 0x0) |
| Name: Port n VoQ Control Status Register Offset: 0x20 + (4\* n) | | | |
| Bits | Name | Part | Section |
| 0 | VoQ Backpressure Symbol Generation Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 1 | VoQ Backpressure Symbol Reception Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 2 | VoQ Backpressure Per VC Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 3:7 | reserved | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 8 | Enable VoQ Symbol Generation | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 9 | Enable VoQ Participation | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 10 | Port XOFF | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 11 | Enable VoQ Backpressure Per VC Transmission | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 12 | Port Group Size 0 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 13 | Port Group Size 1 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 14 | Port Group Size 2 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 15 | Port Group Size 3 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 16 | Port Group Size 4 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 17 | Port Group Size 5 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 18 | Port Group Size 6 Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 19:25 | reserved | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 26:28 | TX Port Group Size | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |
| 29:31 | RX Port Group Size | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - 0x20 + (4\* n)) |

# Block: 0x000D : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.7.2.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.7.2.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Lane n Status 0 CSRs Offset: 0x10, 30, ... , 3F0 | | | |
| Bits | Name | Part | Section |
| 0:7 | Port Number | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 8:11 | Lane Number | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 12 | Transmitter type | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 13 | Transmitter mode | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 14:15 | Receiver type | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 16 | Receiver input inverted | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 17 | Receiver trained | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 18 | Receiver lane sync | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 19 | Receiver lane ready | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 20:23 | 8b/10b decoding errors | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 24 | Lane\_sync state change | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 25 | lane\_trained state change | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 26:27 | Reserved | | |
| 28 | Status 1 CSR implemented | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 29:31 | Status 2-7 CSRs implemented | Part 6 | 7.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| Name: Lane n Status 1 CSRs Offset: 0x14, 34, ... , 3F4 | | | |
| Bits | Name | Part | Section |
| 0 | IDLE received | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 1 | IDLE information current | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 2 | Values changed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 3 | Implementation defined | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 4 | IDLE2 connected port lane receiver trained | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 5:7 | IDLE2 received port width | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 8:11 | IDLE2 lane number in connected port | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 12:13 | IDLE2 connected port transmit emphasis Tap(-1) status | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 14:15 | IDLE2 connected port transmit emphasis Tap(+1) status | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 16 | IDLE2 connected port scrambling/descrambling enabled | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 17 | IDLE3 Loss of Signal | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 18:20 | Training Type | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 21 | IDLE3 DME Training Failed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 22 | IDLE3 DME Training Completed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 23 | CW Training Failed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 24 | CW Training Completed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 25 | CW Retraining Failed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 26 | CW Retraining Completed | Part 6 | 7.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 27:31 | Reserved | | |
| Name: Lane n Status 2 CSRs Offset: 0x18, 38, ... , 3F8 | | | |
| Bits | Name | Part | Section |
| 0:7 | LP Port Number | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 8:11 | LP Lane Number | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 12 | LP Remote training support | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 13 | LP Retraining enabled | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 14 | LP Asymmetric mode enabled | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 15 | LP Port Initialized | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 16 | LP Transmit 1x mode | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 17:19 | LP Receive width | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 20:22 | LP Receive lanes ready | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 23 | LP Receive lane ready | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 24 | LP Lane trained | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 25:27 | LP Change receiver width command | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 28 | LP change receiver width command acknowledge | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 29 | LP change receiver width command negative acknowledge | Part 6 | 7.7.2.4 Lane n Status 2 CSRs (Block Offsets 0x18, 38, ... , 3F8) |
| 30:31 | Reserved | | |
| Name: Lane n Status 3 CSRs Offset: 0x1C, 3C, ... , 3FC | | | |
| Bits | Name | Part | Section |
| 0:2 | LP Transmit width request | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 3 | LP Transmit width request pending | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 4 | LP Transmit SC-sequences | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 5:8 | LP Transmit equalizer tap | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 9:11 | LP Transmit equalizer command | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 12:14 | LP Transmit equalizer status | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 15 | LP Retrain grant | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 16 | LP Retrain ready | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 17 | LP Retraining | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 18 | LP Port Entering Silence | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 19 | LP Lane Entering Silence | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 20:27 | LP State control reserved | Part 6 | 7.7.2.5 Lane n Status 3 CSRs (Block Offsets 0x1C, 3C, ... , 3FC) |
| 28:31 | Reserved | | |

# Block: 0x000E : Switch Routing Table Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Switch Routing Table Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 3 | 3.6.2 Switch Routing Table Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 3 | 3.6.2 Switch Routing Table Register Block Header (Block Offset 0x0) |
| Name: Broadcast Routing Table Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0 | Three Levels | Part 3 | 3.6.3 Broadcast Routing Table Control CSR (Block Offset 0x20) |
| 1 | Dev32 Route Control | Part 3 | 3.6.3 Broadcast Routing Table Control CSR (Block Offset 0x20) |
| 2:5 | Reserved | | |
| 6:7 | Mask\_size | Part 11 | 3.4.2 Broadcast Routing Table Control CSR (Block Offset 0x20) |
| 8:31 | Reserved | | |
| Name: Broadcast Multicast Info CSR Offset: 0x28 | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_Masks | Part 11 | 3.4.3 Broadcast Multicast Info CSR (Block Offset 0x28) |
| 8:21 | Mask\_Ptr | Part 11 | 3.4.3 Broadcast Multicast Info CSR (Block Offset 0x28) |
| 22:31 | Reserved | | |
| Name: Broadcast Level 0 Info CSR Offset: 0x30 | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L0\_Groups | Part 3 | 3.6.4 Broadcast Level 0 Info CSR (Block Offset 0x30) |
| 8:21 | L0\_Group\_Ptr | Part 3 | 3.6.4 Broadcast Level 0 Info CSR (Block Offset 0x30) |
| 22:31 | Reserved | | |
| Name: Broadcast Level 1 Info CSR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L1\_Groups | Part 3 | 3.6.5 Broadcast Level 1 Info CSR (Block Offset 0x34) |
| 8:21 | L1\_Group\_Ptr | Part 3 | 3.6.5 Broadcast Level 1 Info CSR (Block Offset 0x34) |
| 22:31 | Reserved | | |
| Name: Broadcast Level 2 Info CSR Offset: 0x38 | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L2\_Groups | Part 3 | 3.6.6 Broadcast Level 2 Info CSR (Block Offset 0x38) |
| 8:21 | L2\_Group\_Ptr | Part 3 | 3.6.6 Broadcast Level 2 Info CSR (Block Offset 0x38) |
| 22:31 | Reserved | | |
| Name: Port n Routing Table Control CSRs Offset: 0x40 + (0x20 \* n) | | | |
| Bits | Name | Part | Section |
| 0 | Three Levels | Part 3 | 3.6.7 Port n Routing Table Control CSRs (Block Offset 0x40 + (0x20 \* n)) |
| 1 | Dev32 Route Control | Part 3 | 3.6.7 Port n Routing Table Control CSRs (Block Offset 0x40 + (0x20 \* n)) |
| 2:5 | Reserved | | |
| 6:7 | Mask\_size | Part 11 | 3.4.4 Port n Routing Table Control CSR (Block Offset 0x40 + (0x20 \* n)) |
| 8:31 | Reserved | | |
| Name: Port n Multicast Info CSR Offset: 0x48 + 20 \* n | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_Masks | Part 11 | 3.4.5 Port n Multicast Info CSR (Block Offset 0x48 + 20 \* n) |
| 8:21 | Mask\_Ptr | Part 11 | 3.4.5 Port n Multicast Info CSR (Block Offset 0x48 + 20 \* n) |
| 22:31 | Reserved | | |
| Name: Port n Level 0 Info CSRs Offset: 0x50 + (0x20 \* n) | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L0\_Groups | Part 3 | 3.6.8 Port n Level 0 Info CSRs (Block Offset 0x50 + (0x20 \* n)) |
| 8:21 | L0\_Group\_Ptr | Part 3 | 3.6.8 Port n Level 0 Info CSRs (Block Offset 0x50 + (0x20 \* n)) |
| 22:31 | Reserved | | |
| Name: Port n Level 1 Info CSRs Offset: 0x54 + (0x20 \* n) | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L1\_Groups | Part 3 | 3.6.9 Port n Level 1 Info CSRs (Block Offset 0x54 + (0x20 \* n)) |
| 8:21 | L1\_Group\_Ptr | Part 3 | 3.6.9 Port n Level 1 Info CSRs (Block Offset 0x54 + (0x20 \* n)) |
| 22:31 | Reserved | | |
| Name: Port n Level 2 Info CSRs Offset: 0x58 + (0x20 \* n) | | | |
| Bits | Name | Part | Section |
| 0:7 | Num\_L2\_Groups | Part 3 | 3.6.10 Port n Level 2 Info CSRs (Block Offset 0x58 + (0x20 \* n)) |
| 8:21 | L2\_Group\_Ptr | Part 3 | 3.6.10 Port n Level 2 Info CSRs (Block Offset 0x58 + (0x20 \* n)) |
| 22:31 | Reserved | | |
| Name: Level 0 Group x Entry y Routing Table Entry CSR Offset: (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.4 Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.4 Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Broadcast Level 0 Group x Entry y Routing Table Entry CSR Offset: (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) (Broadcast) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.1 Broadcast Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.1 Broadcast Level 0 Group x Entry y Routing Table Entry CSR (Offset = (L0\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Level 1 Group x Entry y Routing Table Entry CSR Offset: (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.5 Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.5 Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Broadcast Level 1 Group x Entry y Routing Table Entry CSR Offset: (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) (Broadcast) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.2 Broadcast Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.2 Broadcast Level 1 Group x Entry y Routing Table Entry CSR (Offset = (L1\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Level 2 Group x Entry y Routing Table Entry CSR Offset: (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.6 Level 2 Group x Entry y Routing Table Entry CSR (Offset = (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.6 Level 2 Group x Entry y Routing Table Entry CSR (Offset = (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Broadcast Level 2 Group x Entry y Routing Table Entry CSR Offset: (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4) (Broadcast) | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation-defined | Part 3 | 3.7.3 Broadcast Level 2 Group x Entry y Routing Table Entry CSR (Offset = (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| 4:21 | Reserved | | |
| 22:31 | Routing Value | Part 3 | 3.7.3 Broadcast Level 2 Group x Entry y Routing Table Entry CSR (Offset = (L2\_Group\_Ptr\*0x400) + (x \* 0x400) + (y\*4)) |
| Name: Broadcast Multicast Mask x Clear Register y CSR Offset: (Mask\_Ptr \* 0x400) + (x \* 8\*2^Mask\_size) + (4\*2^Mask\_size) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:31 | Mcast\_ctl | Part 11 | 3.4.7 Broadcast Multicast Mask x Clear Register y CSR (Offset = (Mask\_Ptr \* 0x400) + (x \* 8\*2^Mask\_size) + (4\*2^Mask\_size) + (y\*4)) |
| Name: Broadcast Multicast Mask x Set Register y CSR Offset: (Mask\_Ptr \* 0x400) + (x\*8\*2^Mask\_size) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:31 | Mcast\_ctl | Part 11 | 3.4.6 Broadcast Multicast Mask x Set Register y CSR (Offset = (Mask\_Ptr \* 0x400) + (x\*8\*2^Mask\_size) + (y\*4)) |
| Name: Port n Multicast Mask x Clear Register y CSR Offset: (Mask\_Ptr \* 400) + (x \* 8\*2^Mask\_size) + (4\*2^Mask\_size) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:31 | Mcast\_ctl | Part 11 | 3.4.9 Port n Multicast Mask x Clear Register y CSR (Offset = (Mask\_Ptr \* 400) + (x \* 8\*2^Mask\_size) + (4\*2^Mask\_size) + (y\*4)) |
| Name: Port n Multicast Mask x Set Register y CSR Offset: (Mask\_Ptr \* 400) + (x \* 8\*2^Mask\_size) + (y\*4) | | | |
| Bits | Name | Part | Section |
| 0:31 | Mcast\_ctl | Part 11 | 3.4.8 Port n Multicast Mask x Set Register y CSR (Offset = (Mask\_Ptr \* 400) + (x \* 8\*2^Mask\_size) + (y\*4)) |

# Block: 0x000F : Timestamp Generation Extension Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Timestamp Generation Extension Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.9.1 Timestamp Generation Extension Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.9.1 Timestamp Generation Extension Block Header (Block Offset 0x0) |
| Name: Timestamp CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0 | Timestamp Slave Supported | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 1 | Timestamp Master Supported | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 2 | Common Clock Frequency Supported | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 3 | MECS Slave Supported | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 4 | MECS Master Supported | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 5 | SMECS Support | Part 6 | 7.9.2 Timestamp CAR (Block Offset 0x04) |
| 6:31 | Reserved | | |
| Name: Timestamp Generator Status CSR Offset: 0x08 | | | |
| Bits | Name | Part | Section |
| 0 | Timestamp Generator Clock Locked | Part 6 | 7.9.3 Timestamp Generator Status CSR (Block Offset 0x08) |
| 1 | Timestamp Generator Common Clock | Part 6 | 7.9.3 Timestamp Generator Status CSR (Block Offset 0x08) |
| 2 | Timestamp Generator Stopped | Part 6 | 7.9.3 Timestamp Generator Status CSR (Block Offset 0x08) |
| 3 | Timestamp Generator Was Stopped | Part 6 | 7.9.3 Timestamp Generator Status CSR (Block Offset 0x08) |
| 4:31 | Reserved | | |
| Name: MECS Tick Interval CSR Offset: 0x10 | | | |
| Bits | Name | Part | Section |
| 0 | MECS Time Synchronization Role | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| 1 | SMECS Selection | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| 2:3 | Lost TSG Sync Error Threshold | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| 4 | Lost Tick Error Status | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| 5 | Lost TSG Sync Error Status | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| 6:7 | Reserved | | |
| 8:31 | Tick Interval | Part 6 | 7.9.4 MECS Tick Interval CSR (Block Offset 0x10) |
| Name: MECS Next Timestamp MSW CSR Offset: 0x18 | | | |
| Bits | Name | Part | Section |
| 0:31 | MSW Bits | Part 6 | 7.9.5 MECS Next Timestamp MSW CSR (Block Offset 0x18) |
| Name: MECS Next Timestamp LSW CSR Offset: 0x1C | | | |
| Bits | Name | Part | Section |
| 0:31 | LSW Bits | Part 6 | 7.9.6 MECS Next Timestamp LSW CSR (Block Offset 0x1C) |
| Name: Timestamp Generator MSW CSR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:31 | MSW Bits | Part 6 | 7.9.7 Timestamp Generator MSW CSR (Block Offset 0x034) |
| Name: Timestamp Generator LSW CSR Offset: 0x38 | | | |
| Bits | Name | Part | Section |
| 0:31 | LSW Bits | Part 6 | 7.9.8 Timestamp Generator LSW CSR (Block Offset 0x038) |
| Name: Port n Timestamp 0 MSW CSRs Offset: 0x44, 0x84, ..., 0x404 | | | |
| Bits | Name | Part | Section |
| 0:31 | MSW Bits | Part 6 | 7.9.9 Port n Timestamp 0 MSW CSRs (Block Offsets 0x44, 0x84, ..., 0x404) |
| Name: Port n Timestamp 0 LSW CSRs Offset: 0x48, 0x88, ..., 0x408 | | | |
| Bits | Name | Part | Section |
| 0:31 | LSW Bits | Part 6 | 7.9.10 Port n Timestamp 0 LSW CSRs (Block Offsets 0x48, 0x88, ..., 0x408) |
| Name: Port n Timestamp 1 MSW CSRs Offset: 0x54, 0x94, ..., 0x414 | | | |
| Bits | Name | Part | Section |
| 0:31 | MSW Bits | Part 6 | 7.9.11 Port n Timestamp 1 MSW CSRs (Block Offsets 0x54, 0x94, ..., 0x414) |
| Name: Port n Timestamp 1 LSW CSRs Offset: 0x58, 0x98, ..., 0x418 | | | |
| Bits | Name | Part | Section |
| 0:31 | LSW Bits | Part 6 | 7.9.12 Port n Timestamp 1 LSW CSRs (Block Offsets 0x58, 0x98, ..., 0x418) |
| Name: Port n Timestamp Generator Synchronization CSRs Offset: 0x60, 0xA0, ..., 0x420 | | | |
| Bits | Name | Part | Section |
| 0 | Accept Timestamps | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| 1 | Disable Clock Compensation Sequence | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| 2 | Auto-update Link Partner Timestamp Generators | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| 3:5 | Reserved | | |
| 6:7 | Port Operating Mode | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| 8:18 | Reserved | | |
| 19 | Tx Has Lower Latency | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| 20:31 | Asymmetry | Part 6 | 7.9.13 Port n Timestamp Generator Synchronization CSRs (Block Offsets 0x60, 0xA0, ..., 0x420) |
| Name: Port n Auto Update Counter CSRs Offset: 0x64, 0xA4, ..., 0x424 | | | |
| Bits | Name | Part | Section |
| 0:31 | Update Period | Part 6 | 7.9.14 Port n Auto Update Counter CSRs (Block Offsets 0x64, 0xA4, ..., 0x424) |
| Name: Port n Timestamp Synchronization Command CSRs Offset: 0x68, 0xA8, ..., 0x428 | | | |
| Bits | Name | Part | Section |
| 0:22 | Reserved | | |
| 23 | Send Zero Timestamp | Part 6 | 7.9.15 Port n Timestamp Synchronization Command CSRs (Block Offsets 0x68, 0xA8, ..., 0x428) |
| 24:26 | Reserved | | |
| 27 | Send Timestamp | Part 6 | 7.9.15 Port n Timestamp Synchronization Command CSRs (Block Offsets 0x68, 0xA8, ..., 0x428) |
| 28 | Reserved | | |
| 29:31 | Command | Part 6 | 7.9.15 Port n Timestamp Synchronization Command CSRs (Block Offsets 0x68, 0xA8, ..., 0x428) |
| Name: Port n Timestamp Synchronization Status CSRs Offset: 0x6C, 0xAC, ..., 0x42C | | | |
| Bits | Name | Part | Section |
| 0 | Response\_valid | Part 6 | 7.9.16 Port n Timestamp Synchronization Status CSRs (Block Offsets 0x6C, 0xAC, ..., 0x42C) |
| 1:21 | Reserved | | |
| 22:31 | Delay | Part 6 | 7.9.16 Port n Timestamp Synchronization Status CSRs (Block Offsets 0x6C, 0xAC, ..., 0x42C) |
| Name: Port n Timestamp Offset CSRs Offset: CSRs (Block Offsets 0x70, 0xB0, ..., 0x430 | | | |
| Bits | Name | Part | Section |
| 0:15 | Offset | Part 6 | 7.9.17 Port n Timestamp Offset CSRs (Block Offsets 0x70, 0xB0, ..., 0x430) |
| 16:31 | Reserved | | |

# Block: 0x0010 : Miscellaneous Physical Layer Extension Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Miscellaneous Physical Layer Extension Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.10.1 Miscellaneous Physical Layer Extension Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.10.1 Miscellaneous Physical Layer Extension Block Header (Block Offset 0x0) |
| Name: Miscellaneous Physical Layer CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0 | SAL Support | Part 6 | 7.10.2 Miscellaneous Physical Layer CAR (Block Offset 0x04) |
| 1 | SMECS Support | Part 6 | 7.10.2 Miscellaneous Physical Layer CAR (Block Offset 0x04) |
| 2 | PRBS Support | Part 6 | 7.10.2 Miscellaneous Physical Layer CAR (Block Offset 0x04) |
| 3:31 | Reserved | | |
| Name: Port n Reinit Control CSR Offset: 0x40, 0x80, 0xC0,..., 0x440 | | | |
| Bits | Name | Part | Section |
| 0:12 | Reserved | | |
| 13:15 | Silence Count | Part 6 | 7.10.3 Port n Reinit Control CSR (Block Offset 0x40, 0x80, 0xC0,..., 0x440) |
| 16:30 | Reserved | | |
| 31 | Pulse Force-Reinit | Part 6 | 7.10.3 Port n Reinit Control CSR (Block Offset 0x40, 0x80, 0xC0,..., 0x440) |
| Name: Port n SAL Control and Status CSR Offset: 0x44, 0x84, 0xC4,..., 0x444 | | | |
| Bits | Name | Part | Section |
| 0 | SAL Enabled | Part 6 | 7.10.4 Port n SAL Control and Status CSR (Block Offset 0x44, 0x84, 0xC4,..., 0x444) |
| 1:11 | Reserved | | |
| 12:15 | SAL RX Width | Part 6 | 7.10.4 Port n SAL Control and Status CSR (Block Offset 0x44, 0x84, 0xC4,..., 0x444) |
| 16:27 | Reserved | | |
| 28:31 | SAL TX Width | Part 6 | 7.10.4 Port n SAL Control and Status CSR (Block Offset 0x44, 0x84, 0xC4,..., 0x444) |
| Name: Port n SMECS Control CSR Offset: 0x48, 0x88, 0xC8,..., 0x448 | | | |
| Bits | Name | Part | Section |
| 0 | Secondary Multicast-Event Participant | Part 6 | 7.10.5 Port n SMECS Control CSR (Block Offset 0x48, 0x88, 0xC8,..., 0x448) |
| 1:31 | Reserved | | |
| Name: Port n PRBS Control CSR Offset: 0x4C, 0x8C, 0xCC,..., 0x44C | | | |
| Bits | Name | Part | Section |
| 0 | PRBS Active | Part 6 | 7.10.6 Port n PRBS Control CSR (Block Offset 0x4C, 0x8C, 0xCC,..., 0x44C) |
| 1 | PRBS Completed | Part 6 | 7.10.6 Port n PRBS Control CSR (Block Offset 0x4C, 0x8C, 0xCC,..., 0x44C) |
| 2:6 | PRBS Pattern Selection | Part 6 | 7.10.6 Port n PRBS Control CSR (Block Offset 0x4C, 0x8C, 0xCC,..., 0x44C) |
| 7:15 | PRBS Lock Interval Threshold | Part 6 | 7.10.6 Port n PRBS Control CSR (Block Offset 0x4C, 0x8C, 0xCC,..., 0x44C) |
| 16:31 | PRBS Test Interval | Part 6 | 7.10.6 Port n PRBS Control CSR (Block Offset 0x4C, 0x8C, 0xCC,..., 0x44C) |
| Name: Port n PRBS Lane Control CSR Offset: 0x50, 0x90, 0xD0,..., 0x450 | | | |
| Bits | Name | Part | Section |
| 0:15 | PRBS Transmit Lane Control | Part 6 | 7.10.7 Port n PRBS Lane Control CSR (Block Offset 0x50, 0x90, 0xD0,..., 0x450) |
| 16:31 | PRBS Receive Lane Control | Part 6 | 7.10.7 Port n PRBS Lane Control CSR (Block Offset 0x50, 0x90, 0xD0,..., 0x450) |
| Name: Port n PRBS Status 0 CSR Offset: 0x54, 0x94, 0xD4,..., 0x454 | | | |
| Bits | Name | Part | Section |
| 0 | Lane 7 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 1:3 | Lane 7 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 4 | Lane 6 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 5:7 | Lane 6 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 8 | Lane 5 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 9:11 | Lane 5 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 12 | Lane 4 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 13:15 | Lane 4 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 16 | Lane 3 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 17:19 | Lane 3 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 20 | Lane 2 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 21:23 | Lane 2 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 24 | Lane 1 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 25:27 | Lane 1 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 28 | Lane 0 PRBS Lock Status | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| 29:31 | Lane 0 PRBS Error Count | Part 6 | 7.10.8 Port n PRBS Status 0 CSR (Block Offset 0x54, 0x94, 0xD4,..., 0x454) |
| Name: Port n PRBS Status 1 CSR Offset: 0x58, 0x98, 0xD8,..., 0x458 | | | |
| Bits | Name | Part | Section |
| 0 | Lane 15 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 1:3 | Lane 15 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 4 | Lane 14 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 5:7 | Lane 14 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 8 | Lane 13 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 9:11 | Lane 13 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 12 | Lane 12 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 13:15 | Lane 12 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 16 | Lane 11 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 17:19 | Lane 11 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 20 | Lane 10 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 21:23 | Lane 10 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 24 | Lane 9 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 25:27 | Lane 9 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 28 | Lane 8 PRBS Lock Status | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| 29:31 | Lane 8 PRBS Error Count | Part 6 | 7.10.9 Port n PRBS Status 1 CSR (Block Offset 0x58, 0x98, 0xD8,..., 0x458) |
| Name: Port n PRBS Locked Time CSR Offset: 0x5C, 0x9C, 0xDC,..., 0x45C | | | |
| Bits | Name | Part | Section |
| 0:15 | All PRBS Locked Time | Part 6 | 7.10.10 Port n PRBS Locked Time CSR (Block Offset 0x5C, 0x9C, 0xDC,..., 0x45C) |
| 16:31 | Reserved | | |
| Name: Port n PRBS Seed CSR Offset: 0x60, 0xA0, 0xE0,..., 0x460 | | | |
| Bits | Name | Part | Section |
| 0:31 | Seed | Part 6 | 7.10.11 Port n PRBS Seed CSR (Block Offset 0x60, 0xA0, 0xE0,..., 0x460) |

# Block: 0x0011 : LP-Serial Register Block

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| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 8C, ... , 40C | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 94, ... , 414 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 98, ... , 418 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 9C, ... , 41C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| Name: Port n Power Management CSRs Offset: 0x68, A8, ... , 428 | | | |
| Bits | Name | Part | Section |
| 0:4 | Asymmetric modes supported | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 5:9 | Asymmetric modes enabled | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 10:12 | Transmit width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 13:15 | Receive width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 16:18 | Change my transmit width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 19:20 | Status of My Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 21:23 | Change Link Partner Transmit Width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 24:25 | Status of Link Partner Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 26:31 | Reserved | | |
| Name: Port n Latency Optimization CSRs Offset: 0x6C, AC, ... , 42C | | | |
| Bits | Name | Part | Section |
| 0 | Multiple Acknowledges Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 1 | Error Recovery with ackID in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 2 | TX AckID\_Status in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 3:7 | Reserved | | |
| 8 | Multiple Acknowledges Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 9 | Error Recovery with ackID in PNA Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 10:31 | Reserved | | |
| Name: Port n Link Timers Control CSRs Offset: 0x70, 0xB0, ... , 0x430 | | | |
| Bits | Name | Part | Section |
| 0:7 | DME Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 8:15 | DME Wait\_Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 16:23 | CW Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 24:31 | Emphasis Command Timeout | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| Name: Port n Link Timers Control 2 CSRs Offset: 0x74, 0xB4, ... , 0x434 | | | |
| Bits | Name | Part | Section |
| 0:7 | Retraining Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 8:15 | Discovery Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 16:23 | Recovery Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 24:31 | Reserved | | |
| Name: Port n Link Timers Control 3 CSRs Offset: 0x78, 0xB8, ... , 0x438 | | | |
| Bits | Name | Part | Section |
| 0:7 | Transmit Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 8:15 | Receive Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 16:21 | Keep-alive Transmission Period | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 22:31 | Keep-alive Transmission Interval | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |

# Block: 0x0012 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 80, ... , 400 | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 7.6.5 Port n Link Maintenance Request CSRs (RM-I Block Offsets 0x40, 60, ... , 220) (RM-II Block Offsets 0x40, 80, ... , 400) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 84, ... , 404 | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 1:2 | Reserved | | |
| 3:14 | port\_status\_cs64 | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 15:26 | ackID\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 27:31 | port\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 8C, ... , 40C | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 94, ... , 414 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 98, ... , 418 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 9C, ... , 41C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| Name: Port n Outbound ackID CSRs Offset: 0x60, 0xA0, ... , 0x420 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| 1:7 | Reserved | | |
| 8:19 | Outstanding\_ackID | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| 20:31 | Outbound\_ackID | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| Name: Port n Inbound ackID CSRs Offset: 0x64, 0xA4, ... , 0x424 | | | |
| Bits | Name | Part | Section |
| 0:19 | Reserved | | |
| 20:31 | Inbound\_ackID | Part 6 | 7.6.13 Port n Inbound ackID CSRs (RM-II Block Offsets 0x64, 0xA4, ... , 0x424) |
| Name: Port n Power Management CSRs Offset: 0x68, A8, ... , 428 | | | |
| Bits | Name | Part | Section |
| 0:4 | Asymmetric modes supported | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 5:9 | Asymmetric modes enabled | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 10:12 | Transmit width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 13:15 | Receive width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 16:18 | Change my transmit width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 19:20 | Status of My Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 21:23 | Change Link Partner Transmit Width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 24:25 | Status of Link Partner Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 26:31 | Reserved | | |
| Name: Port n Latency Optimization CSRs Offset: 0x6C, AC, ... , 42C | | | |
| Bits | Name | Part | Section |
| 0 | Multiple Acknowledges Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 1 | Error Recovery with ackID in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 2 | TX AckID\_Status in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 3:7 | Reserved | | |
| 8 | Multiple Acknowledges Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 9 | Error Recovery with ackID in PNA Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 10:31 | Reserved | | |
| Name: Port n Link Timers Control CSRs Offset: 0x70, 0xB0, ... , 0x430 | | | |
| Bits | Name | Part | Section |
| 0:7 | DME Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 8:15 | DME Wait\_Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 16:23 | CW Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 24:31 | Emphasis Command Timeout | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| Name: Port n Link Timers Control 2 CSRs Offset: 0x74, 0xB4, ... , 0x434 | | | |
| Bits | Name | Part | Section |
| 0:7 | Retraining Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 8:15 | Discovery Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 16:23 | Recovery Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 24:31 | Reserved | | |
| Name: Port n Link Timers Control 3 CSRs Offset: 0x78, 0xB8, ... , 0x438 | | | |
| Bits | Name | Part | Section |
| 0:7 | Transmit Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 8:15 | Receive Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 16:21 | Keep-alive Transmission Period | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 22:31 | Keep-alive Transmission Interval | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |

# Block: 0x0013 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 8C, ... , 40C | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 94, ... , 414 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 98, ... , 418 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 9C, ... , 41C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| Name: Port n Power Management CSRs Offset: 0x68, A8, ... , 428 | | | |
| Bits | Name | Part | Section |
| 0:4 | Asymmetric modes supported | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 5:9 | Asymmetric modes enabled | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 10:12 | Transmit width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 13:15 | Receive width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 16:18 | Change my transmit width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 19:20 | Status of My Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 21:23 | Change Link Partner Transmit Width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 24:25 | Status of Link Partner Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 26:31 | Reserved | | |
| Name: Port n Latency Optimization CSRs Offset: 0x6C, AC, ... , 42C | | | |
| Bits | Name | Part | Section |
| 0 | Multiple Acknowledges Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 1 | Error Recovery with ackID in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 2 | TX AckID\_Status in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 3:7 | Reserved | | |
| 8 | Multiple Acknowledges Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 9 | Error Recovery with ackID in PNA Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 10:31 | Reserved | | |
| Name: Port n Link Timers Control CSRs Offset: 0x70, 0xB0, ... , 0x430 | | | |
| Bits | Name | Part | Section |
| 0:7 | DME Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 8:15 | DME Wait\_Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 16:23 | CW Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 24:31 | Emphasis Command Timeout | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| Name: Port n Link Timers Control 2 CSRs Offset: 0x74, 0xB4, ... , 0x434 | | | |
| Bits | Name | Part | Section |
| 0:7 | Retraining Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 8:15 | Discovery Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 16:23 | Recovery Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 24:31 | Reserved | | |
| Name: Port n Link Timers Control 3 CSRs Offset: 0x78, 0xB8, ... , 0x438 | | | |
| Bits | Name | Part | Section |
| 0:7 | Transmit Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 8:15 | Receive Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 16:21 | Keep-alive Transmission Period | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 22:31 | Keep-alive Transmission Interval | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |

# Block: 0x0017 : Error Management Extensions Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Error Management Extensions Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 8 | 2.5.1 Error Management Extensions Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 8 | 2.5.1 Error Management Extensions Block Header (Block Offset 0x0) |
| Name: Error Management/Hot Swap Extension Block CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0 | Error Management Extensions Not Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 1 | Hot Swap Extensions Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 2 | Physical Layer Error Capture FIFO Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 3 | Logical/Transport Layer Error Capture FIFO Implemented | Part 8 | 2.5.2 Error Management/Hot Swap Extension Block CAR (Block Offset 0x4) |
| 4:31 | Reserved | | |
| Name: Port-Write Target deviceID CSR Offset: 0x28 | | | |
| Bits | Name | Part | Section |
| 0:7 | Dev16\_deviceID\_msb | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 8:15 | Dev8\_deviceID | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 16 | Dev8\_or\_16 | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 17 | Dev32\_PW | Part 8 | 2.5.11 Port-Write Target deviceID CSR (Block Offset 0x28) |
| 18:31 | Reserved | | |
| Name: Packet Time-to-live CSR Offset: 0x2C | | | |
| Bits | Name | Part | Section |
| 0:15 | Time-to-live value | Part 8 | 2.5.12 Packet Time-to-live CSR (Block Offset 0x2C) |
| 16:31 | Reserved | | |
| Name: Port-write Dev32 Target deviceID CSR Offset: 0x30 | | | |
| Bits | Name | Part | Section |
| 0:31 | Dev32\_deviceID | Part 8 | 2.5.13 Port-write Dev32 Target deviceID CSR (Block Offset 0x30) |
| Name: Port-Write Transmission Control CSR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:30 | Reserved | | |
| 31 | Port-write Transmission Disable | Part 8 | 2.5.14 Port-Write Transmission Control CSR (Block Offset 0x34) |
| Name: Port n Error Detect CSR Offset: 0x40, 80,..., 400 | | | |
| Bits | Name | Part | Section |
| 0 | Reserved | | |
| 1 | Link OK to Uninit Transition | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 2 | Link Uninit Packet Discard Active | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 3 | Link Uninit to OK Transition | Part 8 | 2.5.15 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 4:31 | Reserved | | |
| Name: Port n Error Rate Enable CSR Offset: 0x44, 84,..., 404 | | | |
| Bits | Name | Part | Section |
| 0 | Reserved | | |
| 1 | Link OK to Uninit Transition Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 2 | Link Uninit Packet Discard Active Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 3 | Link Uninit to OK Transition Enable | Part 8 | 2.5.16 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 4:31 | Reserved | | |
| Name: Port n Link Uninit Discard Timer CSR Offset: 0x70, 0xB0, ..., 0x430 | | | |
| Bits | Name | Part | Section |
| 0:23 | Link Uninit Timeout | Part 8 | 2.5.25 Port n Link Uninit Discard Timer CSR (Block Offset 0x70, 0xB0, ..., 0x430) |
| 24:31 | Reserved | | |

# Block: 0x0019 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 7.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 7.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 7.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 80, ... , 400 | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 7.6.5 Port n Link Maintenance Request CSRs (RM-I Block Offsets 0x40, 60, ... , 220) (RM-II Block Offsets 0x40, 80, ... , 400) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 84, ... , 404 | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 1:2 | Reserved | | |
| 3:14 | port\_status\_cs64 | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 15:26 | ackID\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| 27:31 | port\_status | Part 6 | 7.6.6 Port n Link Maintenance Response CSRs (RM-I Block Offsets 0x44, 64, ... , 224) (RM-II Block Offsets 0x44, 84, ... , 404) |
| Name: Port n Initialization Status CSRs Offset: 0x4C, 8C, ... , 40C | | | |
| Bits | Name | Part | Section |
| 0:4 | Lane Alignment | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 5 | Reserved | | |
| 6:9 | 1x/2x Mode Detection | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 10 | Reserved | | |
| 11:15 | Port Initialization State Machine | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 16:19 | Received status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 20 | Reserved | | |
| 21:27 | Transmitted status control symbols | Part 6 | 7.6.8 Port n Initialization Status CSRs (RM-I Block Offsets 0x4C, 6C, ... , 22C) (RM-II Block Offsets 0x4C, 8C, ... , 40C) |
| 28:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 94, ... , 414 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 4 | Baudrate Discovery Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 5 | Baudrate Discovery Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 6 | 1.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 7 | 1.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 8 | 2.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 9 | 2.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 10 | 3.125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 11 | 3.125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 12 | 5.0 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 13 | 5.0 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 14 | 6.25 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 15 | 6.25 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 16 | 10.3125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 17 | 10.3125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 18 | 12.5 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 19 | 12.5 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 20 | 25.78125 Gbaud Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 21 | 25.78125 Gbaud Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 22:26 | Reserved | | |
| 27 | 10G Retraining Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 28 | Enable Inactive Lanes | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 29 | Data scrambling disable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 7.6.9 Port n Control 2 CSRs (RM-I Block Offset 0x54, 74, ... , 234) (RM-II Block Offset 0x54, 94, ... , 414) |
| Name: Port n Error and Status CSRs Offset: 0x58, 98, ... , 418 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 1 | Idle Sequence 2 Enable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 2:3 | Idle Sequence | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 4 | Flow Control Mode | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 5 | Output Packet-dropped | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 6 | Output Failed-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 7 | Output Degraded-encountered | Part 8 | 2.2.2 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 8 | IDLE3 Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 9 | IDLE3 Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 12 | Output Retried | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 13 | Output Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 14 | Output Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 15 | Output Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 22 | Input Error-encountered | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 23 | Input Error-stopped | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 24 | DME Supported | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 25 | DME Enabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 26 | Port-write Disabled | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 27 | Port-write Pending | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 28 | Port Unavailable | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 29 | Port Error | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 30 | Port OK | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| 31 | Port Uninitialized | Part 6 | 7.6.10 Port n Error and Status CSRs (RM-I Block Offset 0x58, 78, ... , 238) (RM-II Block Offset 0x58, 98, ... , 418) |
| Name: Port n Control CSRs Offset: 0x5C, 9C, ... , 41C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 2:4 | Initialized Port Width | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 5:7 | Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 8 | Port Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 9 | Output Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 10 | Input Port Enable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 11 | Error Checking Disable | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 12 | Multicast-event Participant | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 13 | Flow Control Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 14 | Enumeration Boundary | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.2.2 Port n Control CSR (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 16:17 | Extended Port Width Override | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 18:19 | Extended Port Width Support | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 20:27 | Implementation-defined | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 29 | Drop Packet Enable | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 30 | Port Lockout | Part 8 | 2.2.1 Port n Control CSRs (RM-I Block Offset 0x5C, 7C, ... , 23C) (RM-II Block Offset 0x5C, 9C, ... , 41C) |
| 31 | Port Type | Part 6 | 7.6.11 Port n Control CSRs (RM-I Block Offsets 0x5C, 7C, ... , 23C) (RM-II Block Offsets 0x5C, 9C, ... , 41C) |
| Name: Port n Outbound ackID CSRs Offset: 0x60, 0xA0, ... , 0x420 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| 1:7 | Reserved | | |
| 8:19 | Outstanding\_ackID | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| 20:31 | Outbound\_ackID | Part 6 | 7.6.12 Port n Outbound ackID CSRs (RM-II Block Offsets 0x60, 0xA0, ... , 0x420) |
| Name: Port n Inbound ackID CSRs Offset: 0x64, 0xA4, ... , 0x424 | | | |
| Bits | Name | Part | Section |
| 0:19 | Reserved | | |
| 20:31 | Inbound\_ackID | Part 6 | 7.6.13 Port n Inbound ackID CSRs (RM-II Block Offsets 0x64, 0xA4, ... , 0x424) |
| Name: Port n Power Management CSRs Offset: 0x68, A8, ... , 428 | | | |
| Bits | Name | Part | Section |
| 0:4 | Asymmetric modes supported | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 5:9 | Asymmetric modes enabled | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 10:12 | Transmit width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 13:15 | Receive width status | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 16:18 | Change my transmit width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 19:20 | Status of My Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 21:23 | Change Link Partner Transmit Width | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 24:25 | Status of Link Partner Transmit Width Change | Part 6 | 7.6.14 Port n Power Management CSRs (RM-II Block Offsets 0x68, A8, ... , 428) |
| 26:31 | Reserved | | |
| Name: Port n Latency Optimization CSRs Offset: 0x6C, AC, ... , 42C | | | |
| Bits | Name | Part | Section |
| 0 | Multiple Acknowledges Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 1 | Error Recovery with ackID in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 2 | TX AckID\_Status in PNA Supported | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 3:7 | Reserved | | |
| 8 | Multiple Acknowledges Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 9 | Error Recovery with ackID in PNA Enabled | Part 6 | 7.6.15 Port n Latency Optimization CSRs (RM-II Block Offset 0x6C, AC, ... , 42C) |
| 10:31 | Reserved | | |
| Name: Port n Link Timers Control CSRs Offset: 0x70, 0xB0, ... , 0x430 | | | |
| Bits | Name | Part | Section |
| 0:7 | DME Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 8:15 | DME Wait\_Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 16:23 | CW Training Completion Timer | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| 24:31 | Emphasis Command Timeout | Part 6 | 7.6.16 Port n Link Timers Control CSRs (RM-II Block Offsets 0x70, 0xB0, ... , 0x430) |
| Name: Port n Link Timers Control 2 CSRs Offset: 0x74, 0xB4, ... , 0x434 | | | |
| Bits | Name | Part | Section |
| 0:7 | Retraining Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 8:15 | Discovery Completion Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 16:23 | Recovery Timer | Part 6 | 7.6.17 Port n Link Timers Control 2 CSRs (RM-II Block Offsets 0x74, 0xB4, ... , 0x434) |
| 24:31 | Reserved | | |
| Name: Port n Link Timers Control 3 CSRs Offset: 0x78, 0xB8, ... , 0x438 | | | |
| Bits | Name | Part | Section |
| 0:7 | Transmit Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 8:15 | Receive Width Command Timeout | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 16:21 | Keep-alive Transmission Period | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |
| 22:31 | Keep-alive Transmission Interval | Part 6 | 7.6.18 Port n Link Timers Control 3 CSRs (RM-II Block Offsets 0x78, 0xB8, ... , 0x438) |

# Block: STD\_REG : Device Identity CAR

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Device Identity CAR Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | DeviceIdentity | Part 1 | 5.4.1 Device Identity CAR (Configuration Space Offset 0x0) |
| 16:31 | DeviceVendorIdentity | Part 1 | 5.4.1 Device Identity CAR (Configuration Space Offset 0x0) |
| Name: Device Information CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0:31 | DeviceRev | Part 1 | 5.4.2 Device Information CAR (Configuration Space Offset 0x4) |
| Name: Assembly Identity CAR Offset: 0x08 | | | |
| Bits | Name | Part | Section |
| 0:15 | AssyIdentity | Part 1 | 5.4.3 Assembly Identity CAR (Configuration Space Offset 0x8) |
| 16:31 | AssyVendorIdentity | Part 1 | 5.4.3 Assembly Identity CAR (Configuration Space Offset 0x8) |
| Name: Assembly Information CAR Offset: 0x0C | | | |
| Bits | Name | Part | Section |
| 0:15 | AssyRev | Part 1 | 5.4.4 Assembly Information CAR (Configuration Space Offset 0xC) |
| 16:31 | ExtendedFeaturesPtr | Part 1 | 5.4.4 Assembly Information CAR (Configuration Space Offset 0xC) |
| Name: Processing Element Features CAR Offset: 0x10 | | | |
| Bits | Name | Part | Section |
| 0 | Bridge | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 1 | Memory | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 2 | Processor | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 3 | Switch | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 4 | Multiport | Part 6 | 7.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 5:9 | Reserved | | |
| 10 | Error Free Mode support | Part 6 | 7.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 11:18 | Reserved | | |
| 19 | Dev32 Support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 20 | Flow Arbitration Support | Part 9 | 4.2.1 Processing Elements Features CAR (Offset 0x10 Word 0) |
| 21 | Multicast Support | Part 11 | 3.2.1 Processing Elements Features CAR (Configuration Space Offset 0x10) |
| 22 | Extended route table configuration support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 23 | Standard route table configuration support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 24 | Flow Control Support | Part 9 | 4.2.1 Processing Elements Features CAR (Offset 0x10 Word 0) |
| 25 | Implementation-defined | Part 6 | 7.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 26 | CRF Support | Part 6 | 7.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 27 | Dev16 support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 28 | Extended features | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 29:31 | Extended addressing support | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| Name: Switch Port Information CAR Offset: 0x14 | | | |
| Bits | Name | Part | Section |
| 0:15 | Reserved | | |
| 16:23 | PortTotal | Part 1 | 5.4.6 Switch Port Information CAR (Configuration Space Offset 0x14) |
| 24:31 | PortNumber | Part 1 | 5.4.6 Switch Port Information CAR (Configuration Space Offset 0x14) |
| Name: Source Operations CAR Offset: 0x18 | | | |
| Bits | Name | Part | Section |
| 0 | Read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 1 | Instruction read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 2 | Read-for-ownership | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 3 | Data cache invalidate | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 4 | Castout | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 5 | Data cache flush | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 6 | I/O read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 7 | Instruction cache invalidate | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 8 | TLB invalidate-entry | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 9 | TLB invalidate-entry sync | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 10:11 | Reserved | | |
| 12 | Data streaming traffic management | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 13 | Data streaming | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 14:15 | Implementation defined | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 16 | Read | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 17 | Write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 18 | Streaming-write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 19 | Write-with-response | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 20 | Data message | Part 2 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 21 | Doorbell | Part 2 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 22 | Atomic (compare-and-swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 23 | Atomic (test-and-swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 24 | Atomic (increment) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 25 | Atomic (decrement) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 26 | Atomic (set) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 27 | Atomic (clear) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 28 | Atomic (swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 29 | Port-write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 30:31 | Implementation defined | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| Name: Destination Operations CAR Offset: 0x1C | | | |
| Bits | Name | Part | Section |
| 0 | Read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 1 | Instruction read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 2 | Read-for-ownership | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 3 | Data cache invalidate | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 4 | Castout | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 5 | Data cache flush | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 6 | I/O read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 7 | Instruction cache invalidate | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 8 | TLB invalidate-entry | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 9 | TLB invalidate-entry sync | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 10:11 | Reserved | | |
| 12 | Data streaming traffic management | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 13 | Data streaming | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 14:15 | Implementation defined | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 16 | Read | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 17 | Write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 18 | Streaming-write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 19 | Write-with-response | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 20 | Data message | Part 2 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 21 | Doorbell | Part 2 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 22 | Atomic (compare-and-swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 23 | Atomic (test-and-swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 24 | Atomic (increment) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 25 | Atomic (decrement) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 26 | Atomic (set) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 27 | Atomic (clear) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 28 | Atomic (swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 29 | Port-write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 30:31 | Implementation defined | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| Name: Switch Multicast Support CAR Offset: 0x30 | | | |
| Bits | Name | Part | Section |
| 0 | Simple\_Assoc | Part 11 | 3.2.2 Switch Multicast Support CAR (Configuration Space Offset 0x30) |
| 1:31 | Reserved | | |
| Name: Switch Route Table Destination ID Limit CAR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:15 | Reserved | | |
| 16:31 | Max\_destID | Part 3 | 3.4.2 Switch Route Table Destination ID Limit CAR (Configuration Space Offset 0x34) |
| Name: Switch Multicast Information CAR Offset: 0x38 | | | |
| Bits | Name | Part | Section |
| 0 | Block\_Assoc | Part 11 | 3.2.3 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 1 | Per\_Port\_Assoc | Part 11 | 3.2.3 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 2:15 | MaxDestIDAssoc | Part 11 | 3.2.3 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 16:31 | MaxMcastMasks | Part 11 | 3.2.3 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| Name: Data Streaming Information CAR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:15 | MaxPDU | Part 10 | 5.5.3 Data Streaming Information CAR (Configuration Space Offset 0x3C) |
| 16:31 | SegSupport | Part 10 | 5.5.3 Data Streaming Information CAR (Configuration Space Offset 0x3C) |
| Name: Data Streaming Logical Layer Control CSR Offset: 0x48 | | | |
| Bits | Name | Part | Section |
| 0:3 | TM Types Supported (read only) | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| 4:7 | TM Mode | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| 8:23 | Reserved | | |
| 24:31 | MTU | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| Name: Processing Element Logical Layer Control CSR Offset: 0x4C | | | |
| Bits | Name | Part | Section |
| 0:25 | Reserved | | |
| 26:27 | LCS Disable | Part 1 | 5.5.1 Processing Element Logical Layer Control CSR (Configuration Space Offset 0x4C) |
| 28 | LCS Disable Present | Part 1 | 5.5.1 Processing Element Logical Layer Control CSR (Configuration Space Offset 0x4C) |
| 29:31 | Extended addressing control | Part 1 | 5.5.1 Processing Element Logical Layer Control CSR (Configuration Space Offset 0x4C) |
| Name: Local Configuration Space Base Address 0 CSR Offset: 0x58 | | | |
| Bits | Name | Part | Section |
| 0 | Reserved | | |
| 1:16 | LCSBA | Part 1 | 5.5.2 Local Configuration Space Base Address 0 CSR (Configuration Space Offset 0x58) |
| 17:31 | LCSBA | Part 1 | 5.5.2 Local Configuration Space Base Address 0 CSR (Configuration Space Offset 0x58) |
| Name: Local Configuration Space Base Address 1 CSR Offset: 0x5C | | | |
| Bits | Name | Part | Section |
| 0 | LCSBA | Part 1 | 5.5.3 Local Configuration Space Base Address 1 CSR (Configuration Space Offset 0x5C) |
| 1:31 | LCSBA | Part 1 | 5.5.3 Local Configuration Space Base Address 1 CSR (Configuration Space Offset 0x5C) |
| Name: Base Device ID CSR Offset: 0x60 | | | |
| Bits | Name | Part | Section |
| 0:7 | Reserved | | |
| 8:15 | Dev8\_Base\_deviceID | Part 3 | 3.5.1 Base Device ID CSR (Configuration Space Offset 0x60) |
| 16:31 | Dev16\_base\_deviceID | Part 3 | 3.5.1 Base Device ID CSR (Configuration Space Offset 0x60) |
| Name: Dev32 Base Device ID CSR Offset: 0x64 | | | |
| Bits | Name | Part | Section |
| 0:31 | Dev32\_Base\_DeviceID | Part 3 | 3.5.2 Dev32 Base Device ID CSR (Configuration Space Offset 0x64) |
| Name: Host Base Device ID Lock CSR Offset: 0x68 | | | |
| Bits | Name | Part | Section |
| 0:15 | Host\_base\_Dev32ID | Part 3 | 3.5.3 Host Base Device ID Lock CSR (Configuration Space Offset 0x68) |
| 16:31 | Host\_base\_deviceID | Part 3 | 3.5.3 Host Base Device ID Lock CSR (Configuration Space Offset 0x68) |
| Name: Component Tag CSR Offset: 0x6C | | | |
| Bits | Name | Part | Section |
| 0:31 | component\_tag | Part 3 | 3.5.4 Component Tag CSR (Configuration Space Offset 0x6C) |
| Name: Standard Route Cfg Destination ID Select CSR Offset: 0x70 | | | |
| Bits | Name | Part | Section |
| 0 | Ext\_config\_en | Part 3 | 3.5.5 Standard Route Cfg Destination ID Select CSR (Configuration Space Offset 0x70) |
| 1:15 | Reserved | | |
| 16:23 | Config\_destID\_msb | Part 3 | 3.5.5 Standard Route Cfg Destination ID Select CSR (Configuration Space Offset 0x70) |
| 24:31 | Config\_destID | Part 3 | 3.5.5 Standard Route Cfg Destination ID Select CSR (Configuration Space Offset 0x70) |
| Name: Standard Route Cfg Port Select CSR Offset: 0x74 | | | |
| Bits | Name | Part | Section |
| 0:3 | Cop3\_msb\_or\_imp\_spec | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| 4:7 | Config\_output\_port3\_lsb | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| 8:15 | Config\_output\_port2 | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| 16:21 | Config\_output\_port1\_msb | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| 22:23 | Config\_output\_port1\_lsb | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| 24:31 | Config\_output\_port | Part 3 | 3.5.6 Standard Route Cfg Port Select CSR (Configuration Space Offset 0x74) |
| Name: Standard Route Default Port CSR Offset: 0x78 | | | |
| Bits | Name | Part | Section |
| 0:3 | Implementation Specific | Part 3 | 3.5.7 Standard Route Default Port CSR (Configuration Space Offset 0x78) |
| 4:21 | Reserved | | |
| 22:23 | Route Type | Part 3 | 3.5.7 Standard Route Default Port CSR (Configuration Space Offset 0x78) |
| 24:31 | Default\_output\_port | Part 3 | 3.5.7 Standard Route Default Port CSR (Configuration Space Offset 0x78) |
| Name: Multicast Mask Port CSR Offset: 0x80 | | | |
| Bits | Name | Part | Section |
| 0:15 | Mcast\_Mask | Part 11 | 3.3.1 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 16:23 | Egress\_Port\_Num | Part 11 | 3.3.1 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 24 | Reserved | | |
| 25:27 | Mask\_Cmd | Part 11 | 3.3.1 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 28:30 | Reserved | | |
| 31 | Port\_Present | Part 11 | 3.3.1 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| Name: Multicast Associate Select CSR Offset: 0x84 | | | |
| Bits | Name | Part | Section |
| 0:7 | Large\_DestID | Part 11 | 3.3.2 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| 8:15 | DestID | Part 11 | 3.3.2 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| 16:31 | Mcast\_Mask\_Num | Part 11 | 3.3.2 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| Name: Multicast Associate Operation CSR Offset: 0x88 | | | |
| Bits | Name | Part | Section |
| 0:15 | Assoc\_Blksize | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 16:23 | Ingress\_Port | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 24 | Large\_Transport | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 25:26 | Assoc\_Cmd | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 27:30 | - | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 31 | Assoc\_Present | Part 11 | 3.3.3 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |