Registers Summary First Cut

Autogenerated register summary from file **Register\_Summaries/register\_summary\_2.2.txt. Generated** 2020-05-31 15:45:21

Note that registers are defined using big endian notation. Bit 0 is the most significant bit!

# Block: 0x0001 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 4 | Baudrate Discovery Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 5 | Baudrate Discovery Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 6 | 1.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 7 | 1.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 8 | 2.5 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 9 | 2.5 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 10 | 3.125 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 11 | 3.125 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 12 | 5.0 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 13 | 5.0 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 14 | 6.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 15 | 6.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 16:27 | Reserved | | |
| 28 | Enable Inactive Lanes | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 29 | Data scrambling disable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 1 | Idle Sequence 2 Enable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 2 | Idle Sequence | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 3 | Reserved | | |
| 4 | Flow Control Mode | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 5 | Output Packet-dropped | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 6 | Output Failed-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 7 | Output Degraded-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 8:10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 12 | Output Retried | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 13 | Output Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 14 | Output Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 15 | Output Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 22 | Input Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 23 | Input Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 24:26 | Reserved | | |
| 27 | Port-write Pending | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 28 | Port Unavailable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 29 | Port Error | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 30 | Port OK | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 31 | Port Uninitialized | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 2:4 | Initialized Port Width | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 5:7 | Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 8 | Port Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 9 | Output Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 10 | Input Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 11 | Error Checking Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 12 | Multicast-event Participant | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 13 | Flow Control Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 14 | Enumeration Boundary | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 16:17 | Extended Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 18:19 | Extended Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 20:27 | Implementation-defined | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 29 | Drop Packet Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 30 | Port Lockout | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 31 | Port Type | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |

# Block: 0x0002 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port Response Timeout Control CSR Offset: 0x24 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.3 Port Response Timeout Control CSR (Block Offset 0x24) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0 | Host | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 1 | Master Enable | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 2 | Discovered | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 60, ... , 220 | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 6.6.5 Port n Link Maintenance Request CSRs (Block Offsets 0x40, 60, ... , 220) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 64, ... , 224 | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| 1:20 | Reserved | | |
| 21:26 | ackID\_status | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| 27:31 | port\_status | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| Name: Port n Local ackID CSRs Offset: 0x48, 68, ... , 228 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 1 | Reserved | | |
| 2:7 | Inbound\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 8:17 | Reserved | | |
| 18:23 | Outstanding\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 24:25 | Reserved | | |
| 26:31 | Outbound\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 4 | Baudrate Discovery Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 5 | Baudrate Discovery Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 6 | 1.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 7 | 1.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 8 | 2.5 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 9 | 2.5 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 10 | 3.125 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 11 | 3.125 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 12 | 5.0 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 13 | 5.0 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 14 | 6.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 15 | 6.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 16:27 | Reserved | | |
| 28 | Enable Inactive Lanes | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 29 | Data scrambling disable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 1 | Idle Sequence 2 Enable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 2 | Idle Sequence | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 3 | Reserved | | |
| 4 | Flow Control Mode | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 5 | Output Packet-dropped | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 6 | Output Failed-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 7 | Output Degraded-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 8:10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 12 | Output Retried | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 13 | Output Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 14 | Output Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 15 | Output Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 22 | Input Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 23 | Input Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 24:26 | Reserved | | |
| 27 | Port-write Pending | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 28 | Port Unavailable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 29 | Port Error | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 30 | Port OK | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 31 | Port Uninitialized | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 2:4 | Initialized Port Width | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 5:7 | Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 8 | Port Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 9 | Output Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 10 | Input Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 11 | Error Checking Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 12 | Multicast-event Participant | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 13 | Flow Control Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 14 | Enumeration Boundary | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 16:17 | Extended Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 18:19 | Extended Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 20:27 | Implementation-defined | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 29 | Drop Packet Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 30 | Port Lockout | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 31 | Port Type | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |

# Block: 0x0003 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 4 | Baudrate Discovery Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 5 | Baudrate Discovery Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 6 | 1.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 7 | 1.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 8 | 2.5 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 9 | 2.5 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 10 | 3.125 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 11 | 3.125 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 12 | 5.0 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 13 | 5.0 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 14 | 6.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 15 | 6.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 16:27 | Reserved | | |
| 28 | Enable Inactive Lanes | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 29 | Data scrambling disable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 1 | Idle Sequence 2 Enable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 2 | Idle Sequence | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 3 | Reserved | | |
| 4 | Flow Control Mode | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 5 | Output Packet-dropped | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 6 | Output Failed-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 7 | Output Degraded-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 8:10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 12 | Output Retried | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 13 | Output Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 14 | Output Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 15 | Output Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 22 | Input Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 23 | Input Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 24:26 | Reserved | | |
| 27 | Port-write Pending | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 28 | Port Unavailable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 29 | Port Error | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 30 | Port OK | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 31 | Port Uninitialized | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 2:4 | Initialized Port Width | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 5:7 | Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 8 | Port Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 9 | Output Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 10 | Input Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 11 | Error Checking Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 12 | Multicast-event Participant | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 13 | Flow Control Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 14 | Enumeration Boundary | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 16:17 | Extended Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 18:19 | Extended Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 20:27 | Implementation-defined | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 29 | Drop Packet Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 30 | Port Lockout | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 31 | Port Type | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |

# Block: 0x0007 : Error Management Extensions Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Error Management Extensions Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 8 | 2.3.2.1 Error Management Extensions Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 8 | 2.3.2.1 Error Management Extensions Block Header (Block Offset 0x0) |
| Name: Logical/Transport Layer Error Detect CSR Offset: 0x08 | | | |
| Bits | Name | Part | Section |
| 0 | IO error response | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 1 | Message error response | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 2 | GSM error response | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 3 | Message Format Error | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 4 | Illegal transaction decode | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 5 | Illegal transaction target error | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 6 | Message Request Timeout | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 7 | Packet Response Timeout | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 8 | Unsolicited Response | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 9 | Unsupported Transaction | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| 10 | Missing data streaming context | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 11 | Open existing data streaming context | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 12 | Long data streaming segment | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 13 | Short data streaming segment | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 14 | Data streaming PDU length error | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x08) |
| 15:23 | Reserved | | |
| 24:31 | Implementation Specific error | Part 8 | 2.3.2.2 Logical/Transport Layer Error Detect CSR (Block Offset 0x08) |
| Name: Logical/Transport Layer Error Enable CSR Offset: 0x0C | | | |
| Bits | Name | Part | Section |
| 0 | IO error response enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 1 | Message error response enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 2 | GSM error response enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 3 | Message Format Error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 4 | Illegal transaction decode enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 5 | Illegal transaction target error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 6 | Message Request timeout error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 7 | Packet Response Timeout error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 8 | Unsolicited Response error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 9 | Unsupported Transaction error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| 10 | Missing data streaming context error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 11 | Open existing data streaming context error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 12 | Long data streaming segment error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 13 | Short data streaming segment error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 14 | Data streaming PDU length error error enable | Part 10 | 5.4 Additions to Existing Registers (Block Offset 0x0C) |
| 15:23 | Reserved | | |
| 24:31 | Implementation Specific error enable | Part 8 | 2.3.2.3 Logical/Transport Layer Error Enable CSR (Block Offset 0x0C) |
| Name: Logical/Transport Layer High Address Capture CSR Offset: 0x10 | | | |
| Bits | Name | Part | Section |
| 0:31 | address[0-31] | Part 8 | 2.3.2.4 Logical/Transport Layer High Address Capture CSR (Block Offset 0x10) |
| Name: Logical/Transport Layer Address Capture CSR Offset: 0x14 | | | |
| Bits | Name | Part | Section |
| 0:28 | address[32-60] | Part 8 | 2.3.2.5 Logical/Transport Layer Address Capture CSR (Block Offset 0x14) |
| 29 | Reserved | | |
| 30:31 | xamsbs | Part 8 | 2.3.2.5 Logical/Transport Layer Address Capture CSR (Block Offset 0x14) |
| Name: Logical/Transport Layer Device ID Capture CSR Offset: 0x18 | | | |
| Bits | Name | Part | Section |
| 0:7 | MSB destinationID | Part 8 | 2.3.2.6 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 8:15 | destinationID | Part 8 | 2.3.2.6 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 16:23 | MSB sourceID | Part 8 | 2.3.2.6 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| 24:31 | sourceID | Part 8 | 2.3.2.6 Logical/Transport Layer Device ID Capture CSR (Block Offset 0x18) |
| Name: Logical/Transport Layer Control Capture CSR Offset: 0x1C | | | |
| Bits | Name | Part | Section |
| 0:3 | ftype | Part 8 | 2.3.2.7 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 4:7 | ttype | Part 8 | 2.3.2.7 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 8:15 | msg info | Part 8 | 2.3.2.7 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| 16:31 | Implementation specific | Part 8 | 2.3.2.7 Logical/Transport Layer Control Capture CSR (Block Offset 0x1C) |
| Name: Port-write Target deviceID CSR Offset: 0x28 | | | |
| Bits | Name | Part | Section |
| 0:7 | deviceID\_msb | Part 8 | 2.3.2.8 Port-write Target deviceID CSR (Block Offset 0x28) |
| 8:15 | deviceID | Part 8 | 2.3.2.8 Port-write Target deviceID CSR (Block Offset 0x28) |
| 16 | large\_transport | Part 8 | 2.3.2.8 Port-write Target deviceID CSR (Block Offset 0x28) |
| 17:31 | Reserved | | |
| Name: Packet Time-to-live CSR Offset: 0x2C | | | |
| Bits | Name | Part | Section |
| 0:15 | Time-to-live value | Part 8 | 2.3.2.9 Packet Time-to-live CSR (Block Offset 0x2C) |
| 16:31 | Reserved | | |
| Name: Port n Error Detect CSR Offset: 0x40, 80,..., 400 | | | |
| Bits | Name | Part | Section |
| 0 | Implementation specific error | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 1:7 | Reserved | | |
| 8 | Received S-bit error | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 9 | Received corrupt control symbol | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 10 | Received acknowledge control symbol with unexpected ackID | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 11 | Received packet-not-accepted control symbol | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 12 | Received packet with unexpected ackID | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 13 | Received packet with bad CRC | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 14 | Received packet exceeds 276 Bytes | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 15 | Received illegal or invalid character | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 16 | Received data character in IDLE1 sequence | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 17 | Loss of descrambler synchronization | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 18:25 | Reserved | | |
| 26 | Non-outstanding ackID | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 27 | Protocol error | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 28 | Frame toggle edge error | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 29 | Delineation error | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 30 | Unsolicited acknowledgement control symbol | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| 31 | Link timeout | Part 8 | 2.3.2.10 Port n Error Detect CSR (Block Offset 0x40, 80,..., 400) |
| Name: Port n Error Rate Enable CSR Offset: 0x44, 84,..., 404 | | | |
| Bits | Name | Part | Section |
| 0 | Implementation specific error enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 1:7 | Reserved | | |
| 8 | Received S-bit error enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 9 | Received corrupt control symbol enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 10 | Received out-of-sequence acknowledgement control symbol enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 11 | Received packet-not-accepted control symbol enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 12 | Received packet with unexpected ackID enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 13 | Received packet with bad CRC enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 14 | Received packet exceeds 276 Bytes enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 15 | Received illegal or invalid character enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 16 | Received data character in an IDLE1 sequence enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 17 | Loss of descrambler synchronization enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 18:25 | Reserved | | |
| 26 | Non-outstanding ackID enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 27 | Protocol error enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 28 | Frame toggle edge error enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 29 | Delineation error enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 30 | Unsolicited acknowledgement control symbol enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| 31 | Link timeout enable | Part 8 | 2.3.2.11 Port n Error Rate Enable CSR (Block Offset 0x44, 84,..., 404) |
| Name: Port n Attributes Capture CSR Offset: 0x48, 88,..., 408 | | | |
| Bits | Name | Part | Section |
| 0:2 | Info type | Part 8 | 2.3.2.12 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 3:7 | Error type | Part 8 | 2.3.2.12 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 8:27 | Implementation Dependent | Part 8 | 2.3.2.12 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| 28:30 | Reserved | | |
| 31 | Capture valid info | Part 8 | 2.3.2.12 Port n Attributes Capture CSR (Block Offset 0x48, 88,..., 408) |
| Name: Port n Packet/Control Symbol Capture 0 CSR Offset: 0x4C, 8C,..., 40C | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 0 | Part 8 | 2.3.2.13 Port n Packet/Control Symbol Capture 0 CSR (Block Offset 0x4C, 8C,..., 40C) |
| Name: Port n Packet Capture 1 CSR Offset: 0x50, 90,..., 410 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 1 | Part 8 | 2.3.2.14 Port n Packet Capture 1 CSR (Block Offset 0x50, 90,..., 410) |
| Name: Port n Packet Capture 2 CSR Offset: 0x54, 94,..., 414 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 2 | Part 8 | 2.3.2.15 Port n Packet Capture 2 CSR (Block Offset 0x54, 94,..., 414) |
| Name: Port n Packet Capture 3 CSR Offset: 0x58, 98,..., 418 | | | |
| Bits | Name | Part | Section |
| 0:31 | Capture 3 | Part 8 | 2.3.2.16 Port n Packet Capture 3 CSR (Block Offset 0x58, 98,..., 418) |
| Name: Port n Error Rate CSR Offset: 0x68, A8,..., 428 | | | |
| Bits | Name | Part | Section |
| 0:7 | Error Rate Bias | Part 8 | 2.3.2.17 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 8:13 | Reserved | | |
| 14:15 | Error Rate Recovery | Part 8 | 2.3.2.17 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 16:23 | Peak Error Rate | Part 8 | 2.3.2.17 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| 24:31 | Error Rate Counter | Part 8 | 2.3.2.17 Port n Error Rate CSR (Block Offset 0x68, A8,..., 428) |
| Name: Port n Error Rate Threshold CSR Offset: 0x6C, AC,..., 42C | | | |
| Bits | Name | Part | Section |
| 0:7 | Error Rate Failed Threshold Trigger | Part 8 | 2.3.2.18 Port n Error Rate Threshold CSR (Block Offset 0x6C, AC,..., 42C) |
| 8:15 | Error Rate Degraded Threshold Trigger | Part 8 | 2.3.2.18 Port n Error Rate Threshold CSR (Block Offset 0x6C, AC,..., 42C) |
| 16:31 | Reserved | | |

# Block: 0x0009 : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.6.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Port Link Timeout Control CSR Offset: 0x20 | | | |
| Bits | Name | Part | Section |
| 0:23 | timeout value | Part 6 | 6.6.2 Port Link Timeout Control CSR (Block Offset 0x20) |
| 24:31 | Reserved | | |
| Name: Port General Control CSR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:1 | Reserved | | |
| 2 | Discovered | Part 6 | 6.6.4 Port General Control CSR (Block Offset 0x3C) |
| 3:31 | Reserved | | |
| Name: Port n Link Maintenance Request CSRs Offset: 0x40, 60, ... , 220 | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Command | Part 6 | 6.6.5 Port n Link Maintenance Request CSRs (Block Offsets 0x40, 60, ... , 220) |
| Name: Port n Link Maintenance Response CSRs Offset: 0x44, 64, ... , 224 | | | |
| Bits | Name | Part | Section |
| 0 | response\_valid | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| 1:20 | Reserved | | |
| 21:26 | ackID\_status | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| 27:31 | port\_status | Part 6 | 6.6.6 Port n Link Maintenance Response CSRs (Block Offsets 0x44, 64, ... , 224) |
| Name: Port n Local ackID CSRs Offset: 0x48, 68, ... , 228 | | | |
| Bits | Name | Part | Section |
| 0 | Clr\_outstanding\_ackIDs | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 1 | Reserved | | |
| 2:7 | Inbound\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 8:17 | Reserved | | |
| 18:23 | Outstanding\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| 24:25 | Reserved | | |
| 26:31 | Outbound\_ackID | Part 6 | 6.6.7 Port n Local ackID CSRs (Block Offsets 0x48, 68, ... , 228) |
| Name: Port n Control 2 CSRs Offset: 0x54, 74, ... , 234 | | | |
| Bits | Name | Part | Section |
| 0:3 | Selected Baudrate | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 4 | Baudrate Discovery Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 5 | Baudrate Discovery Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 6 | 1.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 7 | 1.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 8 | 2.5 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 9 | 2.5 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 10 | 3.125 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 11 | 3.125 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 12 | 5.0 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 13 | 5.0 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 14 | 6.25 GBaud Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 15 | 6.25 GBaud Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 16:27 | Reserved | | |
| 28 | Enable Inactive Lanes | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 29 | Data scrambling disable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 30 | Remote Transmit Emphasis Control Support | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| 31 | Remote Transmit Emphasis Control Enable | Part 6 | 6.6.10 Port n Control 2 CSRs (Block Offset 0x54, 74, ... , 234) |
| Name: Port n Error and Status CSRs Offset: 0x58, 78, ... , 238 | | | |
| Bits | Name | Part | Section |
| 0 | Idle Sequence 2 Support | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 1 | Idle Sequence 2 Enable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 2 | Idle Sequence | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 3 | Reserved | | |
| 4 | Flow Control Mode | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 5 | Output Packet-dropped | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 6 | Output Failed-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 7 | Output Degraded-encountered | Part 8 | 2.2 Additions to Existing Registers (Block Offset 0x58, 78, ... , 238) |
| 8:10 | Reserved | | |
| 11 | Output Retry-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 12 | Output Retried | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 13 | Output Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 14 | Output Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 15 | Output Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 16:20 | Reserved | | |
| 21 | Input Retry-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 22 | Input Error-encountered | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 23 | Input Error-stopped | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 24:26 | Reserved | | |
| 27 | Port-write Pending | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 28 | Port Unavailable | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 29 | Port Error | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 30 | Port OK | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| 31 | Port Uninitialized | Part 6 | 6.6.8 Port n Error and Status CSRs (Block Offset 0x58, 78, ... , 238) |
| Name: Port n Control CSRs Offset: 0x5C, 7C, ... , 23C | | | |
| Bits | Name | Part | Section |
| 0:1 | Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 2:4 | Initialized Port Width | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 5:7 | Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 8 | Port Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 9 | Output Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 10 | Input Port Enable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 11 | Error Checking Disable | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 12 | Multicast-event Participant | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 13 | Flow Control Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 14 | Enumeration Boundary | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 15 | Flow Arbitration Participant | Part 9 | 4.3 Port n Control CSR (Block Offsets 0x5C, 7C, ... , 23C) |
| 16:17 | Extended Port Width Override | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 18:19 | Extended Port Width Support | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 20:27 | Implementation-defined | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |
| 28 | Stop on Port Failed-encountered Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 29 | Drop Packet Enable | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 30 | Port Lockout | Part 8 | 2.2 Additions to Existing Registers (Block Offsets 0x5C, 7C, ... , 23C) |
| 31 | Port Type | Part 6 | 6.6.9 Port n Control CSRs (Block Offsets 0x5C, 7C, ... , 23C) |

# Block: 0x000A : VC Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: VC Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.8.2.1 VC Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.8.2.1 VC Register Block Header (Block Offset 0x0) |
| Name: Port n VCx BW Allocation Registers Offset: ((((port number) + 1) \* 0x20) + . (offset based on VC #, see Table 6-23)) | | | |
| Bits | Name | Part | Section |
| 0:15 | Bandwidth Allocation | Part 6 | 6.8.2.4 Port n VCx BW Allocation Registers (Block Offset ((((port number) + 1) \* 0x20) + . (offset based on VC #, see Table 6-23))) |
| 16:31 | Bandwidth Allocation | Part 6 | 6.8.2.4 Port n VCx BW Allocation Registers (Block Offset ((((port number) + 1) \* 0x20) + . (offset based on VC #, see Table 6-23))) |
| Name: Port n VC0 BW Allocation Registers Offset: (((port number) + 1) \* 0x20) + 0x04) | | | |
| Bits | Name | Part | Section |
| 0 | VC0 Bandwidth Reservation Capable | Part 6 | 6.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 1 | VC0 BW Res Enable | Part 6 | 6.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 2:7 | Reserved | | |
| 8:15 | Bandwidth Reservation Precision | Part 6 | 6.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| 16:31 | Bandwidth Allocation | Part 6 | 6.8.2.3 Port n VC0 BW Allocation Registers (Block Offset (((port number) + 1) \* 0x20) + 0x04)) |
| Name: Port n VC Control and Status Registers Offset: ((port number) + 1) \* 0x20) | | | |
| Bits | Name | Part | Section |
| 0:7 | VC Refresh Interval | Part 6 | 6.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 8:15 | CT Mode | Part 6 | 6.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 16:23 | VCs Support | Part 6 | 6.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |
| 24:31 | VCs Enable | Part 6 | 6.8.2.2 Port n VC Control and Status Registers (Block Offset ((port number) + 1) \* 0x20)) |

# Block: 0x000B : LP-Serial VC Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial VC Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 12 | 5.1.2.1 LP-Serial VC Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 12 | 5.1.2.1 LP-Serial VC Register Block Header (Block Offset 0x0) |
| Name: Port n VoQ Control Status Register Offset: Variable, see Section 5.1.1 | | | |
| Bits | Name | Part | Section |
| 0 | VoQ Backpressure Symbol Generation Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 1 | VoQ Backpressure Symbol Reception Supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 2 | Linking with VCs supported | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 3:7 | reserved | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 8 | Enable VoQ Symbol Generation | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 9 | Enable VoQ Participation | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 10 | Port XOFF | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 11 | Enable VC linking | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |
| 12:31 | reserved | Part 12 | 5.1.2.2 Port n VoQ Control Status Register (Block Offset - Variable, see Section 5.1.1) |

# Block: 0x000D : LP-Serial Register Block

|  |  |  |  |
| --- | --- | --- | --- |
| Name: LP-Serial Register Block Header Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | EF\_PTR | Part 6 | 6.7.2.1 LP-Serial Register Block Header (Block Offset 0x0) |
| 16:31 | EF\_ID | Part 6 | 6.7.2.1 LP-Serial Register Block Header (Block Offset 0x0) |
| Name: Lane n Status 0 CSRs Offset: 0x10, 30, ... , 3F0 | | | |
| Bits | Name | Part | Section |
| 0:7 | Port Number | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 8:11 | Lane Number | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 12 | Transmitter type | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 13 | Transmitter mode | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 14:15 | Receiver type | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 16 | Receiver input inverted | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 17 | Receiver trained | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 18 | Receiver lane sync | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 19 | Receiver lane ready | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 20:23 | 8b/10b decoding errors | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 24 | Lane\_sync state change | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 25 | Rcvr\_trained state change | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 26:27 | Reserved | | |
| 28 | Status 1 CSR implemented | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| 29:31 | Status 2-7 CSRs implemented | Part 6 | 6.7.2.2 Lane n Status 0 CSRs (Block Offsets 0x10, 30, ... , 3F0) |
| Name: Lane n Status 1 CSRs Offset: 0x14, 34, ... , 3F4 | | | |
| Bits | Name | Part | Section |
| 0 | IDLE2 received | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 1 | IDLE2 information current | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 2 | Values changed | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 3 | Implementation defined | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 4 | Connected port lane receiver trained | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 5:7 | Received port width | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 8:11 | Lane number in connected port | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 12:13 | Connected port transmit emphasis Tap(-1) status | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 14:15 | Connected port transmit emphasis Tap(+1) status | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 16 | Connected port scrambling/descrambling enabled | Part 6 | 6.7.2.3 Lane n Status 1 CSRs (Block Offsets 0x14, 34, ... , 3F4) |
| 17:31 | Reserved | | |

# Block: STD\_REG : Device Identity CAR

|  |  |  |  |
| --- | --- | --- | --- |
| Name: Device Identity CAR Offset: 0x00 | | | |
| Bits | Name | Part | Section |
| 0:15 | DeviceIdentity | Part 1 | 5.4.1 Device Identity CAR (Configuration Space Offset 0x0) |
| 16:31 | DeviceVendorIdentity | Part 1 | 5.4.1 Device Identity CAR (Configuration Space Offset 0x0) |
| Name: Device Information CAR Offset: 0x04 | | | |
| Bits | Name | Part | Section |
| 0:31 | DeviceRev | Part 1 | 5.4.2 Device Information CAR (Configuration Space Offset 0x4) |
| Name: Assembly Identity CAR Offset: 0x08 | | | |
| Bits | Name | Part | Section |
| 0:15 | AssyIdentity | Part 1 | 5.4.3 Assembly Identity CAR (Configuration Space Offset 0x8) |
| 16:31 | AssyVendorIdentity | Part 1 | 5.4.3 Assembly Identity CAR (Configuration Space Offset 0x8) |
| Name: Assembly Information CAR Offset: 0x0C | | | |
| Bits | Name | Part | Section |
| 0:15 | AssyRev | Part 1 | 5.4.4 Assembly Information CAR (Configuration Space Offset 0xC) |
| 16:31 | ExtendedFeaturesPtr | Part 1 | 5.4.4 Assembly Information CAR (Configuration Space Offset 0xC) |
| Name: Processing Element Features CAR Offset: 0x10 | | | |
| Bits | Name | Part | Section |
| 0 | Bridge | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 1 | Memory | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 2 | Processor | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 3 | Switch | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 4 | Multiport | Part 6 | 6.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 5:19 | Reserved | | |
| 20 | Flow Arbitration Support | Part 9 | 4.2 Processing Elements Features CAR (Offset 0x10 Word 0) |
| 21 | Multicast Support | Part 11 | 3.2 Processing Elements Features CAR (Configuration Space Offset 0x10) |
| 22 | Extended route table configuration support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 23 | Standard route table configuration support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 24 | Flow Control Support | Part 9 | 4.2 Processing Elements Features CAR (Offset 0x10 Word 0) |
| 25 | Implementation-defined | Part 6 | 6.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 26 | CRF Support | Part 6 | 6.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 27 | Common transport large system support | Part 3 | 3.4.1 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 28 | Extended features | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| 29:31 | Extended addressing support | Part 1 | 5.4.5 Processing Element Features CAR (Configuration Space Offset 0x10) |
| Name: Switch Port Information CAR Offset: 0x14 | | | |
| Bits | Name | Part | Section |
| 0:15 | Reserved | | |
| 16:23 | PortTotal | Part 1 | 5.4.6 Switch Port Information CAR (Configuration Space Offset 0x14) |
| 24:31 | PortNumber | Part 1 | 5.4.6 Switch Port Information CAR (Configuration Space Offset 0x14) |
| Name: Source Operations CAR Offset: 0x18 | | | |
| Bits | Name | Part | Section |
| 0 | Read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 1 | Instruction read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 2 | Read-for-ownership | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 3 | Data cache invalidate | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 4 | Castout | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 5 | Data cache flush | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 6 | I/O read | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 7 | Instruction cache invalidate | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 8 | TLB invalidate-entry | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 9 | TLB invalidate-entry sync | Part 5 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 10:11 | Reserved | | |
| 12 | Data streaming traffic management | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 13 | Data streaming | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 14:15 | Implementation defined | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 16 | Read | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 17 | Write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 18 | Streaming-write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 19 | Write-with-response | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 20 | Data message | Part 2 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 21 | Doorbell | Part 2 | 5.4.1 Source Operations CAR (Configuration Space Offset 0x18) |
| 22 | Atomic (compare-and-swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 23 | Atomic (test-and-swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 24 | Atomic (increment) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 25 | Atomic (decrement) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 26 | Atomic (set) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 27 | Atomic (clear) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 28 | Atomic (swap) | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 29 | Port-write | Part 1 | 5.4.7 Source Operations CAR (Configuration Space Offset 0x18) |
| 30:31 | Implementation defined | Part 10 | 5.5.1 Source Operations CAR (Configuration Space Offset 0x18) |
| Name: Destination Operations CAR Offset: 0x1C | | | |
| Bits | Name | Part | Section |
| 0 | Read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 1 | Instruction read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 2 | Read-for-ownership | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 3 | Data cache invalidate | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 4 | Castout | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 5 | Data cache flush | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 6 | I/O read | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 7 | Instruction cache invalidate | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 8 | TLB invalidate-entry | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 9 | TLB invalidate-entry sync | Part 5 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 10:11 | Reserved | | |
| 12 | Data streaming traffic management | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 13 | Data streaming | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 14:15 | Implementation defined | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 16 | Read | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 17 | Write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 18 | Streaming-write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 19 | Write-with-response | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 20 | Data message | Part 2 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 21 | Doorbell | Part 2 | 5.4.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 22 | Atomic (compare-and-swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 23 | Atomic (test-and-swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 24 | Atomic (increment) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 25 | Atomic (decrement) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 26 | Atomic (set) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 27 | Atomic (clear) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 28 | Atomic (swap) | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 29 | Port-write | Part 1 | 5.4.8 Destination Operations CAR (Configuration Space Offset 0x1C) |
| 30:31 | Implementation defined | Part 10 | 5.5.2 Destination Operations CAR (Configuration Space Offset 0x1C) |
| Name: Switch Multicast Support CAR Offset: 0x30 | | | |
| Bits | Name | Part | Section |
| 0 | Simple\_Assoc | Part 11 | 3.3 Switch Multicast Support CAR (Configuration Space Offset 0x30) |
| 1:31 | Reserved | | |
| Name: Switch Route Table Destination ID Limit CAR Offset: 0x34 | | | |
| Bits | Name | Part | Section |
| 0:15 | Reserved | | |
| 16:31 | Max\_destID | Part 3 | 3.4.2 Switch Route Table Destination ID Limit CAR (Configuration Space Offset 0x34) |
| Name: Switch Multicast Information CAR Offset: 0x38 | | | |
| Bits | Name | Part | Section |
| 0 | Block\_Assoc | Part 11 | 3.4 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 1 | Per\_Port\_Assoc | Part 11 | 3.4 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 2:15 | MaxDestIDAssoc | Part 11 | 3.4 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| 16:31 | MaxMcastMasks | Part 11 | 3.4 Switch Multicast Information CAR (Configuration Space Offset 0x38) |
| Name: Data Streaming Information CAR Offset: 0x3C | | | |
| Bits | Name | Part | Section |
| 0:15 | MaxPDU | Part 10 | 5.5.3 Data Streaming Information CAR (Configuration Space Offset 0x3C) |
| 16:31 | SegSupport | Part 10 | 5.5.3 Data Streaming Information CAR (Configuration Space Offset 0x3C) |
| Name: Data Streaming Logical Layer Control CSR Offset: 0x48 | | | |
| Bits | Name | Part | Section |
| 0:3 | TM Types Supported (read only) | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| 4:7 | TM Mode | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| 8:23 | Reserved | | |
| 24:31 | MTU | Part 10 | 5.6.1 Data Streaming Logical Layer Control CSR (Configuration Space Offset 0x48) |
| Name: Processing Element Logical Layer Control CSR Offset: 0x4C | | | |
| Bits | Name | Part | Section |
| 0:28 | Reserved | | |
| 29:31 | Extended addressing control | Part 1 | 5.5.1 Processing Element Logical Layer Control CSR (Configuration Space Offset 0x4C) |
| Name: Local Configuration Space Base Address 0 CSR Offset: 0x58 | | | |
| Bits | Name | Part | Section |
| 0 | Reserved | | |
| 1:16 | LCSBA | Part 1 | 5.5.2 Local Configuration Space Base Address 0 CSR (Configuration Space Offset 0x58) |
| 17:31 | LCSBA | Part 1 | 5.5.2 Local Configuration Space Base Address 0 CSR (Configuration Space Offset 0x58) |
| Name: Local Configuration Space Base Address 1 CSR Offset: 0x5C | | | |
| Bits | Name | Part | Section |
| 0 | LCSBA | Part 1 | 5.5.3 Local Configuration Space Base Address 1 CSR (Configuration Space Offset 0x5C) |
| 1:31 | LCSBA | Part 1 | 5.5.3 Local Configuration Space Base Address 1 CSR (Configuration Space Offset 0x5C) |
| Name: Base Device ID CSR Offset: 0x60 | | | |
| Bits | Name | Part | Section |
| 0:7 | Reserved | | |
| 8:15 | Base\_deviceID | Part 3 | 3.5.1 Base Device ID CSR (Configuration Space Offset 0x60) |
| 16:31 | Large\_base\_deviceID | Part 3 | 3.5.1 Base Device ID CSR (Configuration Space Offset 0x60) |
| Name: Host Base Device ID Lock CSR Offset: 0x68 | | | |
| Bits | Name | Part | Section |
| 0:15 | Reserved | | |
| 16:31 | Host\_base\_deviceID | Part 3 | 3.5.2 Host Base Device ID Lock CSR (Configuration Space Offset 0x68) |
| Name: Component Tag CSR Offset: 0x6C | | | |
| Bits | Name | Part | Section |
| 0:31 | component\_tag | Part 3 | 3.5.3 Component Tag CSR (Configuration Space Offset 0x6C) |
| Name: Standard Route Configuration Destination ID Select CSR Offset: 0x70 | | | |
| Bits | Name | Part | Section |
| 0 | Ext\_config\_en | Part 3 | 3.5.4 Standard Route Configuration Destination ID Select CSR (Configuration Space Offset 0x70) |
| 1:15 | Reserved | | |
| 16:23 | Config\_destID\_msb | Part 3 | 3.5.4 Standard Route Configuration Destination ID Select CSR (Configuration Space Offset 0x70) |
| 24:31 | Config\_destID | Part 3 | 3.5.4 Standard Route Configuration Destination ID Select CSR (Configuration Space Offset 0x70) |
| Name: Standard Route Configuration Port Select CSR Offset: 0x74 | | | |
| Bits | Name | Part | Section |
| 0:7 | Config\_output\_port3 | Part 3 | 3.5.5 Standard Route Configuration Port Select CSR (Configuration Space Offset 0x74) |
| 8:15 | Config\_output\_port2 | Part 3 | 3.5.5 Standard Route Configuration Port Select CSR (Configuration Space Offset 0x74) |
| 16:23 | Config\_output\_port1 | Part 3 | 3.5.5 Standard Route Configuration Port Select CSR (Configuration Space Offset 0x74) |
| 24:31 | Config\_output\_port | Part 3 | 3.5.5 Standard Route Configuration Port Select CSR (Configuration Space Offset 0x74) |
| Name: Standard Route Default Port CSR Offset: 0x78 | | | |
| Bits | Name | Part | Section |
| 0:23 | Reserved | | |
| 24:31 | Default\_output\_port | Part 3 | 3.5.6 Standard Route Default Port CSR (Configuration Space Offset 0x78) |
| Name: Multicast Mask Port CSR Offset: 0x80 | | | |
| Bits | Name | Part | Section |
| 0:15 | Mcast\_Mask | Part 11 | 3.5 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 16:23 | Egress\_Port\_Num | Part 11 | 3.5 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 24 | Reserved | | |
| 25:27 | Mask\_Cmd | Part 11 | 3.5 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| 28:30 | Reserved | | |
| 31 | Port\_Present | Part 11 | 3.5 Multicast Mask Port CSR (Configuration Space Offset 0x80) |
| Name: Multicast Associate Select CSR Offset: 0x84 | | | |
| Bits | Name | Part | Section |
| 0:7 | Large\_DestID | Part 11 | 3.6 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| 8:15 | DestID | Part 11 | 3.6 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| 16:31 | Mcast\_Mask\_Num | Part 11 | 3.6 Multicast Associate Select CSR (Configuration Space Offset 0x84) |
| Name: Multicast Associate Operation CSR Offset: 0x88 | | | |
| Bits | Name | Part | Section |
| 0:15 | Assoc\_Blksize | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 16:23 | Ingress\_Port | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 24 | Large\_Transport | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 25:26 | Assoc\_Cmd | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 27:30 | - | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |
| 31 | Assoc\_Present | Part 11 | 3.7 Multicast Associate Operation CSR (Configuration Space Offset 0x88) |