Data Center RDIMM DDR5 Tester

HyperRAM

File: hyperram.kicad_sch

DDR5

File: DDR5.kicad_sch

Interfaces

File: interfaces.kicad_sch

Ethernet

File: ethernet.kicad_sch

Supply

File: supply.kicad_sch

Config SPI flash

File: config-spi.kicad_sch

FPGA power

File: fpga-power.kicad_sch

FPGA banks 12-15

File: fpga-banks-12-15.kicad_sch

FPGA banks 16-34

File: fpga-banks-16-34.kicad_sch

Logo N2 oshw_logo

Logo N1 antmicro_logo

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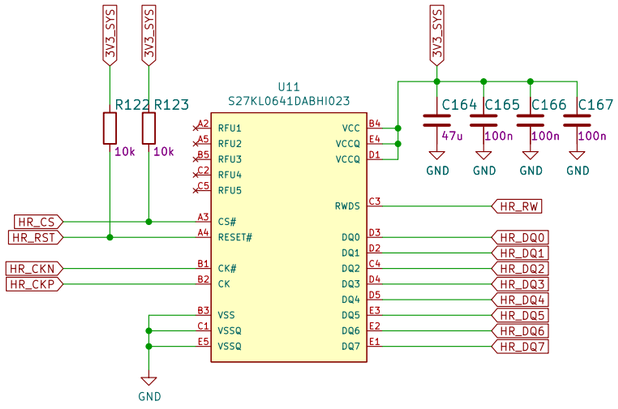
Sheet: /
File: data-center-rdimm-ddr5-tester.kicad_sch

Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 1/10

HyperRAM



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Sheet: /HyperRAM/
File: hyperram.kicad_sch

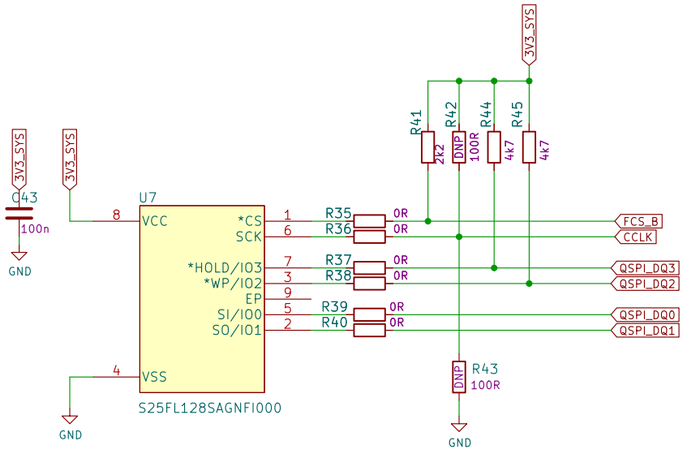
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1		Id: 2/10

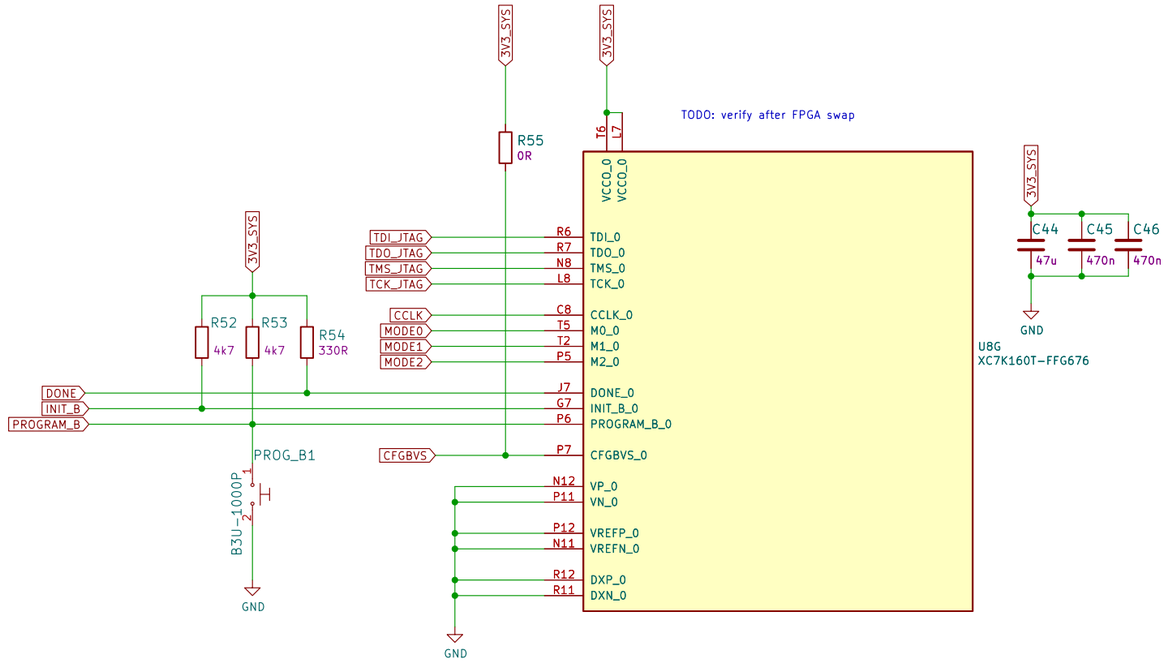
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

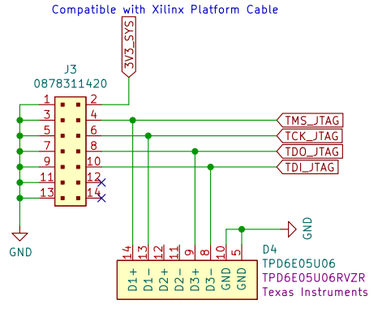


FPGA BANK 0

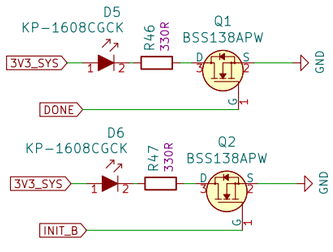


JTAG Connector

Compatible with Xilinx Platform Cable

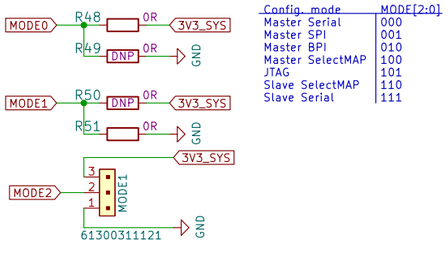


STATUS LEDs



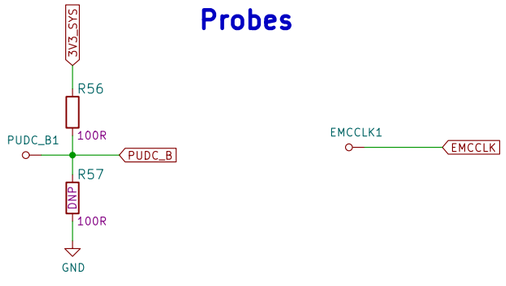
Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Probes



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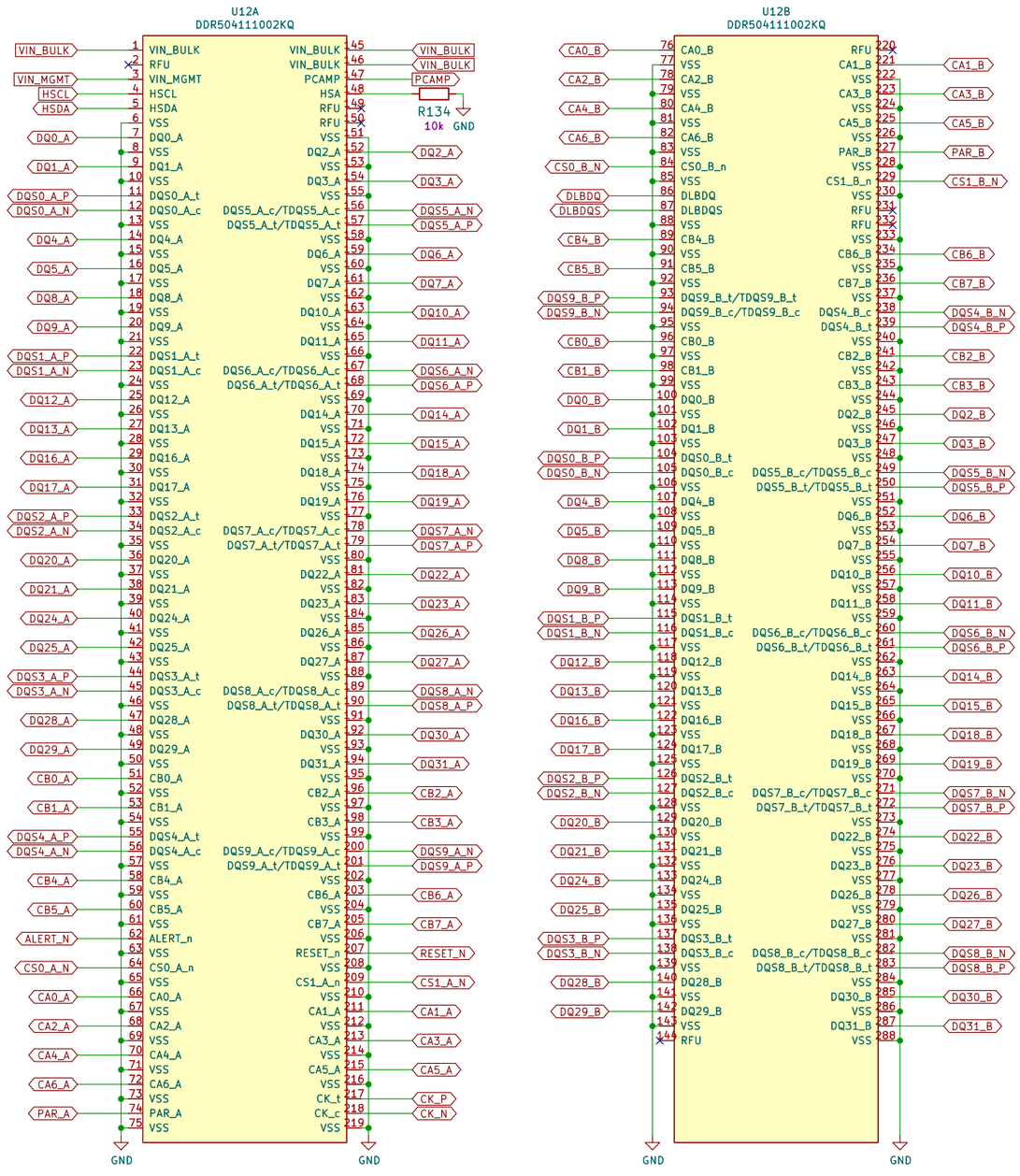
Sheet: /Config SPI flash/
File: config-spi.kicad_sch

Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 3/10

DDR5 RDIMM connector



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Sheet: /DDR5/
File: DDR5.kicad_sch

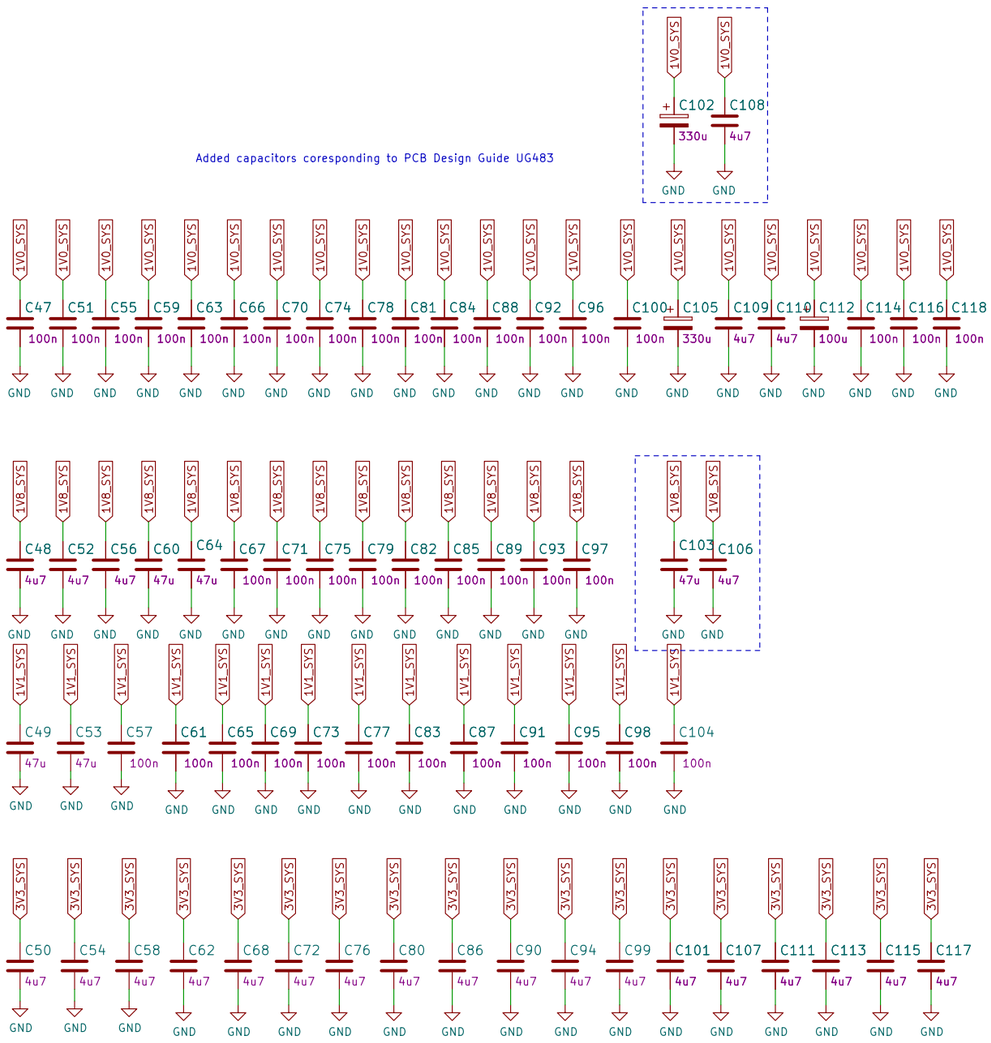
Title: Data Center RDIMM DDR5 Tester

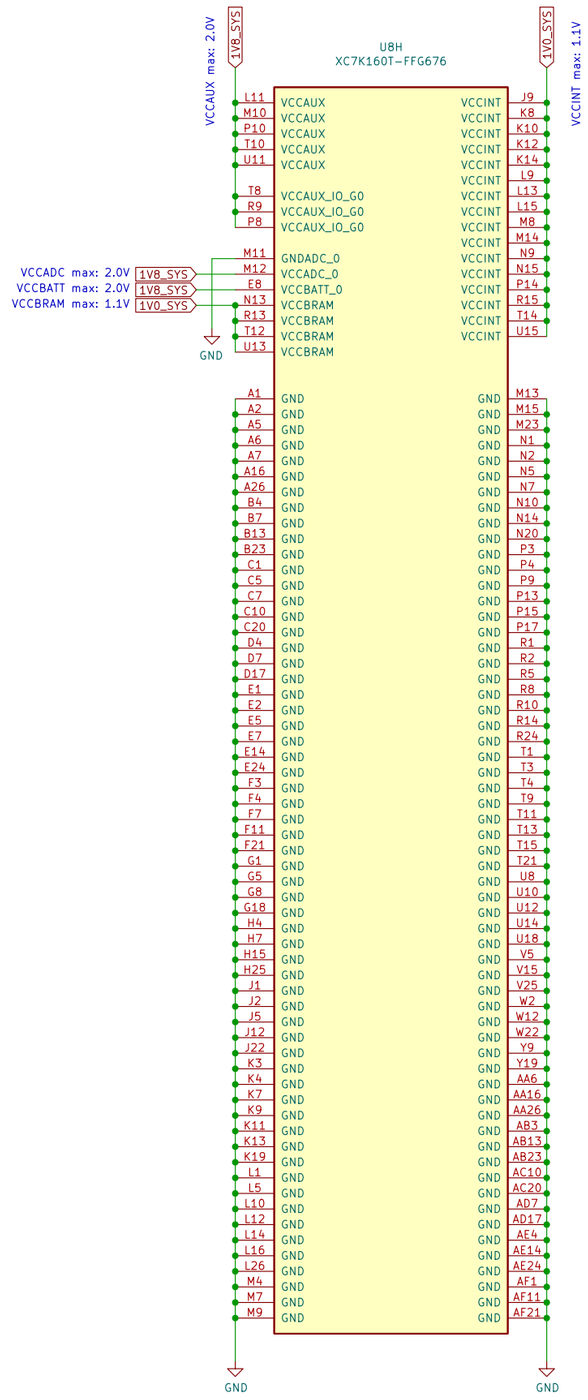
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 4/10

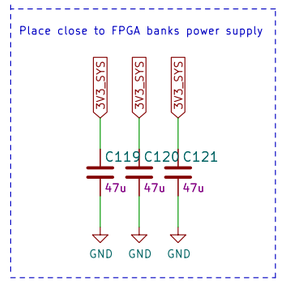
POWER RAILS

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!

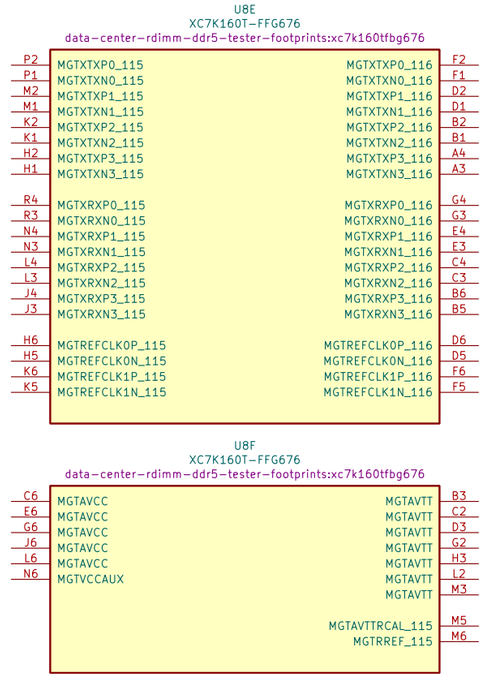
Added capacitors coresponding to PCB Design Guide UG483







UNUSED



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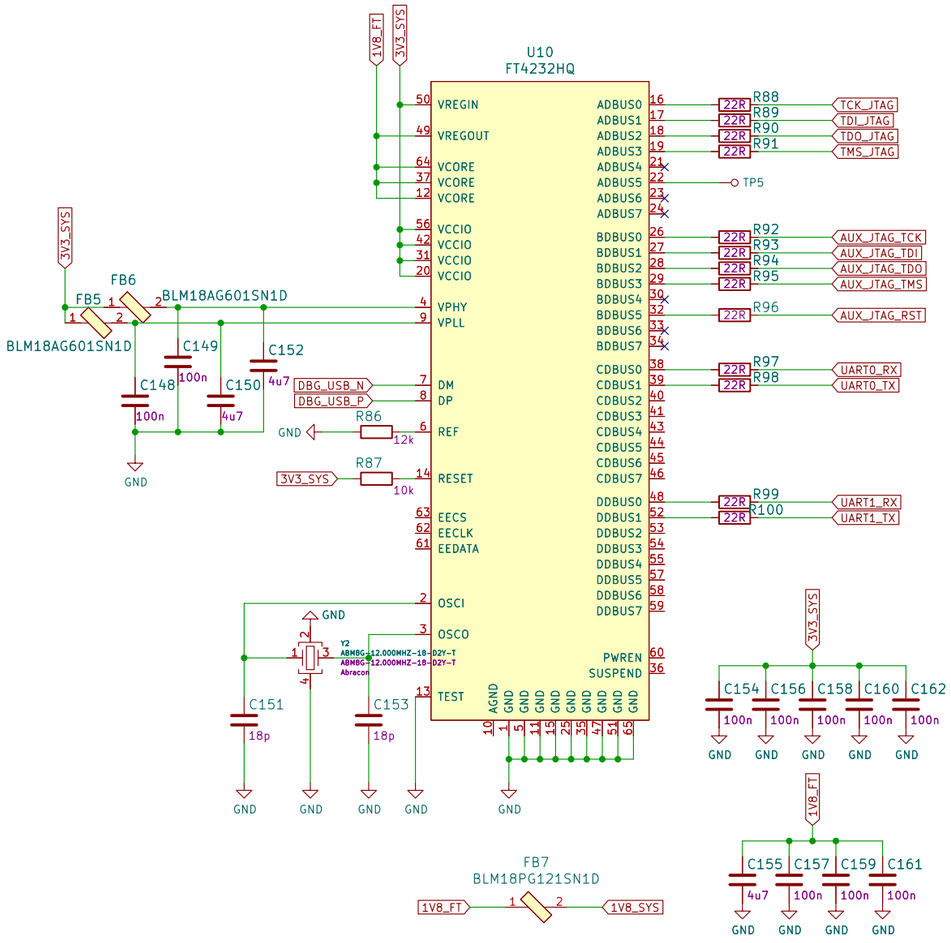
Sheet: /FPGA power/
File: fpga-power.kicad_sch

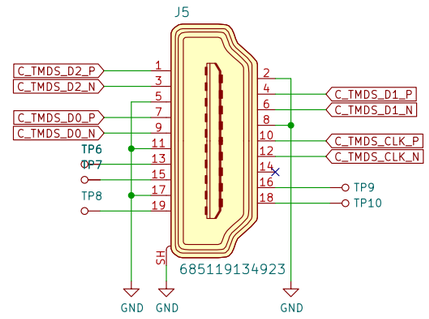
Title: Data Center RDIMM DDR5 Tester

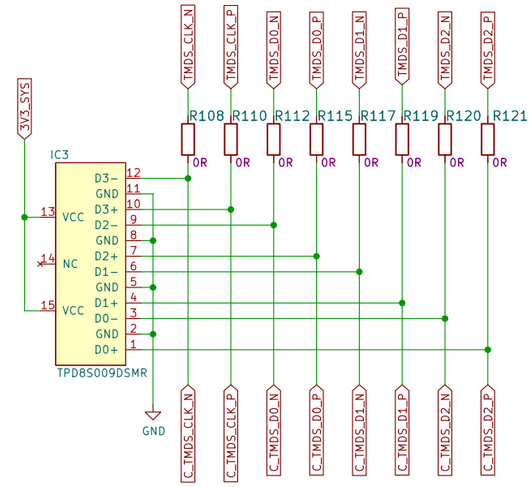
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 5/10

Debug UART

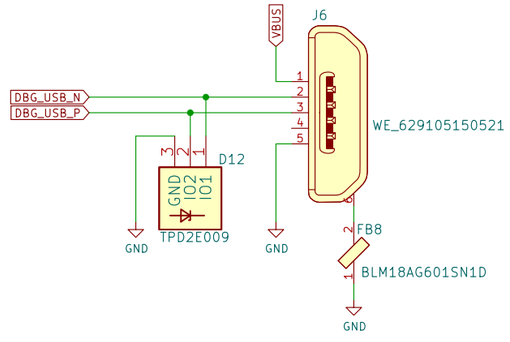


HDMI

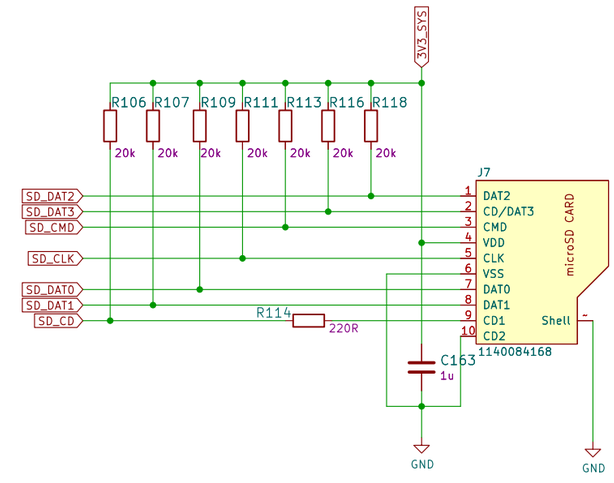




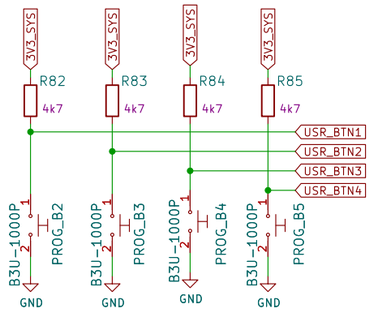
Debug USB



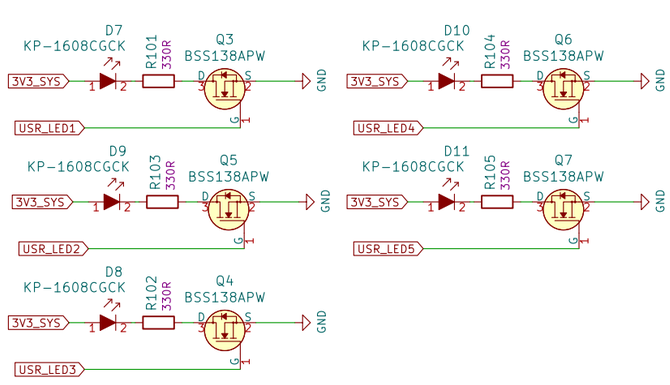
SD card



User buttons



User LEDs



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Sheet: /Interfaces/
File: interfaces.kicad_sch

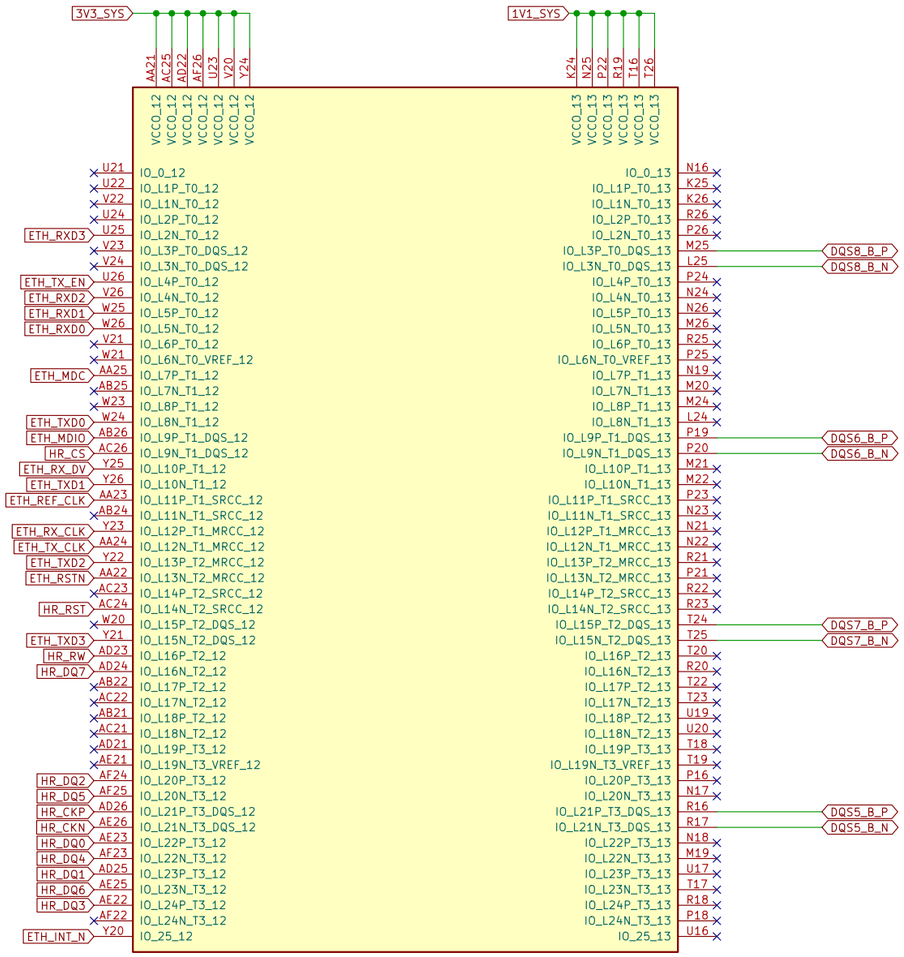
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 6/10

BANK 12

BANK 13

VCCO (HR banks) max: 3.6V

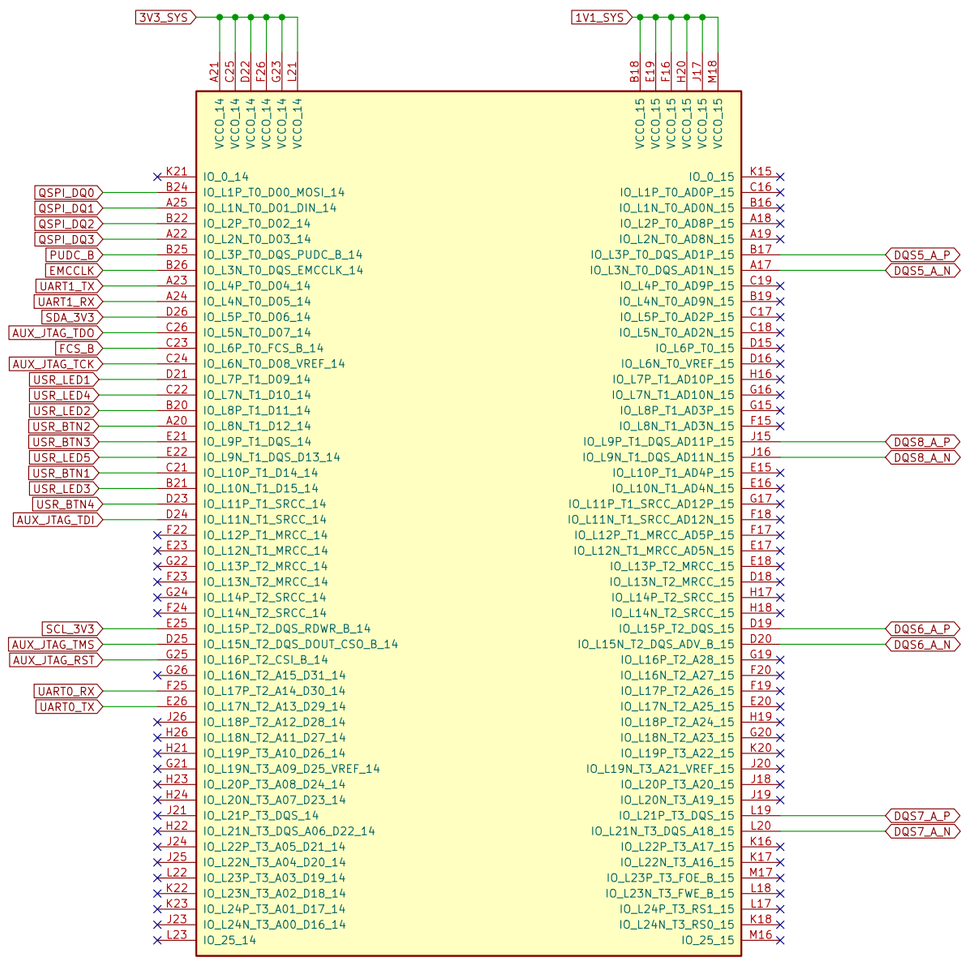


U8A
XC7K160T-FFG676
data-center-rdimm-ddr5-tester-footprints:xc7k160tfbg676

BANK 14

BANK 15

VCCO (HR banks) max: 3.6V



U8B
XC7K160T-FFG676
data-center-rdimm-ddr5-tester-footprints:xc7k160tfbg676

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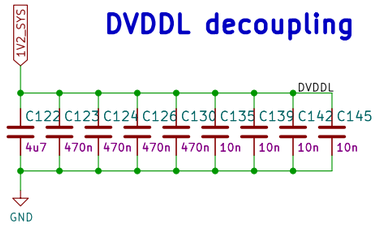
Sheet: /FPGA banks 12-15/
File: fpga-banks-12-15.kicad_sch

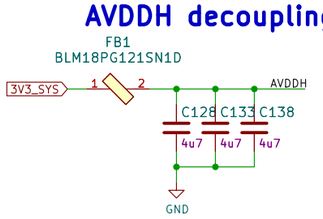
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 7/10

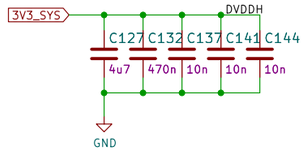
DVDDL decoupling



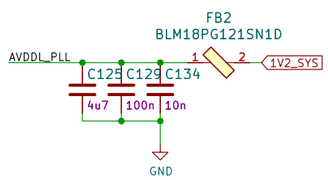
AVDDH decoupling



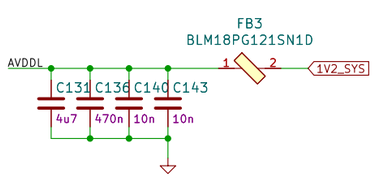
DVDDH decoupling



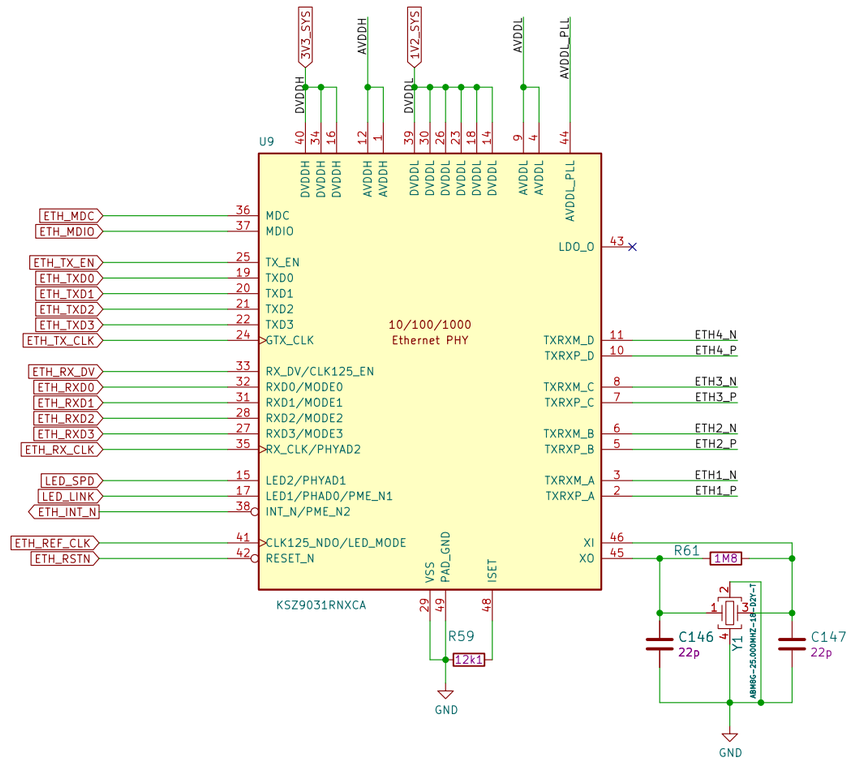
AVDDL_PLL decoupling



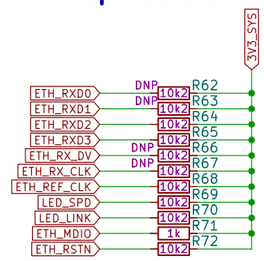
AVDDL decoupling



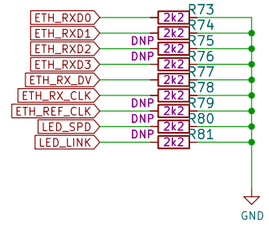
PHY



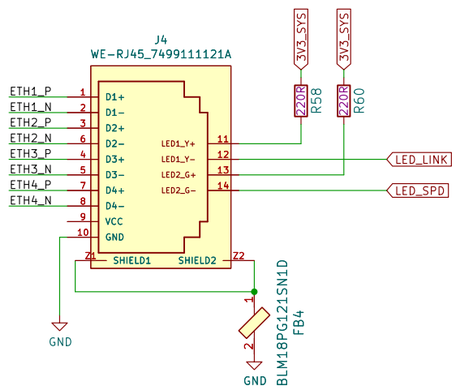
Pull up resistors



Pull down resistors



RJ45 Connector



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Sheet: /Ethernet/
File: ethernet.kicad_sch

Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 8/10

BANK 16

VCCO (HR bank) max: 3.6V

3V3_SYS

A11 B8 C15 D12 E9 G13 H10

VCCO_16 ×7

J8	IO_0_16
H9	IO_L1P_T0_16
H8	IO_L1N_T0_16
G10	IO_L2P_T0_16
G9	IO_L2N_T0_16
J13	IO_L3P_T0_DQS_16
H13	IO_L3N_T0_DQS_16
J11	IO_L4P_T0_16
J10	IO_L4N_T0_16
H14	IO_L5P_T0_16
G14	IO_L5N_T0_16
H12	IO_L6P_T0_16
H11	IO_L6N_T0_VREF_16
F9	IO_L7P_T1_16 — SD_CD
F8	IO_L7N_T1_16 — SD_DAT1
D9	IO_L8P_T1_16 — SD_DAT3
D8	IO_L8N_T1_16 — SD_CMD
A9	IO_L9P_T1_DQS_16
A8	IO_L9N_T1_DQS_16
C9	IO_L10P_T1_16 — SD_DAT2
B9	IO_L10N_T1_16
G11	IO_L11P_T1_SRCC_16
F10	IO_L11N_T1_SRCC_16
E10	IO_L12P_T1_MRCC_16 — SD_DAT0
D10	IO_L12N_T1_MRCC_16 — SD_CLK
C12	IO_L13P_T2_MRCC_16 — GCLK100
C11	IO_L13N_T2_MRCC_16
E11	IO_L14P_T2_SRCC_16
D11	IO_L14N_T2_SRCC_16
F14	IO_L15P_T2_DQS_16
F13	IO_L15N_T2_DQS_16
G12	IO_L16P_T2_16
F12	IO_L16N_T2_16
D14	IO_L17P_T2_16
D13	IO_L17N_T2_16
E13	IO_L18P_T2_16
E12	IO_L18N_T2_16
C14	IO_L19P_T3_16
C13	IO_L19N_T3_VREF_16
B12	IO_L20P_T3_16
B11	IO_L20N_T3_16
B14	IO_L21P_T3_DQS_16 — TMDS_D0_P
A14	IO_L21N_T3_DQS_16 — TMDS_D0_N
B10	IO_L22P_T3_16 — TMDS_D2_P
A10	IO_L22N_T3_16 — TMDS_D2_N
B15	IO_L23P_T3_16 — TMDS_CLK_P
A15	IO_L23N_T3_16 — TMDS_CLK_N
A13	IO_L24P_T3_16 — TMDS_D1_P
A12	IO_L24N_T3_16 — TMDS_D1_N
J14	IO_25_16

BANK 32

VCCO (HP bank) max: 2.0V

1V1_SYS

AB18 AC15 AE19 AF16 W17 Y14

VCCO_32 ×7

V13	IO_0_VRN_32 — VRN_32
AE17	IO_L1P_T0_32 — DQ4_B
AF17	IO_L1N_T0_32 — DQ3_B
AF14	IO_L2P_T0_32 — DQ0_B
AF15	IO_L2N_T0_32 — DQ2_B
AE18	IO_L3P_T0_DQS_32 — DQS0_B_P
AF18	IO_L3N_T0_DQS_32 — DQS0_B_N
AD15	IO_L4P_T0_32 — DQ5_B
AE15	IO_L4N_T0_32 — DQ1_B
AF19	IO_L5P_T0_32 — DQ6_B
AF20	IO_L5N_T0_32 — DQ7_B
AD16	IO_L6P_T0_32
AE16	IO_L6N_T0_VREF_32 — VREF_32
AA14	IO_L7P_T1_32 — DQ9_B
AA15	IO_L7N_T1_32 — DQ11_B
AC14	IO_L8P_T1_32 — DQ8_B
AD14	IO_L8N_T1_32 — DQ10_B
Y15	IO_L9P_T1_DQS_32 — DQS1_B_P
Y16	IO_L9N_T1_DQS_32 — DQS1_B_N
AB14	IO_L10P_T1_32 — DQ12_B
AB15	IO_L10N_T1_32 — DQ14_B
AA17	IO_L11P_T1_SRCC_32 — DQ13_B
AA18	IO_L11N_T1_SRCC_32 — DQ15_B
AB16	IO_L12P_T1_MRCC_32 — DLBDQ
AC16	IO_L12N_T1_MRCC_32 — DLBDQS
AC18	IO_L13P_T2_MRCC_32 — DQ19_B
AD18	IO_L13N_T2_MRCC_32 — DQ16_B
AB17	IO_L14P_T2_SRCC_32 — DQ20_B
AC17	IO_L14N_T2_SRCC_32 — DQ18_B
AD20	IO_L15P_T2_DQS_32 — DQS2_B_P
AE20	IO_L15N_T2_DQS_32 — DQS2_B_N
AA19	IO_L16P_T2_32 — DQ21_B
AA20	IO_L16N_T2_32 — DQ23_B
AC19	IO_L17P_T2_32 — DQ22_B
AD19	IO_L17N_T2_32 — DQ17_B
AB19	IO_L18P_T2_32
AB20	IO_L18N_T2_32 — DQ24_B
Y17	IO_L19P_T3_32 — DQ25_B
Y18	IO_L19N_T3_VREF_32 — VREF_32
V16	IO_L20P_T3_32 — DQ31_B
V17	IO_L20N_T3_32 — DQ29_B
W18	IO_L21P_T3_DQS_32 — DQS3_B_P
W19	IO_L21N_T3_DQS_32 — DQS3_B_N
W15	IO_L22P_T3_32 — DQ26_B
W16	IO_L22N_T3_32 — DQ27_B
V18	IO_L23P_T3_32 — DQ30_B
V19	IO_L23N_T3_32 — DQ28_B
V14	IO_L24P_T3_32
W14	IO_L24N_T3_32
W13	IO_25_VRP_32 — VRP_32

U8C
XC7K160T-FFG676
data-center-rdimm-ddr5-tester-footprints:xc7k160tfbg676

BANK 33

VCCO (HP bank) max: 2.0V

1V1_SYS

AA11 AB8 AD12 AE9 V10 W7

VCCO_33 ×7

U9	IO_0_VRN_33 — VRN_33
V11	IO_L1P_T0_33 — CA5_A
W11	IO_L1N_T0_33 — CA4_A
V8	IO_L2P_T0_33 — CA3_A
V7	IO_L2N_T0_33 — CA0_A
W10	IO_L3P_T0_DQS_33 — DQS9_A_P
W9	IO_L3N_T0_DQS_33 — DQS9_A_N
Y8	IO_L4P_T0_33 — CA2_A
Y7	IO_L4N_T0_33 — CA1_A
Y11	IO_L5P_T0_33 — PAR_A
Y10	IO_L5N_T0_33 — CA6_A
V9	IO_L6P_T0_33
W8	IO_L6N_T0_VREF_33 — VREF_33
AE7	IO_L7P_T1_33 — CB4_A
AF7	IO_L7N_T1_33 — CB6_A
AA8	IO_L8P_T1_33 — CB5_A
AA7	IO_L8N_T1_33 — CB2_A
AC8	IO_L9P_T1_DQS_33 — DQS4_A_P
AD8	IO_L9N_T1_DQS_33 — DQS4_A_N
AB7	IO_L10P_T1_33 — CB0_A
AC7	IO_L10N_T1_33 — CB1_A
AA9	IO_L11P_T1_SRCC_33 — CB7_A
AB9	IO_L11N_T1_SRCC_33 — CB3_A
AC9	IO_L12P_T1_MRCC_33 — CK_P
AD9	IO_L12N_T1_MRCC_33 — CK_N
AB11	IO_L13P_T2_MRCC_33 — CS1_B_N
AC11	IO_L13N_T2_MRCC_33 — CS0_B_N
AA10	IO_L14P_T2_SRCC_33 — CB6_B
AB10	IO_L14N_T2_SRCC_33 — CB4_B
AB12	IO_L15P_T2_DQS_33 — DQS9_B_N
AC12	IO_L15N_T2_DQS_33 — DQS9_B_P
AA13	IO_L16P_T2_33 — CB3_B
AA12	IO_L16N_T2_33 — CB1_B
AC13	IO_L17P_T2_33 — CB2_B
AD13	IO_L17N_T2_33 — CB0_B
Y13	IO_L18P_T2_33
Y12	IO_L18N_T2_33 — CB7_B
AD11	IO_L19P_T3_33 — CB5_B
AE11	IO_L19N_T3_VREF_33 — VREF_33
AD10	IO_L20P_T3_33 — CA5_B
AE10	IO_L20N_T3_33 — CA4_B
AE12	IO_L21P_T3_DQS_33 — DQS4_B_N
AF12	IO_L21N_T3_DQS_33 — DQS4_B_P
AE8	IO_L22P_T3_33 — CA1_B
AF8	IO_L22N_T3_33 — CA0_B
AE13	IO_L23P_T3_33 — CA6_B
AF13	IO_L23N_T3_33 — PAR_B
AF10	IO_L24P_T3_33 — CA3_B
AF9	IO_L24N_T3_33 — CA2_B
V12	IO_25_VRP_33 — VRP_33

BANK 34

VCCO (HP bank) max: 2.0V

1V1_SYS

AA1 AC5 AD2 AE6 U3 Y4

VCCO_34 ×7

U4	IO_0_VRN_34 — VRN_34
U6	IO_L1P_T0_34 — DQ0_A
U5	IO_L1N_T0_34 — DQ1_A
U2	IO_L2P_T0_34 — DQ6_A
U1	IO_L2N_T0_34 — DQ4_A
W6	IO_L3P_T0_DQS_34 — DQS0_A_P
W5	IO_L3N_T0_DQS_34 — DQS0_A_N
V3	IO_L4P_T0_34 — DQ5_A
W3	IO_L4N_T0_34 — DQ7_A
U7	IO_L5P_T0_34 — DQ2_A
V6	IO_L5N_T0_34 — DQ3_A
V4	IO_L6P_T0_34
W4	IO_L6N_T0_VREF_34 — VREF_34
Y3	IO_L7P_T1_34 — DQ13_A
Y2	IO_L7N_T1_34 — DQ12_A
V2	IO_L8P_T1_34 — DQ10_A
V1	IO_L8N_T1_34 — DQ8_A
AB1	IO_L9P_T1_DQS_34 — DQS1_A_P
AC1	IO_L9N_T1_DQS_34 — DQS1_A_N
W1	IO_L10P_T1_34 — DQ9_A
Y1	IO_L10N_T1_34 — DQ11_A
AB2	IO_L11P_T1_SRCC_34 — DQ14_A
AC2	IO_L11N_T1_SRCC_34 — DQ15_A
AA3	IO_L12P_T1_MRCC_34 — CS1_A_N
AA2	IO_L12N_T1_MRCC_34 — CS0_A_N
AA4	IO_L13P_T2_MRCC_34 — DQ17_A
AB4	IO_L13N_T2_MRCC_34 — DQ19_A
AC4	IO_L14P_T2_SRCC_34 — DQ21_A
AC3	IO_L14N_T2_SRCC_34 — DQ22_A
AA5	IO_L15P_T2_DQS_34 — DQS2_A_P
AB5	IO_L15N_T2_DQS_34 — DQS2_A_N
AB6	IO_L16P_T2_34 — DQ20_A
AC6	IO_L16N_T2_34 — DQ23_A
Y6	IO_L17P_T2_34 — DQ18_A
Y5	IO_L17N_T2_34 — DQ16_A
AD6	IO_L18P_T2_34
AD5	IO_L18N_T2_34 — DQ29_A
AD4	IO_L19P_T3_34 — DQ28_A
AD3	IO_L19N_T3_VREF_34 — VREF_34
AD1	IO_L20P_T3_34 — DQ26_A
AE1	IO_L20N_T3_34 — DQ27_A
AF5	IO_L21P_T3_DQS_34 — DQS3_A_P
AF4	IO_L21N_T3_DQS_34 — DQS3_A_N
AE3	IO_L22P_T3_34 — DQ24_A
AE2	IO_L22N_T3_34 — DQ25_A
AE6	IO_L23P_T3_34 — DQ31_A
AE5	IO_L23N_T3_34 — DQ30_A
AF3	IO_L24P_T3_34 — RESET_N
AF2	IO_L24N_T3_34 — ALERT_N
T7	IO_25_VRP_34 — VRP_34

U8D
XC7K160T-FFG676
data-center-rdimm-ddr5-tester-footprints:xc7k160tfbg676

Clock source

IC2 U13 ASFLMB-100.000MHZ-XY-T

3V3_SYS — C168 100n — GND

STDB 1 — VDD 4 — GND 2 — OUT 3 — GCLK100

GND

antmicro

open source hardware

VREF

1V1_SYS — FB9 BLM15AG601SN1D — R124 1k — R125 1k — C173 100n — C174 100n — VREF_32 — GND

1V1_SYS — FB10 BLM15AG601SN1D — R128 1k — R129 1k — C175 100n — C176 100n — VREF_33 — GND

1V1_SYS — FB11 BLM15AG601SN1D — R159 1k — R160 1k — C169 100n — C170 100n — VREF_34 — GND

R127 120R — 1V1_SYS — VRN_32

R126 120R — VRP_32 — GND

R131 120R — 1V1_SYS — VRN_33

R130 120R — VRP_33 — GND

R161 120R — 1V1_SYS — VRN_34

R162 120R — VRP_34 — GND

I2C/I3C logic translator

3V3_SYS

R171 4k7 — R172 4k7 — U14 TCA39306DCUR — R173 4k7 — R174 4k7 — VREF1

3V3_SYS — R132 200k — VREF2 7 — Vref2 Vref1 — 2 VREF1 — R137 0R — 1V0_SYS

SCL_3V3 — R135 0R — SCL2 6 — SCL2 SCL1 — 3 SCL1 — R138 0R — HSCL

SDA_3V3 — R136 0R — SDA2 5 — SDA2 SDA1 — 4 SDA1 — R139 0R — HSDA

R133 0R — EN 8 — EN GND — 1 GND_ — R140 0R — GND

J8 PinHeader_2x4 DNP

SDA2	1	2	SDA1
SCL2	3	4	SCL1
VREF2	5	6	VREF1
EN	7	8	GND_

VREF2 — C171 100n — C172 100n — VREF1

GND GND

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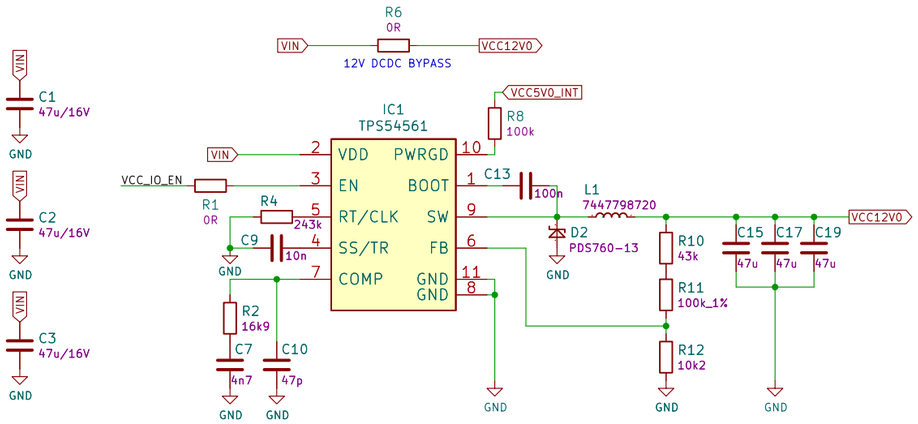
Sheet: /FPGA banks 16-34/
File: fpga-banks-16-34.kicad_sch

Title: Data Center RDIMM DDR5 Tester

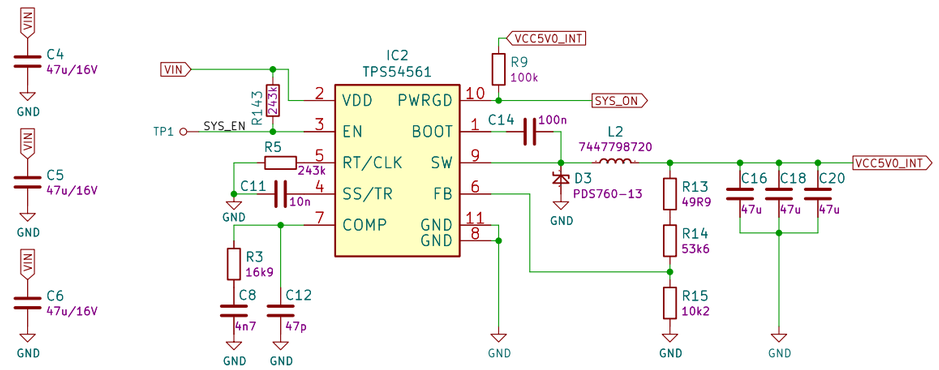
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 9/10

Input power connector

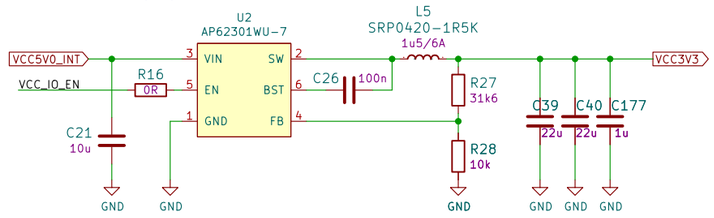
Main supply (12V 5A)



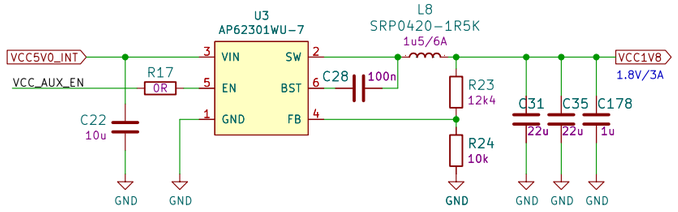
5V0 supply



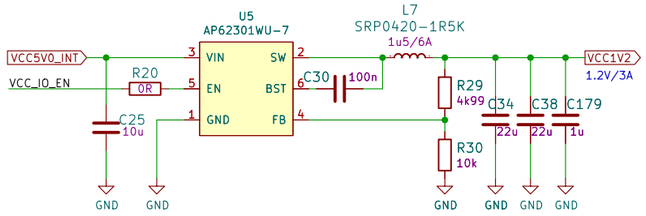
3V3 supply (3A)



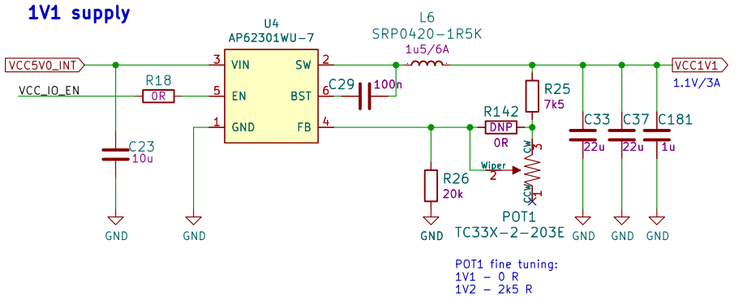
1V8 supply



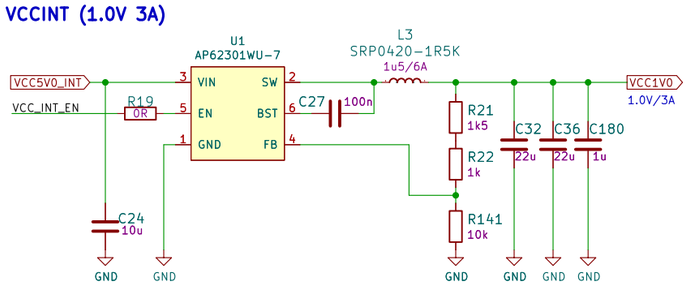
1V2 supply



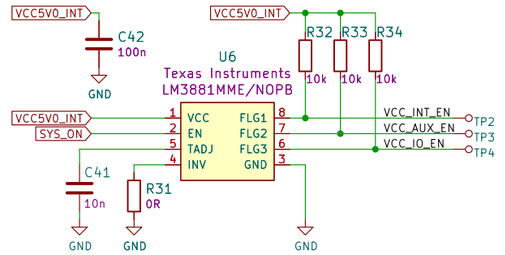
1V1 supply



VCCINT (1.0V 3A)

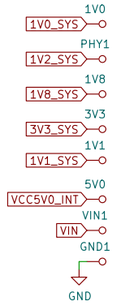


Power sequencer

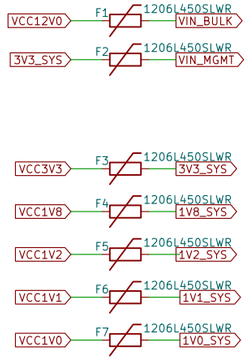


STEP1 – VCCINT (1.0V) for FPGA
STEP2 – VCCAUX (1.8V, 2.5V, 1.2V) for FPGA and DDR
STEP3 – VCCIO (3.3V, 1.2V, 0.6V) for FPGA, PHY and DDR

Probes

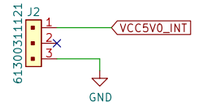


Fuses



Power switch

Optional FAN connector



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Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 10/10