Data Center RDIMM DDR5 Tester

HyperRAM

File: hyperram.kicad_sch

DDR5

File: DDR5.kicad_sch

Interfaces

File: interfaces.kicad_sch

Ethernet

File: ethernet.kicad_sch

Supply

File: supply.kicad_sch

Config SPI flash

File: config-spi.kicad_sch

FPGA power

File: fpga-power.kicad_sch

FPGA banks 12-15

File: fpga-banks-12-15.kicad_sch

FPGA banks 16-34

File: fpga-banks-16-34.kicad_sch

Logo N2 oshw_logo

Logo N1 antmicro_logo

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Sheet: /
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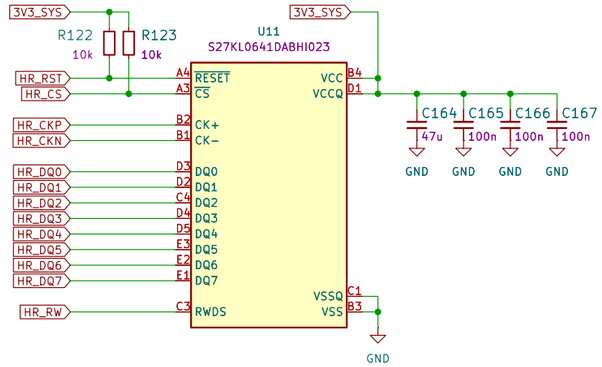
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 1/10

HyperRAM



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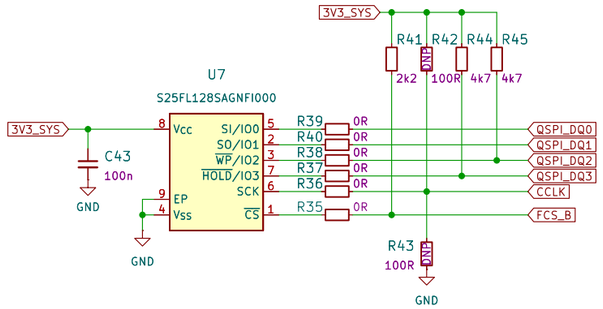
Title: Data Center RDIMM DDR5 Tester		
Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1		Id: 2/10

Master SPI Quad (x4) configuration scheme

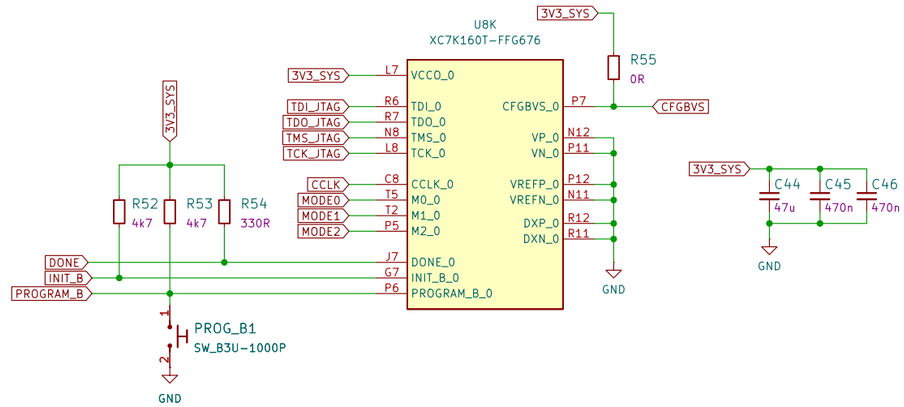
Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash



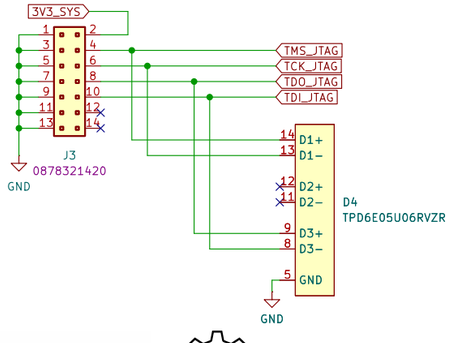
FPGA BANK 0

TODO: verify after FPGA swap

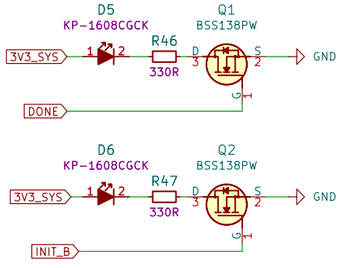


JTAG Connector

Compatible with Xilinx Platform Cable

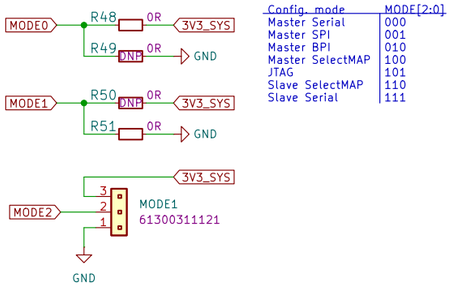


STATUS LEDs



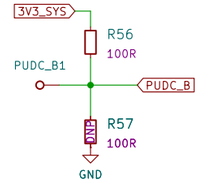
Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Probes



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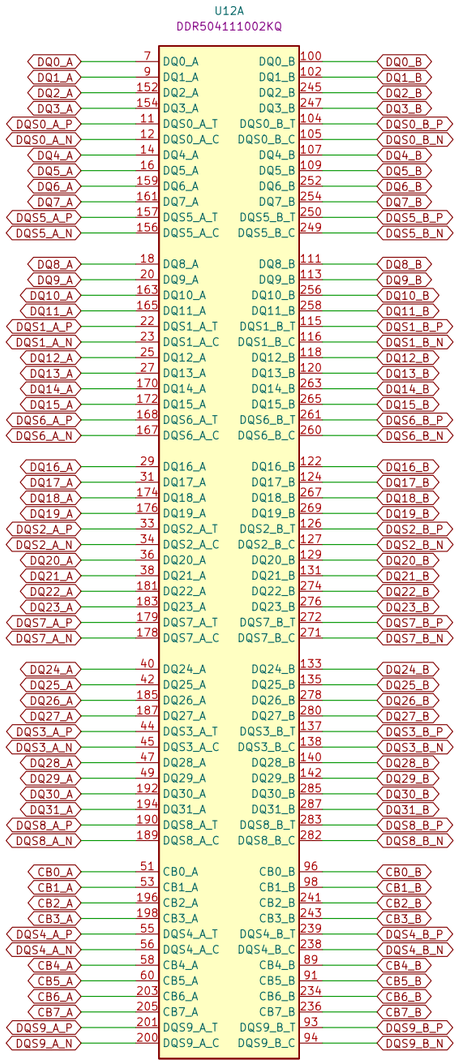
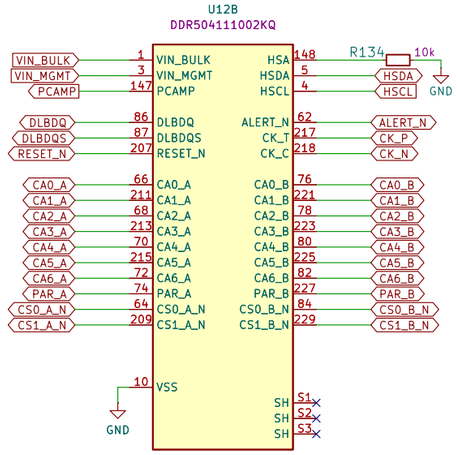
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1		Id: 3/10

DDR5 RDIMM connector





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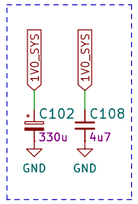
Title: Data Center RDIMM DDR5 Tester

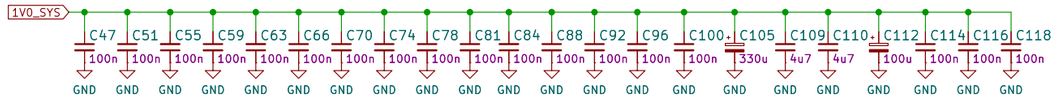
Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 4/10

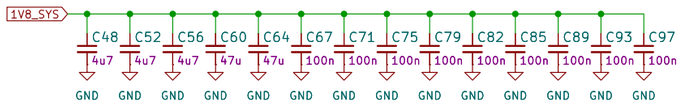
POWER RAILS

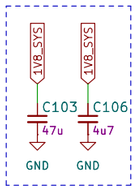
Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!

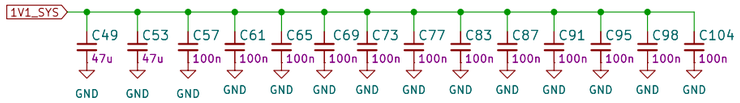
Added capacitors coresponding to PCB Design Guide UG483

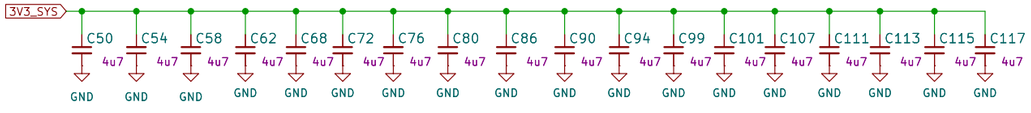




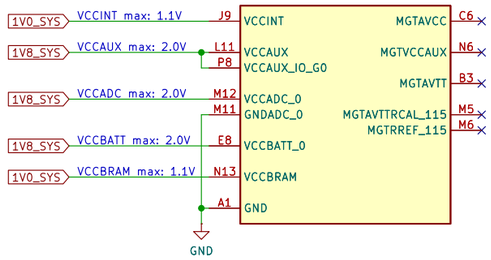




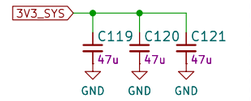




U8J
XC7K160T-FFG676

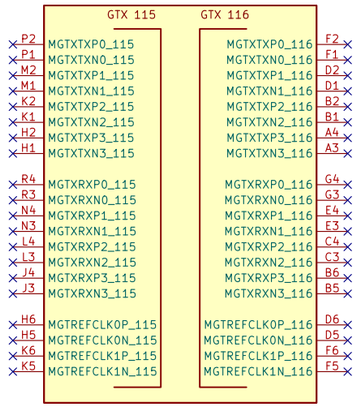


Place close to FPGA banks power supply



UNUSED

U8I
XC7K160T-FFG676



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Sheet: /FPGA power/
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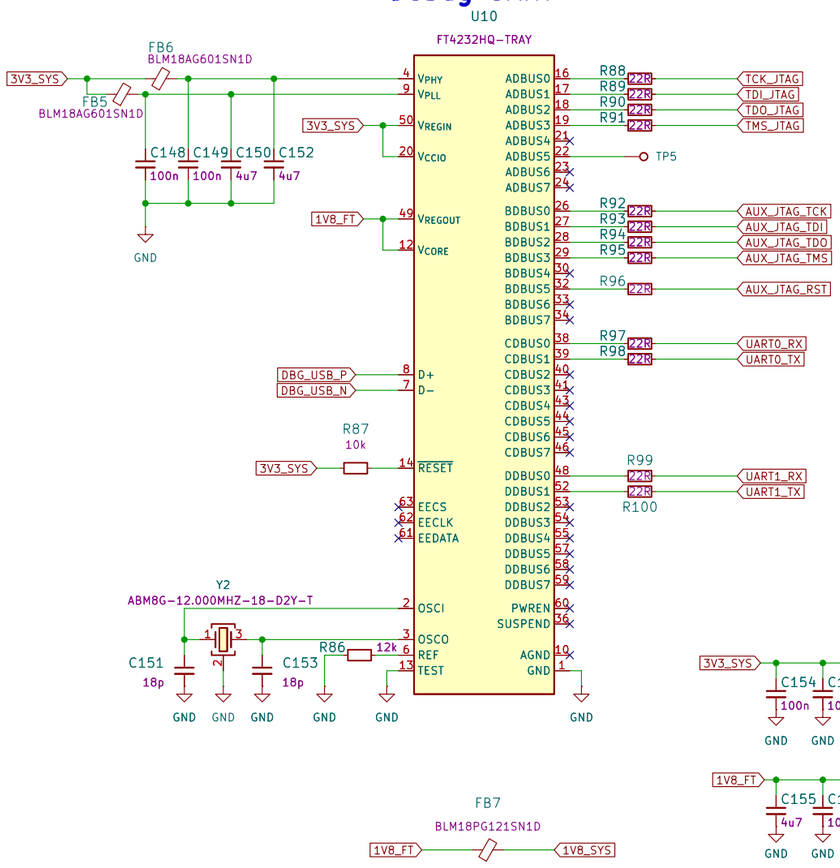
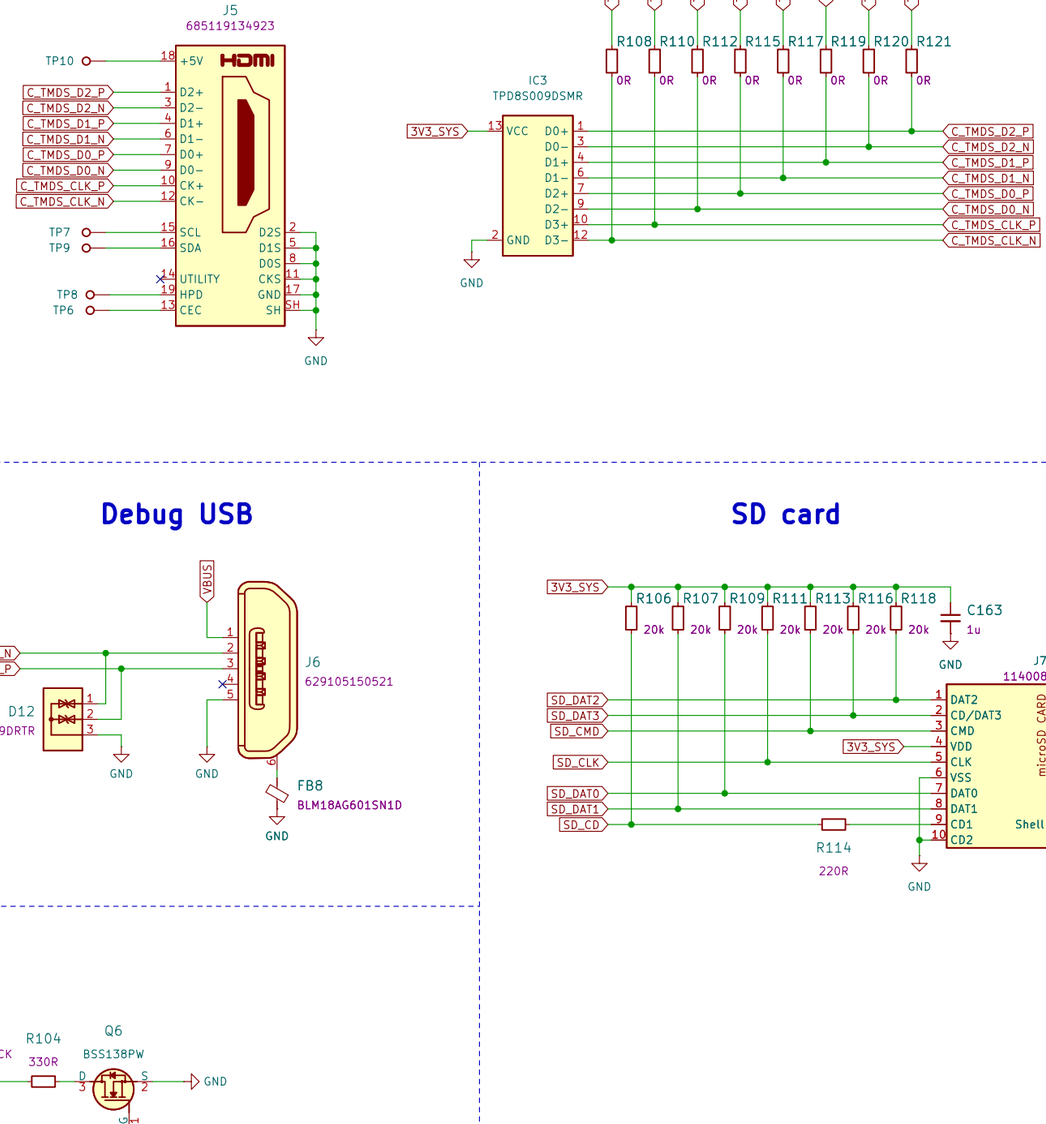
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1		Id: 5/10

Debug UART



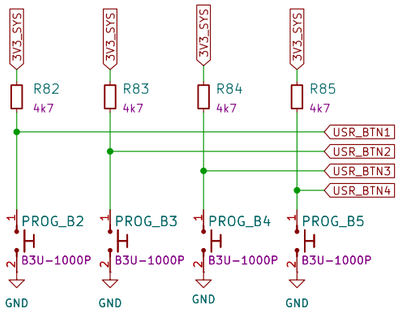
HDMI



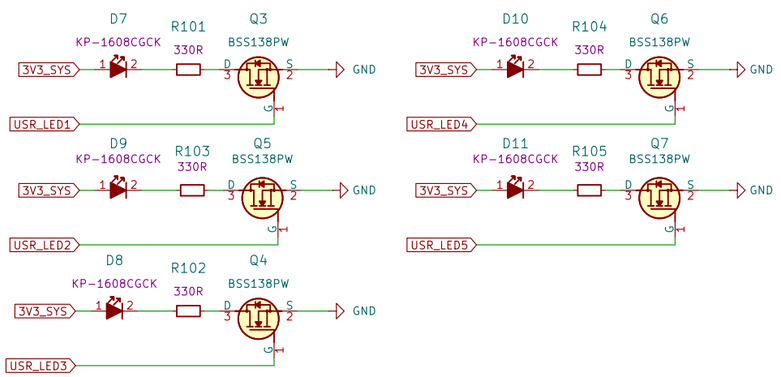
Debug USB

SD card

User buttons



User LEDs



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Sheet: /Interfaces/
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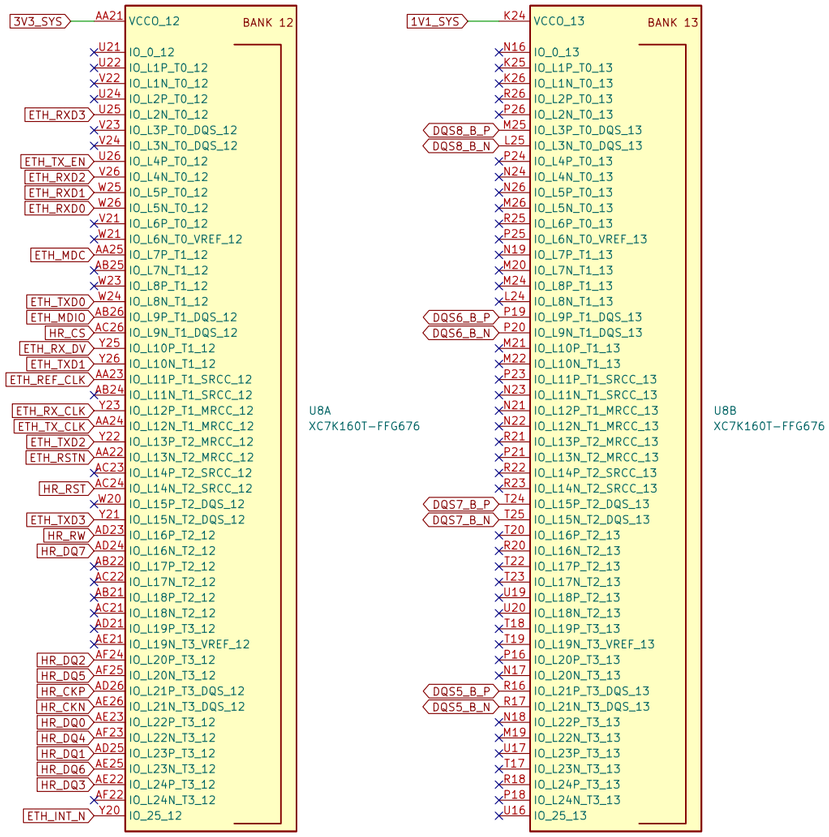
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 6/10

BANK 12

BANK 13

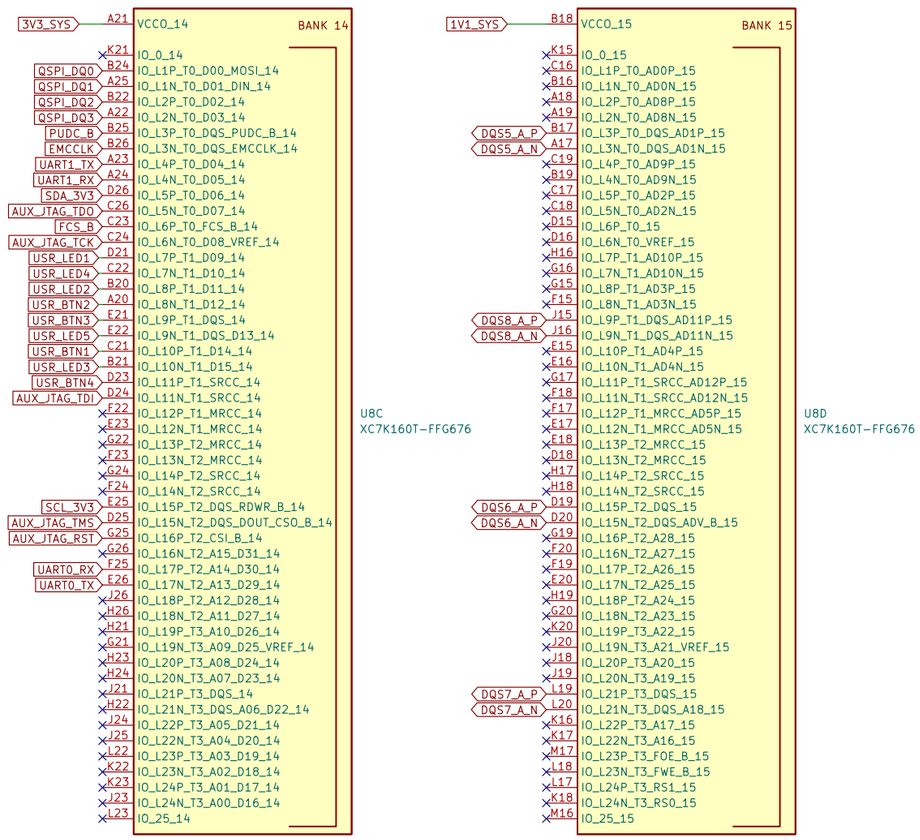
VCCO (HR banks) max: 3.6V



BANK 14

BANK 15

VCCO (HR banks) max: 3.6V



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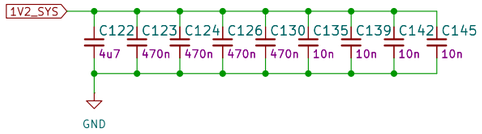
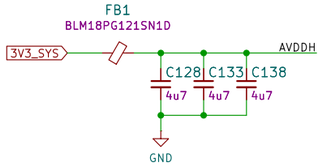
Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1~bpo11+1	Id: 7/10

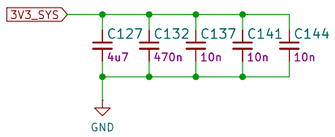
DVDDL decoupling



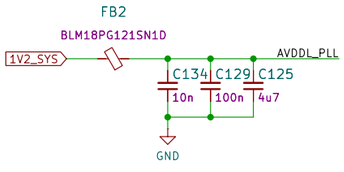
AVDDH decoupling



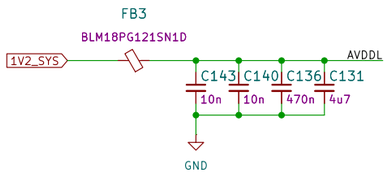
DVDDH decoupling



AVDDL_PLL decoupling



AVDDL decoupling



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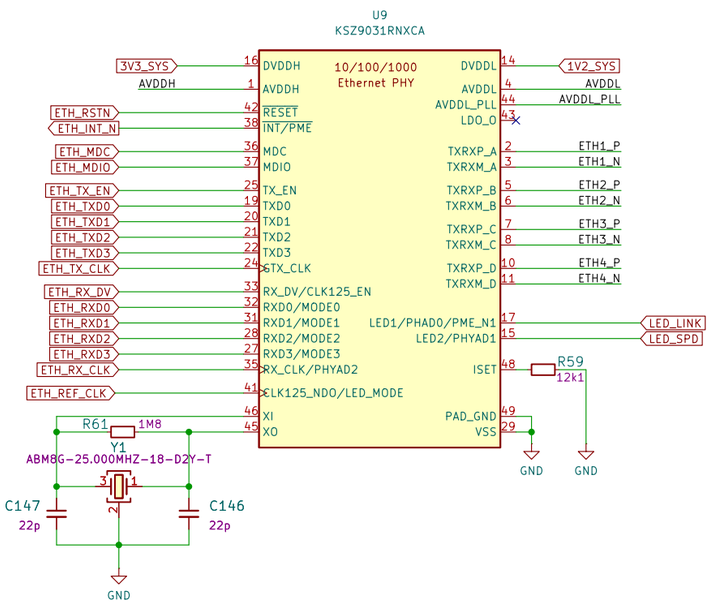
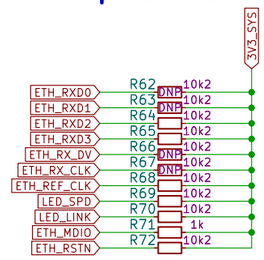
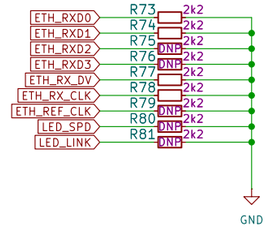


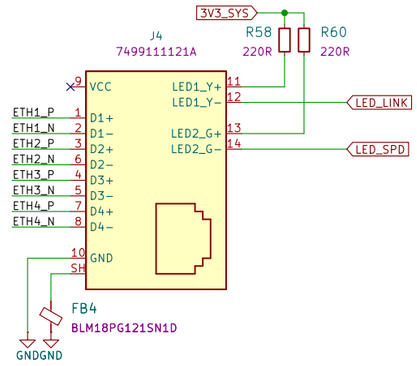
Pull up resistors



Pull down resistors



RJ45 Connector



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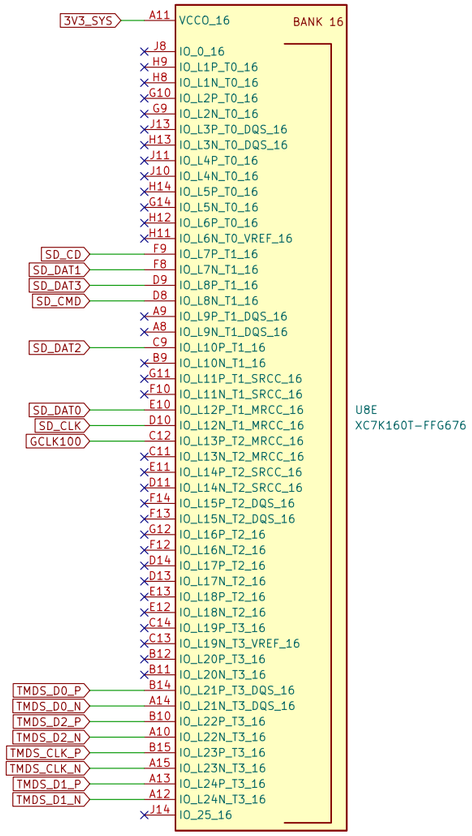
Sheet: /Ethernet/ File: ethernet.kicad_sch	
Title: Data Center RDIMM DDR5 Tester	
Size: A3	Date: 2023-07-27
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1	Id: 8/10

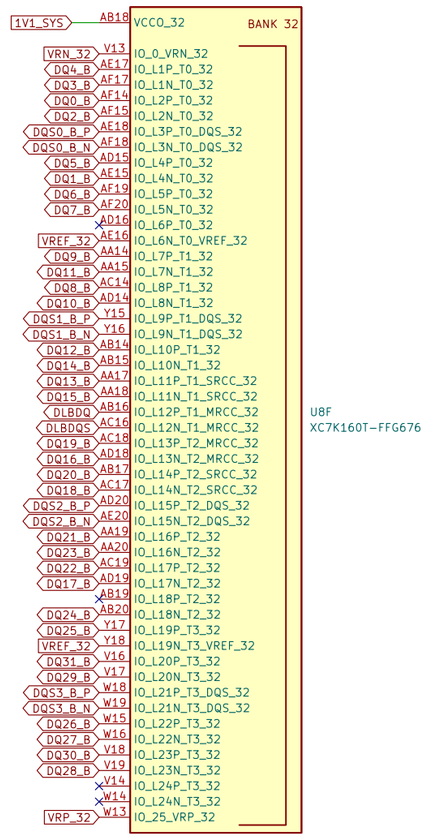
BANK 16

VCCO (HR bank) max: 3.6V



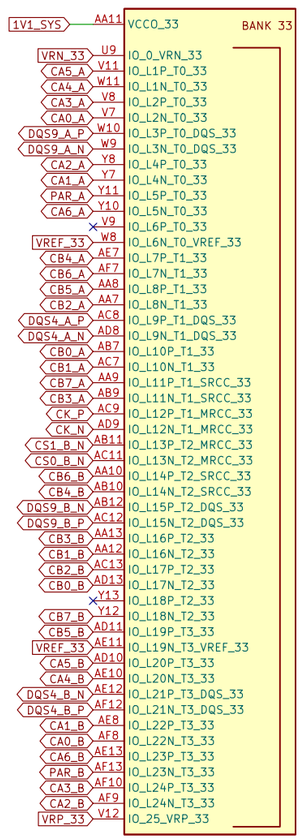
BANK 32

VCCO (HP bank) max: 2.0V



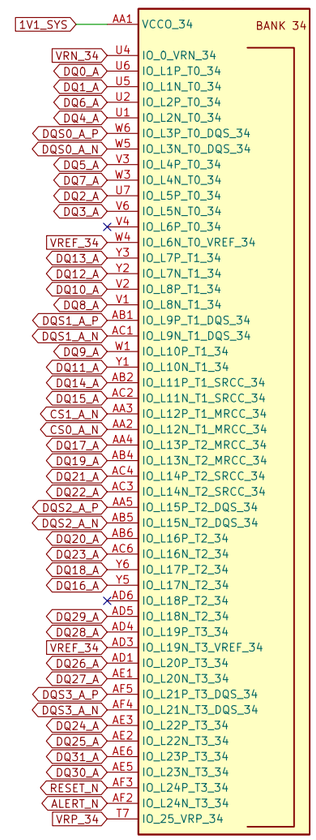
BANK 33

VCCO (HP bank) max: 2.0V

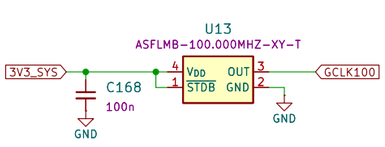


BANK 34

VCCO (HP bank) max: 2.0V



Clock source



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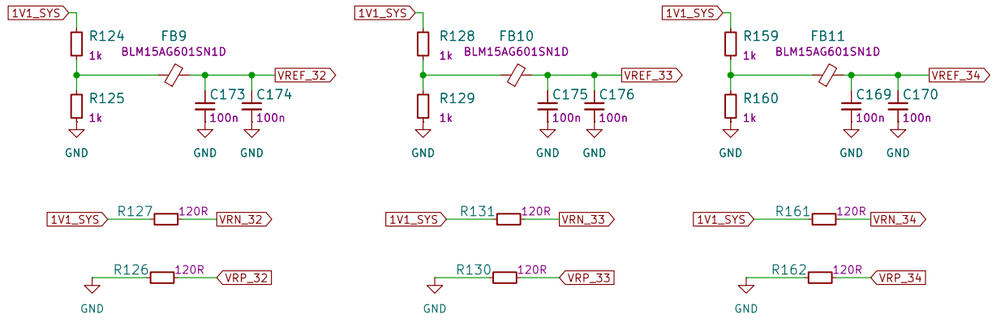
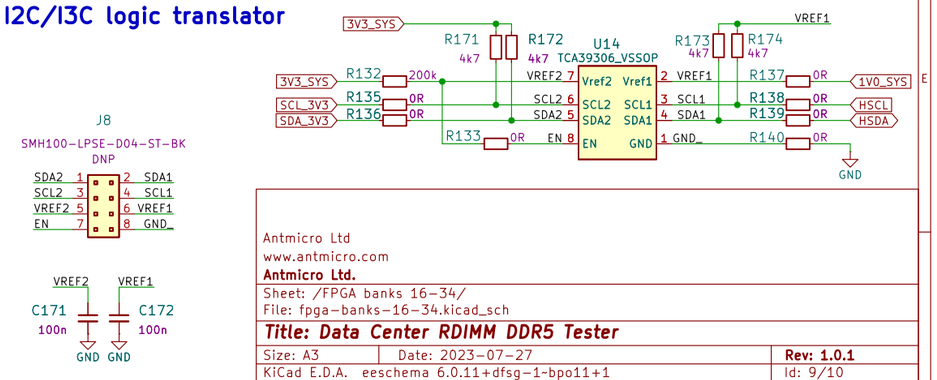


I2C/I3C logic translator



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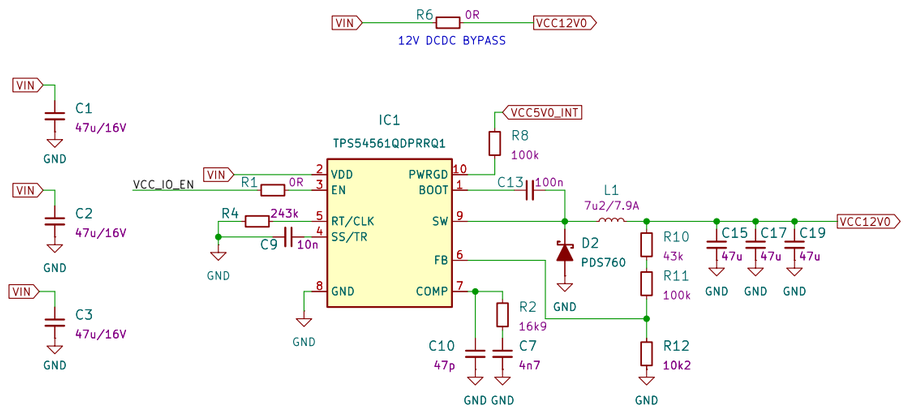
Sheet: /FPGA banks 16-34/
File: fpga-banks-16-34.kicad_sch

Title: Data Center RDIMM DDR5 Tester

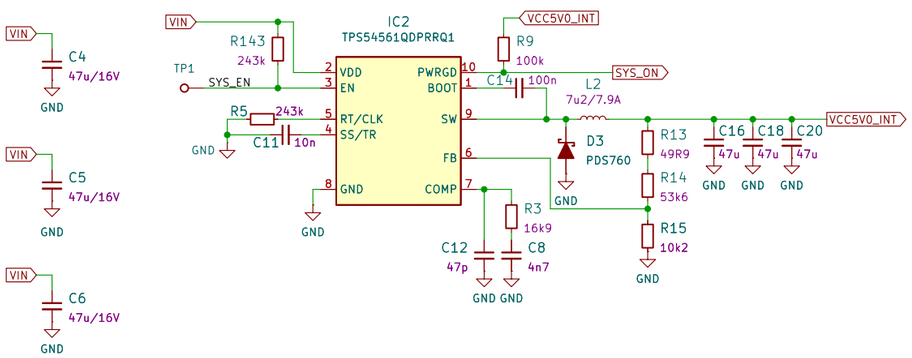
Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 9/10

Input power connector

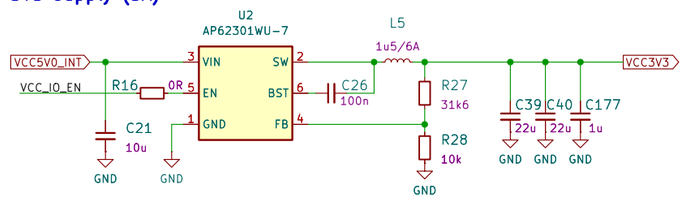
Main supply (12V 5A)



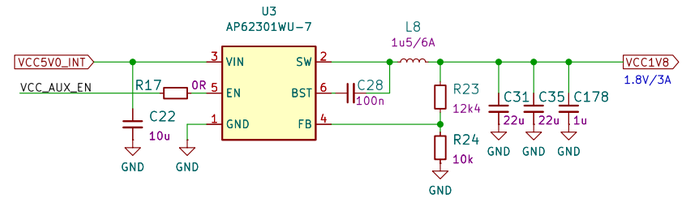
5V0 supply



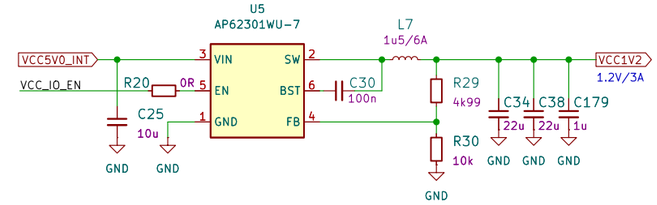
3V3 supply (3A)



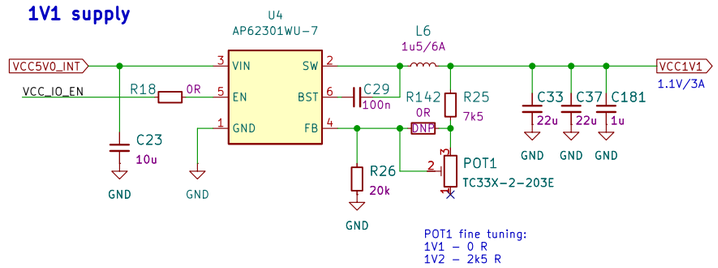
1V8 supply



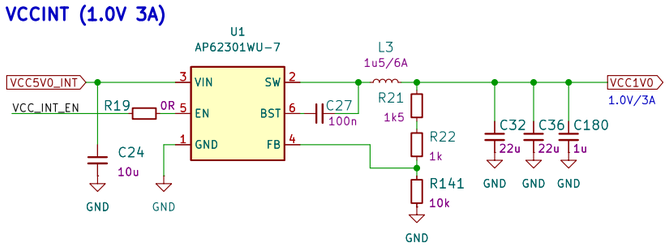
1V2 supply



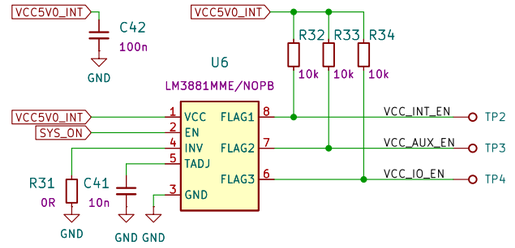
1V1 supply



VCCINT (1.0V 3A)

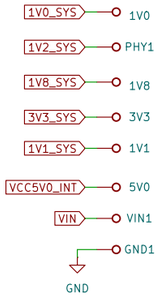


Power sequencer

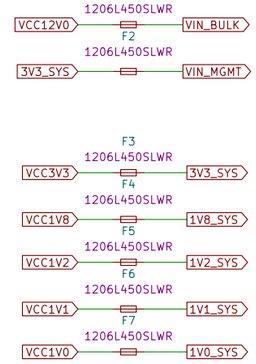


STEP1 – VCCINT (1.0V) for FPGA
STEP2 – VCCAUX (1.8V, 2.5V, 1.2V) for FPGA and DDR
STEP3 – VCCIO (3.3V, 1.2V, 0.6V) for FPGA, PHY and DDR

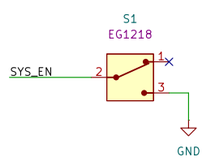
Probes



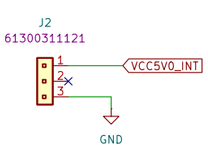
Fuses



Power switch



Optional FAN connector



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Title: Data Center RDIMM DDR5 Tester

Size: A3	Date: 2023-07-27	**Rev: 1.0.1**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 10/10