DDR5 Tester

Sheet: HyperRAM
File: hyperram.sch

Sheet: DDR5
File: DDR5.sch

Sheet: Interfaces
File: interfaces.sch

Sheet: Ethernet
File: ethernet.sch

Sheet: Supply
File: supply.sch

Sheet: Config SPI flash
File: config-spi.sch

Sheet: FPGA power
File: fpga-power.sch

Sheet: FPGA banks 12-15
File: fpga-banks-12-15.sch

Sheet: FPGA banks 16-34
File: fpga-banks-16-34.sch

Logo N2 oshw_logo

Logo N1 antmicro_logo

antmicro

open source hardware

Antmicro Ltd
www.antmicro.com

Sheet: /
File: data-center-ddr5-tester.sch

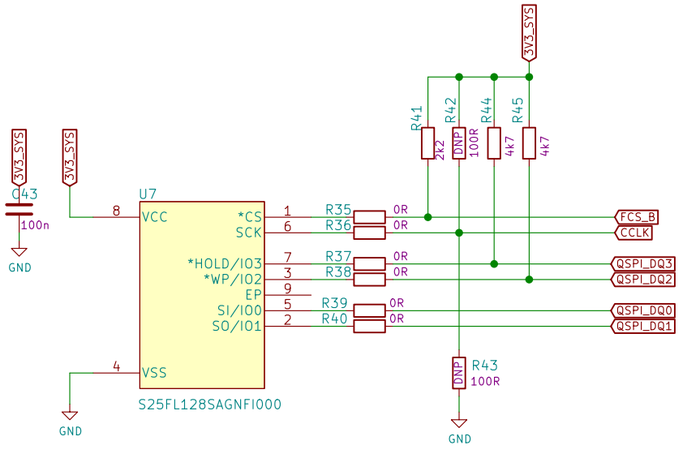
Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 1/10

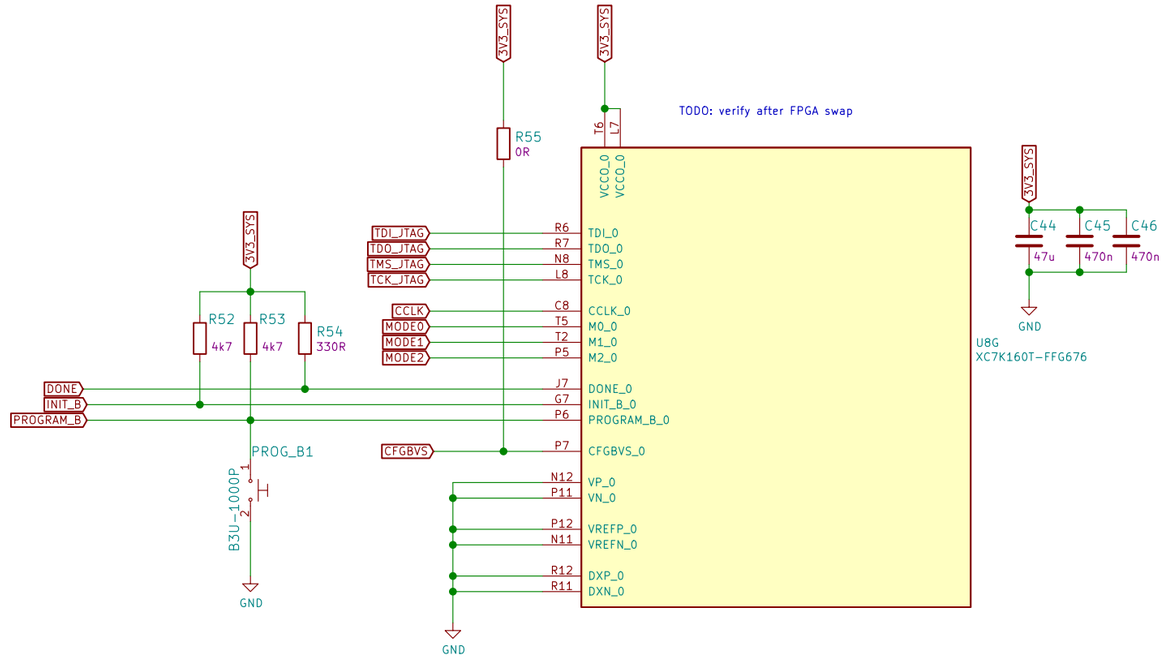
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

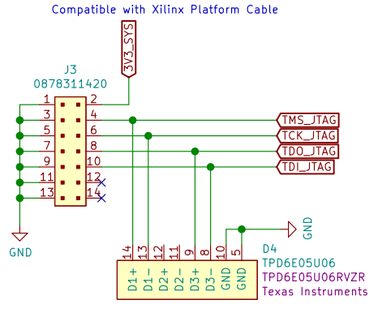


FPGA BANK 0

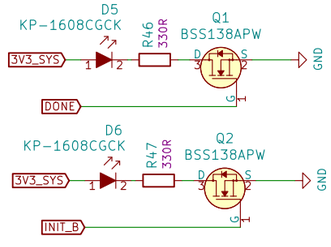


JTAG Connector

Compatible with Xilinx Platform Cable

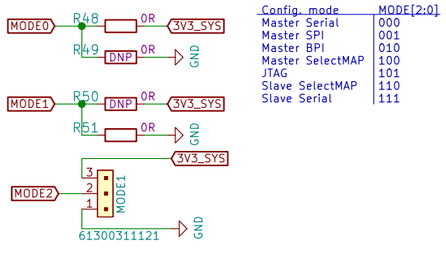


STATUS LEDs



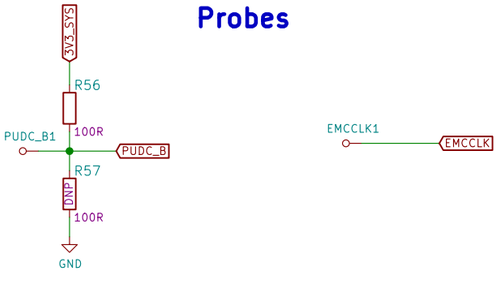
Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Probes



antmicro

open source hardware

Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

Sheet: /Config SPI flash/
File: config–spi.sch

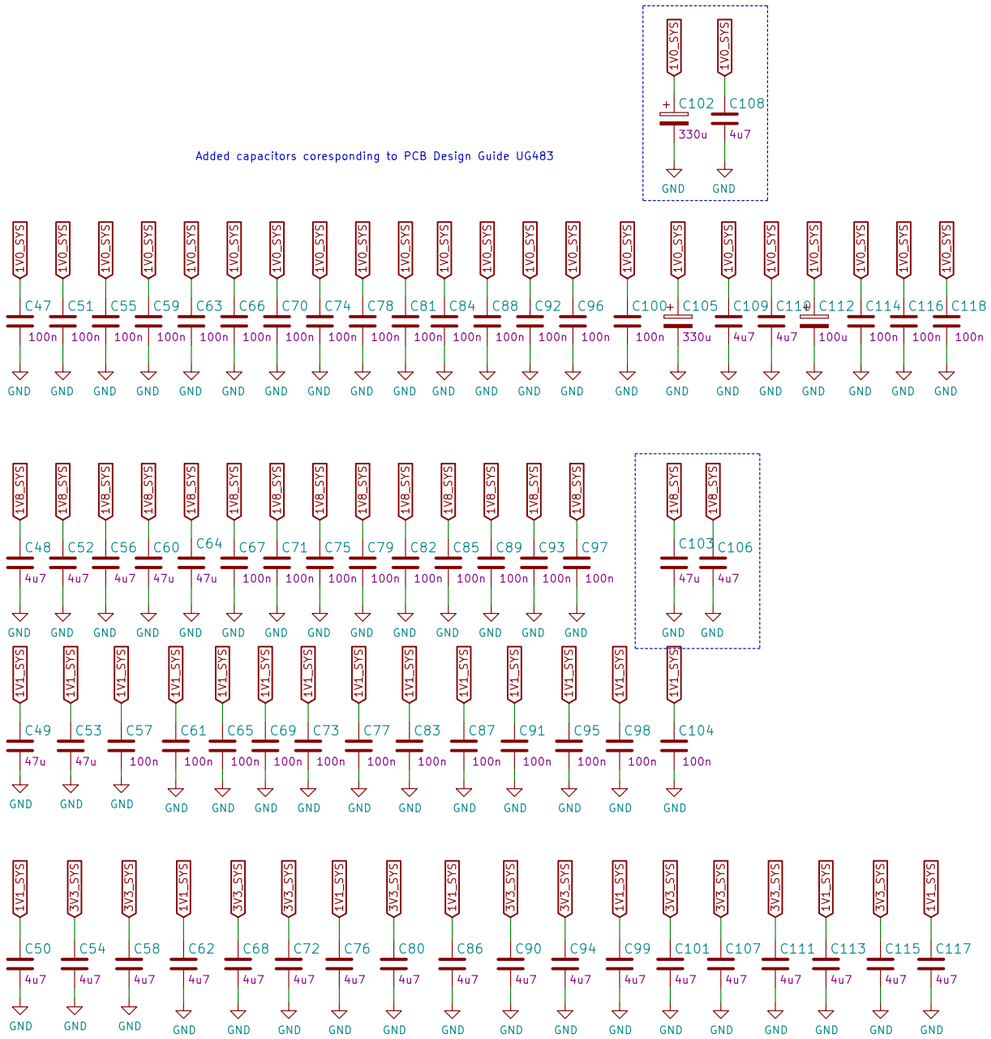
Title: DDR5 Tester

Size: A3	Date: 2022–03–08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1–1	Id: 2/10

POWER RAILS

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!

Added capacitors coresponding to PCB Design Guide UG483

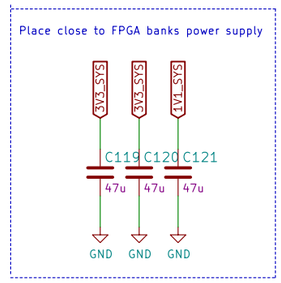


U8H
XC7K160T-FFG676

VCCAUX max: 2.0V
VCCINT max: 1.1V
VCCADC max: 2.0V
VCCBATT max: 2.0V
VCCBRAM max: 1.1V

L11	VCCAUX	VCCINT	J9
M10	VCCAUX	VCCINT	K8
P10	VCCAUX	VCCINT	K10
T10	VCCAUX	VCCINT	K12
U11	VCCAUX	VCCINT	K14
		VCCINT	L9
T8	VCCAUX_IO_G0	VCCINT	L13
R9	VCCAUX_IO_G0	VCCINT	L15
P8	VCCAUX_IO_G0	VCCINT	M8
		VCCINT	M14
M11	GNDADC_0	VCCINT	N9
M12	VCCADC_0	VCCINT	N15
E8	VCCBATT_0	VCCINT	P14
N13	VCCBRAM	VCCINT	R15
R13	VCCBRAM	VCCINT	T14
T12	VCCBRAM	VCCINT	U15
U13	VCCBRAM	VCCINT	
A1	GND	GND	M13
A2	GND	GND	M15
A5	GND	GND	M23
A6	GND	GND	N1
A7	GND	GND	N2
A16	GND	GND	N5
A26	GND	GND	N7
B4	GND	GND	N10
B7	GND	GND	N14
B13	GND	GND	N20
B23	GND	GND	P3
C1	GND	GND	P4
C5	GND	GND	P9
C7	GND	GND	P13
C10	GND	GND	P15
C20	GND	GND	P17
D4	GND	GND	R1
D7	GND	GND	R2
D17	GND	GND	R5
E1	GND	GND	R8
E2	GND	GND	R10
E5	GND	GND	R14
E7	GND	GND	R24
E14	GND	GND	T1
E24	GND	GND	T3
F3	GND	GND	T4
F4	GND	GND	T9
F7	GND	GND	T11
F11	GND	GND	T13
F21	GND	GND	T15
G1	GND	GND	T21
G5	GND	GND	U8
G8	GND	GND	U10
G18	GND	GND	U12
H4	GND	GND	U14
H7	GND	GND	U18
H15	GND	GND	V5
H25	GND	GND	V15
J1	GND	GND	V25
J2	GND	GND	W2
J5	GND	GND	W12
J12	GND	GND	W22
J22	GND	GND	Y9
K3	GND	GND	Y19
K4	GND	GND	AA6
K7	GND	GND	AA16
K9	GND	GND	AA26
K11	GND	GND	AB3
K13	GND	GND	AB13
K19	GND	GND	AB23
L1	GND	GND	AC10
L5	GND	GND	AC20
L10	GND	GND	AD7
L12	GND	GND	AD17
L14	GND	GND	AE4
L16	GND	GND	AE14
L26	GND	GND	AE24
M4	GND	GND	AF1
M7	GND	GND	AF11
M9	GND	GND	AF21

Place close to FPGA banks power supply



UNUSED

U8E
XC7K160T-FFG676
data-center-ddr5-tester-footprints:BGA676C100P26X26_2700X2700X254

P2	MGTXTXP0_115	MGTXTXP0_116	F2
P1	MGTXTXN0_115	MGTXTXN0_116	F1
M2	MGTXTXP1_115	MGTXTXP1_116	D2
M1	MGTXTXN1_115	MGTXTXN1_116	D1
K2	MGTXTXP2_115	MGTXTXP2_116	B2
K1	MGTXTXN2_115	MGTXTXN2_116	B1
H2	MGTXTXP3_115	MGTXTXP3_116	A4
H1	MGTXTXN3_115	MGTXTXN3_116	A3
R4	MGTXRXP0_115	MGTXRXP0_116	G4
R3	MGTXRXN0_115	MGTXRXN0_116	G3
N4	MGTXRXP1_115	MGTXRXP1_116	E4
N3	MGTXRXN1_115	MGTXRXN1_116	E3
L4	MGTXRXP2_115	MGTXRXP2_116	C4
L3	MGTXRXN2_115	MGTXRXN2_116	C3
J4	MGTXRXP3_115	MGTXRXP3_116	B6
J3	MGTXRXN3_115	MGTXRXN3_116	B5
H6	MGTREFCLK0P_115	MGTREFCLK0P_116	D6
H5	MGTREFCLK0N_115	MGTREFCLK0N_116	D5
K6	MGTREFCLK1P_115	MGTREFCLK1P_116	F6
K5	MGTREFCLK1N_115	MGTREFCLK1N_116	F5

U8F
XC7K160T-FFG676
data-center-ddr5-tester-footprints:BGA676C100P26X26_2700X2700X254

C6	MGTAVCC	MGTAVTT	B3
E6	MGTAVCC	MGTAVTT	C2
G6	MGTAVCC	MGTAVTT	D3
J6	MGTAVCC	MGTAVTT	G2
L6	MGTAVCC	MGTAVTT	H3
N6	MGTVCCAUX	MGTAVTT	L2
		MGTAVTT	M3
		MGTAVTTRCAL_115	M5
		MGTRREF_115	M6

antmicro
open source hardware

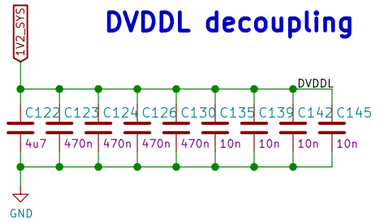
Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

Sheet: /FPGA power/
File: fpga-power.sch

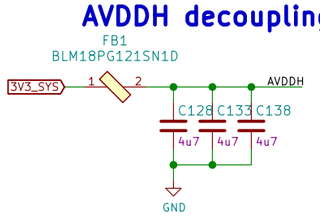
Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 3/10

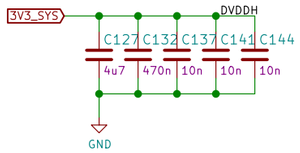
DVDDL decoupling



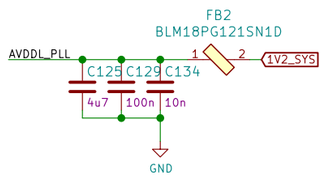
AVDDH decoupling



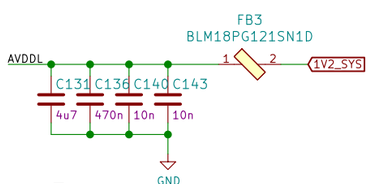
DVDDH decoupling



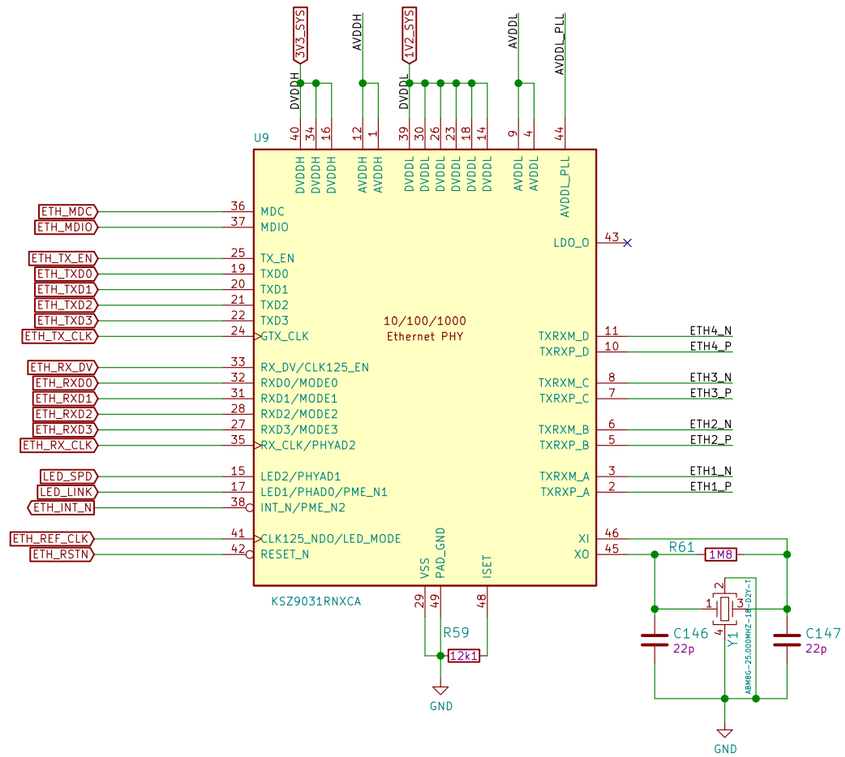
AVDDL_PLL decoupling



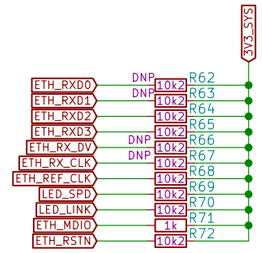
AVDDL decoupling



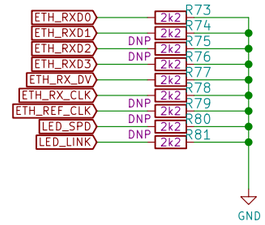
PHY



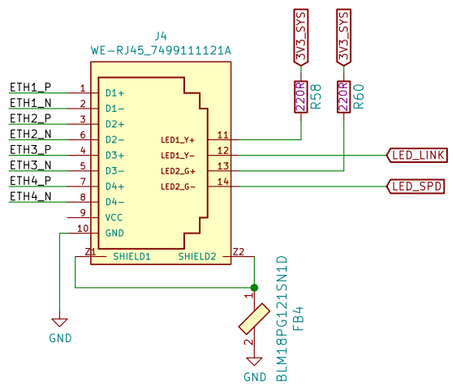
Pull up resistors



Pull down resistors



RJ45 Connector



antmicro

open source hardware

Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

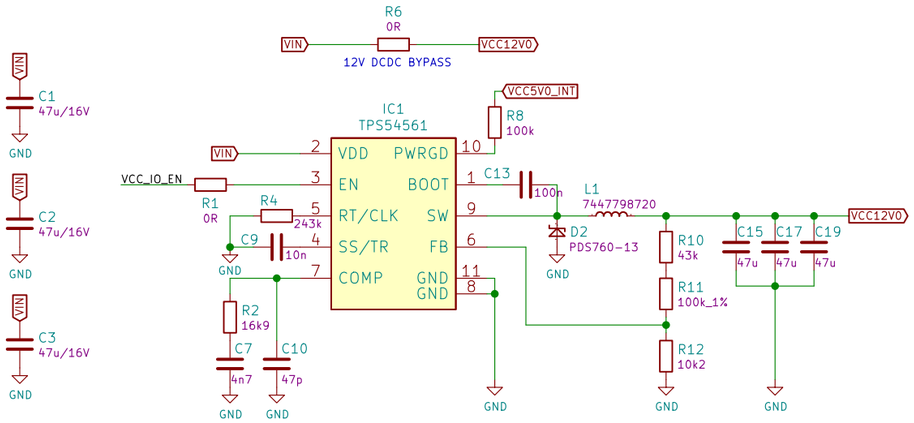
Sheet: /Ethernet/
File: ethernet.sch

Title: DDR5 Tester

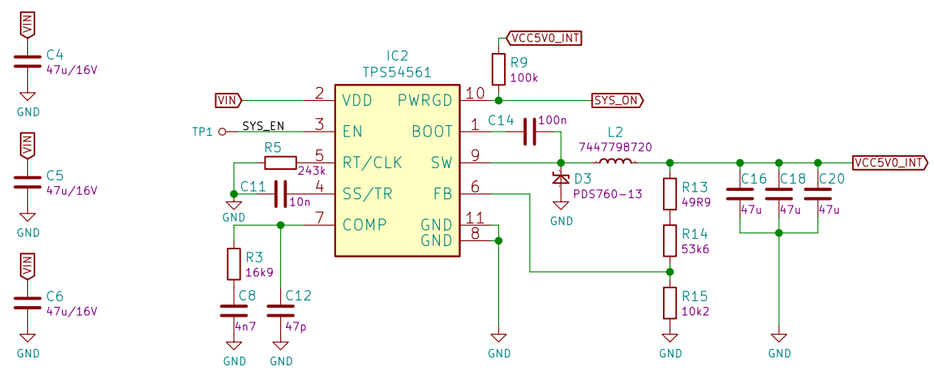
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 4/10

Input power connector

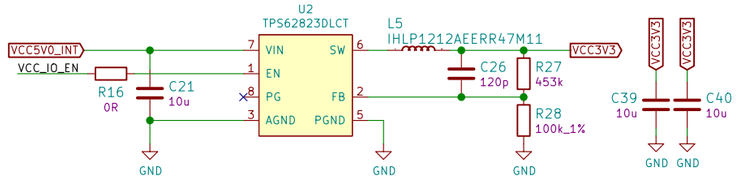
Main supply (12V 5A)



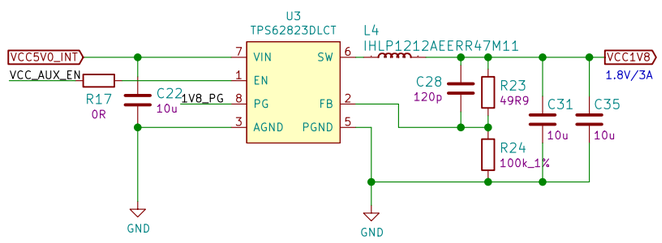
5V0 supply



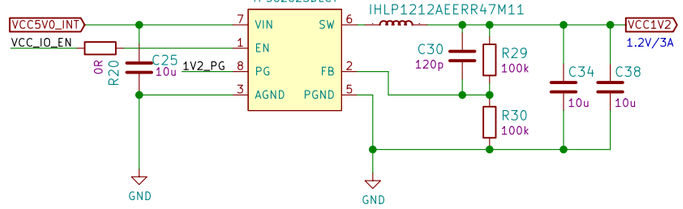
3V3 supply (2A)



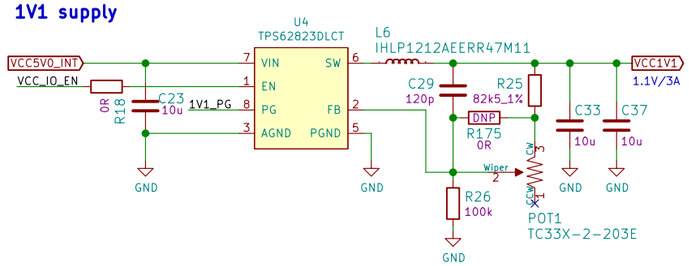
1V8 supply



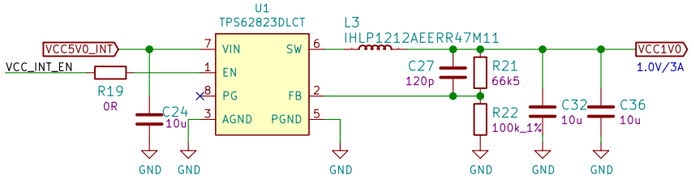
1V2 supply



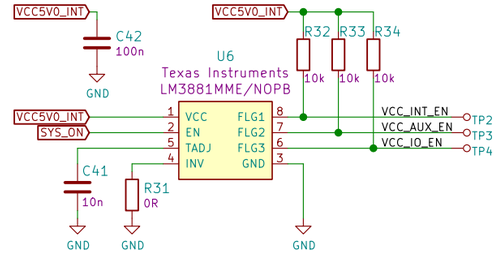
1V1 supply



VCCINT (1.0V 2A)

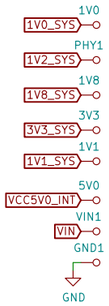


Power sequencer

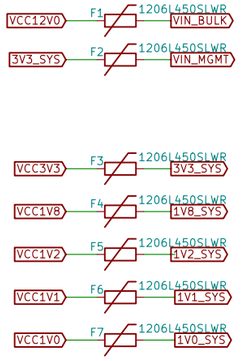


STEP1 – VCCINT (1.0V) for FPGA
STEP2 – VCCAUX (1.8V, 2.5V, 1.2V) for FPGA and DDR
STEP3 – VCCIO (3.3V, 1.2V, 0.6V) for FPGA, PHY and DDR

Probes

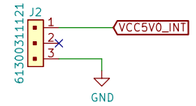


Fuses



Power switch

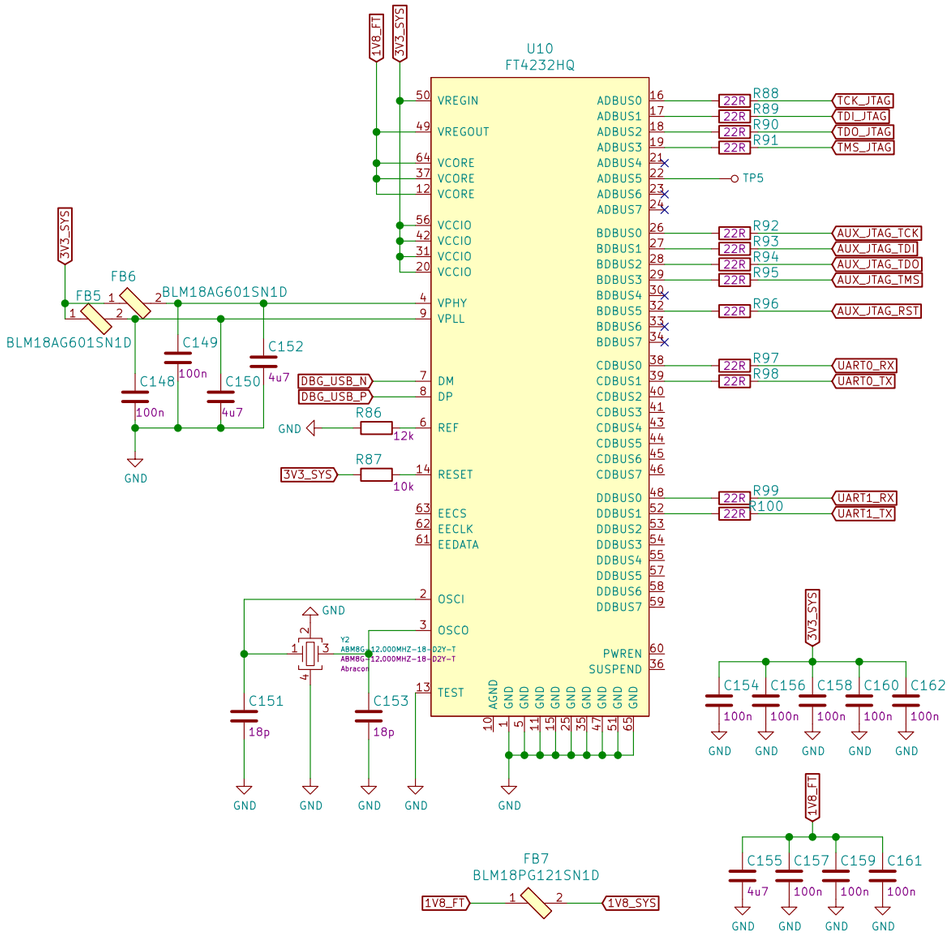
Optional FAN connector



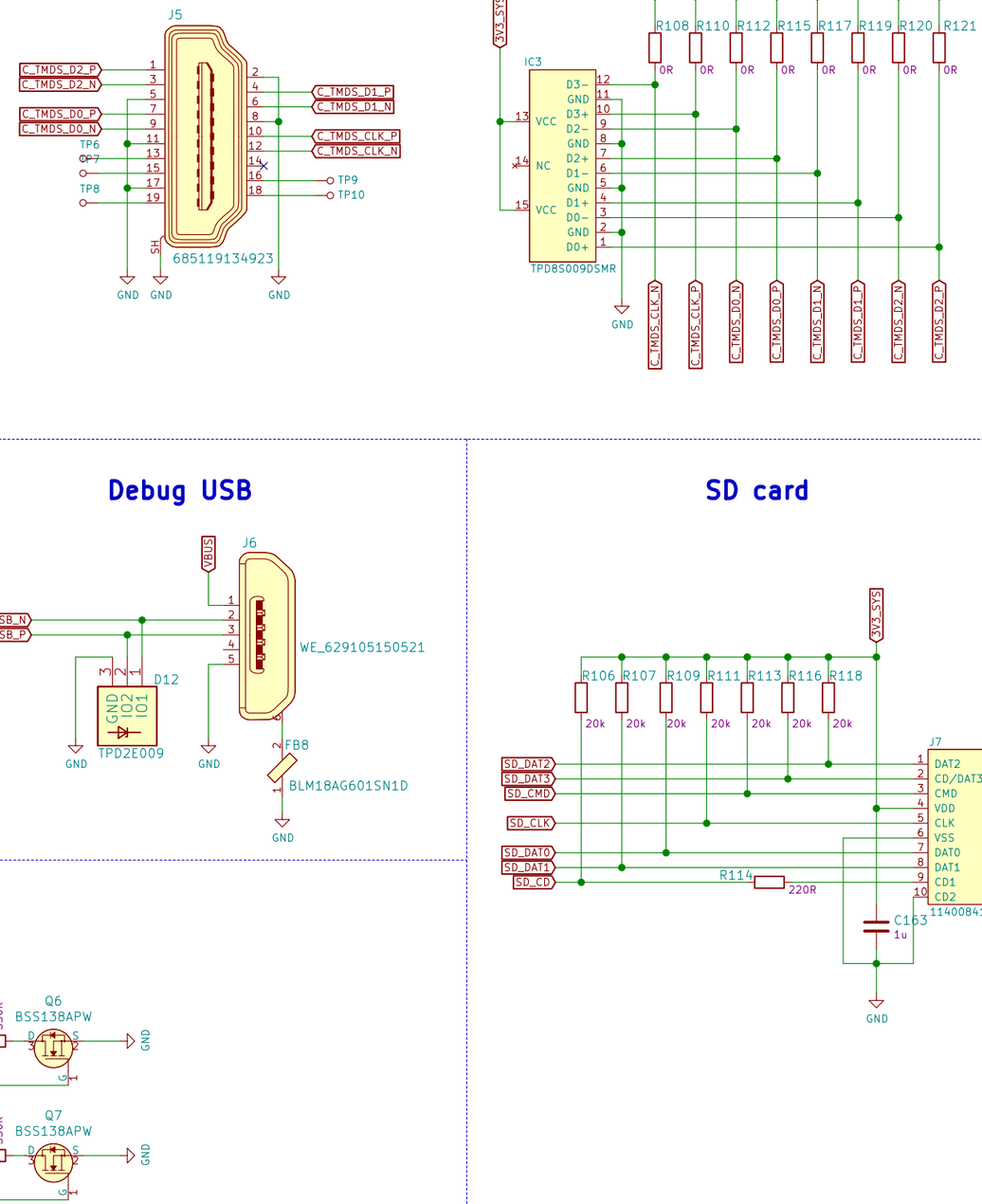
antmicro
open source hardware

Antmicro Ltd www.antmicro.com **Antmicro Ltd.**	
Sheet: /Supply/ File: supply.sch	
Title: DDR5 Tester	
Size: A3	Date: 2022-03-08
KiCad E.D.A. eeschema 5.1.9+dfsg1-1	**Rev: 1.0.0** Id: 5/10

Debug UART



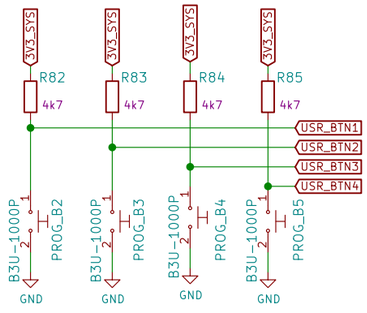
HDMI



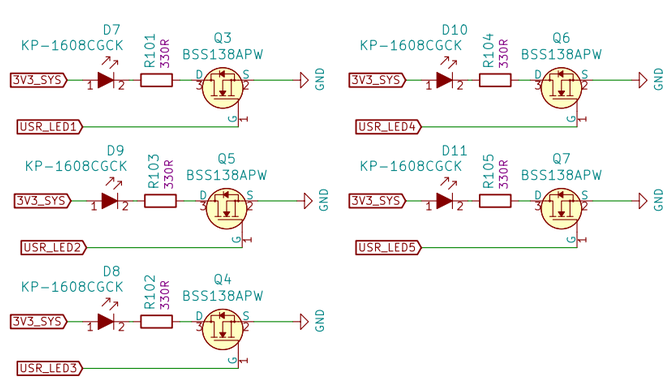
Debug USB

SD card

User buttons



User LEDs



antmicro

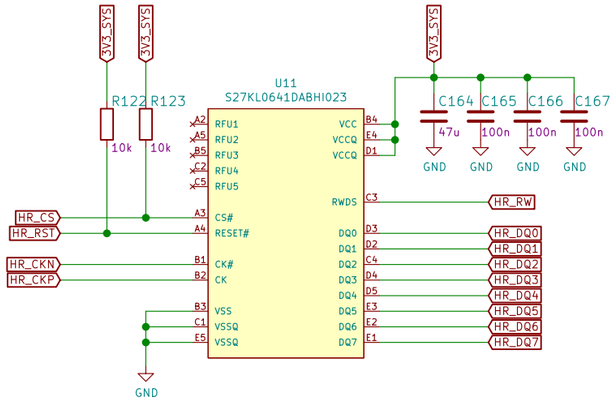
open source hardware

Antmicro Ltd
www.antmicro.com
Antmicro Ltd.
Sheet: /Interfaces/
File: interfaces.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 6/10

HyperRAM



antmicro

open source hardware

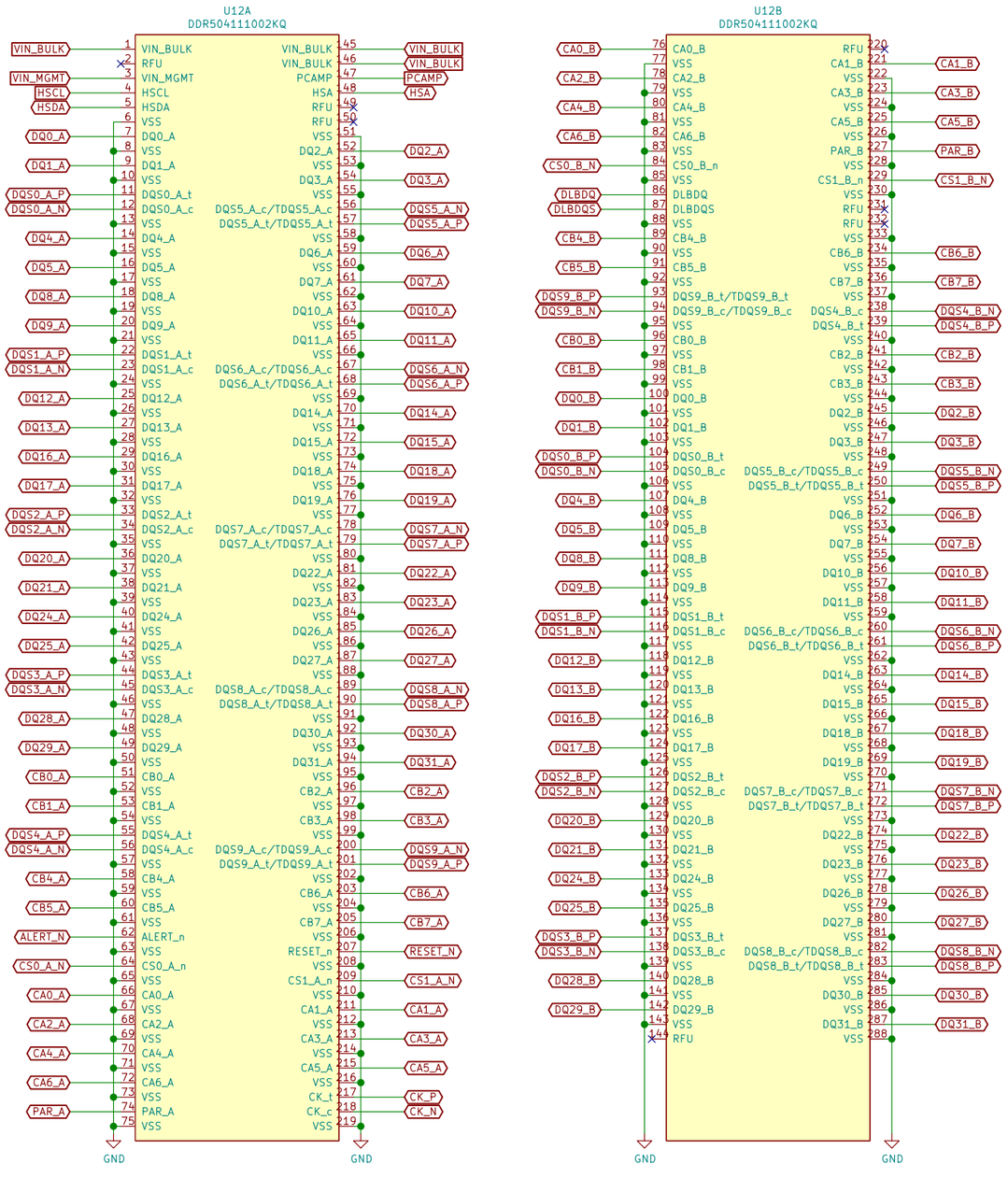
Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

Sheet: /HyperRAM/
File: hyperram.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 7/10

DDR5 RDIMM connector



antmicro

open source hardware

Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

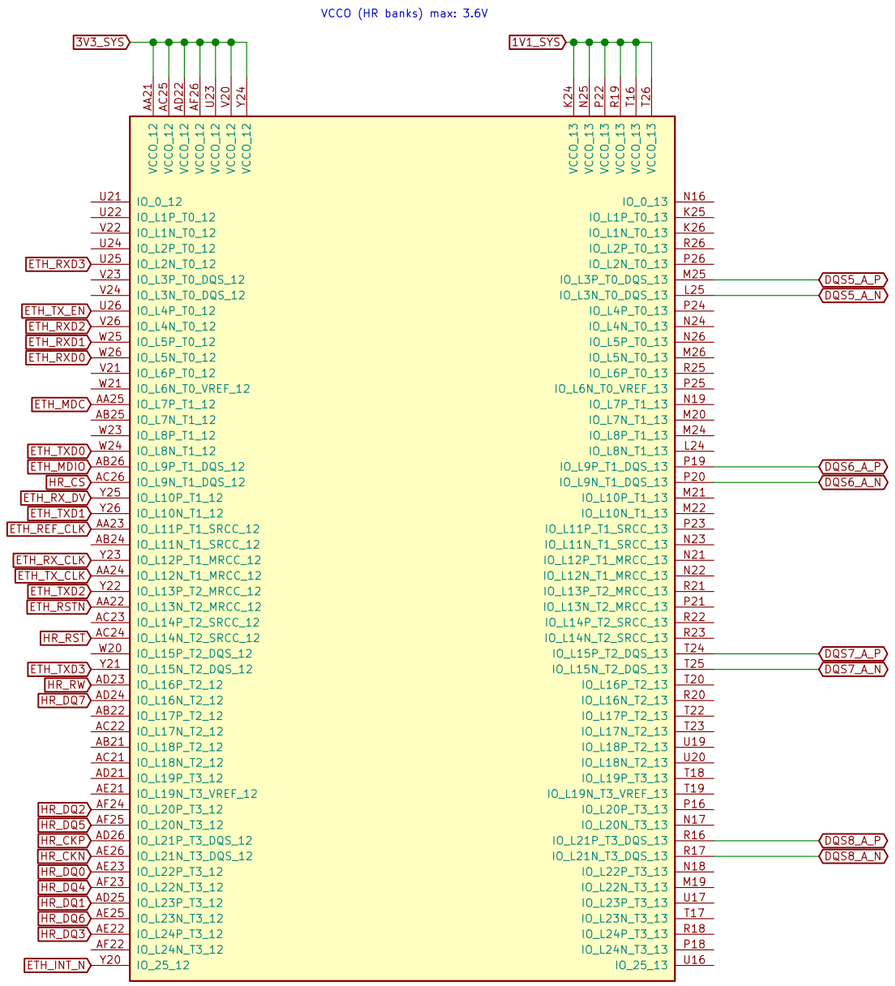
Sheet: /DDR5/
File: DDR5.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A. eeschema 5.1.9+dfsg1-1		Id: 8/10

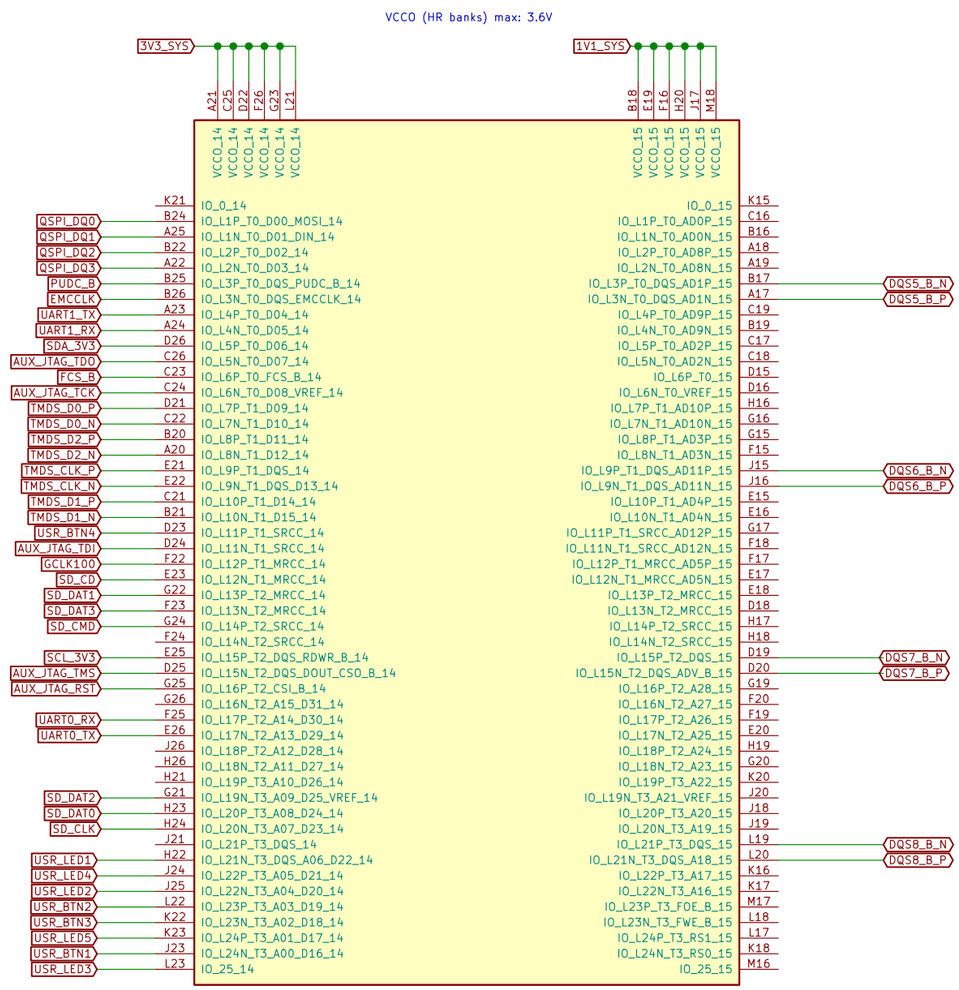
BANK 12

BANK 13



BANK 14

BANK 15



antmicro

open source hardware

Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

Sheet: /FPGA banks 12-15/
File: fpga-banks-12-15.sch

Title: DDR5 Tester

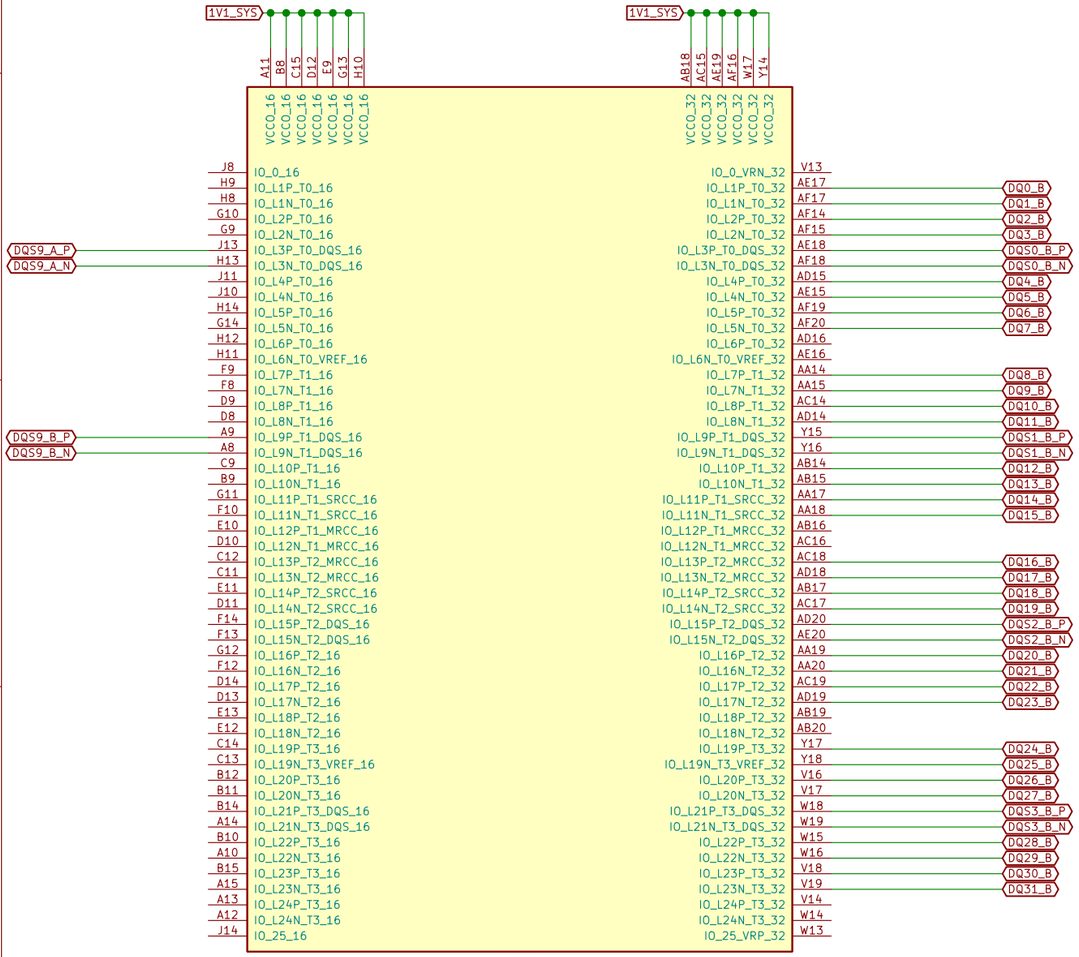
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A. eeschema 5.1.9+dfsg1-1		Id: 9/10

BANK 16

BANK 32

VCCO (HR bank) max: 3.6V

VCCO (HP bank) max: 2.0V



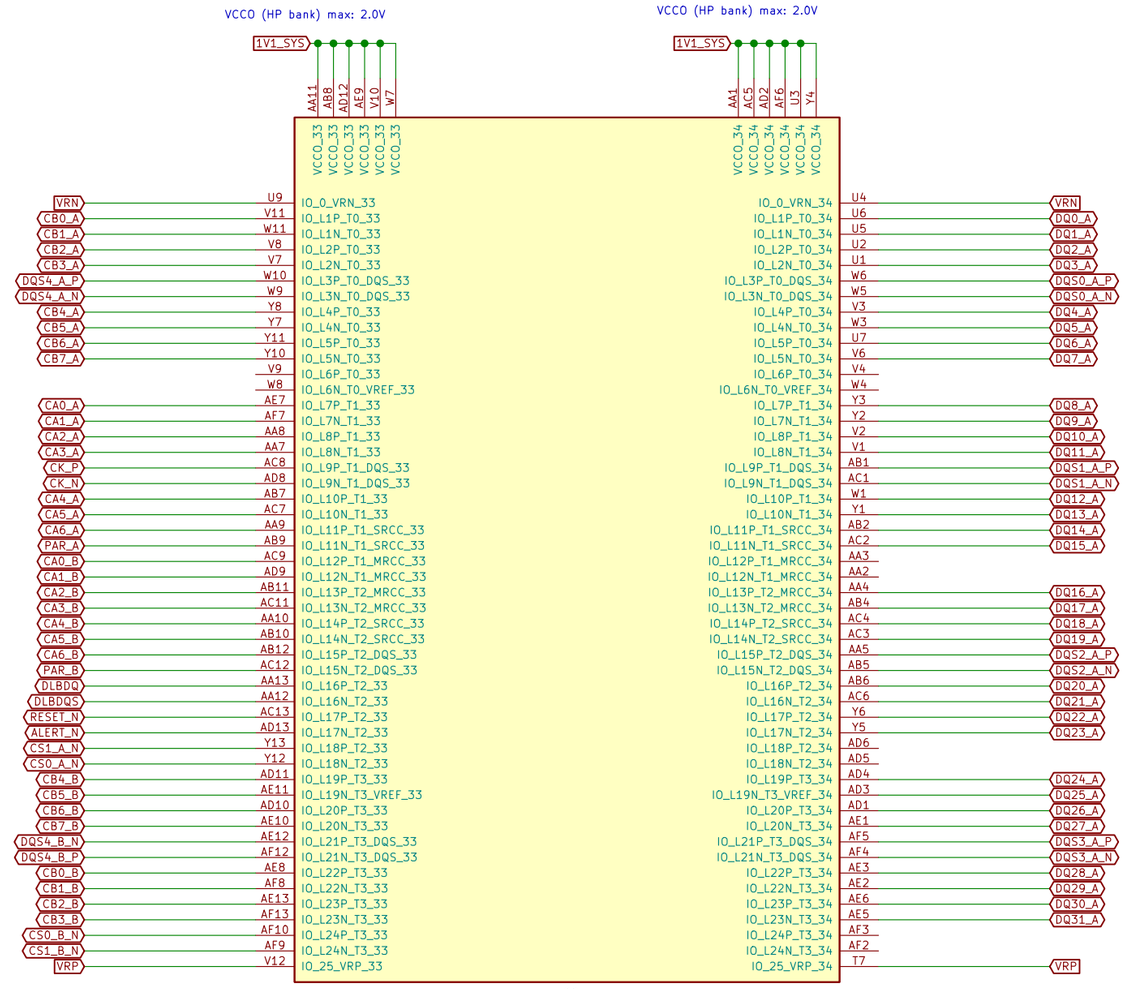
U8C
XC7K160T-FFG676
data-center-ddr5-tester-footprints:BGA676C100P26X26_2700X2700X254

BANK 33

BANK 34

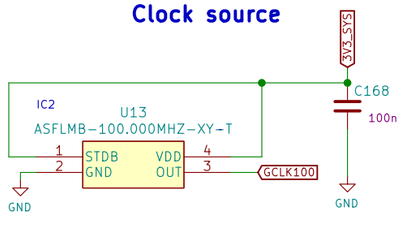
VCCO (HP bank) max: 2.0V

VCCO (HP bank) max: 2.0V

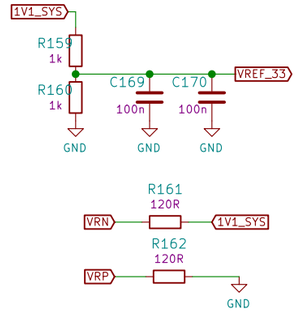


U8D
XC7K160T-FFG676
data-center-ddr5-tester-footprints:BGA676C100P26X26_2700X2700X254

Clock source

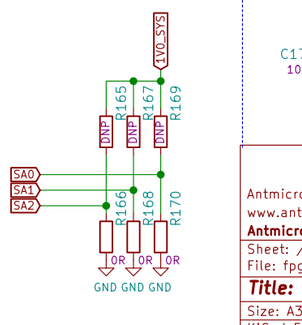


VREF

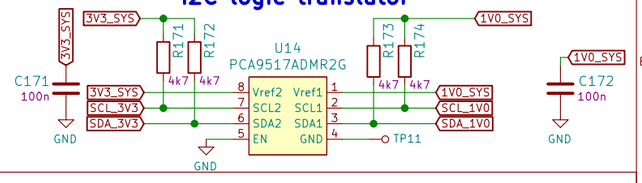


Serial adress select

Default 000



I2C logic translator



Antmicro Ltd
www.antmicro.com
Antmicro Ltd.

Sheet: /FPGA banks 16-34/
File: fpga-banks-16-34.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A. eeschema 5.1.9+dfsg1-1		Id: 10/10

antmicro

open source hardware