

# DDR5 Tester

Sheet: HyperRAM



File: hyperram.sch

Sheet: DDR5



File: DDR5.sch

Sheet: Interfaces



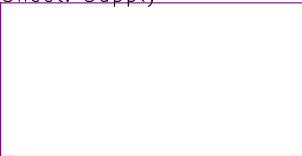
File: interfaces.sch

Sheet: Ethernet



File: ethernet.sch

Sheet: Supply



File: supply.sch

Sheet: Config SPI flash



File: config-spi.sch

Sheet: FPGA power



File: fpga-power.sch

Sheet: FPGA banks 12-15



File: fpga-banks-12-15.sch

Sheet: FPGA banks 16-34



File: fpga-banks-16-34.sch

Logo <sup>N2</sup> oshw\_logo  
Logo <sup>N1</sup> antmicro\_logo



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Sheet: /  
File: ddr5-testboard.sch

**Title: DDR5 Tester**

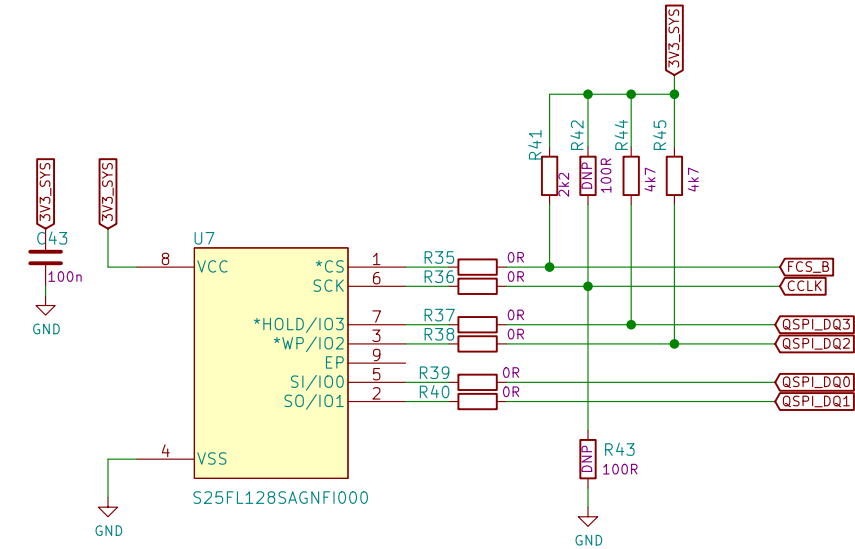
Size: A3      Date: 2022-03-08  
KiCad E.D.A. eeschema 5.1.9+dfsg1-1

**Rev: 1.0.0**  
Id: 1/10

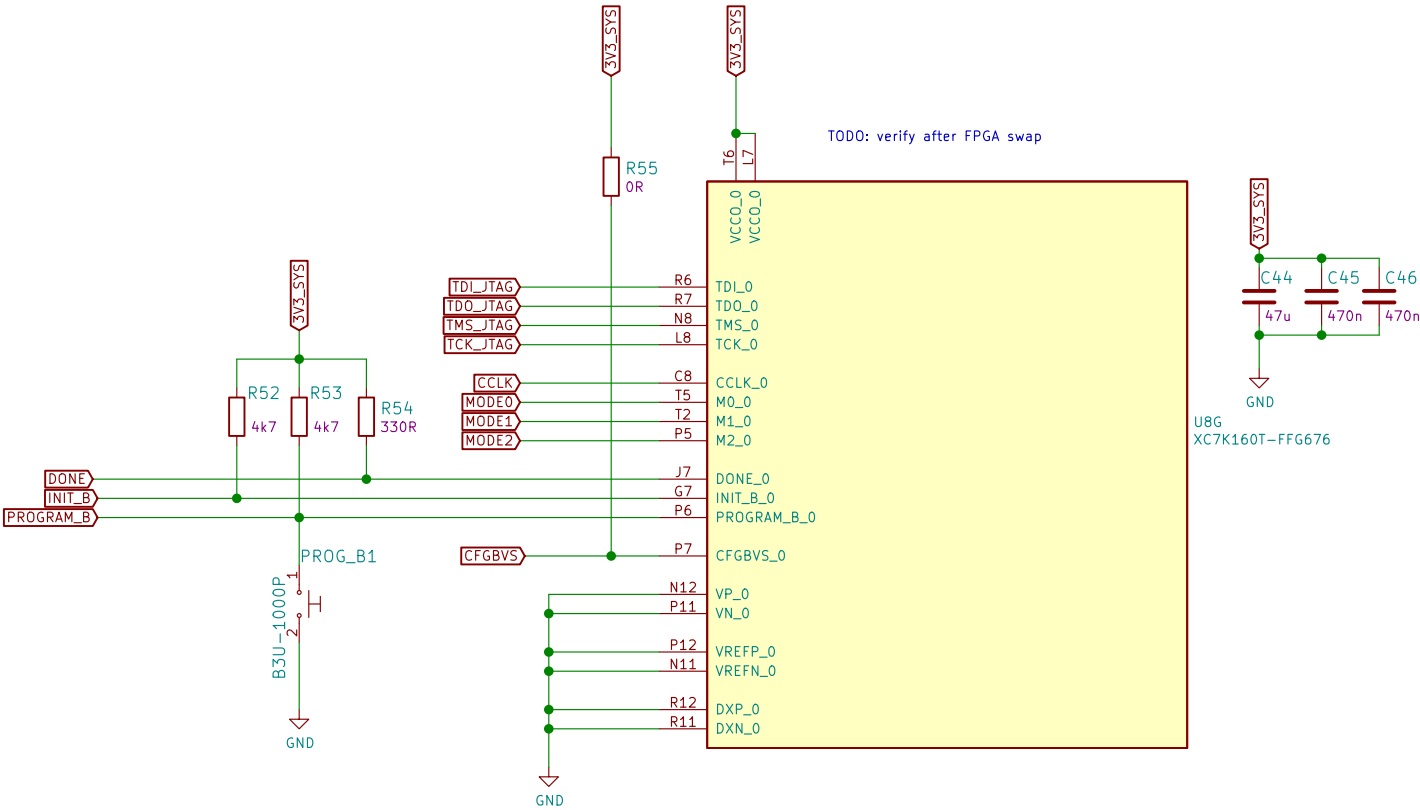
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide  
UG470 (v1.13.1)

(Q)SPI flash

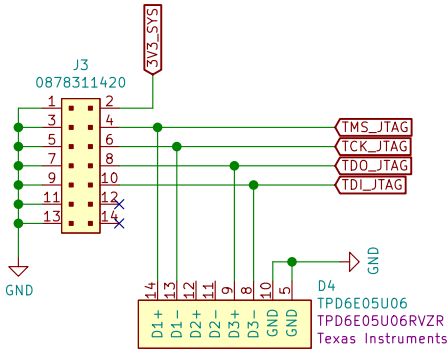


FPGA BANK 0

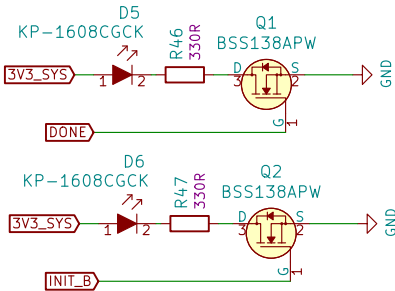


JTAG Connector

Compatible with Xilinx Platform Cable

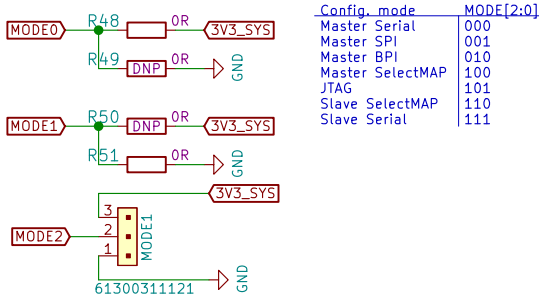


STATUS LEDs

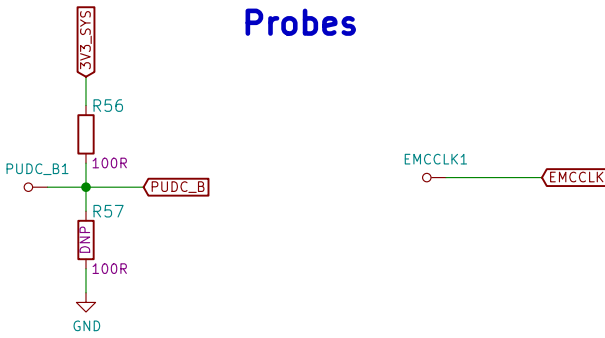


Configuration Modes

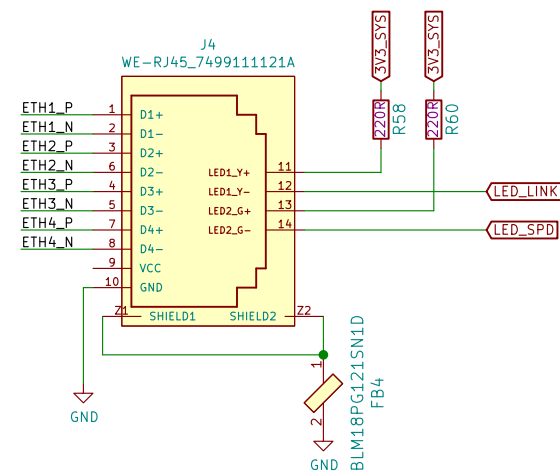
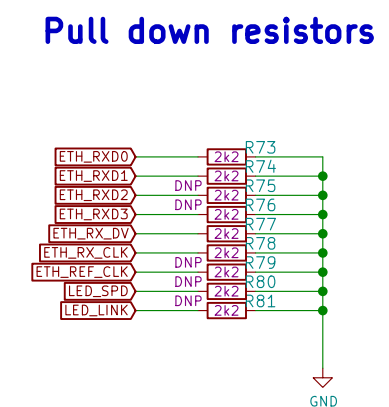
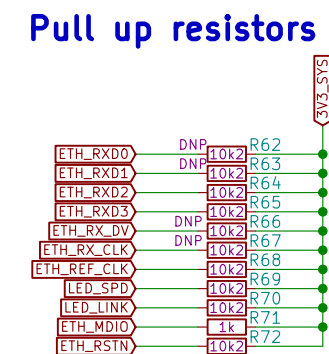
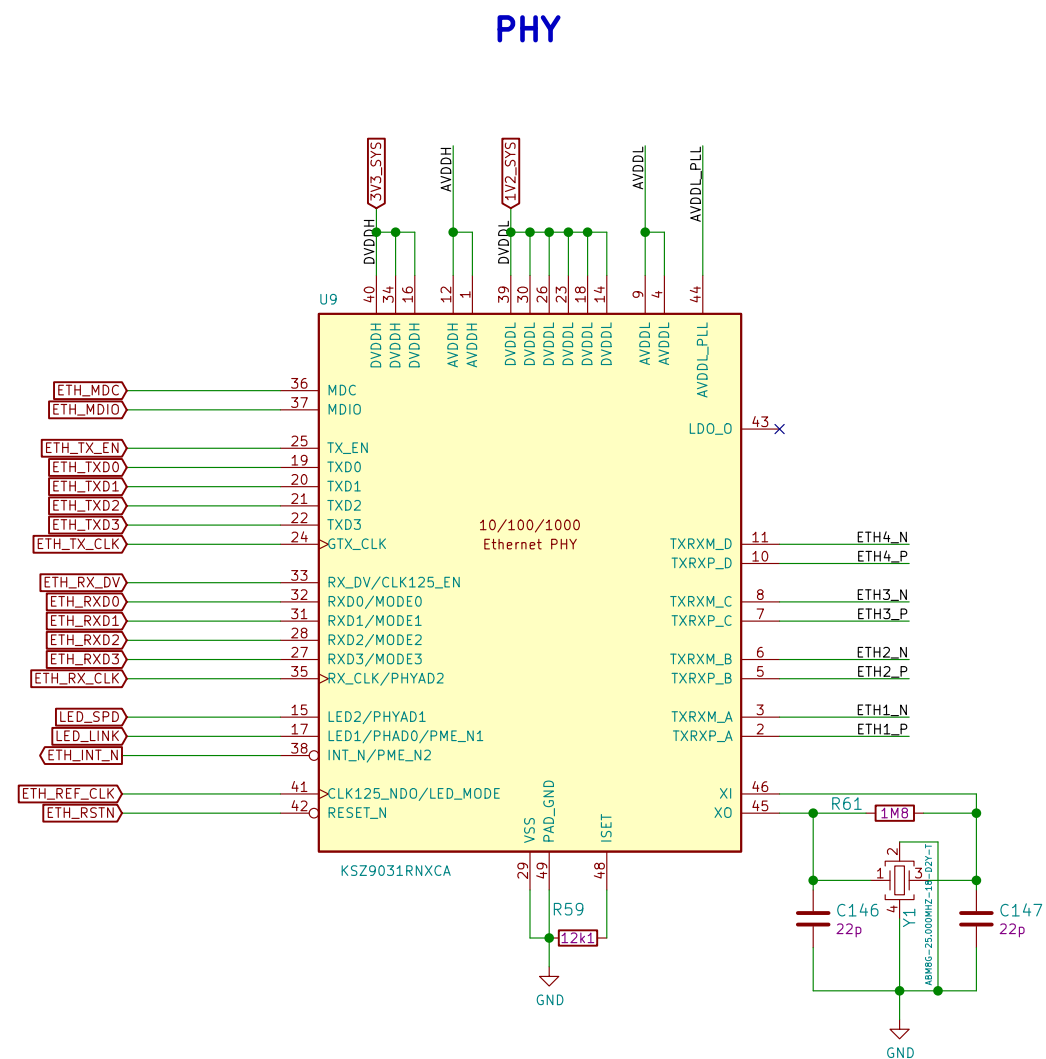
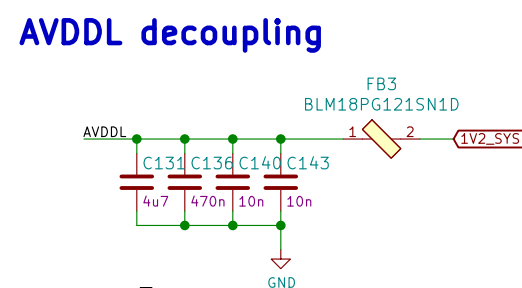
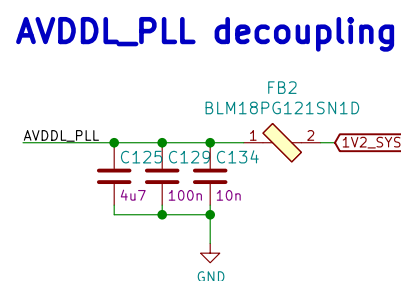
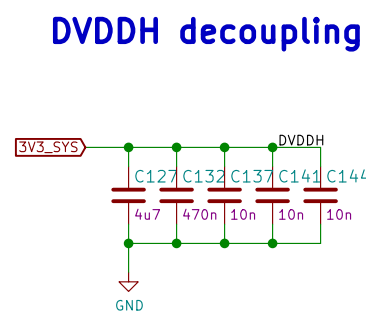
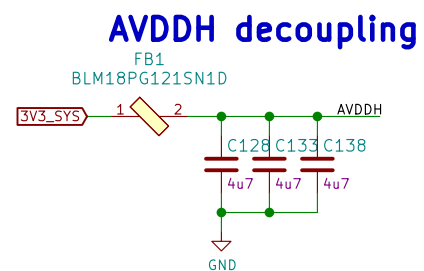
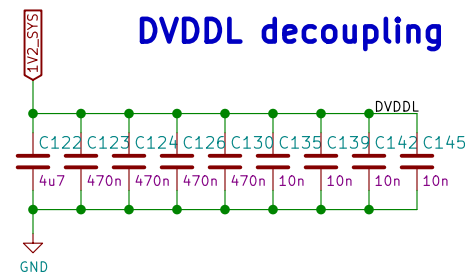
For details, see UG470 p. 21



Probes



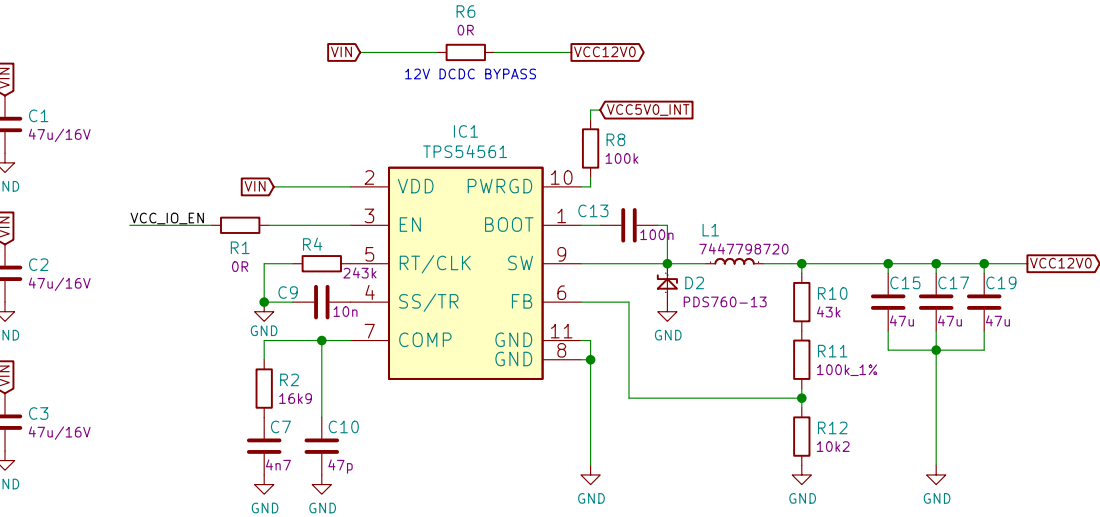




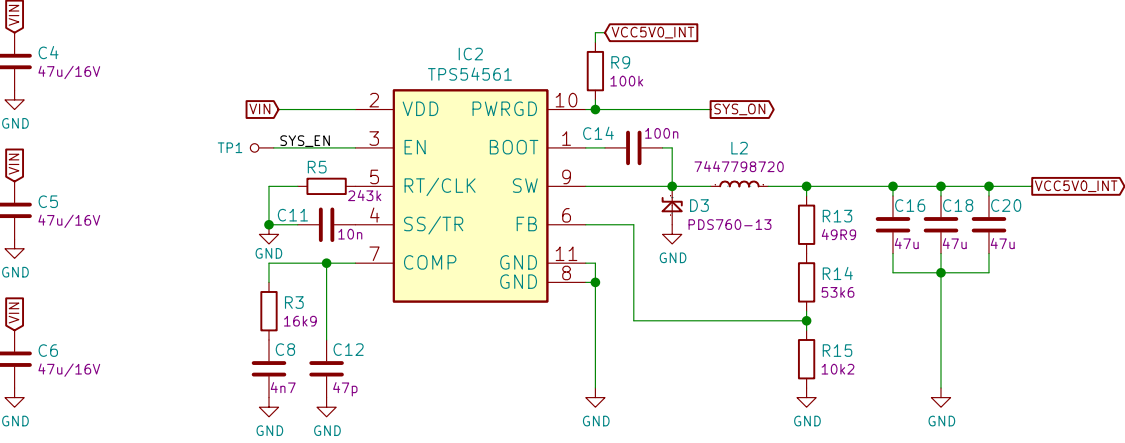
Input power connector



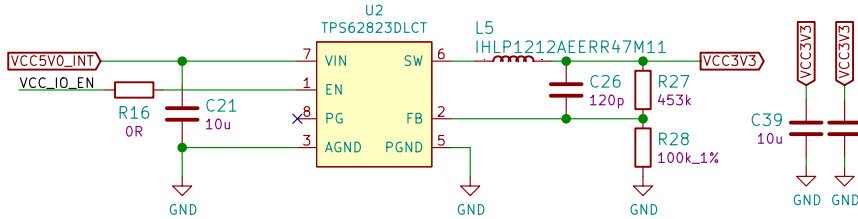
Main supply (12V 5A)



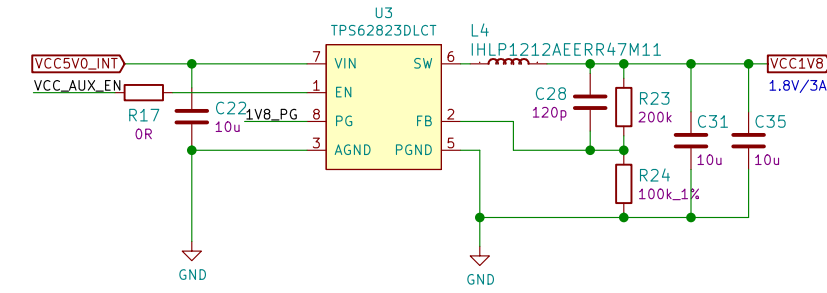
5V0 supply



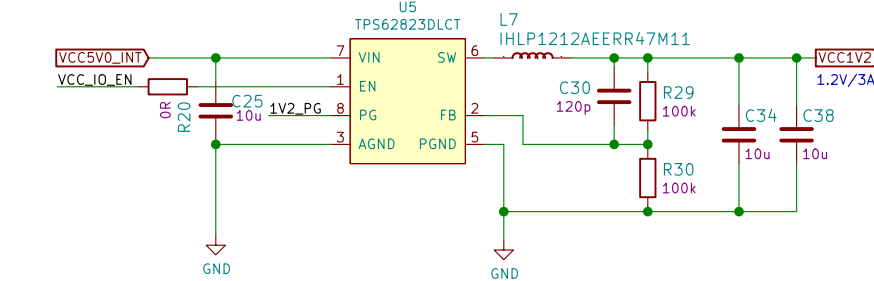
3V3 supply (2A)



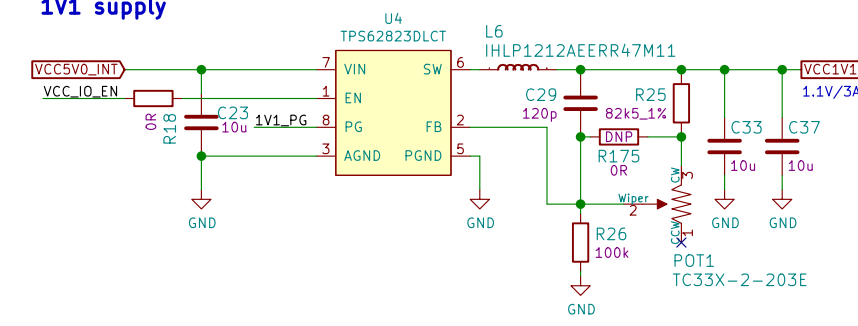
1V8 supply



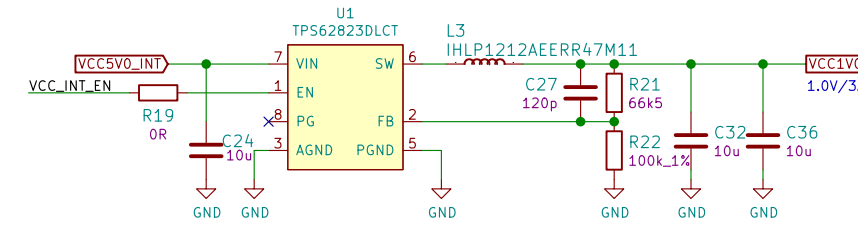
1V2 supply



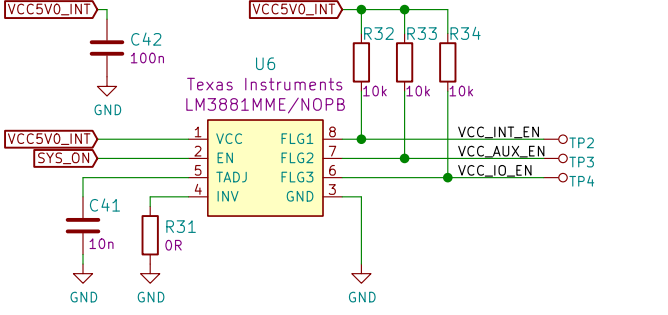
1V1 supply



VCCINT (1.0V 2A)

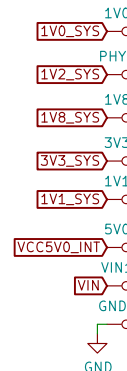


Power sequencer

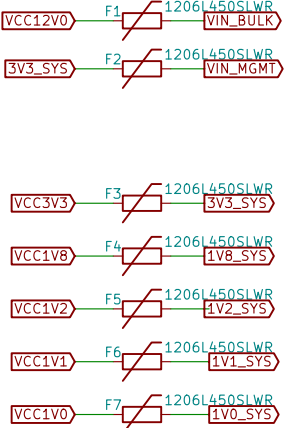


STEP1 - VCCINT (1.0V) for FPGA  
STEP2 - VCCAUX (1.8V, 2.5V, 1.2V) for FPGA and DDR  
STEP3 - VCCIO (3.3V, 1.2V, 0.6V) for FPGA, PHY and DDR

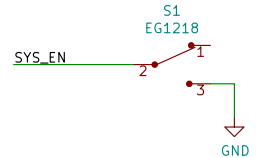
Probes



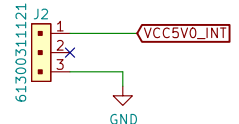
Fuses



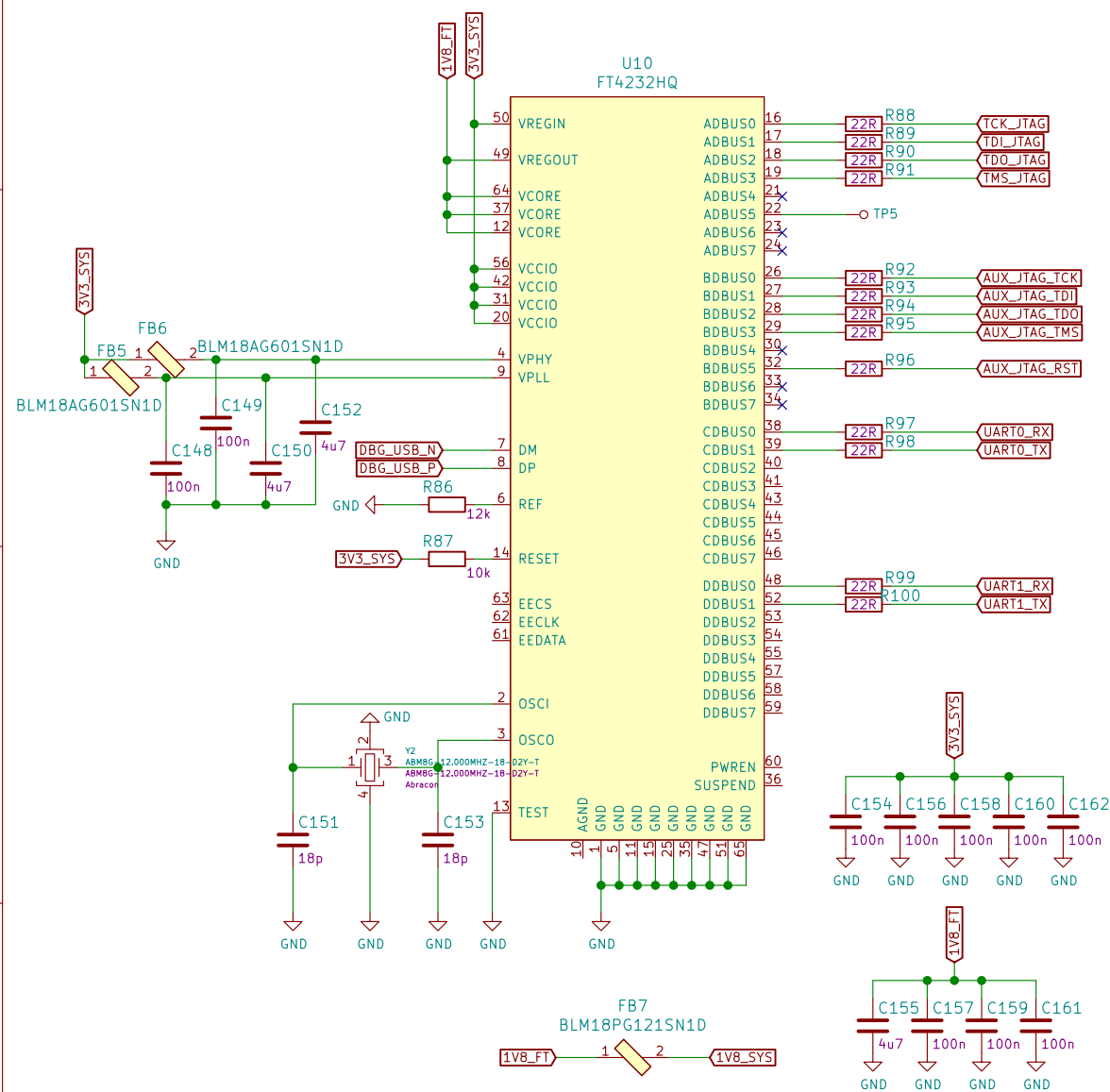
Power switch



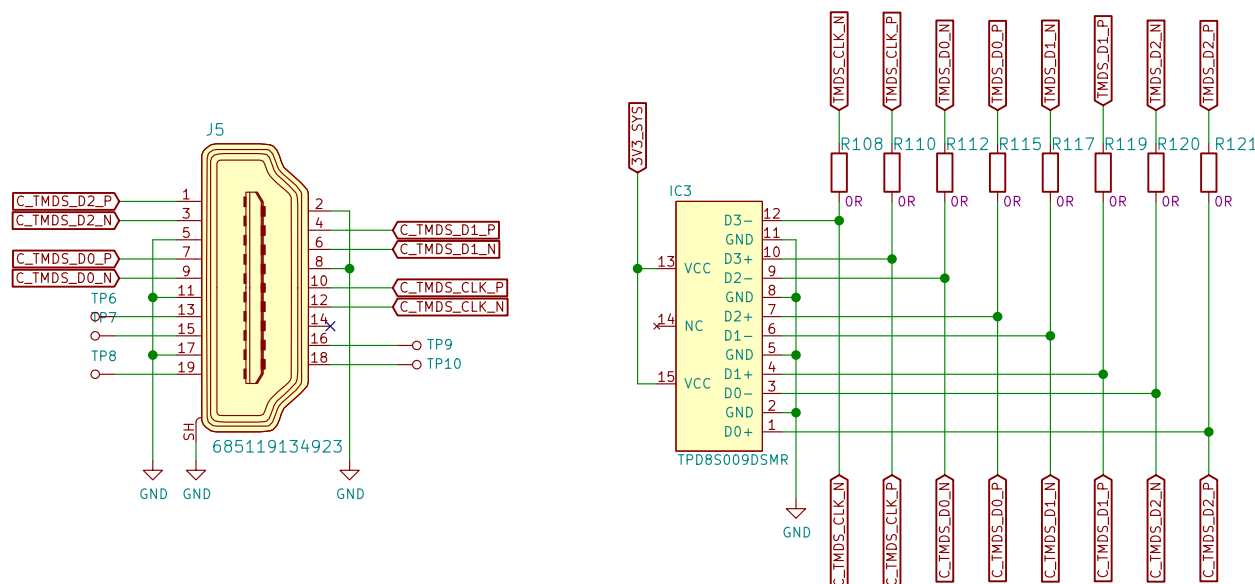
Optional FAN connector



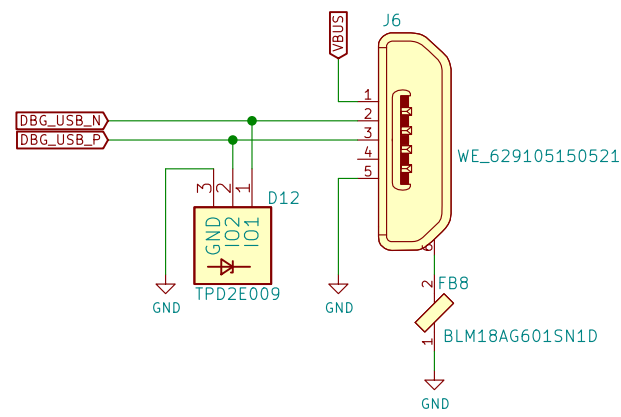
## Debug UART



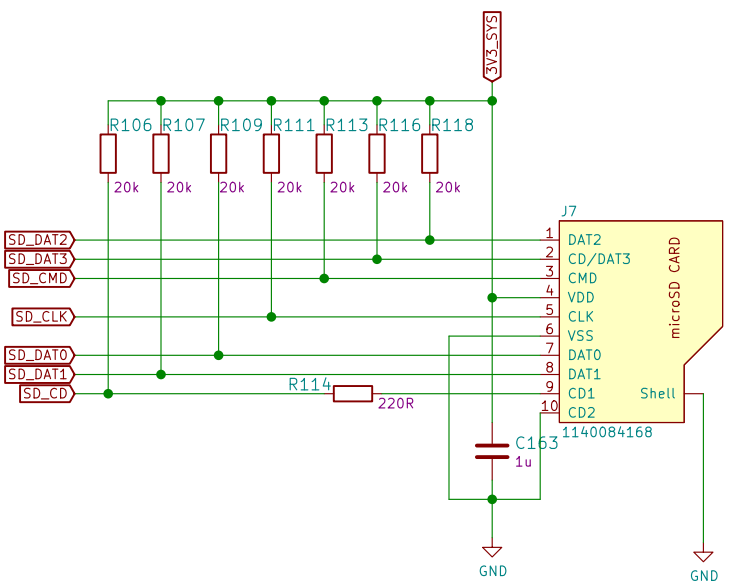
## HDMI



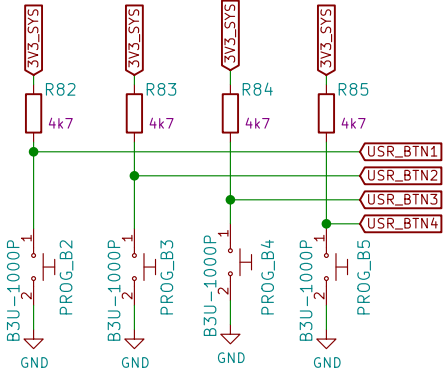
## Debug USB



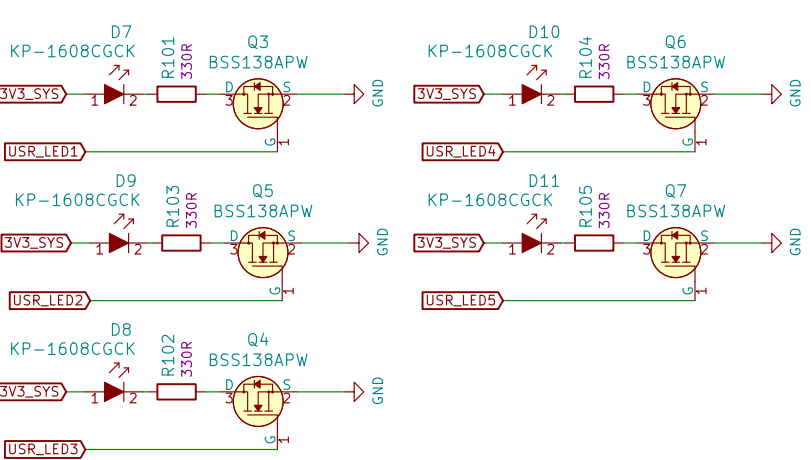
## SD card

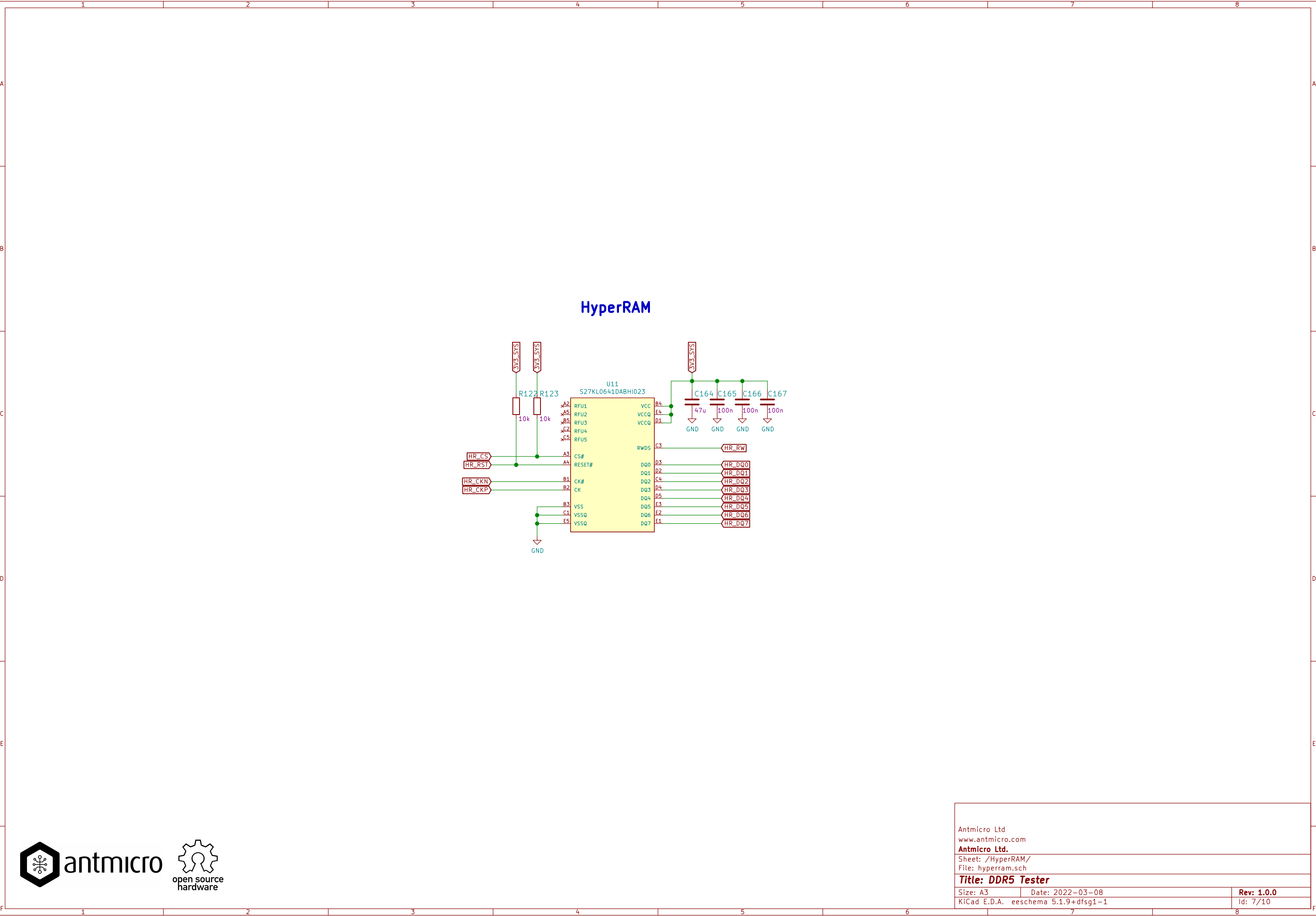


## User buttons



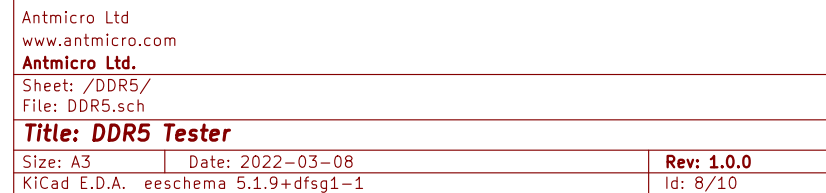
## User LEDs







U12A										U12B									
DDR504111002KQ										DDR504111002KQ									
VIN_BULK	1	VIN_BULK	45	VIN_BULK	76	CA0_B	220	RFU	220	VIN_BULK	46	VIN_BULK	77	VSS	221	CA1_B	221		
VIN_MGMT	2	RFU	46	VIN_BULK	78	VSS	222	CA1_B	222	VIN_MGMT	47	PCAMP	79	CA2_B	223	VSS	223		
HSC_L	3	VIN_MGMT	48	PCAMP	80	CA4_B	224	CA3_B	224	HSDA	4	RFU	81	VSS	225	CA5_B	225		
HSDA	5	HSC_L	49	RFU	82	CA6_B	226	VSS	226	DQ0_A	6	VSS	83	PAR_B	227	PAR_B	227		
DQ0_A	7	DQ0_A	50	DQ2_A	84	CS0_B_N	228	VSS	228	DQ1_A	8	DQ2_A	85	CS1_B_N	229	CS1_B_N	229		
DQ1_A	9	DQ1_A	51	DQ3_A	86	DLBDQ	230	DLBDQ	230	DQ2_A	10	DQ3_A	87	DLBDQ	231	DLBDQ	231		
DQ50_A_P	11	DQ50_A_t	52	DQ55_A_N	88	DLBDQ	232	DLBDQ	232	DQ50_A_N	12	DQ55_A_N	89	CB4_B	233	CB4_B	233		
DQ50_A_N	13	DQ50_A_c	53	DQ55_A_P	90	CB5_B	234	CB5_B	234	DQ4_A	14	DQ55_A_P	91	CB6_B	235	CB6_B	235		
DQ4_A	15	DQ4_A	54	DQ6_A	92	DQ9_B_P	236	DQ9_B_t/DQ95_B_t	236	DQ5_A	16	DQ4_A	93	DQ9_B_c/DQ95_B_c	237	DQ54_B_N	237		
DQ5_A	17	VSS	55	DQ6_A	94	DQ9_B_N	238	DQ95_B_t/DQ95_B_c	238	DQ8_A	18	DQ5_A	95	DQ95_B_t	239	DQ54_B_P	239		
DQ8_A	19	DQ8_A	56	DQ7_A	96	CB0_B	240	CB0_B	240	DQ9_A	20	DQ8_A	97	CB1_B	241	CB2_B	241		
DQ9_A	21	VSS	57	DQ7_A	98	CB1_B	242	CB1_B	242	DQ51_A_P	22	DQ9_A	99	CB3_B	243	CB3_B	243		
DQ51_A_P	23	DQ51_A_t	58	DQ10_A	100	DQ0_B	244	DQ0_B	244	DQ51_A_N	24	DQ51_A_t	101	DQ2_B	245	DQ2_B	245		
DQ51_A_N	25	DQ51_A_c	59	DQ10_A	102	DQ1_B	246	DQ1_B	246	DQ12_A	26	DQ51_A_c	103	DQ3_B	247	DQ3_B	247		
DQ12_A	27	DQ12_A	60	DQ11_A	104	DQ50_B_P	248	DQ50_B_t	248	DQ13_A	28	DQ12_A	105	DQ50_B_c	249	DQ55_B_N	249		
DQ16_A	29	DQ16_A	61	DQ11_A	106	DQ50_B_N	250	DQ50_B_c	250	DQ17_A	30	DQ13_A	107	DQ55_B_t/DQ55_B_c	251	DQ55_B_P	251		
DQ17_A	31	VSS	62	DQ12_A	108	DQ4_B	252	DQ4_B	252	DQ52_A_P	32	DQ16_A	109	DQ5_B	253	DQ6_B	253		
DQ52_A_P	33	DQ52_A_t	63	DQ13_A	110	DQ5_B	254	DQ5_B	254	DQ52_A_N	34	DQ17_A	111	DQ7_B	255	DQ7_B	255		
DQ52_A_N	35	DQ52_A_c	64	DQ14_A	112	DQ8_B	256	DQ8_B	256	DQ20_A	36	DQ52_A_c	113	DQ9_B	257	DQ10_B	257		
DQ20_A	37	DQ20_A	65	DQ15_A	114	DQ9_B	258	DQ9_B	258	DQ21_A	38	DQ20_A	115	DQ11_B	259	DQ11_B	259		
DQ21_A	39	DQ21_A	66	DQ16_A	116	DQ51_B_P	260	DQ51_B_t	260	DQ24_A	40	DQ21_A	117	DQ51_B_c	261	DQ56_B_N	261		
DQ24_A	41	VSS	67	DQ17_A	118	DQ51_B_N	262	DQ51_B_c	262	DQ25_A	42	DQ24_A	119	DQ56_B_t/DQ56_B_c	263	DQ56_B_P	263		
DQ25_A	43	DQ25_A	68	DQ18_A	120	DQ12_B	264	DQ12_B	264	DQ53_A_P	44	DQ25_A	121	DQ13_B	265	DQ13_B	265		
DQ53_A_P	45	DQ53_A_t	69	DQ19_A	122	DQ16_B	266	DQ16_B	266	DQ53_A_N	46	DQ53_A_t	123	DQ17_B	267	DQ17_B	267		
DQ53_A_N	47	DQ53_A_c	70	DQ20_A	124	DQ17_B	268	DQ17_B	268	DQ28_A	48	DQ53_A_c	125	DQ19_B	269	DQ19_B	269		
DQ28_A	49	DQ28_A	71	DQ21_A	126	DQ52_B_P	270	DQ52_B_t	270	DQ29_A	50	DQ28_A							



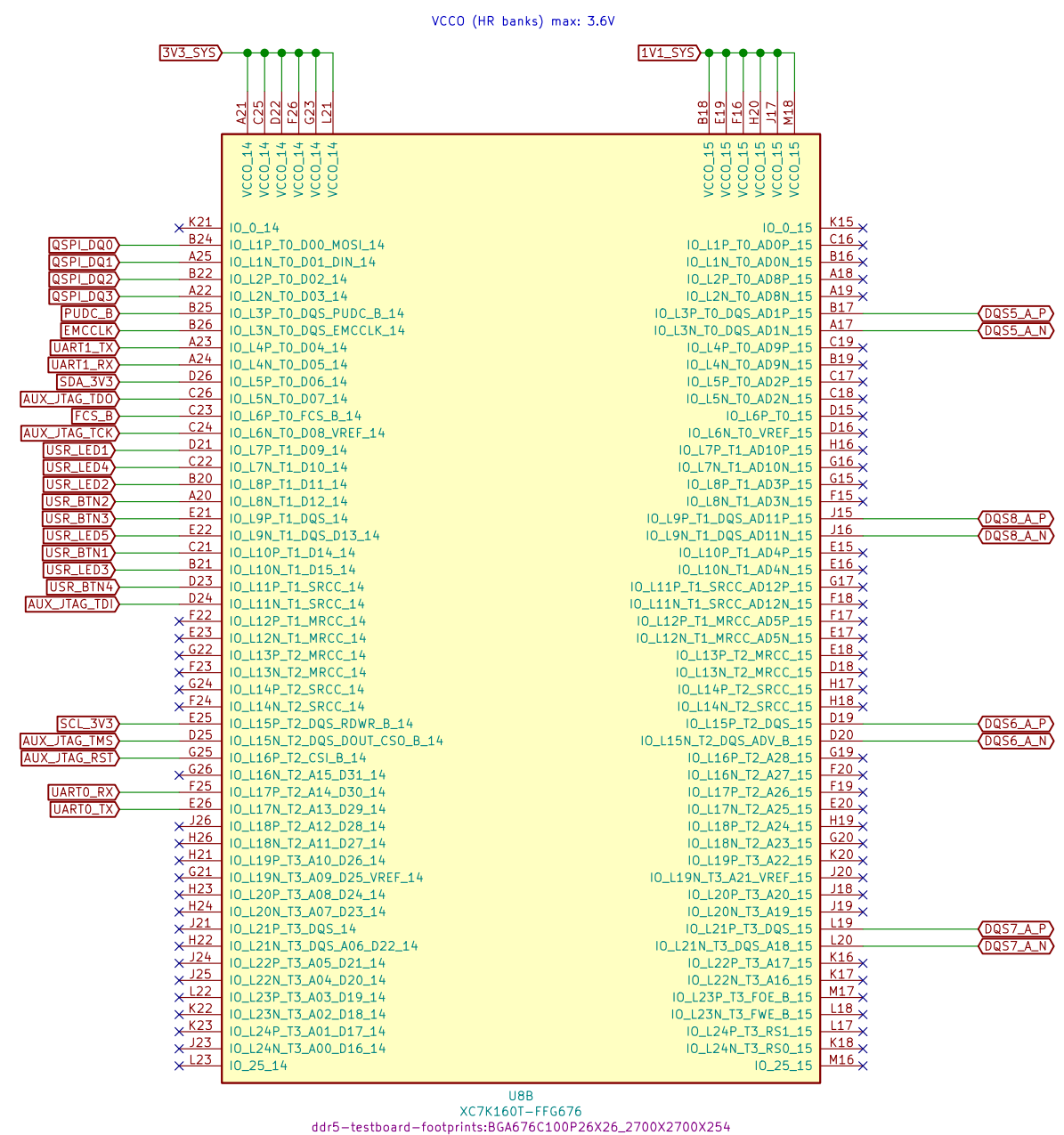
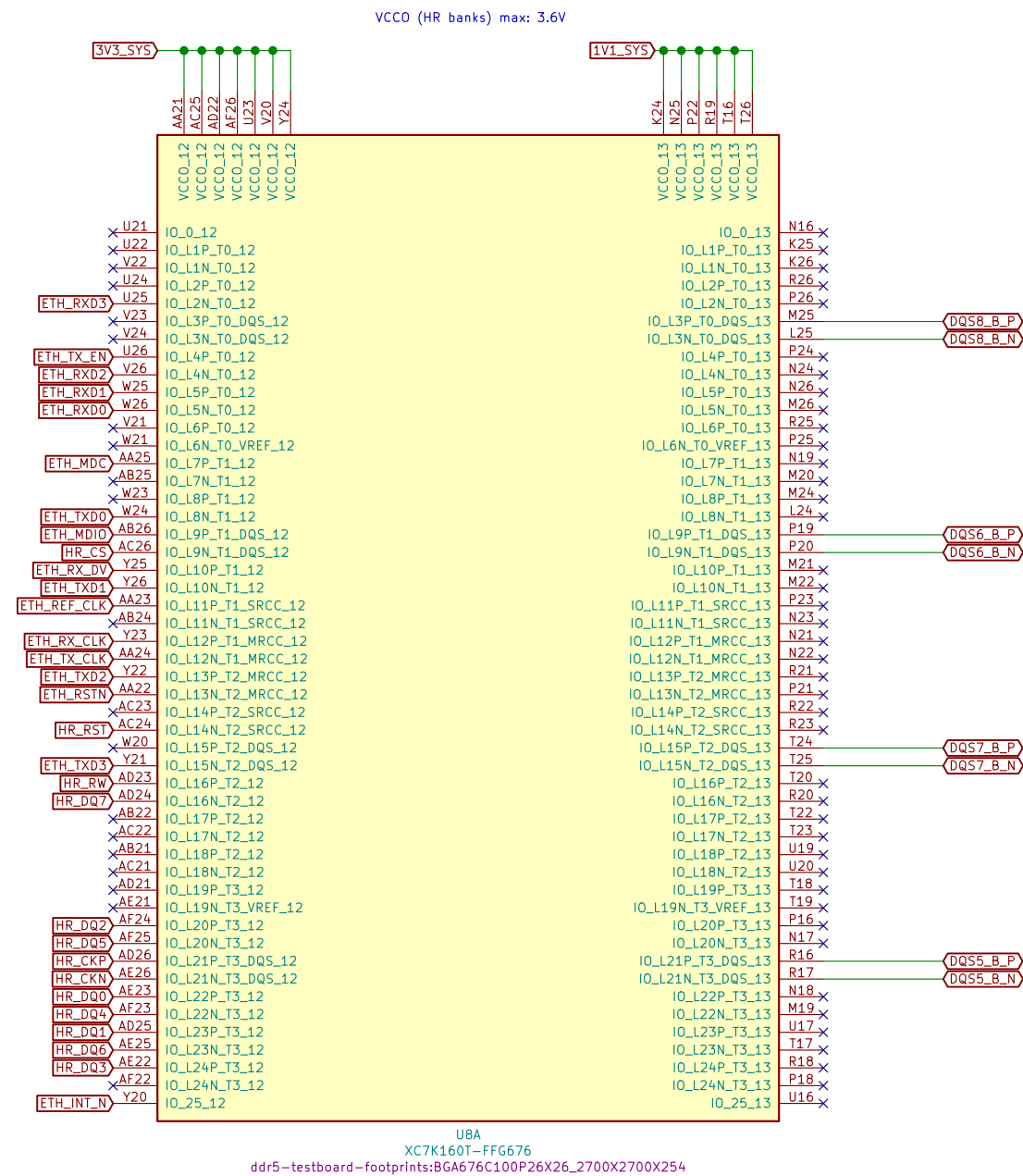


## BANK 12

## BANK 13

## BANK 14

## BANK 15

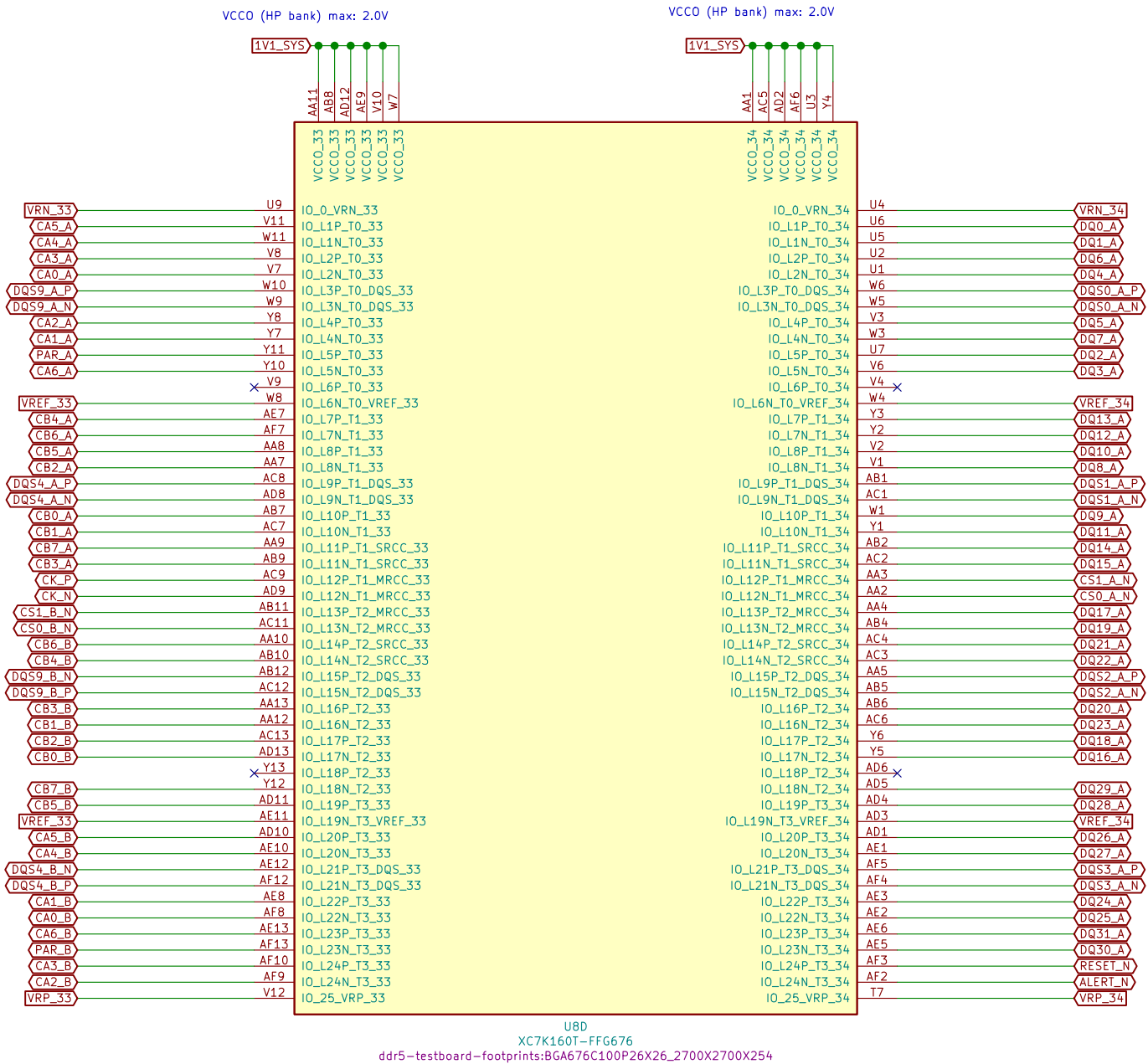
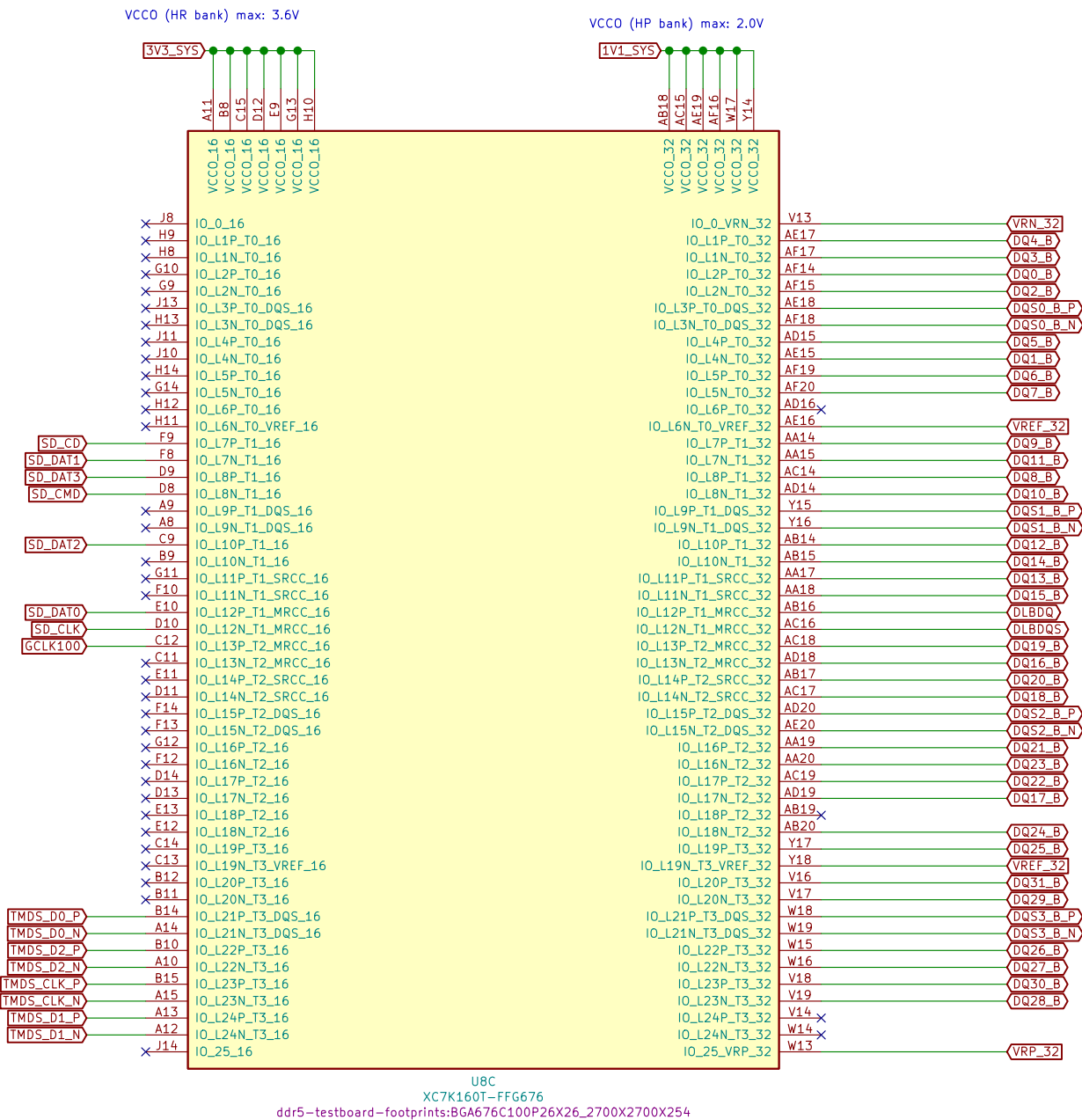


## BANK 16

## BANK 32

## BANK 33

## BANK 34



## Clock source

## VREF

## I2C/I3C logic translator

