DDR5 Tester

Sheet: HyperRAM
File: hyperram.sch

Sheet: DDR5
File: DDR5.sch

Sheet: Interfaces
File: interfaces.sch

Sheet: Ethernet
File: ethernet.sch

Sheet: Supply
File: supply.sch

Sheet: Config SPI flash
File: config-spi.sch

Sheet: FPGA power
File: fpga-power.sch

Sheet: FPGA banks 12-15
File: fpga-banks-12-15.sch

Sheet: FPGA banks 16-34
File: fpga-banks-16-34.sch

Logo N2 oshw_logo

Logo N1 antmicro_logo

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Sheet: /
File: ddr5-testboard.sch

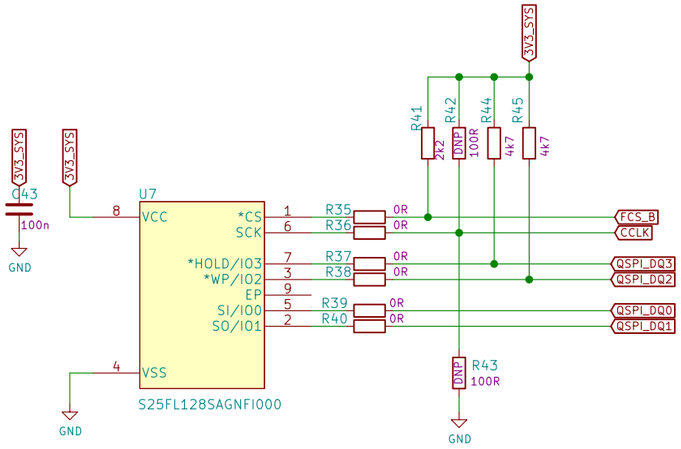
Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 1/10

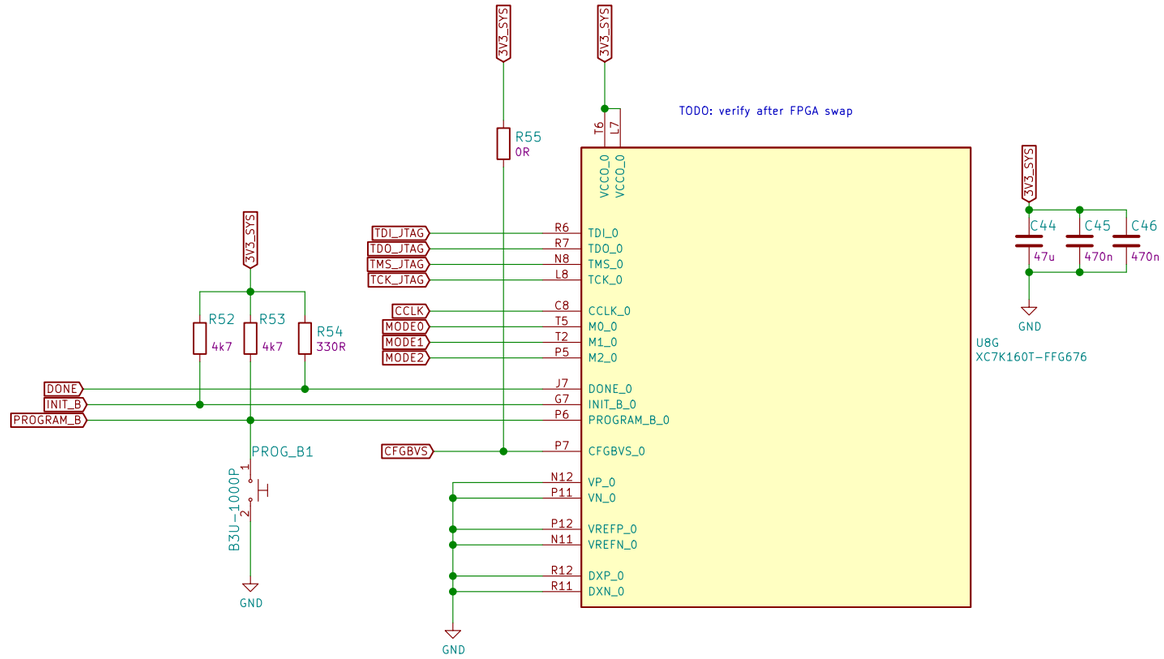
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

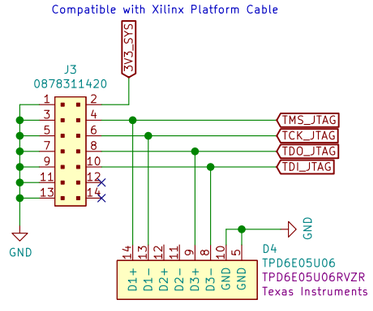


FPGA BANK 0

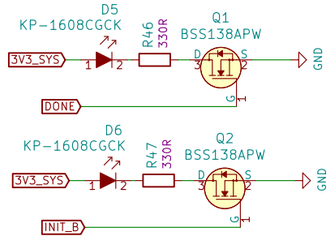


JTAG Connector

Compatible with Xilinx Platform Cable

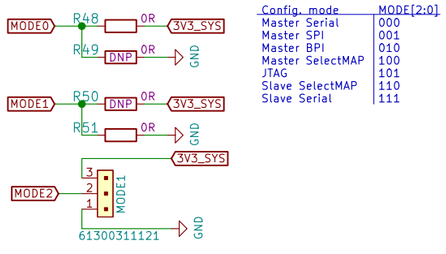


STATUS LEDs



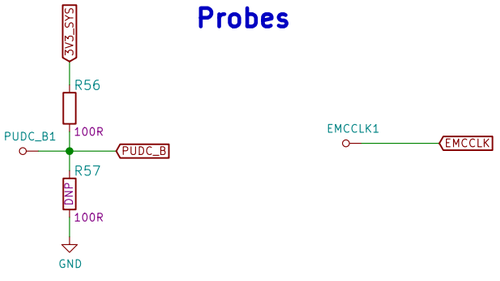
Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Probes



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Sheet: /Config SPI flash/
File: config–spi.sch

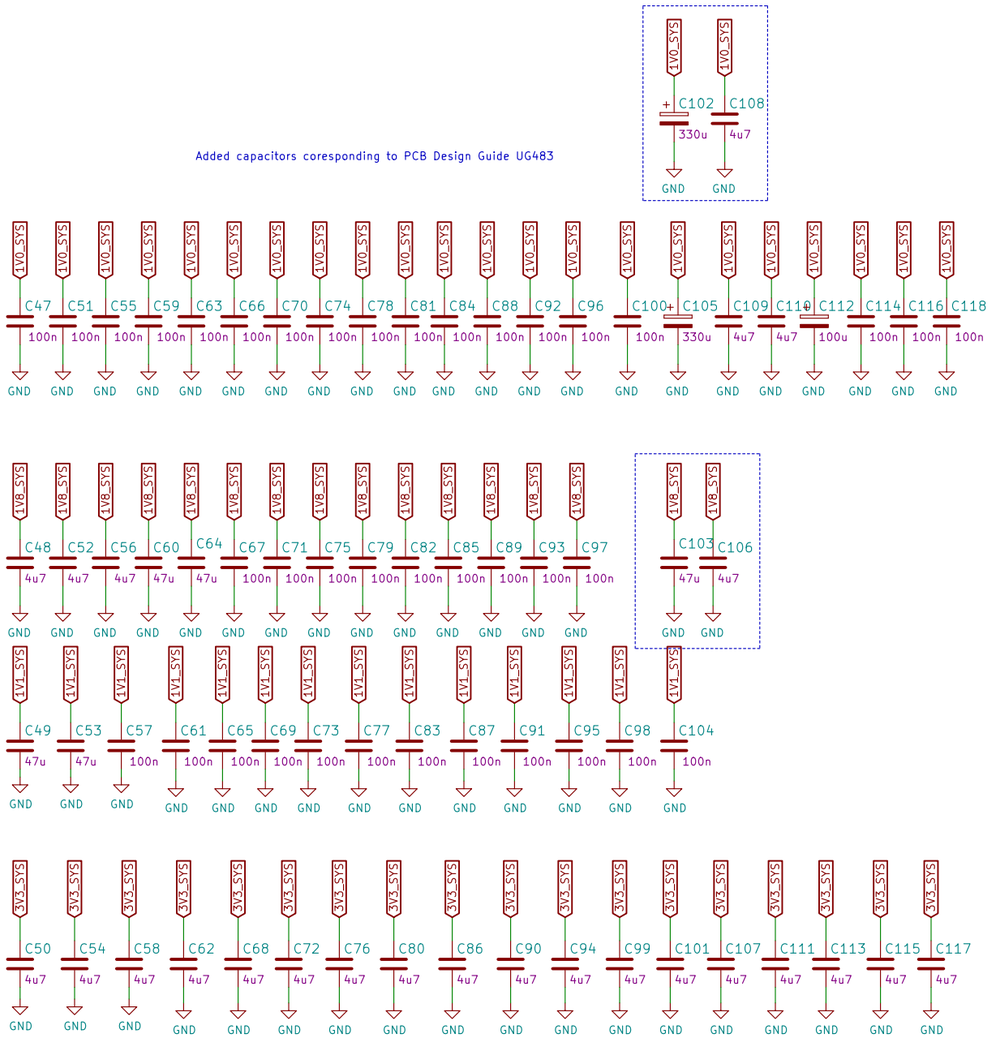
Title: DDR5 Tester

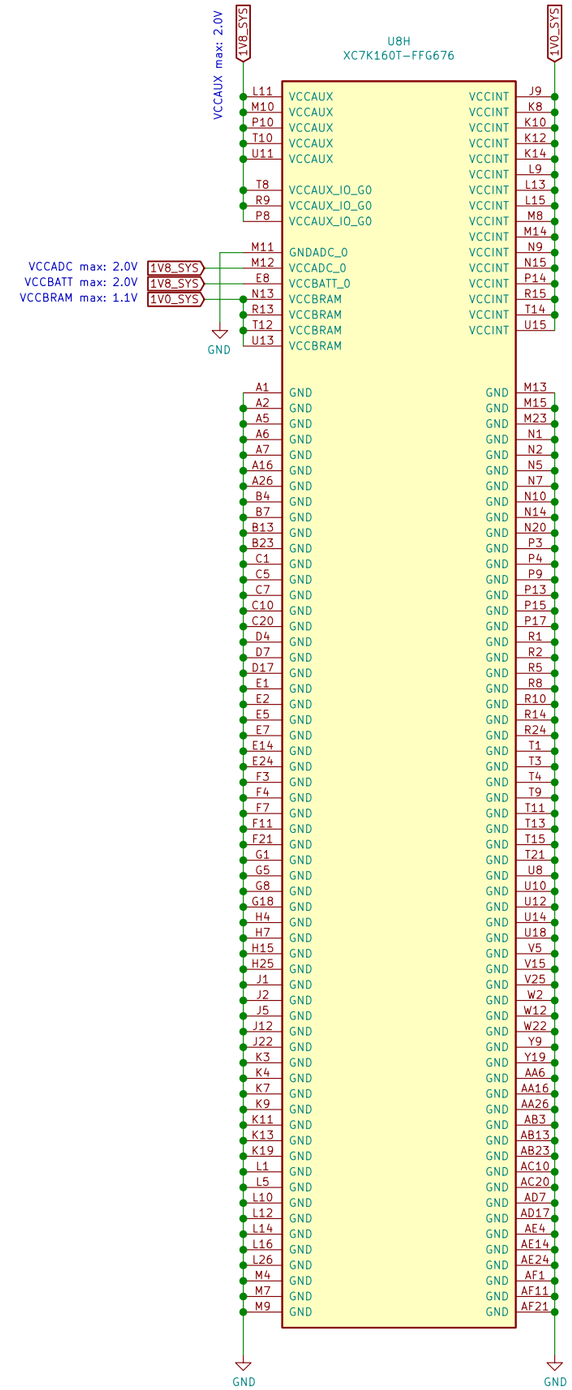
Size: A3	Date: 2022–03–08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1–1	Id: 2/10

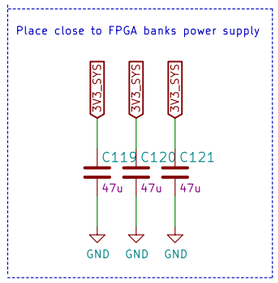
POWER RAILS

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!

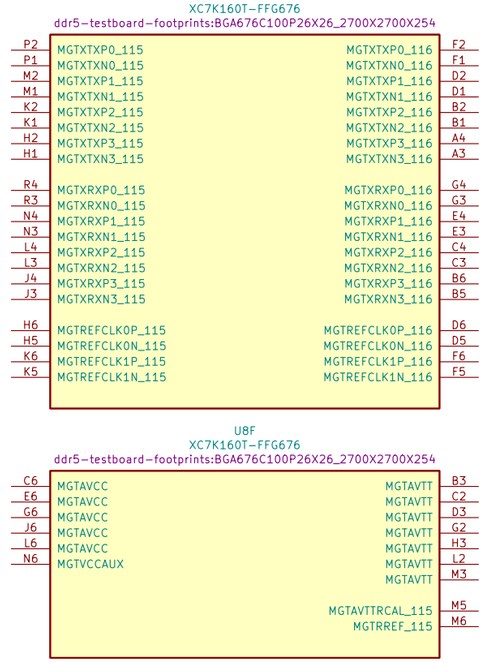
Added capacitors coresponding to PCB Design Guide UG483







UNUSED



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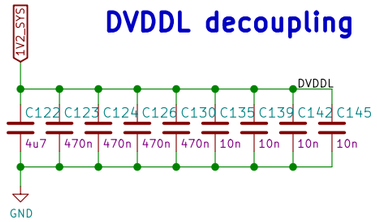
Sheet: /FPGA power/
File: fpga-power.sch

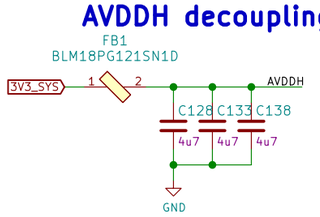
Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 3/10

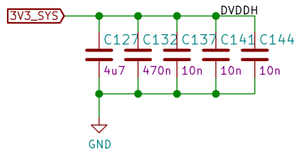
DVDDL decoupling



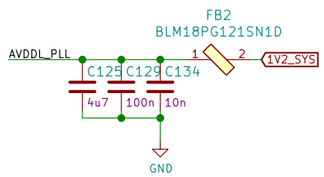
AVDDH decoupling



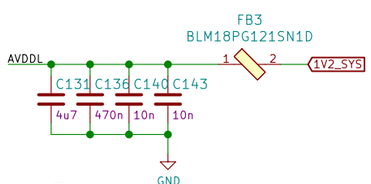
DVDDH decoupling



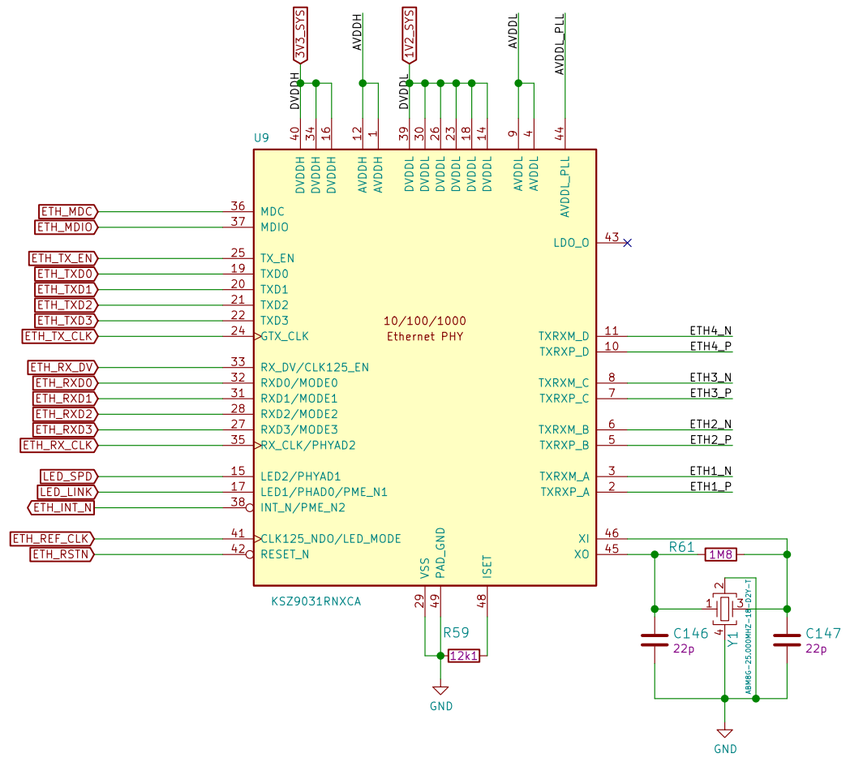
AVDDL_PLL decoupling



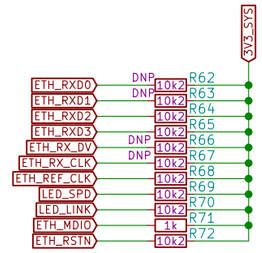
AVDDL decoupling



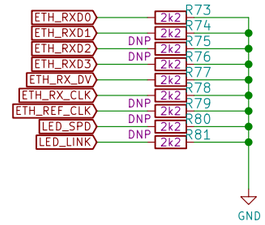
PHY



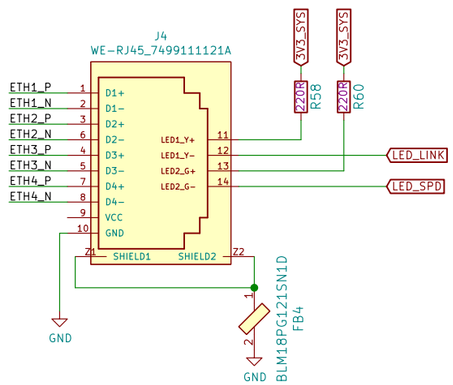
Pull up resistors



Pull down resistors



RJ45 Connector



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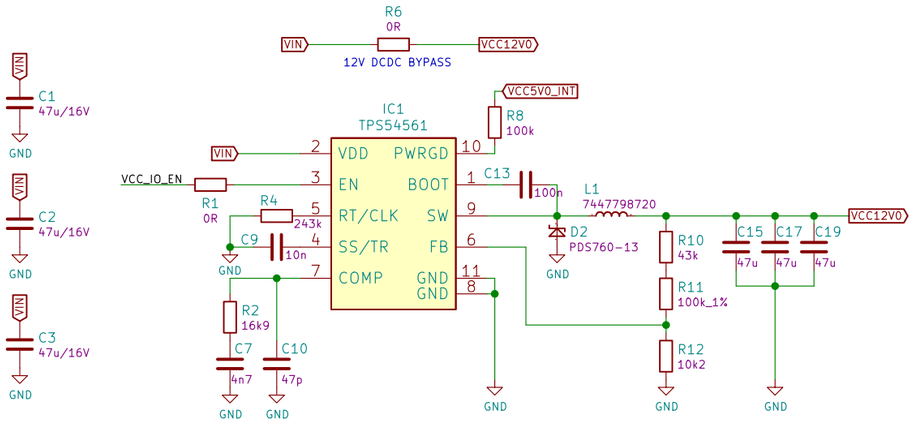
Sheet: /Ethernet/
File: ethernet.sch

Title: DDR5 Tester

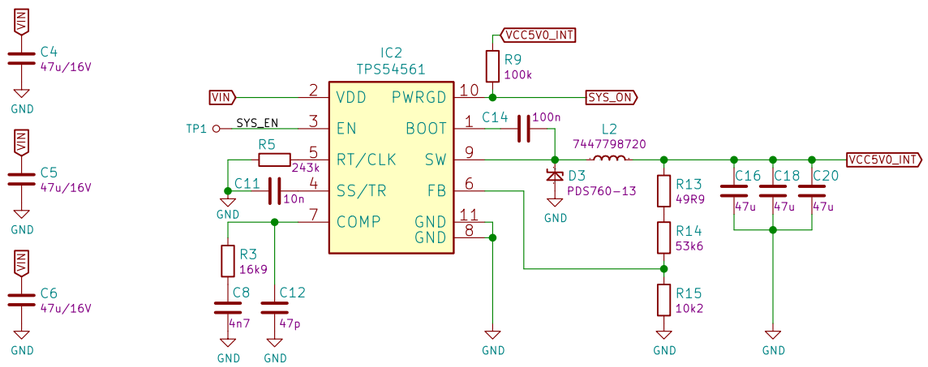
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 4/10

Input power connector

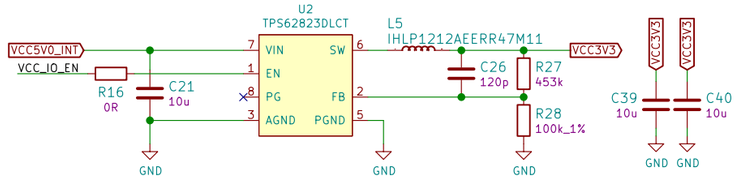
Main supply (12V 5A)



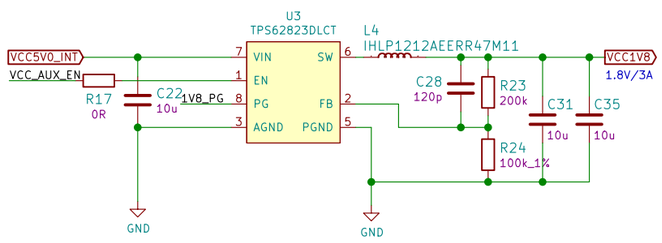
5V0 supply



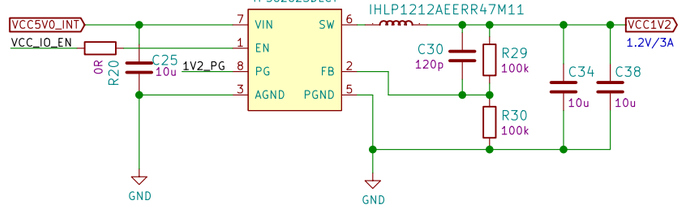
3V3 supply (2A)



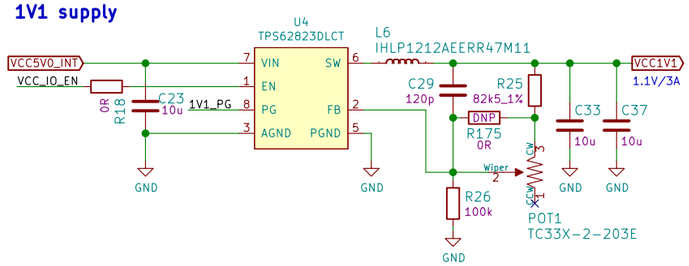
1V8 supply



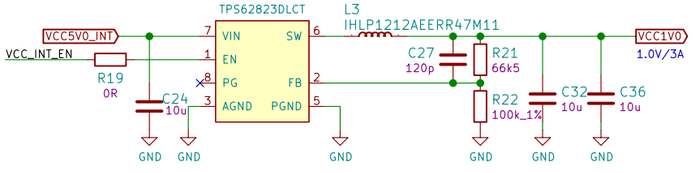
1V2 supply



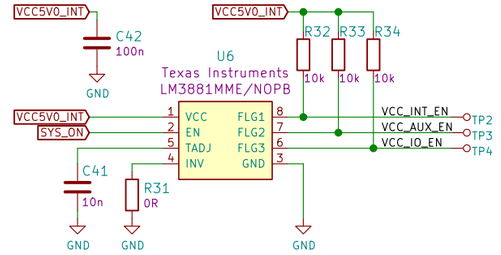
1V1 supply



VCCINT (1.0V 2A)

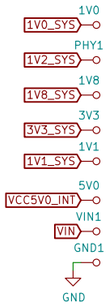


Power sequencer

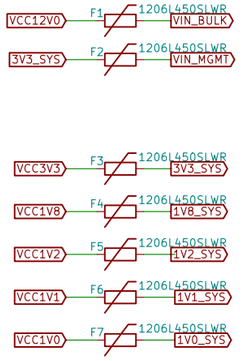


STEP1 – VCCINT (1.0V) for FPGA
STEP2 – VCCAUX (1.8V, 2.5V, 1.2V) for FPGA and DDR
STEP3 – VCCIO (3.3V, 1.2V, 0.6V) for FPGA, PHY and DDR

Probes

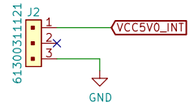


Fuses



Power switch

Optional FAN connector



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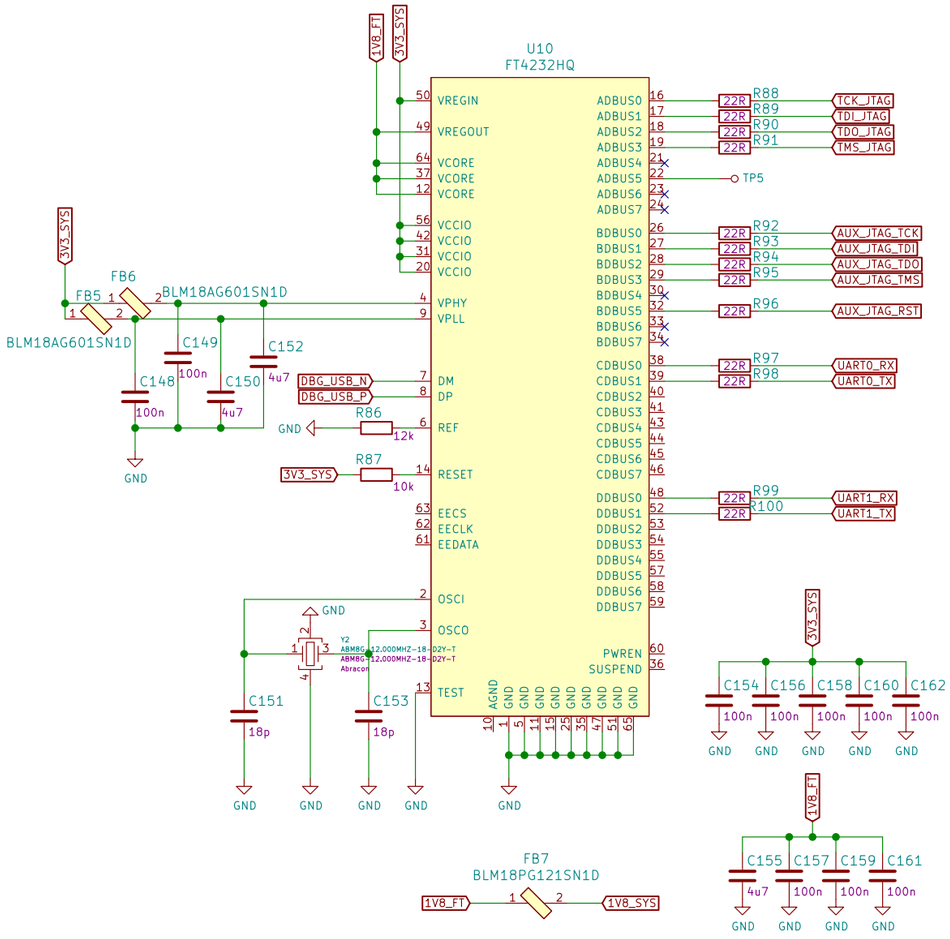
Sheet: /Supply/
File: supply.sch

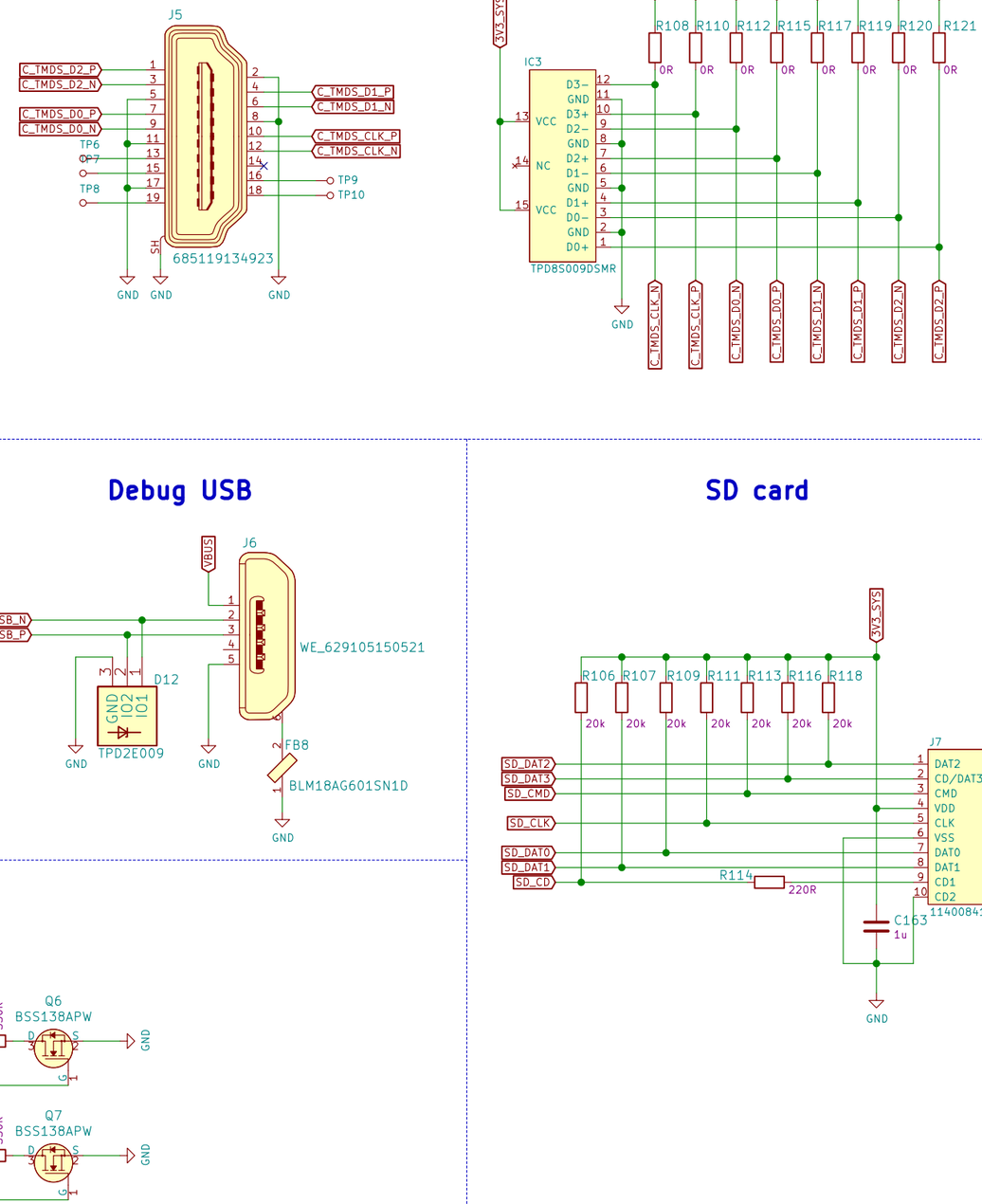
Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A. eeschema 5.1.9+dfsg1-1		Id: 5/10

Debug UART



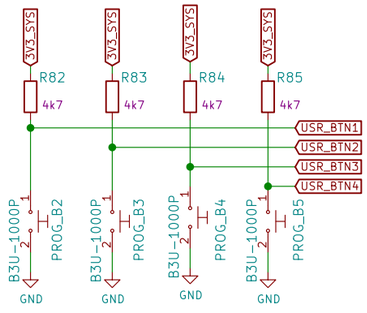
HDMI



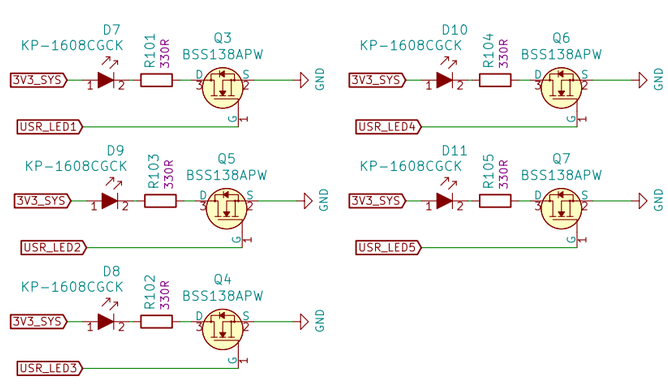
Debug USB

SD card

User buttons



User LEDs



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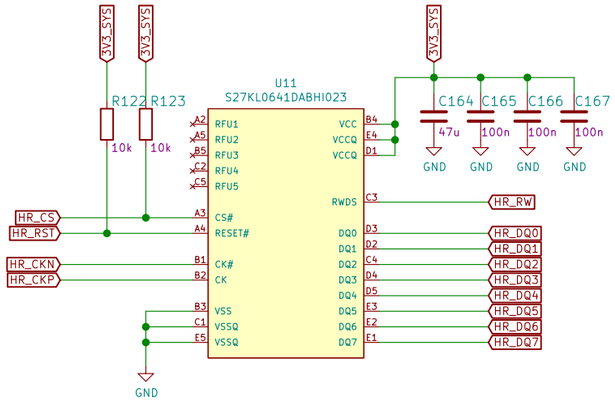
Sheet: /Interfaces/
File: interfaces.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 6/10

HyperRAM



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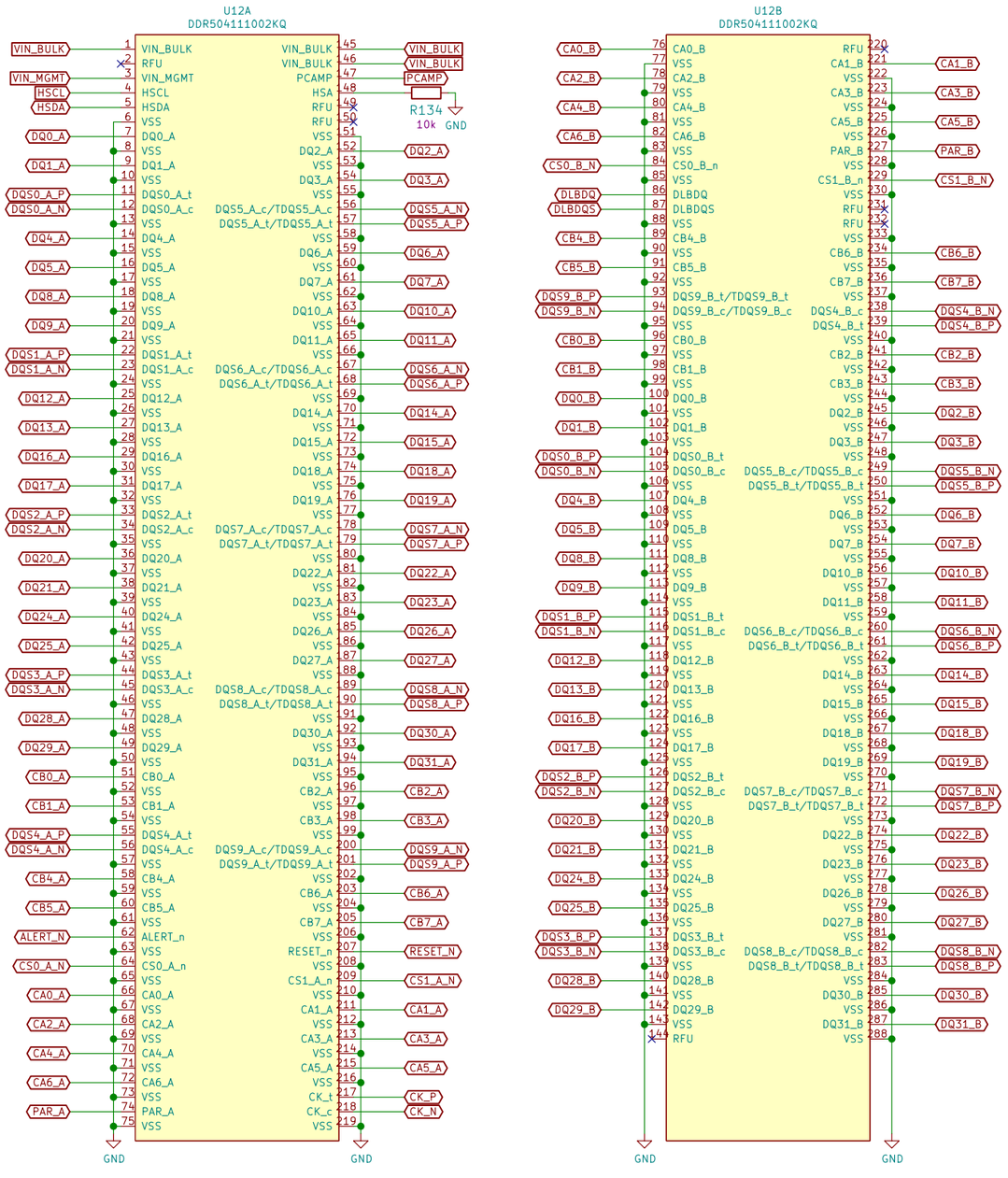
Sheet: /HyperRAM/
File: hyperram.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 7/10

DDR5 RDIMM connector



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Sheet: /DDR5/
File: DDR5.sch

Title: DDR5 Tester

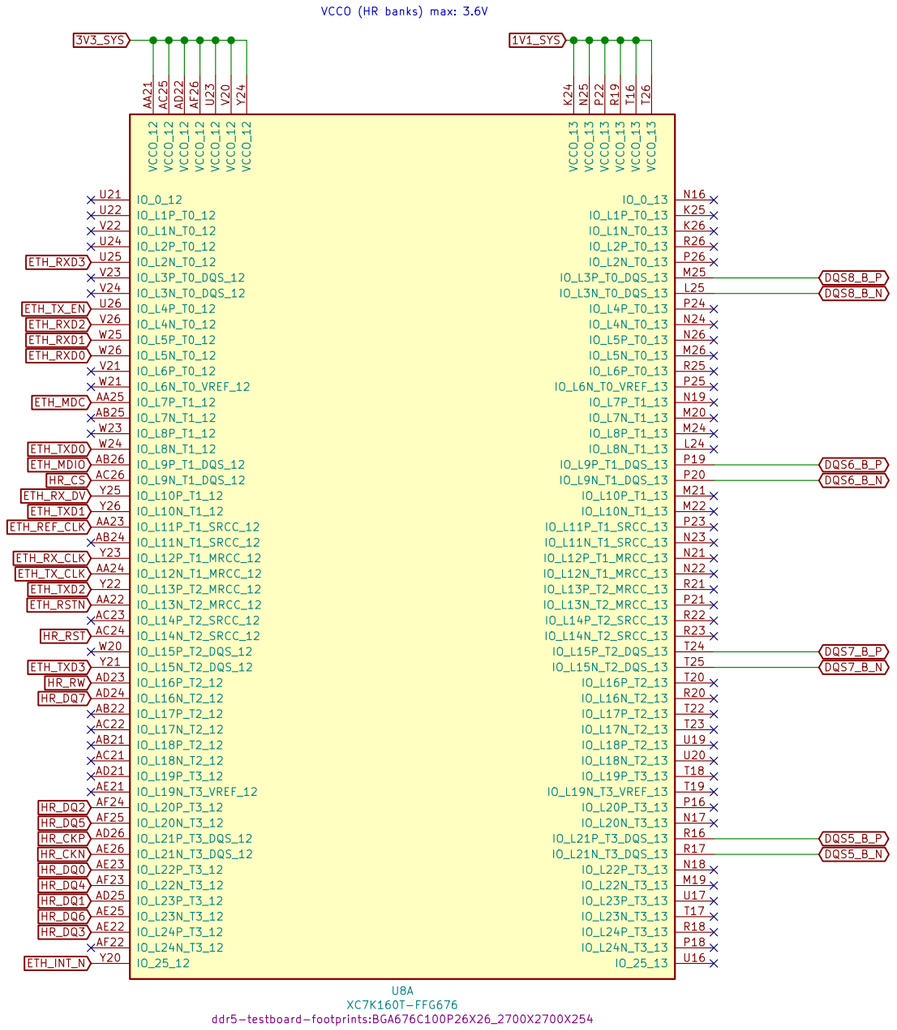
Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 8/10

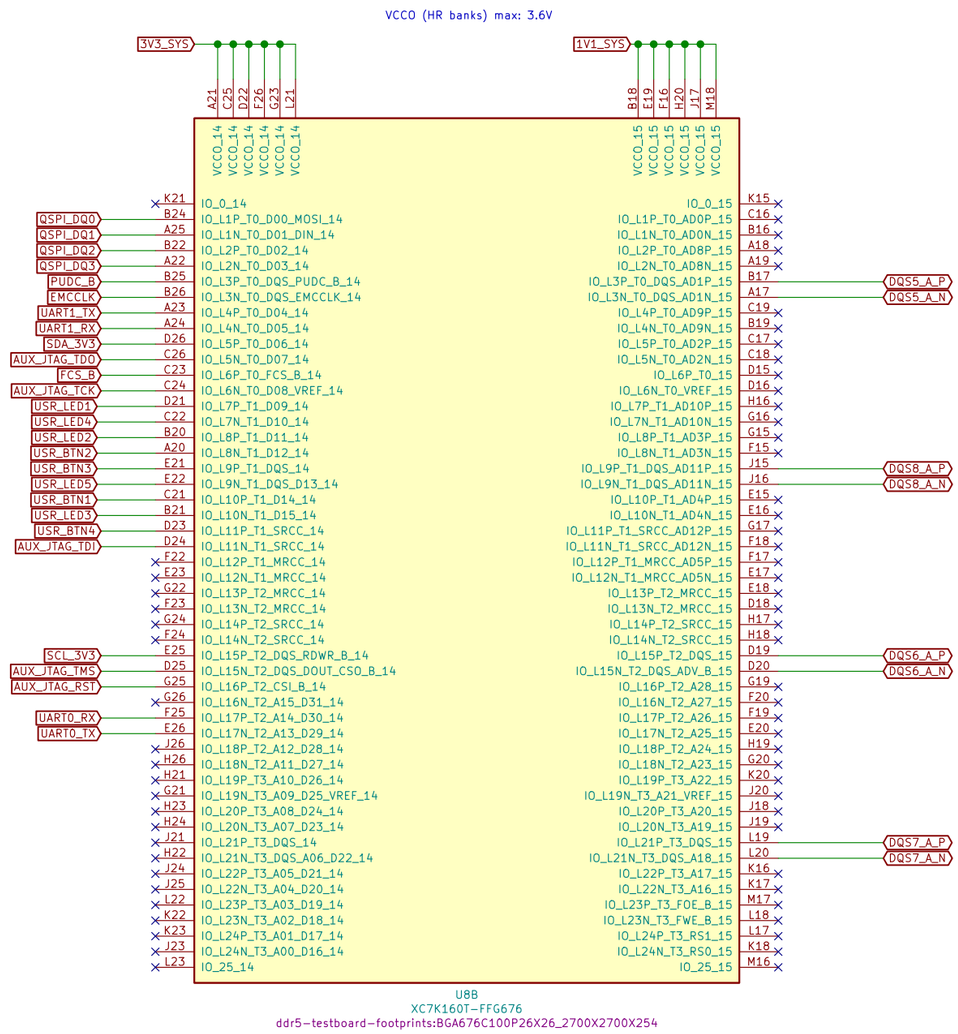
BANK 12

BANK 13

BANK 14

BANK 15





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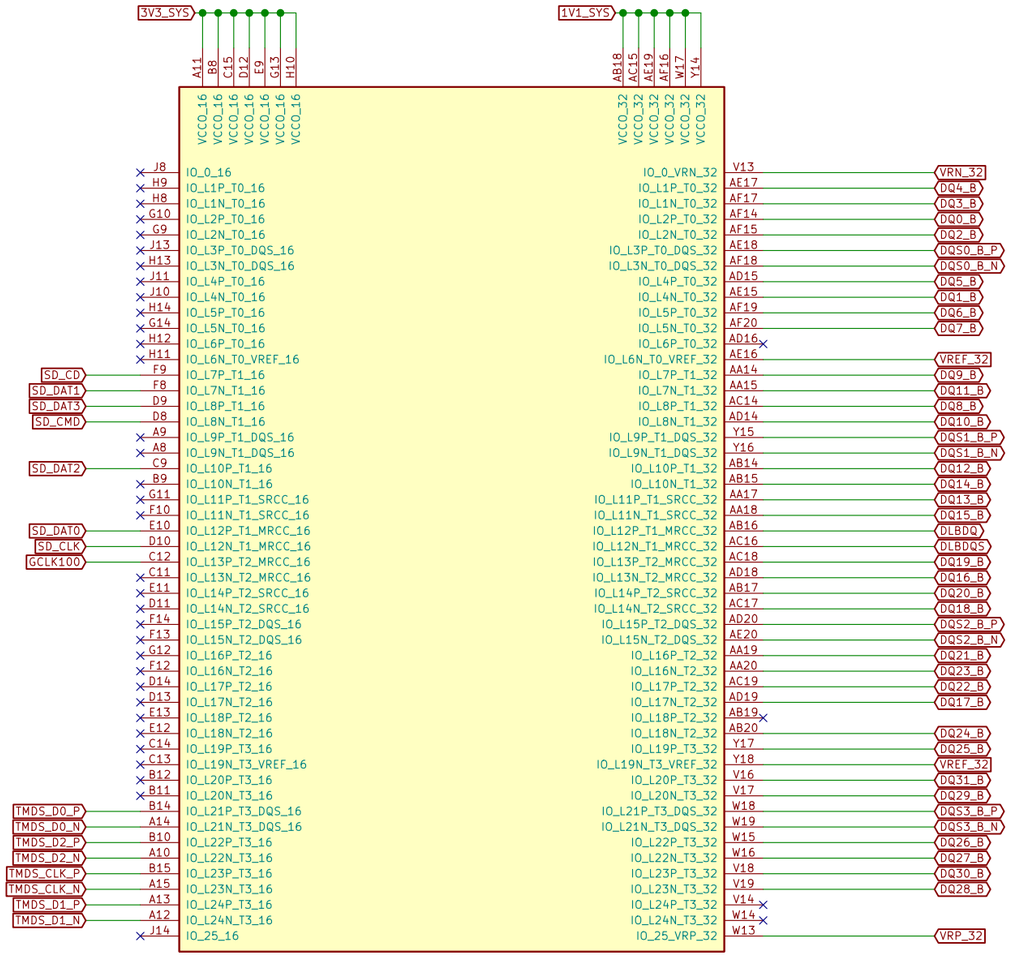
Sheet: /FPGA banks 12-15/
File: fpga-banks-12-15.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 9/10

BANK 16

VCCO (HR bank) max: 3.6V



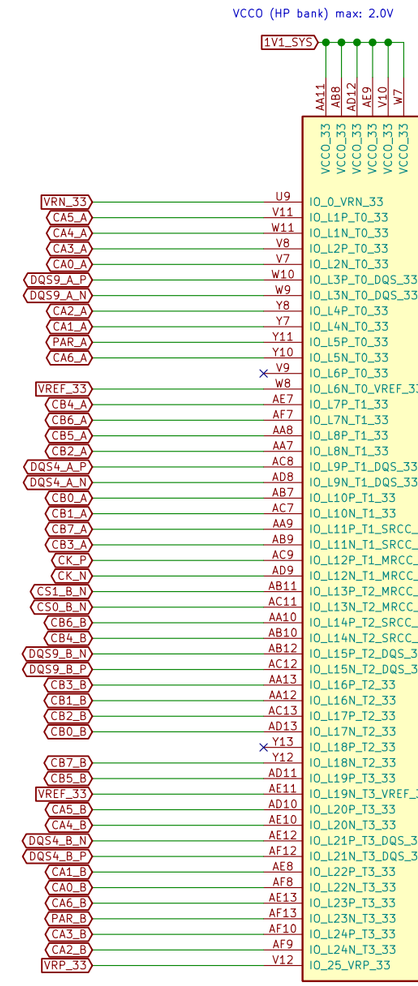
BANK 32

VCCO (HP bank) max: 2.0V

U8C
XC7K160T-FFG676
ddr5-testboard-footprints:BGA676C100P26X26_2700X2700X254

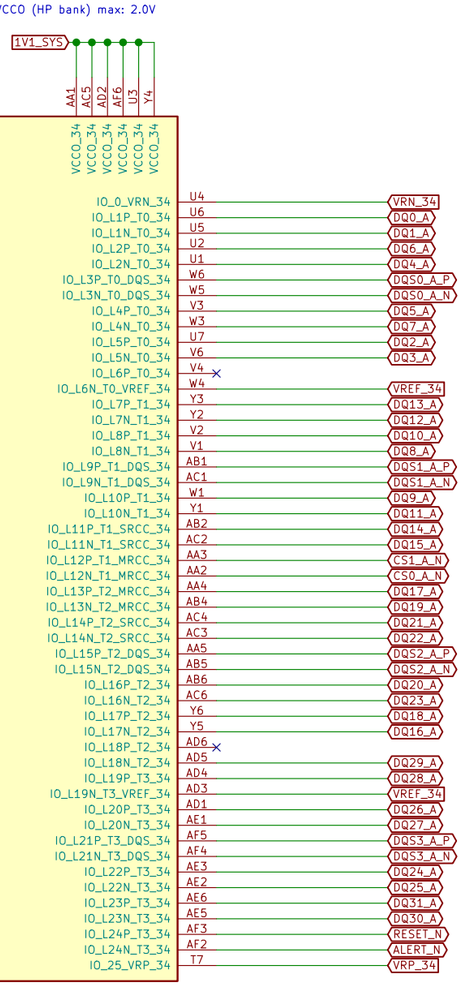
BANK 33

VCCO (HP bank) max: 2.0V



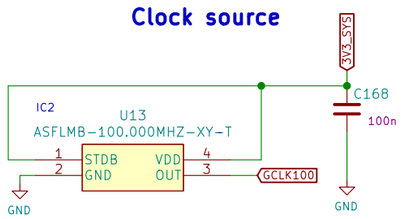
BANK 34

VCCO (HP bank) max: 2.0V

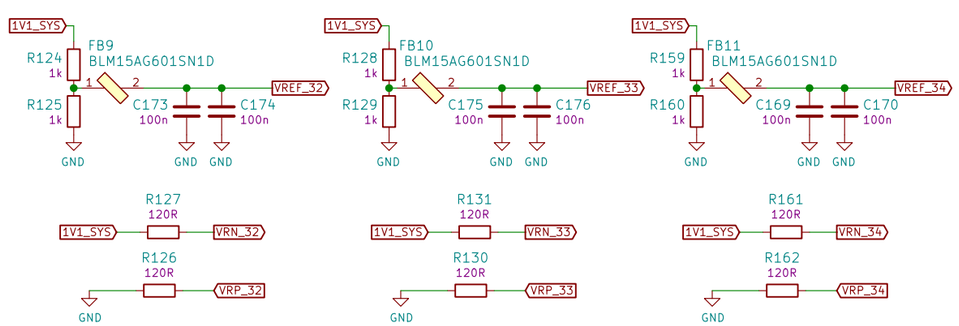


U8D
XC7K160T-FFG676
ddr5-testboard-footprints:BGA676C100P26X26_2700X2700X254

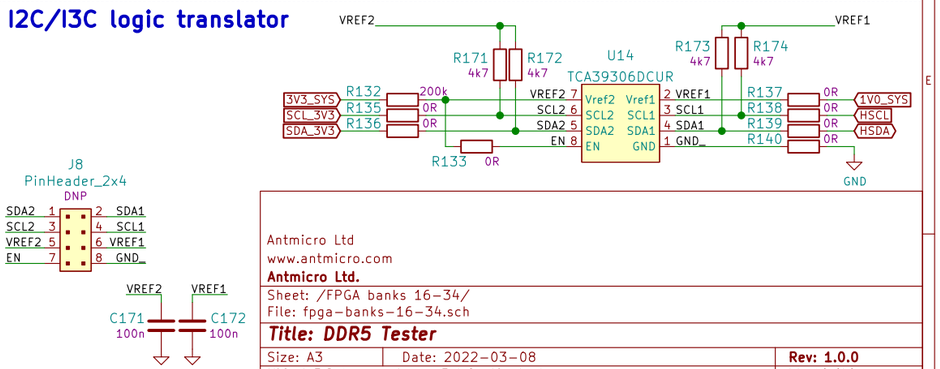
Clock source



VREF



I2C/I3C logic translator



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Sheet: /FPGA banks 16-34/
File: fpga-banks-16-34.sch

Title: DDR5 Tester

Size: A3	Date: 2022-03-08	**Rev: 1.0.0**
KiCad E.D.A.	eeschema 5.1.9+dfsg1-1	Id: 10/10