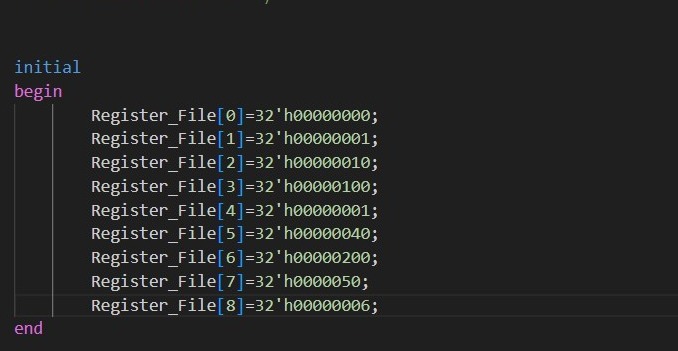
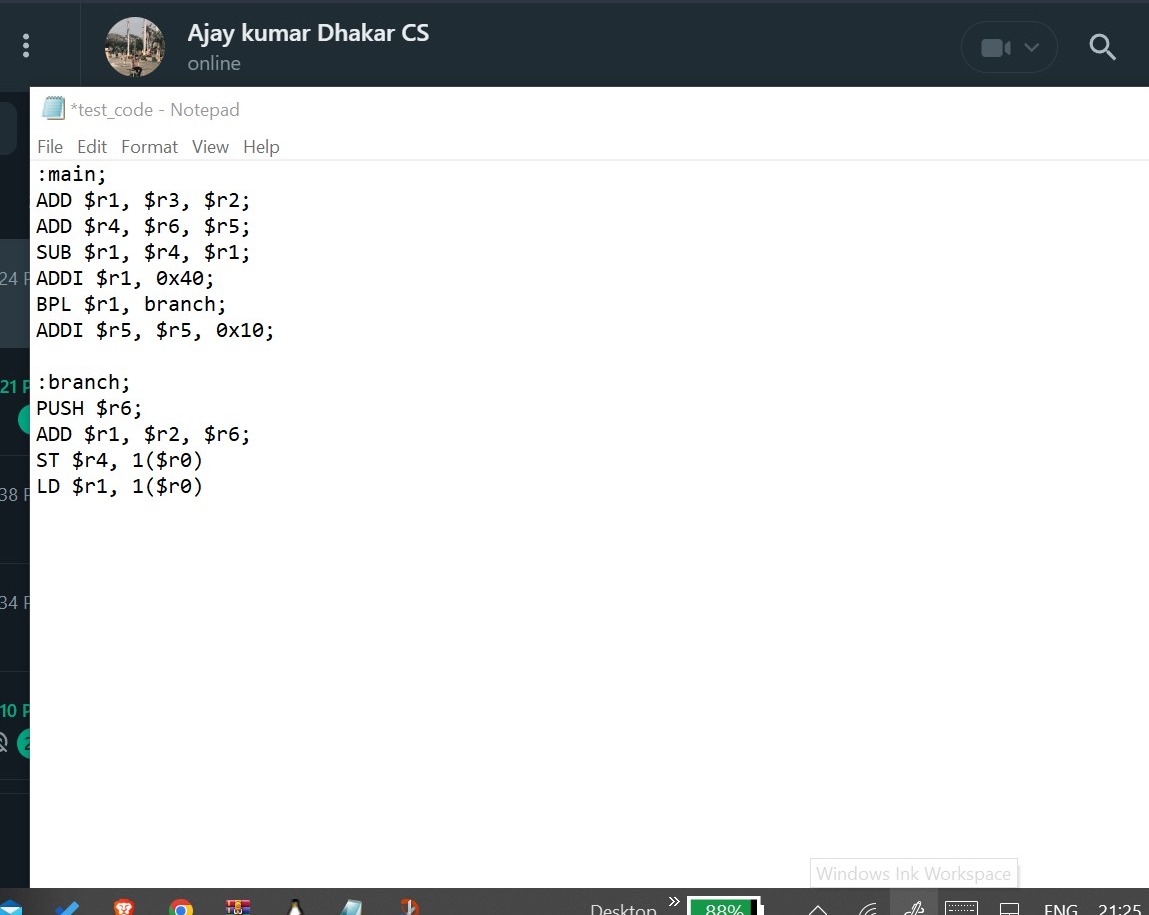
**Initial Values of Register bank :**

****

**Instructions for Test cases:**

****

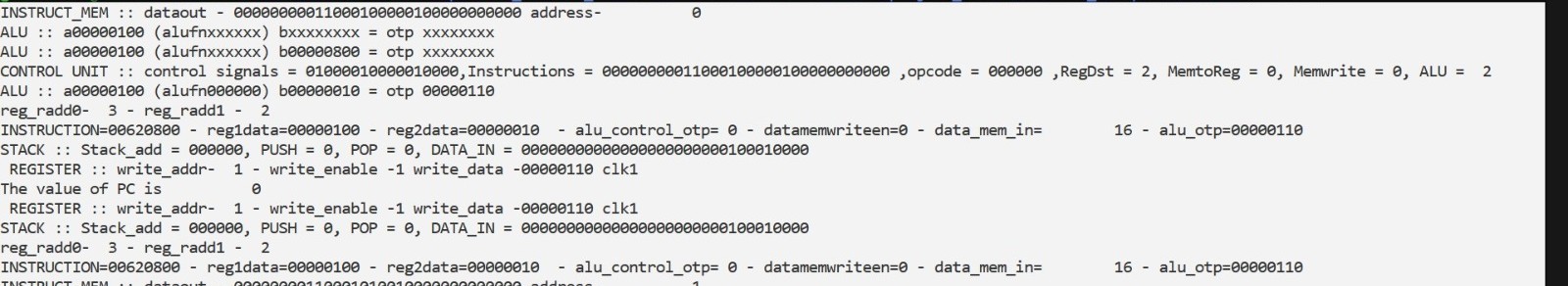
**Output for Each Instruction:**

**Commands to compile using Iverilog**

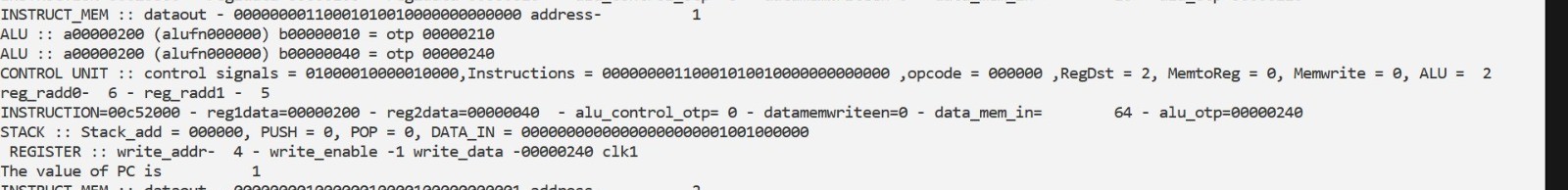
****

**0. ADD $r1, $r3, $r2;**

Instruction = 00000000011000100000100000000000

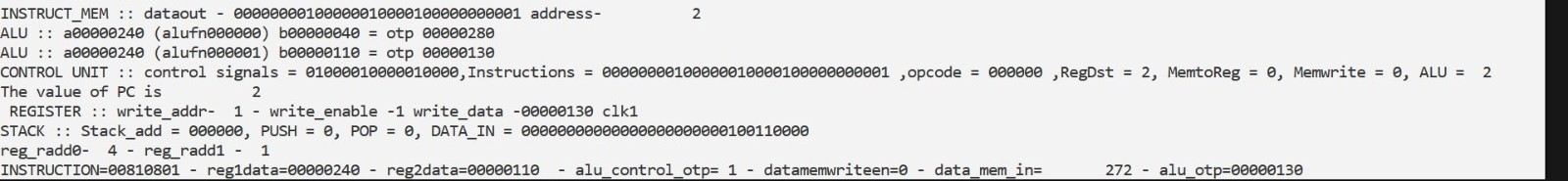


**1. ADD $r4, $r5, $r6;**

Instruction = 00000000110001010010000000000000

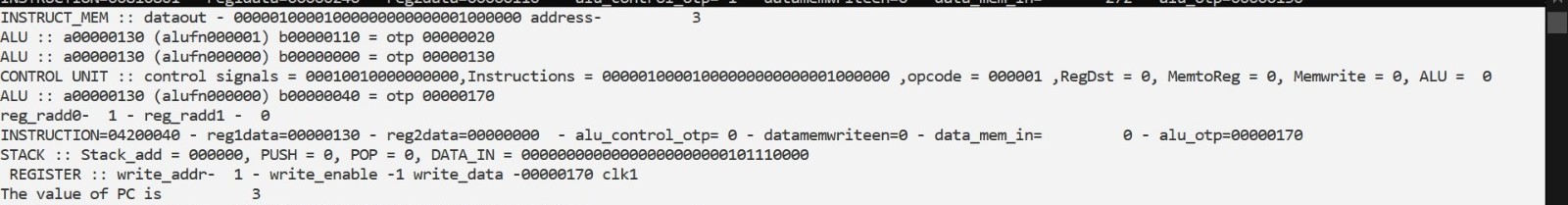
**2. SUB $r1, $r4, $r1;**

Instruction = 00000000100000010000100000000001



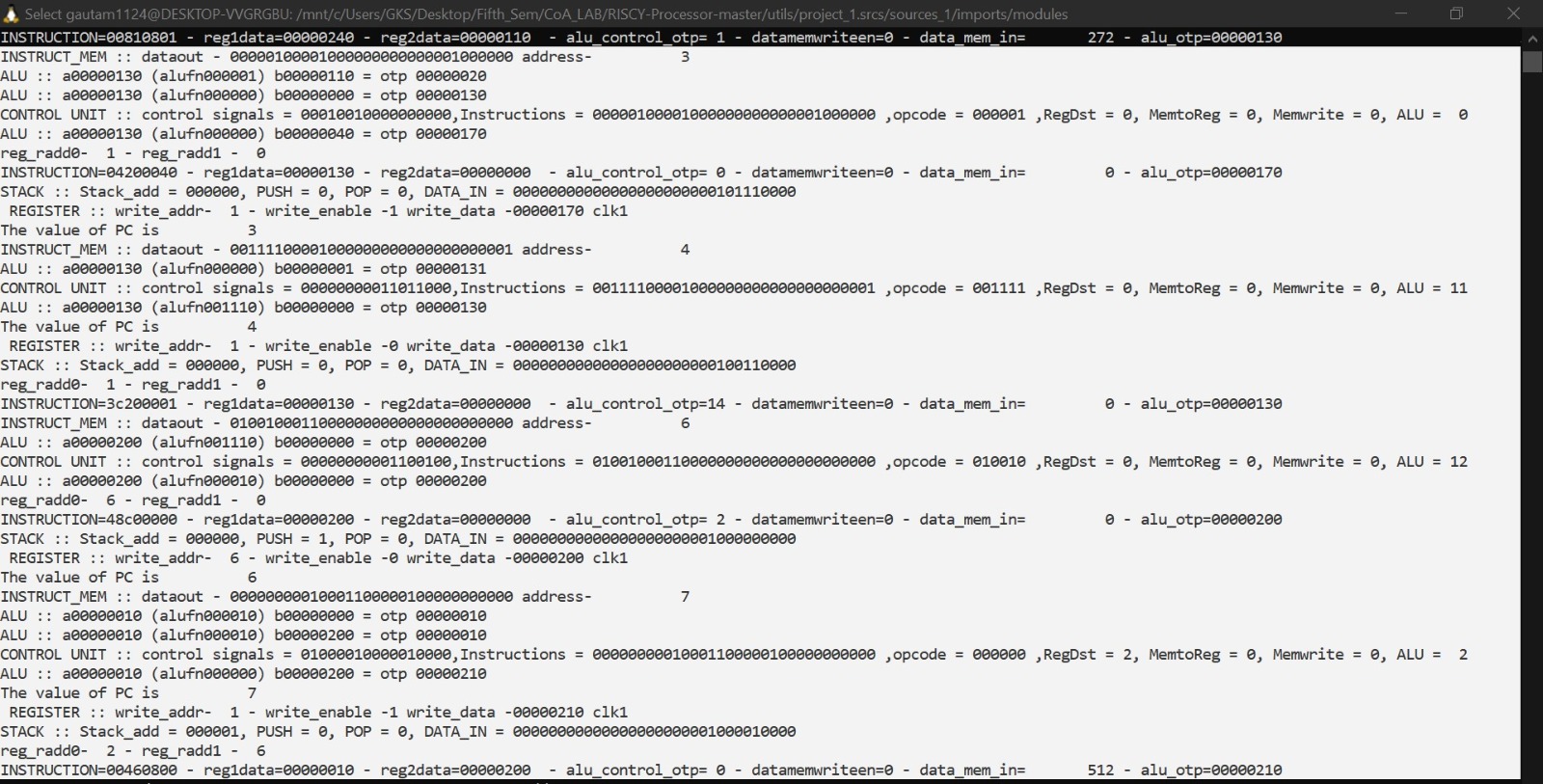
**3. ADDI $r1, 0x40;**

Instruction = 00000100001000000000000001000000



**4. BPL $r1, branch;**

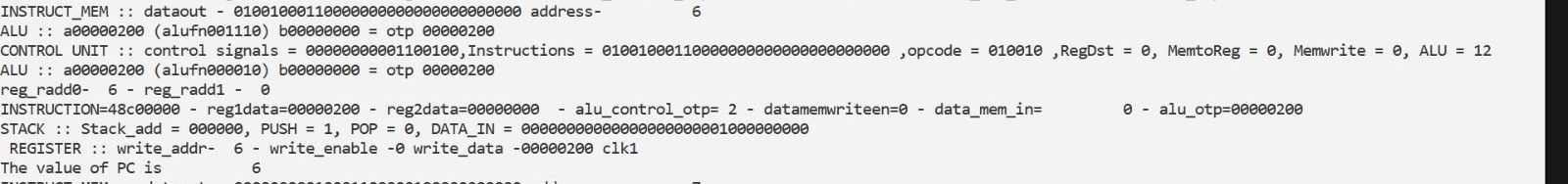
Instruction = 00111100001000000000000000000001



As this is branch instruction so it will jump to instruction address 6(instruction address of branch)

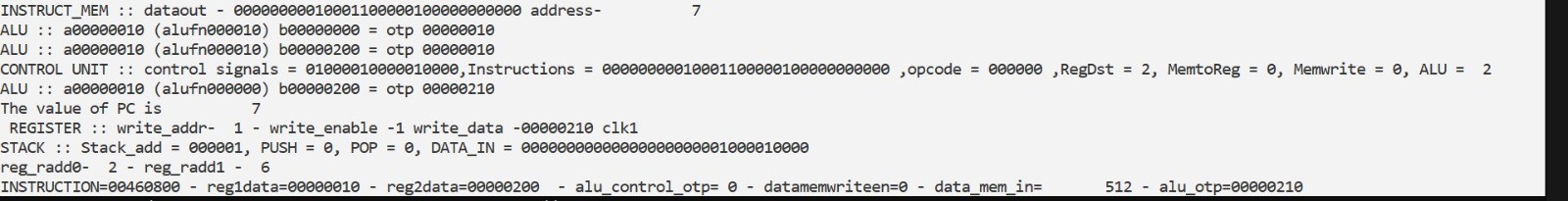
**5. Push $r6;**

Instruction = 01001000110000000000000000000000

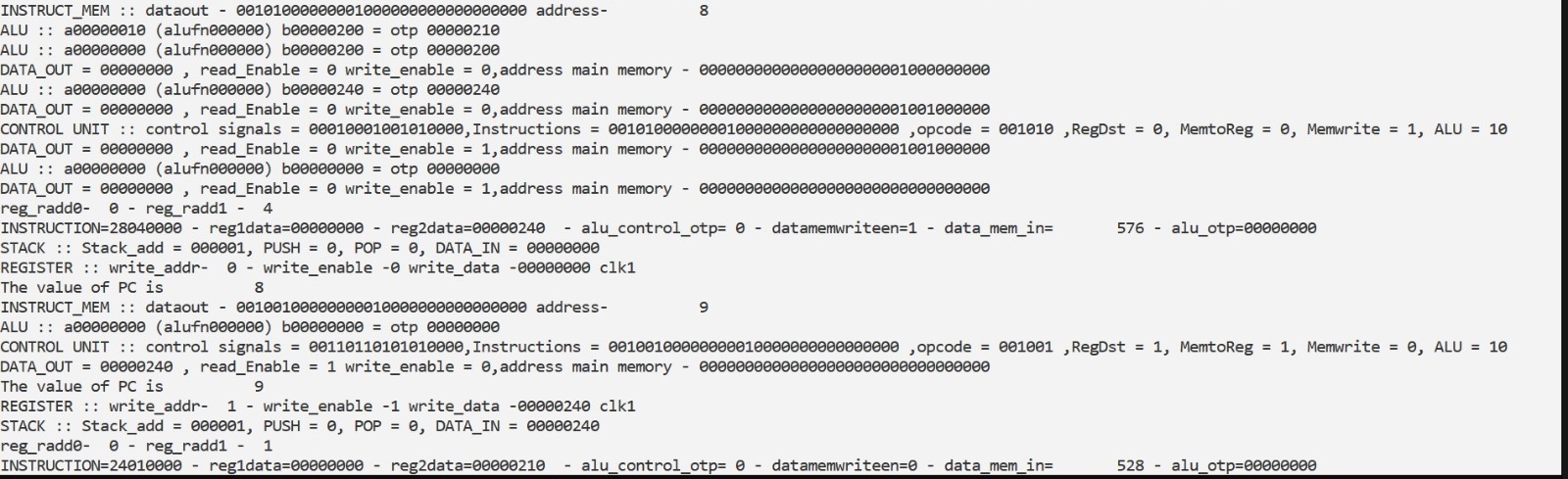


**6. ADD $r1, $r2, $r6;**

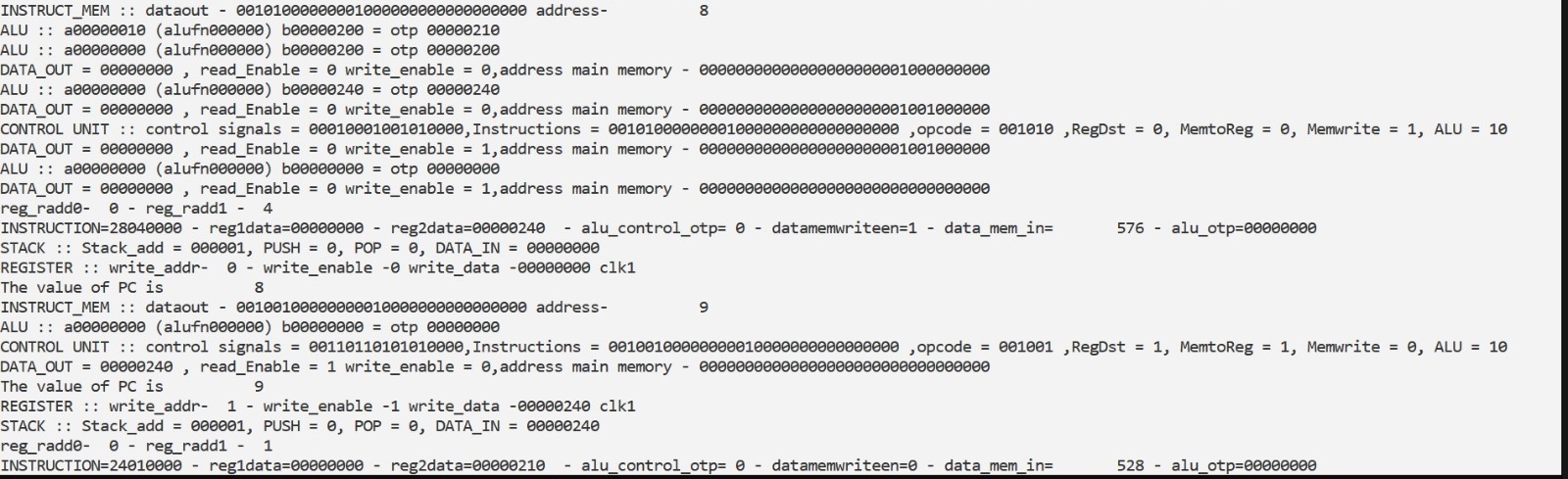
Instruction = 00000000010001100000100000000000



**7. ST $r4, 1(r0);**

Instruction = 00101000000001000000000000000000

**8. LD $r1, 1($r0);**

Instruction = 00100100000000010000000000000000

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