University of Applied Sciences and Arts
Northwestern Switzerland

Distributed FPGA for enhanced image processing

Technical Requirements

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Table of contents

1 Dates

Project start	18.09.2017
Submission of planning	06.10.2017
Submission of documentation	12.01.2018
Presentation	26.01.2018

2 Contact

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3 Work environment

The team Jan Stocker and Noah Hütter are working at FHNW Brugg-Windisch. They are doing a weekly digest by Mail to Nomoko.

4 Documentation

4.1 Technical requirements sheet

The technical requirement sheet is in form of a table with keywords.

4.2 Organizational requirements sheet

A Rough time plan is created showing the milestones and the 4 tasks:

1. Research and feasibility check (20%)
2. Investigate and evaluate computer vision algorithms (30%)
3. Implement the distributed FPGA algorithm (40%)
4. Present you achievement (10%)

4.3 Technical documentation

A technical report is written showing the problems and solutions. The code is commented. One documentation is sufficient for both companies.

4.4 Presentation

The team will perform a presentation about the results achieved at FHNW and Nomoko.

5 Goals

The project is divided into two parts.

5.1 First semester

By the 12/01/2018 a working platform is implemented with the following features:

- Data transmission from PC to FPGA and back
- Basic image processing task performed by the FPGA
- Keep the possibility open to distribute the workload to multiple FPGAs

5.2 Second semester

- Distribute the workload onto multiple FPGAs
- Implement a more demanding image processing task
- Benchmark the performance against a CPU/GPU

6 Technical specifications

6.1 Data transmission

The data is transmitted over Ethernet to the FPGA system. As an alternative, PCI could be an option.

6.2 Data format

The images have the data format of tiff and for the raw images dng.

6.3 Data size

A reference image exists.

6.4 Image processing algorithm

Different algorithms are compared. A simple and suitable algorithm is implemented on the FPGA. For example, debayering or edge detection.

6.5 Platform

The platform used is a Xilinx AC-701 board with Artix 7 series FPGA provided by Nomoko. It features:

- DDR3 SODIMM 1GB up to 533MHz / 1066Mbps
- 10/100/1000 Mbps Ethernet (RGMII)
- PCI Express 4-lane edge connector
- Onboard JTAG configuration circuitry to enable configuration over USB
- UART To USB Bridge

6.6 Design entry

6.6.1 Image processing

The image processing algorithm is programmed in C/C++ and then compiled to HDL using the Vivado HLS environment. VHDL is used as hardware description language.

6.6.2 Communications

The communication is implemented using configurable IP blocks provided by Xilinx or others.