

P5 Aufgabenstellung für

Herr Noah Hütter Herr Jan Stocker

Distributed FPGA for enhanced Image Processing

1. Ausgangslage

Die Firma Nomoko AG ist ein Spin-off der ETH Zürich. Ihre Vision ist, mit einer hochauflösenden Kamera ein digitales Abbild der Realität zu erzeugen. Hierzu entwickeln sie eine 1500 Megapixel Kamera!

2. Aufgabenstellung

Es sollen die Vorzüge der parallelen Bildverarbeitung auf mehreren FPGAs untersucht werden. Dazu soll ein Prototyp mit geeigneten Algorithmen implementiert werden. Detaillierte Informationen können aus der Technical Note – STP0005 von Nomoko AG entnommen werden.

3. Organisation

Auftraggeber: Nomoko AG

Experte: -

Betreuer: Michael Pichler

Arbeitsort: 4.223 (IME Labor, Steinackerstr. 5, Windisch)

Meetings: nach Bedarf

4. Form des Resultats

- Abgabe einer Planung
- Schriftliche Dokumentation in Papierform und Design-Daten in elektronischer Form
- Mündliche Präsentation vor dem Auftraggeber, den Dozierenden und weiteren Interessenten.
- Weitere Deliverables gemäss den Anforderungen des Studiengangs

5. Termine

Ausgabe der Arbeit: 18. September 2017 Abgabe der Planung: 06. Oktober 2017

Abgabe der Dokumentation: 12. Januar 2018. 12:00 Uhr

Präsentation: 26. Januar 2018

Windisch, den 13. September 2017

Michael Pichler

Distributed FPGA for enhanced Imaged Processing

Keywords

FPGA, LAN, Computer Vision, Digital Circuit Design

Abstract

In order to accelerate the intense image processing tasks we want to investigate a distributed dedicated hardware approach. To do so, basic computer vision algorithms such as Edge-Detection should be implemented on a Network consisting out of 4 FPGA boards such as the ARTIX7. To keep it simple, the network should be built up over Ethernet or any preferable other protocol. The FPGAs should then sharing the workload and contribute individually to the greater good.

Contents

Task Description	1
Task 1: Research and Feasibility Check (20 %)	2
Task 2: Investigate and Evaluate Computer Vision Algorithms (30 %)	2
Task 3: Implement the distributed FPGA Algorithm (40 %)	2
Task 4: Present your achievement (10 %)	2
Milestones	2
Requirements	3
Correspondence	3

Task Description

The student is asked to evaluate a distributed FPGA system for the purpose of image processing. A hardware module has to be implemented that performs a basic computer vision task in a distributed matter. Once this is achieved the system should either be extended to perform a more sophisticated task or to more than 4 FPGAs. During the Project, the student is expected to perform the following tasks. These task do not necessarily have to be done in the following order.

Task 1: Research and Feasibility Check (20 %)

- Set up the FPGA network and check project feasibility.
- Find related research considering distributed FPGA designs.

Task 2: Investigate and Evaluate Computer Vision Algorithms (30 %)

- What algorithms can easily be implemented on an FPGA or a system of FPGAs try!.
- What part of the algorithms can be distributed.
- Evaluate and take a decision with respect to consumed area, timing issues and own defined metrics. (e.g. AT-product, Throughput, etc.).

Task 3: Implement the distributed FPGA Algorithm (40 %)

- Implement the chosen algorithm on the 4 FPGAs.
- Compare different use cases with 1, 2, 3 and for FPGAs involved.
- Push the system by either implementing a more complex algorithm or extend it to more FPGAs, how does it scale?

Task 4: Present your achievement (10 %)

- Write a report, document your project and comment your code.
- Prepare a presentation!

Milestones

The goal of the project is to evaluate the benefits of a distributed FPGA system. We want to know if it makes sense to rely on such a system and integrate it into our network to perform certain tasks. Over the project the following milestones are expected to be reached:

- Successfully set up the FPGA network.
- Find a suitable computer vision algorithm to be implemented on the network.
- Implement the algorithm on the network and compare performance in between different use cases.
- Perform an outstanding presentation.

Requirements

Students that are interested in hardware design and networks. Generally students that are able to work independently and want to explore new technical challenges.

- VHDL/Verilog
- Computer Vision
- Ethernet Protocol

Correspondence

Engineer: Matteo Pavan, Patrick Oschatz

Email: matteo(at)nomoko.camera, patrick(at)nomoko.camera