Assignment-3

1) *Introduction*

In this lab we have extended previous lab work by displaying all 4 digit by using "clock" and "4: 1 multiplexer" for selection of any one anode activation in each cycle .

2) *Implementation Design*

For display of each 4 digit uniformly we have taken 20 bit vector named "refresh− timer" which is initialised to 0.

At each "rising edge of clock" we increment the refresh − timer value by 1 and extract "19 and 18" bits value from it.

These 2 bit value of refresh − timer vector can be "00" , "01", "10" and "11" which is stored in 2 bit vector "LED − activation" and this value is used for selection from 4 different anodes basically working as 2 − bit select input for the multiplexe .

We have also used 4 − bit vector "which− led" to store 4 bit values from 16 − bit "Input" which is divided into 4 equal parts each consisting of 4 bits which are stored in "which − led" as per value of "LED − activation" .

LED_activation	Anode_Activate
00	0111
01	1011
10	1101
11	1110

Schematic Diagram of 4digit 7 Segment LED display using clock

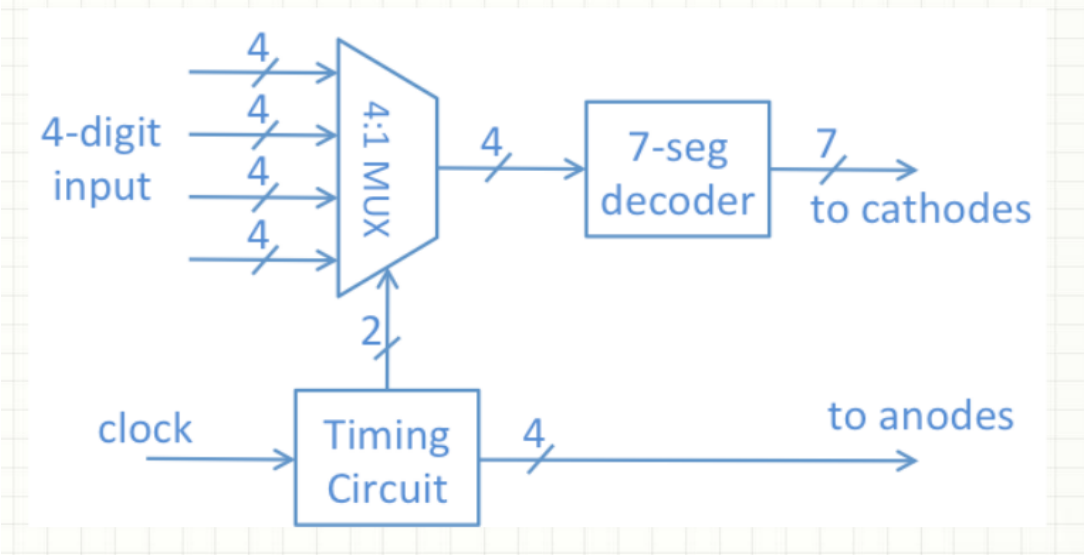


Fig 1: Basic circuit showing use of 4: 1 MUX and clock

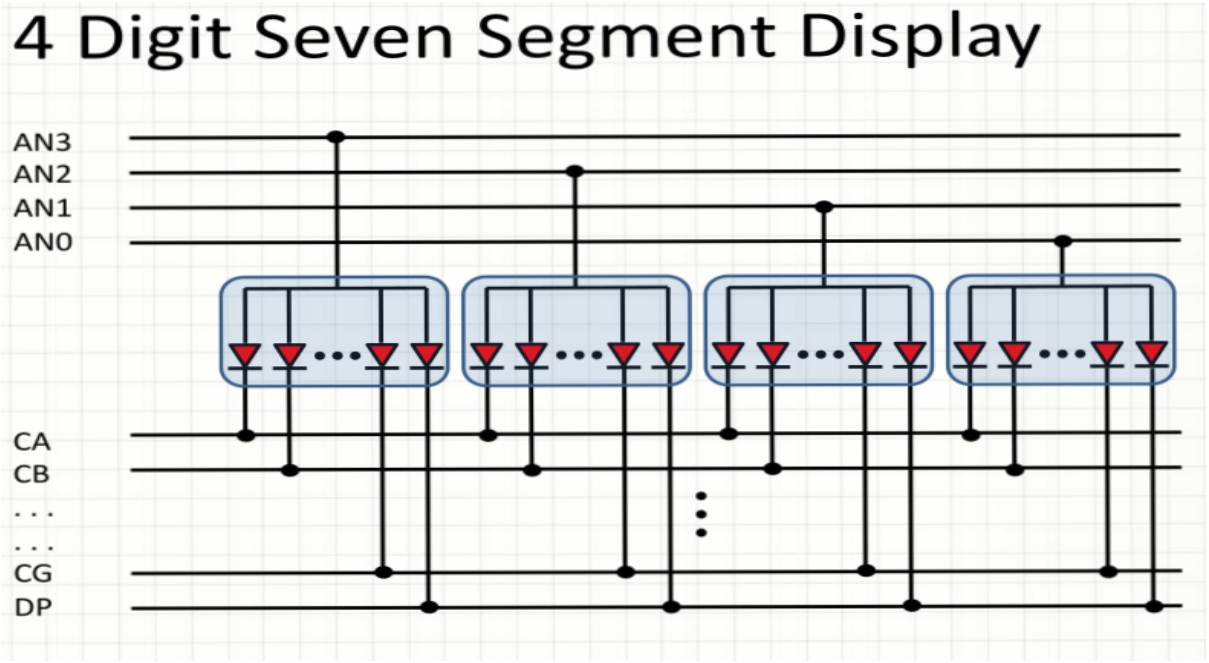


Fig 2 : 4 digit 7 segment display along with its anode and cathode

3) *Simulation Waveform for 4 digit 7 segment display*

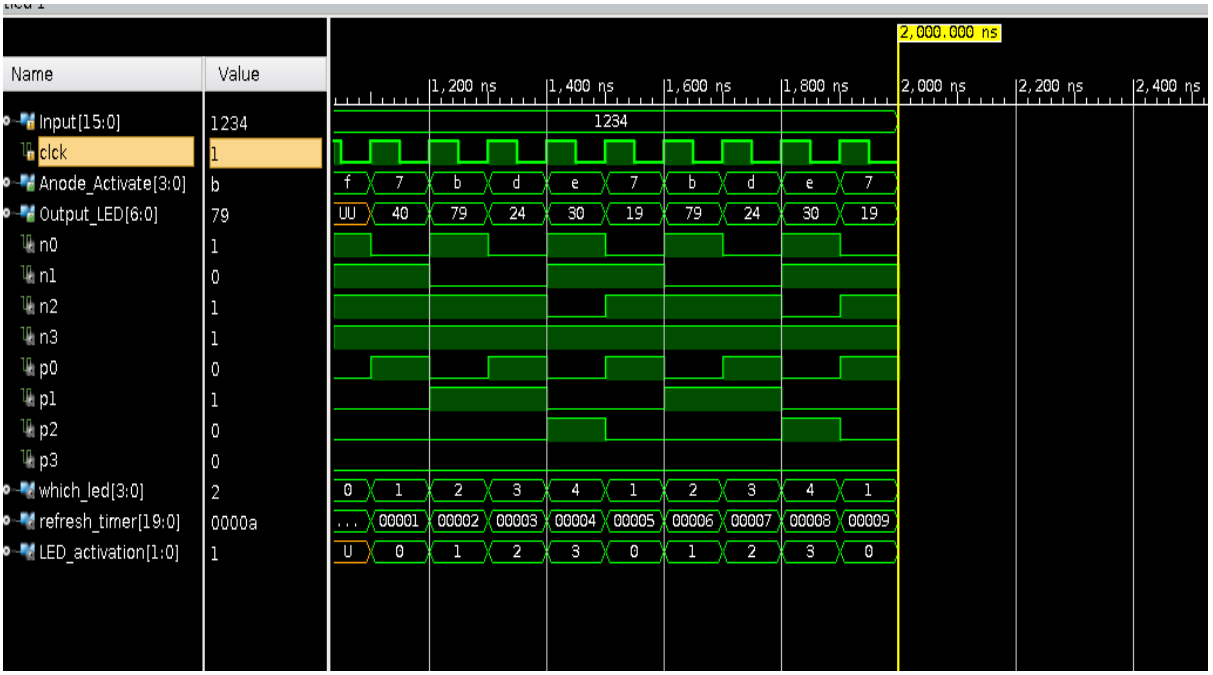


Fig 3 : Waveform of Input and Output of 4 digit – 7 segment display

4) *Digital Circuit for* 4 − *digit* 7 *Segment Display for displaying* 4 *digit*

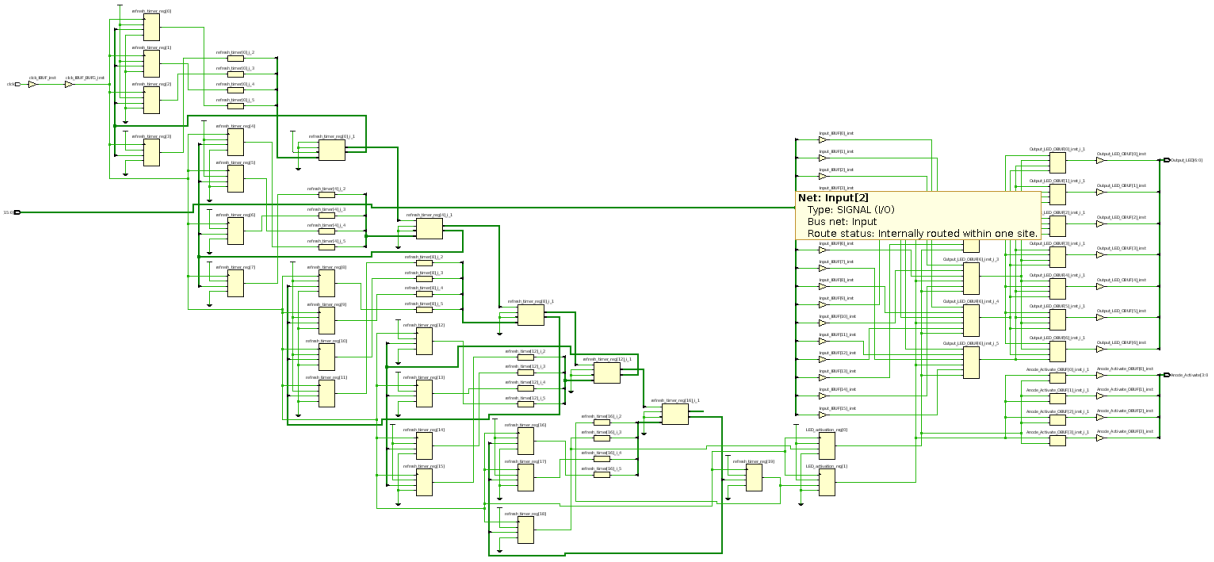


Fig 4 : *Digit Circuit of* 4 *digit* − 7 *segment display each digit range from* 0 − *F*

5) *Resource Utilisation*

a) LUT Memory =0
b) LUT logic = 30
c) DSP =0
d) Flip Flops =22
e) BRAM = 0

6) *Some other relevant diagram for resource utilisation*

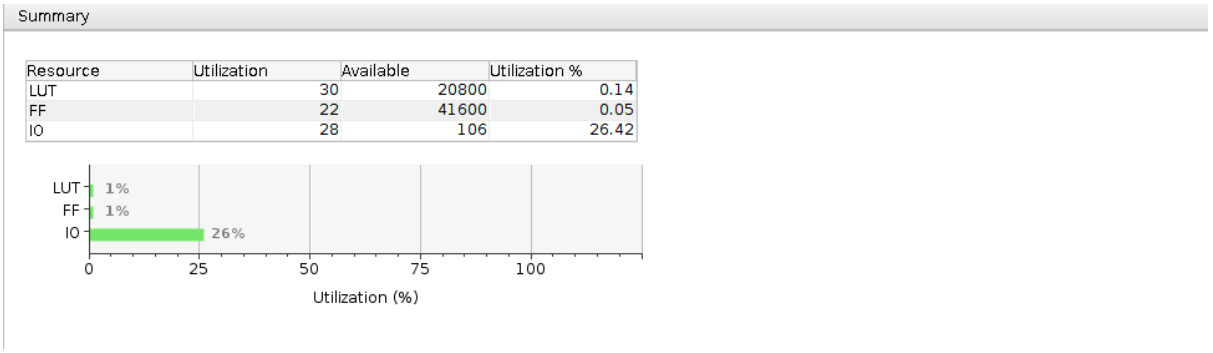


Fig 5 : *Summary*

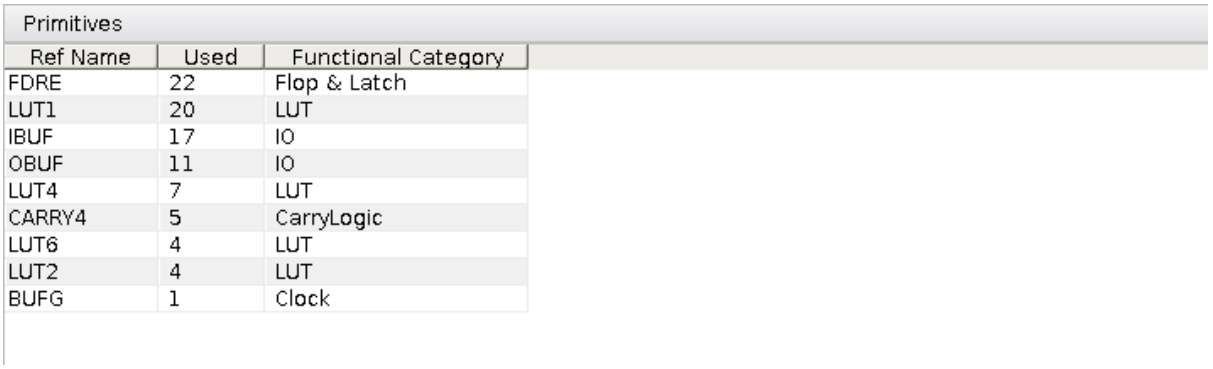


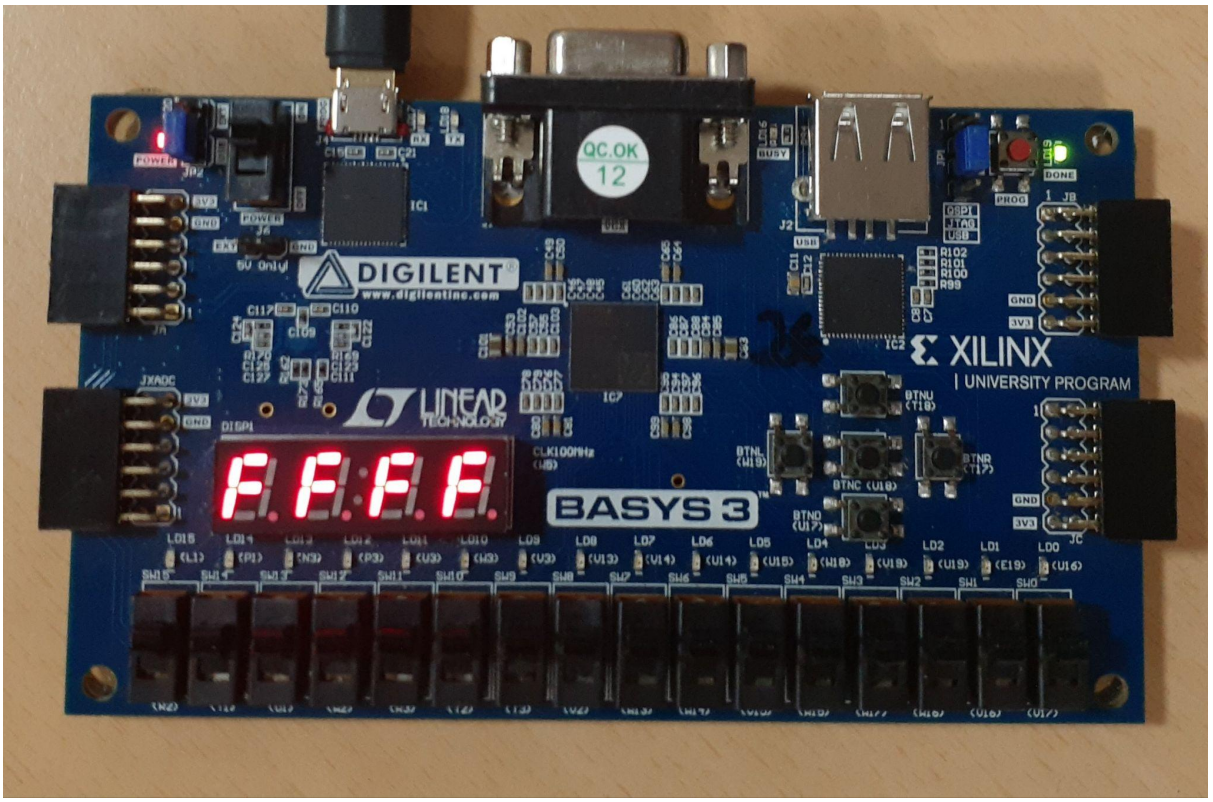
Fig 6 : *Primitives*

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
four_digit_display	30	22	28	1

Fig 7 : Hierarchy

7) *Some photographs of FPGA Board*



(a)