Digital logic and Design.

Lab Assessment Test - 2.

Slot: L43 + L44.

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Q1. Design a four bit BCD synchronous down counter using D Flip flop.

=) Answer.

Aim: To design a four bit BCD synchronous down counter using D Flip flop.

Software required: Multism.

Design steps:

Excitation Table of D-Flip flop.

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

since, it is a BCD down counter, it counts from decimal 9 i.e binary 1001 to decimal 0 i.e 0000.

Now, constructing the truth table for the given problem.

We get,

Present				Next state				Flipflop I/ps.			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{B+1}	D_D	D_C	D_B	D_A
1	0	0	1	1	0	0	0	1	0	0	0
1	0	0	0	0	1	1	1	0	1	1	1
0	1	1	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	0	0	0	1	0	0
0	1	0	0	0	0	1	1	0	0	1	1
0	0	1	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0

Now,
Using K, map to simplify the obtained truth table and finding equations for D_D, D_C, D_B and D_A.

Now,

a) For D_D.

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

$$D_D = Q_D Q_C' Q_B' Q_A$$

b). For D_C.

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	0	0	0
10	1	0	0	0

So, $D_C = Q_D Q_C' Q_B' Q_A' + Q_D' Q_C Q_A + Q_D' Q_C Q_B$.

c) For D_B.

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	1	0
01	1	0	1	0
11	0	0	0	0
10	1	0	0	0

So, $D_B = Q_D' Q_C Q_B' Q_A' + Q_D Q_C' Q_B' Q_A' + Q_D' Q_B Q_A$.

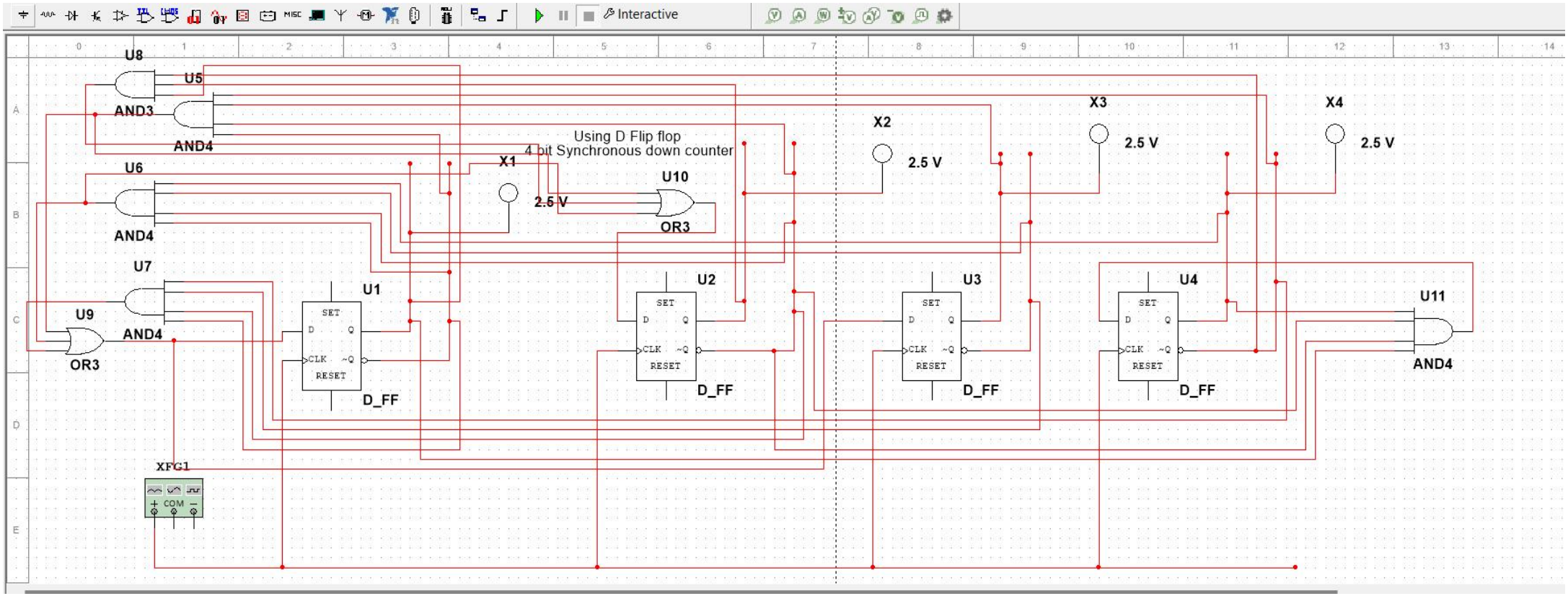
d) For D_A.

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	0	0	0	0
10	1	0	0	0

So, $D_A = Q_D' Q_C Q_B' Q_A' + Q_D Q_C' Q_B' Q_A' + Q_D' Q_B Q_A'$

Circuit Diagram:

Result:- Hence, 4 bit BCD down counter is designed and implemented sucessfully ~~in~~ using multism.


Interactive
Using D Flip flop
4 bit Synchronous down counter
U8
U5
AND3
AND4
U6
AND4
U7
AND4
U9
OR3
X1
2.5 V
U10
OR3
X2
2.5 V
X3
2.5 V
X4
2.5 V
U1
U2
U3
U4
U11
AND4
SET
D
Q
CLK
~Q
RESET
D_FF
XFG1
COM