Hari Narayana

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PROFILE SUMMARY

ECE Master's candidate at UMass Amherst with a thesis focused on Physical Design, gaining hands-on experience in RTL-to-GDSII flows including synthesis, floorplanning, place-and-route (PnR), clock tree synthesis (CTS), and static timing analysis (STA). Proficient in industry-standard EDA tools (Cadence, Synopsys) and TCL scripting for automating synthesis-to-signoff flows. Co-author of a GLSVLSI 2025 publication on security-aware placement for split-manufactured ICs.

EDUCATION

Master of Science in Electrical and Computer Engineering — Expected Sep 2025
University of Massachusetts Amherst, Amherst, MA — GPA: 3.86/4.0

Bachelor of Technology in Electronics and Communication Engineering — May 2022
National Institute of Technology Andhra Pradesh, Tadepalligudem, India — GPA: 8.33/10

TECHNICAL SKILLS

- **Programming Languages**: C, C++, Python, Verilog, SystemVerilog, Tcl, Perl, Matlab
- **Electronic Design Automation (EDA) tools**: Cadence (Virtuoso, Innovus, Assura), Synopsys (Design Compiler, VCS, PrimeTime, Formality, HSPICE, CosmosScope), Siemens ModelSim
- **VLSI Design Flow**: Custom Design, RTL-to-GDSII Flow, Clock Tree Synthesis (CTS), Timing Closure, Clock Domain Crossing (CDC), Static Timing Analysis (STA), Low-Power Design, and Design for Testability (DFT)
- **Industry Standard Protocols**: AMBA (APB, AHB, AXI, CHI), I2C, SPI, UART
- **Operating Systems & Tools**: Linux, Windows, Version Control using GIT

RELEVANT EXPERIENCE

Graduate Research Assistant, Dept of ECE — Sep 2024 - Present
VLSI CAD Lab, University of Massachusetts Amherst

- Developed a novel security-aware place-and-route (PnR) methodology that optimizes cell placement in k-secure designs, achieving 12.55% lower power consumption, 41.16% higher operating frequency, and 16.49% wirelength reduction across benchmark circuits compared to non-security-aware placement techniques.
- Executed RTL-to-GDSII flow for digital designs (>10M gates) at 45nm, including synthesis (DC Shell), place-and-route (Innovus), equivalence checking (Formality), static timing analysis (PrimeTime), and DRC/LVS verification.
- Designed ASIC circuits with asynchronous TX/RX clock domains, integrating two-flip-flop synchronizers for metastability mitigation and tunable delay lines for clock phase shifting. Measured signal propagation delays to enable delay-based Physical Unclonable Functions (PUFs) for chiplet authentication.

PROJECTS

ASIC Design and Implementation — Sep 2023 - Dec 2023
VLSI Design Principles, EC-ENG 658 — University of Massachusetts Amherst

- Built transistor-level schematics and manual layouts using Cadence Virtuoso Schematic XL, Virtuoso Layout GXL; performed DRC and LVS checks, parasitic extraction (PEX) using Cadence Assura, and PPA analysis using HSPICE.
- Automated RTL-to-GDSII flow using TCL scripts to streamline synthesis (Synopsys DC), floorplanning, power grid design, Place and Route (Cadence Innovus), clock tree synthesis, and timing closure (PrimeTime).

PPSFP Fault Simulation and Built-In Self-Test (BIST) Design — Sep 2024 - Dec 2024
Testing and Diagnosis of VLSI Systems, EC-ENG 654 — University of Massachusetts Amherst

- Engineered a PPSFP fault simulator and a BIST framework with a 32-bit LFSR-based Test Pattern Generator and 16-bit MISR-based Output Response Analyzer, achieving 95% average fault coverage with 0.0015% aliasing probability across ISCAS benchmark circuits (c17, c432, c499, c880, c1355) using random input patterns.

MIPS32 Pipeline Implementation — Sep 2023 - Dec 2023
Computer Architecture, EC-ENG 668 — University of Massachusetts Amherst

- Implemented a MIPS32 pipeline in Verilog for R-type and I-type instructions, with 14 ALU operations, HALT instruction support, and a specialized flip-flop for handling branch-taken scenarios effectively.
- Created a comprehensive testbench to verify functionalities and ensure proper operation of the pipeline.

Design and Optimization of a Basic ALU — Sep 2024 - Dec 2024
Advanced VLSI Design Project, EC-ENG 669 — University of Massachusetts Amherst

- Designed a 16-bit Arithmetic Logic Unit (ALU) using multiplexers and full adders, performed synthesis (Synopsys DC Shell) and Place and Route (Cadence Innovus), and implemented a scan chain for testability.
- Evaluated various adder architectures and applied High-Level Synthesis (HLS) techniques to optimize performance, power, and area (PPA), while analyzing trade-offs to improve design efficiency and scalability.

PUBLICATIONS

- Arjun Suresh, Hari Narayana Burra, Wei-Huan Chen, Daniel Holcomb, *"Security Aware Placement for Split Manufactured Integrated Circuit Design Flows," Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2025. (Accepted as a full research paper; to be published)