EE2019 Analog Systems and Lab: Problem Set 7

Problem-1

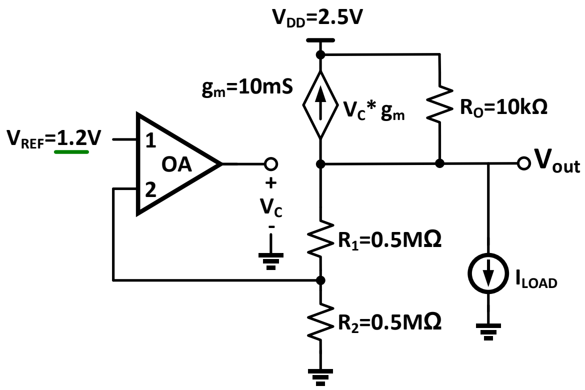


Figure 1: Circuit for Problem-1

Figure 1 shows a linear regulator. Assuming op-amp OA is ideal:

a) Determine the polarity of input terminals 1 & 2 of the op-amp for negative feedback operation.

b) Find the output voltage Vout.

c) Find the minimum and maximum value of V_C if I_{LOAD} varies from 1mA to 10mA.

d) Find the error in output voltage if OA is replaced with an op-amp of gain = 100 and R_{LOAD}=

Problem-2

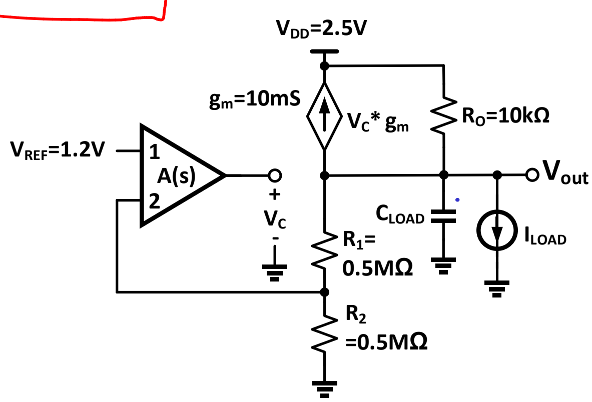


Figure 2: Circuit for Problem-2

Figure 2 shows the linear regulator of Figure 1 with a real 2-stage compensated op-amp having transfer function:

$$A(s) = \frac{100}{(1+5x10^{-6}s)(1+5x10^{-8}s)}$$

a) Assuming op-amp pole as dominant, find the maximum value of the load capacitor, C_{LOAD} to maintain the phase margin > 45º. Support your answer with bode magnitude and phase plot.

b) Is it possible to use C_{LOAD} larger than the value found in (a) and still achieve a phase margin > 45º? Support your answer with bode magnitude and phase plot.

c) Determine the value of C_{LOAD} for which phase margin becomes 0º.

Problem-3

Simulate the circuit of Figure 2 on LTSpice and compare the result of problem-2 with your simulated results. Comment on differences, if there are any.

Problem-4

In class, we saw that the response of a "slow" linear time-invariant system to a rapidly varying input like v_i in Figure 4 is approximately the same as that due to v_i^. In this problem, we will convince ourselves of this by working a specific example on LTSpice simulation.
Assume that v_i has a frequency of 1 MHz, and a duty cycle of 10%. *RC* = 1 mS. On the same graph, plot $v_o(t)$ when the input is $v_i(t)$, and when it is v_i^(t).

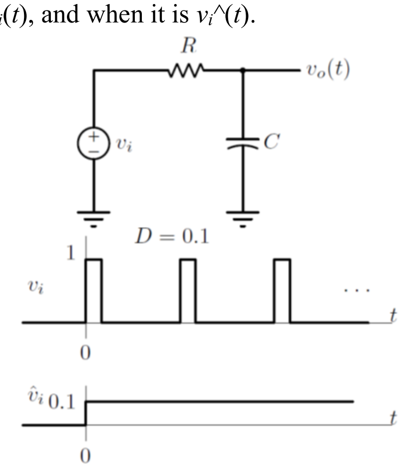


Figure 4: Circuit for Problem-4

Problem-5

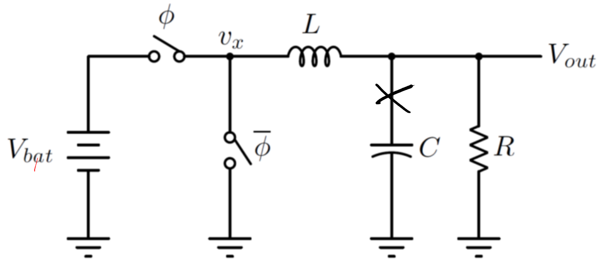


Figure 5: Circuit for Problem-5

Figure 5 shows a buck converter. The battery voltage *Vbat* is 5V. ϕ and $\overline{\phi}$ are complementary switch drive signals. The duty cycle of ϕ is denoted by D. The switching frequency is 1.5 MHz. $L = 2.2\ \mu$H and $C = 22\ \mu$F. The load resistor $R = 10\Omega$.

a) Determine D needed to achieve $Vout = 3{:}3$V.
b) Determine the transfer function from vx to $Vout$.
c) Using the observation that the pole frequency of the LC filter is much lower than the switching frequency, determine the ripple in the inductor current and output voltage.
d) Sketch the current waveforms in the inductor and capacitor in steady state.
e) Sketch the voltage waveform $Vout$ in steady state.

Problem-6

As usual, the switching period Ts is much smaller than the time-constant of the LC network. S1 and S2 are controlled by complementary waveforms, and the waveform controlling S1 is shown in the figure. Determine the average output voltage vo, and the average current drawn from the source. Draw the steady state current and voltage waveforms through/across the inductor and capacitor.

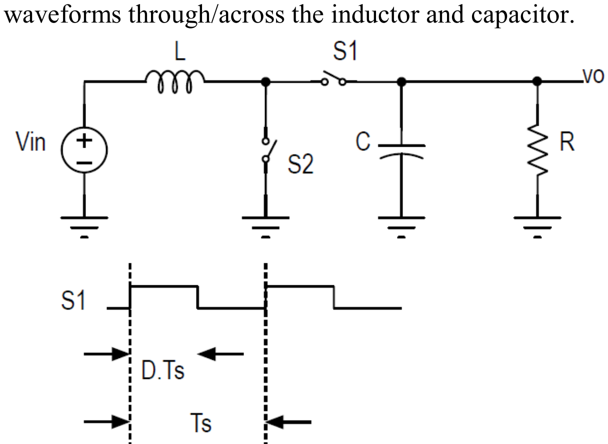


Figure 6: Circuit for Problem-6

Problem-7

Figure 7 shows the circuit diagram of a type-I (integral) compensated buck converter with output voltage, Vout regulated at 2.5V for input supply, V_{DD}=5V and load current, I_{LOAD}=1A. . Assuming switches S_P and S_N are ideal.

a) Model the buck converter in continuous time domain and find the small signal loop gain transfer function.
b) Determine the value of capacitor C_1 to achieve the gain margin of > 20dB and draw the bode magnitude and phase plot.
c) Find the value of control voltage, V_{CTRL} and duty cycle, D to regulate the output voltage at 2.5V.
d) Find the value of peak to peak inductor ripple current and peak-to-peak output ripple voltage.
e) Draw the steady state waveforms for PWM voltage (V_{PWM}), switch currents (I_P and I_N), inductor current (I_L) and output voltage (Vout).

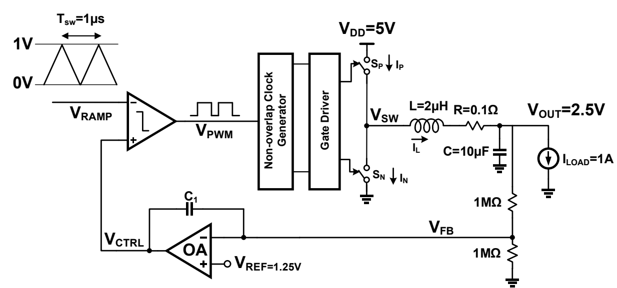


Figure 7: Circuit for Problem-7

Problem-8

Design the buck converter circuit shown in Figure 7 and its continuous time model in LTSpice.

a) Perform AC analysis and plot the loop gain magnitude and phase response of the continuous time model and verify your results found in Problem-7 (b). Observe and comment on the effect of varying capacitor (C_1) value on unity gain frequency (w_u) and gain margin. Use enough points per decade in your AC simulation to get the correct value of Q_O due to LC resonance.
b) Perform transient analysis and plot waveforms V_{CTRL} and V_{OUT} of buck converter and corresponding signals in its continuous time mode on the same graph. Verify that V_{CTRL} and V_{OUT} of the buck converter have the average value as of its continuous time model. Comment on the difference if observed any. Use initial condition V_{OUT}=0 in your transient simulation. Verify your results found in Problem 7 (c), (d) and (e).

Problem-1

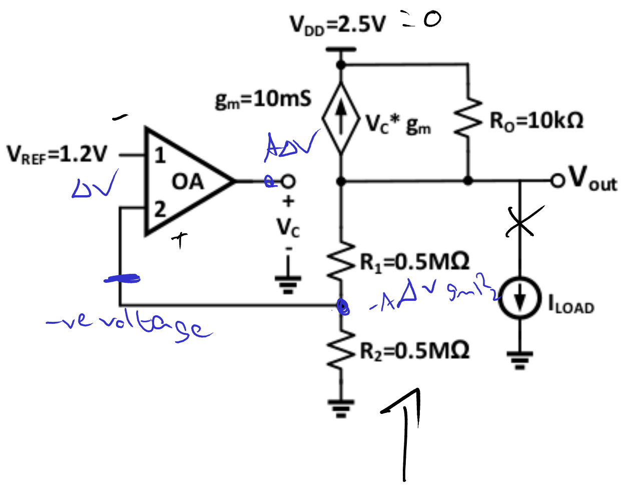


Figure 1: Circuit for Problem-1

a) Since for less voltage, terminal 2 V+ is -ve, $\boxed{1 \text{ is +ve}}$

$\boxed{1 \text{ is -ve, } 2 \text{ is +ve}}$

Figure 1 shows a linear regulator. Assuming op-amp OA is ideal:

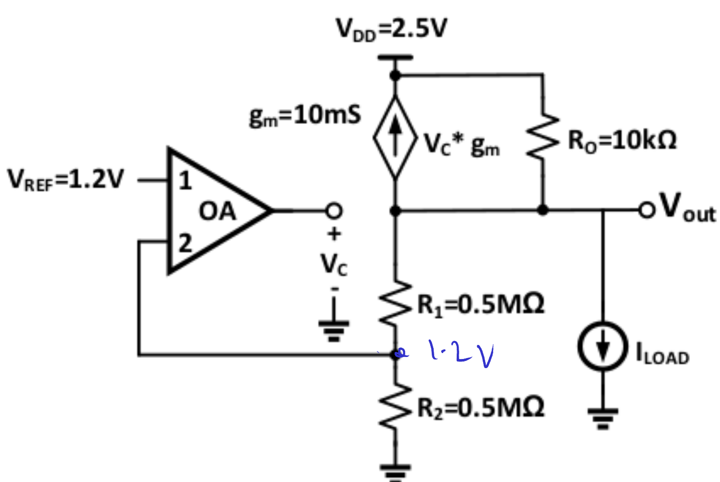
a) Determine the polarity of input terminals 1 & 2 of the op-amp for negative feedback operation.

b) Find the output voltage Vout.

c) Find the minimum and maximum value of V_C if I_{LOAD} varies from 1mA to 10mA.

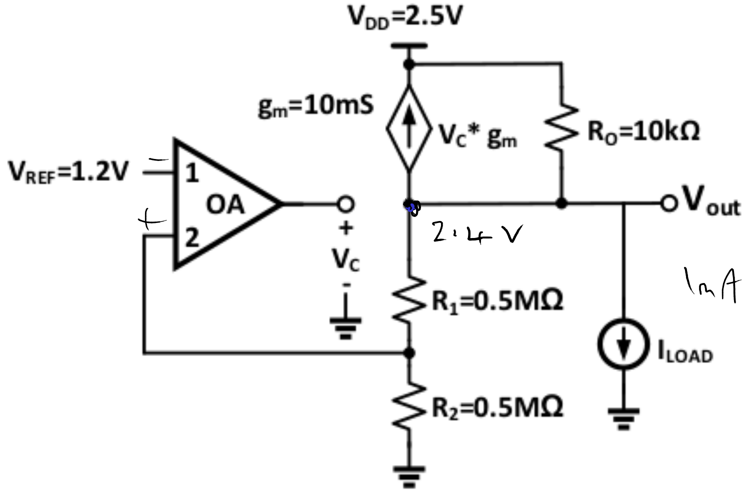
d) Find the error in output voltage if OA is replaced with an op-amp of gain = 100 and R_{LOAD}=

b)



$\boxed{2.4\text{ V}}$

c) V_{min}



Doing KCL,

$$\cancel{\frac{2.4}{1M\Omega}}^{0} + 1mA + \left(\frac{2.4-2.5}{10k\Omega}\right) + g_m v_C = 0$$

$$1mA - \frac{0.1}{10^4} + g_m v_C = 0$$

$$99 \times 10^{-5} = -g_m V_C$$

$$v_C = \frac{-99\times10^{-5}}{10^{-2}}$$

$$= -99\times10^{-3} = \boxed{-0.099V}$$

Max

$$10mA - \frac{0.1}{10^4} + g_m v_C = 0 \qquad V_C = -0.999V$$

d) Find the error in output voltage if OA is replaced with an op-amp of gain = 100 and $R_{LOAD}= \infty$

$$V_C = \left(\frac{V_{out}}{2} - 1.2\right)100 \qquad V_C g_m + \frac{V_{out}-2.5}{R_O} + 0 + \cancel{I_{Load}} = 0$$

$$\frac{V_{out}}{2} - 1.2 + \frac{V_{out}-2.5}{10k} + \cancel{I_{Load}} = 0$$

$$V_{out}\left[\frac{1}{2} + \frac{1}{10k}\right] = 1.2$$

$$\Delta V = 2.4 - \frac{1.2}{\frac{1}{2}+\frac{1}{10k}} = \boxed{0.00047V}$$

Problem-2

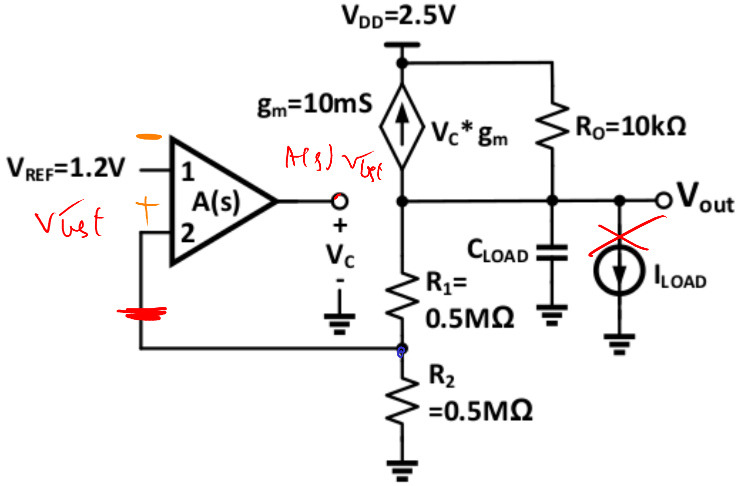


Figure 2: Circuit for Problem-2

Figure 2 shows the linear regulator of Figure 1 with a real 2-stage compensated op-amp having transfer function:

$$A(s) = \frac{100}{(1+5x10^{-6}s)(1+5x10^{-8}s)}$$

a) Assuming op-amp pole as dominant, find the maximum value of the load capacitor, C_{LOAD} to maintain the phase margin > 45º. Support your answer with bode magnitude and phase plot.

b) Is it possible to use C_{LOAD} larger than the value found in (a) and still achieve a phase margin > 45º? Support your answer with bode magnitude and phase plot.

c) Determine the value of C_{LOAD} for which phase margin becomes 0º.

$V_c = A(s) V_{test}$

$\boxed{R = 1k\Omega}$

$V_{out} s C_{Load} + \frac{V_{out} - 0}{R_O} + \frac{V_{out}}{1 M\Omega} + V_c g_m = 0$

$V_{out}\left[s C_{Load} + \frac{1}{R} + \frac{1}{R_d} \right] = -g_m A(s) V_{test}$

$LL(s) = \frac{V_{out}/2}{V_{test}} = \frac{1}{2}\frac{-g_m A(s)}{\left(s C_{Load} + \cancel{\frac{1}{R}} + \frac{1}{R_o}\right)}$

$= \frac{-g_m 100 R_o A(s)}{2(s C_{Load} R_o + 1)}$

$= \frac{-1 \times \cancel{10^{-2}} \times \cancel{100} \times 10^4}{2\left(1+\frac{s}{2\times10^5}\right)\left(\frac{s}{P_o}+1\right)\left(1+\frac{s}{2\times10^7}\right)}$

$= \frac{5\times10^3}{\underbrace{\left(1+\frac{s}{2\times10^5}\right)}_{\text{Dom pole}}\left(1+\frac{s}{P_o}\right)\left(1+\frac{s}{2\times10^7}\right)}$

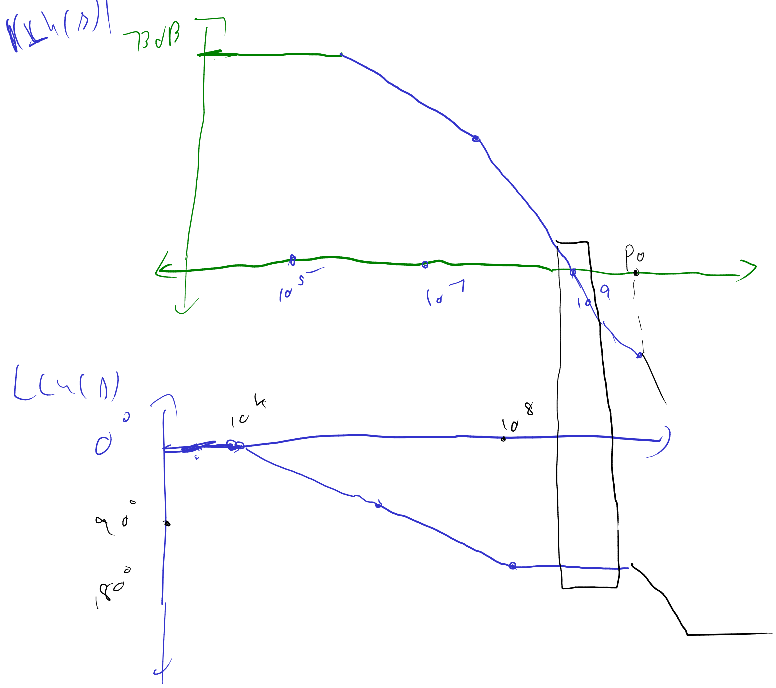
$\boxed{\omega_{ug} = p_o}$

$\omega_{ug} = 10^9 \text{ rads}^{-1}$

Now, $P.M = 45° = 180 - \underbrace{\tan^{-1}\frac{w_{ug}}{2\times10^5}}_{\simeq 90°} - \underbrace{\tan^{-1}\frac{w_{ug}}{2\times10^7}}_{\simeq 90°} - \underbrace{\tan^{-1}\frac{w_{ug}}{P_o}}$

$\Rightarrow \tan^{-1}\frac{w_{ug}}{P_o} \simeq -45°$ $\boxed{C_{Load} = -5\times10^{-16} F}$

$\Rightarrow$ C is -ve, so assumption is wrong



At w_{ug}, phase is 180°, so extra pole cannot bring phase to 135°

b) Is it possible to use C_{LOAD} larger than the value found in (a) and still achieve a phase margin > 45°? Support your answer with bode magnitude and phase plot.

If w_c pole is dominant pole, then P.M > 45° is achievable

If w_c is dominant pole, then $w_{ug} = p_1 = \boxed{2\times10^5 \text{ rad s}^{-1}}$

$$L(s) = \frac{5\times10^3}{\left(1+\frac{s}{2\times10^5}\right)\left(1+\frac{s}{p_o}\right)\left(1+\frac{s}{2\times10^7}\right)}$$

$$\frac{5\times10^3}{(\sqrt{2})(1)\,\frac{2\times10^5}{p_0}} = 1$$

$$5\times10^3 = \sqrt{2}\times\frac{2\times10^5}{p_0}$$

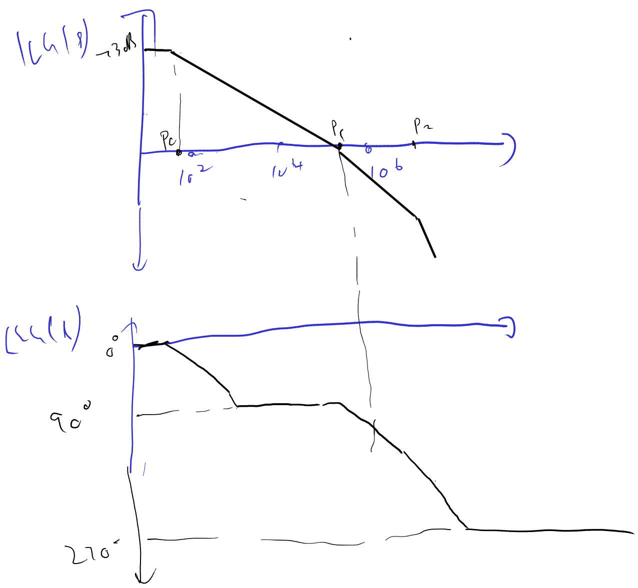
$$p_0 = \frac{\sqrt{2}\times2\times\cancel{10^5}^{100}}{5\times\cancel{10^3}} = \sqrt{2}\times2\times20$$

$$= \boxed{40\sqrt{2}\ \text{rads}^{-1}}$$

$$40\sqrt{2} = \frac{1}{C_{Load}\times R_0} = \frac{1}{C_{Load}\times10^4}$$

$$C_{Load} = \frac{1}{40\sqrt{2}\times10^4}\ \boxed{1.76\,\mu F}$$

For $C_{Load} > 1.76\,\mu F$, $PM > 45^\circ$



c) Determine the value of C_{LOAD} for which phase margin becomes 0º.

$P.M. = 0°$ $\Rightarrow$ $\omega_{ug} = 10 p_1 = \boxed{2 \times 10^6 \text{ rad s}^{-1}$}

$$LG(s) = \frac{5 \times 10^3}{\left(1 + \frac{s}{2 \times 10^5}\right)\left(1 + \frac{s}{p_0}\right)\left(1 + \frac{s}{2 \times 10^7}\right)}$$

$$1 = \frac{5 \times 10^3}{10 \times \frac{2 \times 10^6}{p_0}}$$

$$\frac{2 \times 10^7}{p_0} = 5 \times 10^3$$

$$p_0 = \frac{2 \times \cancel{10^7}^{\,10^4}}{5 \times \cancel{10^3}} = \boxed{4 \times 10^3 \text{ rad s}^{-1}}$$

$$= \frac{1}{10^4 C_{Load}}$$

$$C_{Load} = \frac{1}{10^4 \times 4 \times 10^3}$$

$$= \frac{1}{4 \times 10^7}$$

$$= 2.5 \times 10^{-8}$$

$$= \boxed{25\,nF}$$

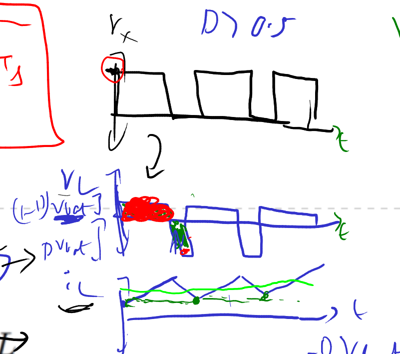
$(V_L)_{DC} = 0$

$(i_L)_{DC} = \frac{D V_{bat}}{R}$

$(i_c)_{DC} = 0$

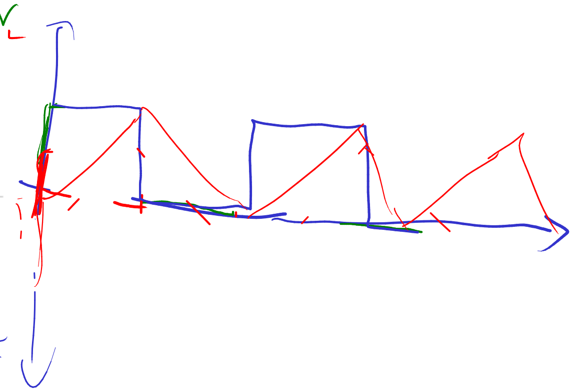
$\boxed{\frac{1}{L}(1-D)V_{bat} D T_s = \Delta i}$

$D > 0.5$



$\Delta V = \frac{\frac{1}{2}\left(\frac{\Delta i}{2}\right)\frac{T}{2}}{C}$

$= \frac{1}{LC}[\quad]$



Problem-5

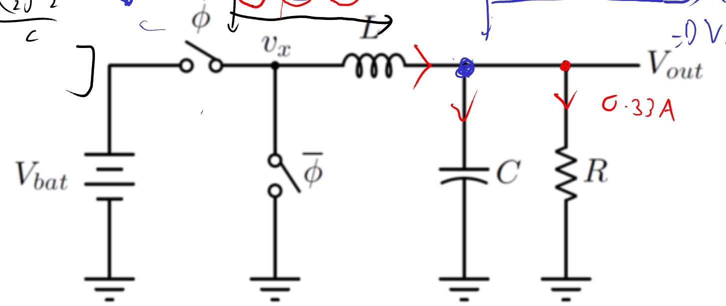


Figure 5: Circuit for Problem-5

Figure 5 shows a buck converter. The battery voltage *Vbat* is 5V. ϕ and $\bar{\phi}$ are complementary switch drive signals. The duty cycle of ϕ is denoted by D. The switching frequency is 1.5 MHz. $L = 2.2\,\mu$H and $C = 22$ µF. The load resistor $R = 10\Omega$.

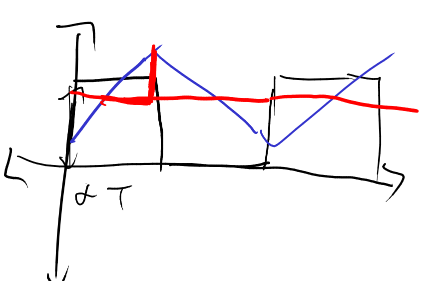
a) Determine D needed to achieve *Vout* = [illegible]V. 3.3 V
b) Determine the transfer function from *vx* to *Vout*.
c) Using the observation that the pole frequency of the LC filter is much lower than the switching frequency, determine the ripple in the inductor current and output voltage.
d) Sketch the current waveforms in the inductor and capacitor in steady state.
e) Sketch the voltage waveform *Vout* in steady state.

a) $\phi = \frac{3.3}{5} = \boxed{66\%}$

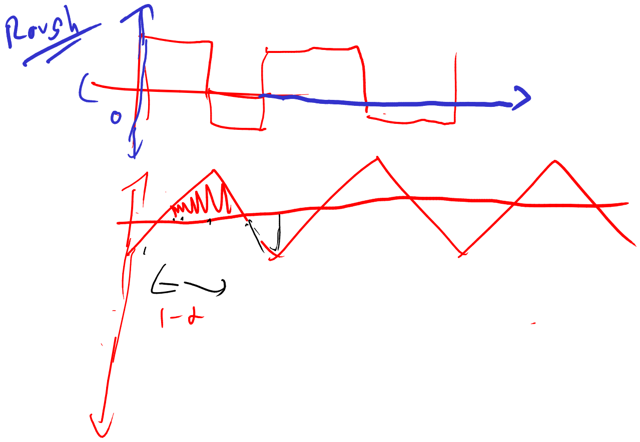
b) $$V_{out} = \frac{R \parallel \frac{1}{sC}}{R \parallel \frac{1}{sC} + sL} = \frac{\frac{R}{RsC+1}}{\frac{R}{RsC+1} + sL} = \boxed{\frac{R}{R + s^2 RLC + sL}} = \frac{1}{s^2 LC + \frac{sL}{R} + 1}$$

c) $$\omega_n = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{22 \times 2.2 \times 10^{-12}}} = \frac{0.14}{10^{-6}} = \boxed{1.43 \times 10^{5}\ \text{rads}^{-1}}$$

d)



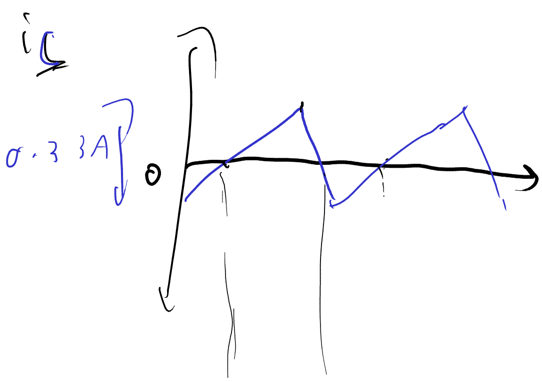
$$i_{ripple} = \frac{1}{L}\int v\,dt = \frac{1}{L}(V_s - V_o)T_{on}$$

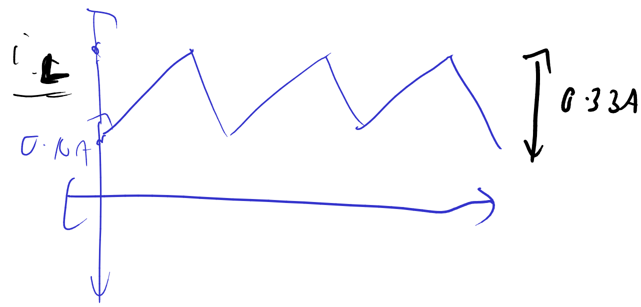


$$= \frac{1}{L}(1-\alpha) V_{bat}\, \alpha T = 0.33\,A$$

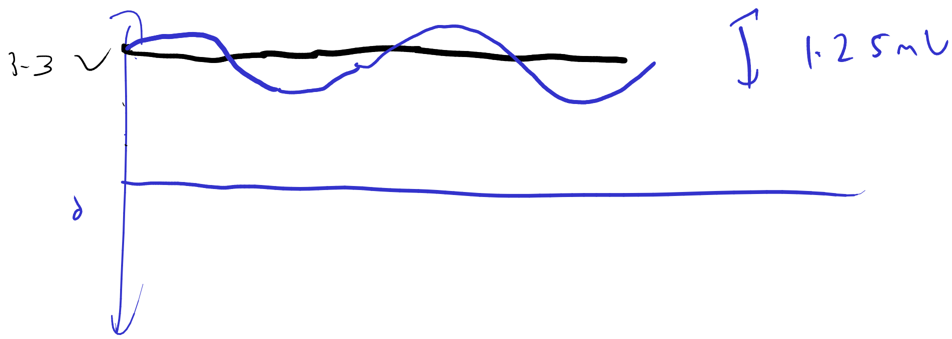
$$V_C = \frac{1}{C}\int i\,dt$$

$$= \frac{1}{C}\left(\frac{1}{2}\right)\left(\frac{T}{2}\right)\frac{\Delta i}{2} = 1.25\,mV$$



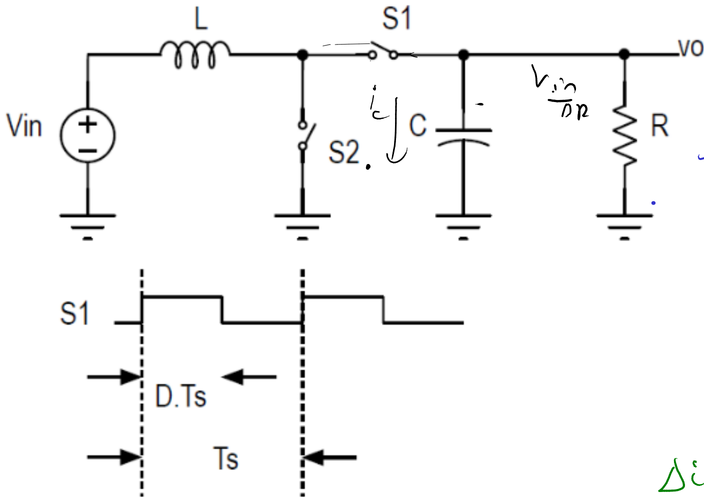


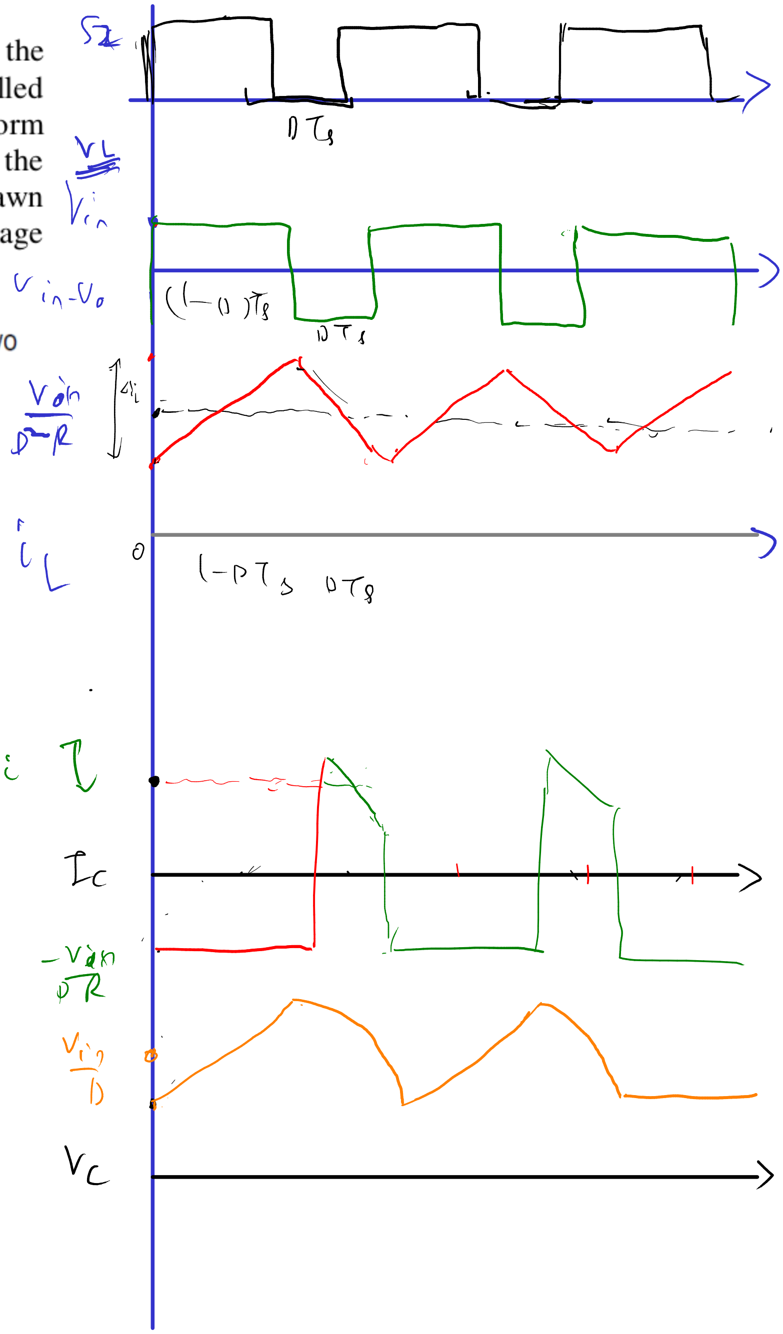
e)



Problem-6

As usual, the switching period T_s is much smaller than the time-constant of the LC network. S1 and S2 are controlled by complementary waveforms, and the waveform controlling S1 is shown in the figure. Determine the average output voltage v_o, and the average current drawn from the source. Draw the steady state current and voltage waveforms through/across the inductor and capacitor.





$$(V_{in}-V_o)\, D\, \cancel{T_s} = -V_{in}(1-D)\cancel{T_s}$$

$$-V_o D = -V_{in}$$

$$\boxed{V_o = \frac{V_{in}}{D}}$$

$$\boxed{\Delta i = \frac{V_{in}(1-D)T_s}{L}}$$

$$\Delta V_{out} = \boxed{\frac{-V_{in}(1-D)T_s}{D \cdot R\, C}}$$

$$(i_{avg})\, D = \frac{+V_{in}(1-D)}{D\, R}$$

$$i_{avg} = \boxed{\frac{+V_{in}(1-D)}{D^2 R}}$$

Problem-7

Figure 7 shows the circuit diagram of a type-I (integral) compensated buck converter with output voltage, Vout regulated at 2.5V for input supply, V_{DD}=5V and load current, I_{LOAD}=1A. . Assuming switches S_P and S_N are ideal.

a) Model the buck converter in continuous time domain and find the small signal loop gain transfer function.

b) Determine the value of capacitor C_1 to achieve the gain margin of > 20dB and draw the bode magnitude and phase plot.

c) Find the value of control voltage, V_{CTRL} and duty cycle, D to regulate the output voltage at 2.5V.

d) Find the value of peak to peak inductor ripple current and peak-to-peak output ripple voltage.

e) Draw the steady state waveforms for PWM voltage (V_{PWM}), switch currents (I_P and I_N), inductor current (I_L) and output voltage (Vout).

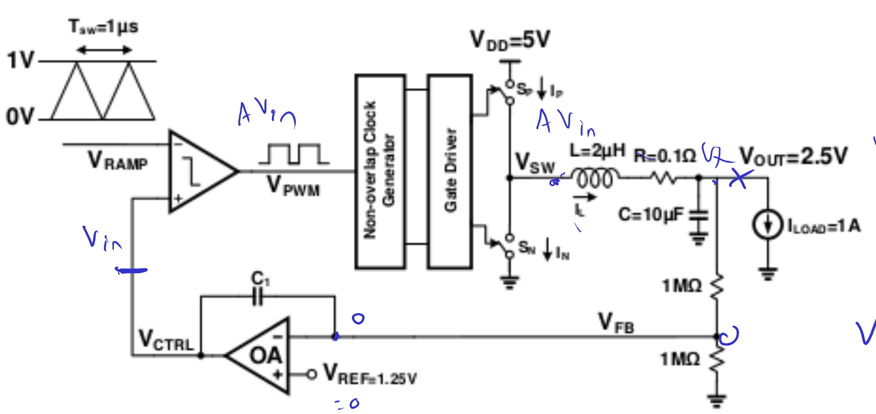


Figure 7: Circuit for Problem-7

V_x

$$\frac{A V_{in} \frac{1}{sC}}{\frac{1}{sC} + sL + R}$$

$$V_x = \frac{A V_{in}}{1 + s^2 LC + RsC}$$

$$V_{FB}\, sC_1 = -\frac{V_x}{R_1}$$

$$\boxed{LL(s) = \frac{V_{FB}}{V_{in}} = \frac{-1 \cdot 5}{(R_1 s C_1)(1 + s^2 LC + RsC)}}$$

$$= \frac{-5}{(sR_1C_1)(1 + s^2\, 2\times10^{-11} + s\, 10^{-6})}$$

b)

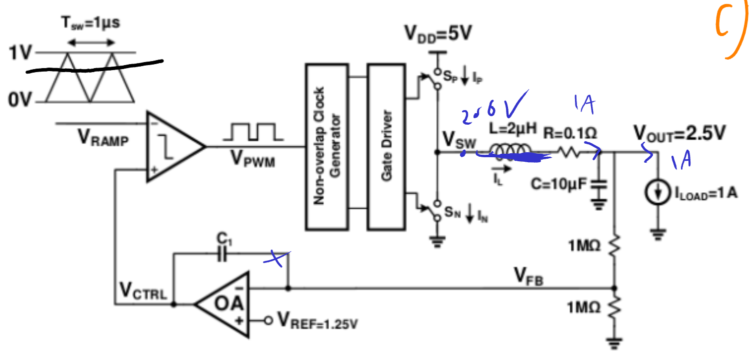
$$\angle LL(s) = -90 - \angle\left((1 - \omega^2\, 2\times10^{-11}) + j\omega\, 10^{-6}\right) = -180$$

$$\omega_{-180}^2 = \frac{1}{2\times10^{-11}}, \quad \omega_{-180} = \sqrt{2.24\times10^5 \text{ rads}^{-1}}$$

$G.M = |L(\omega_{-180})| = \dfrac{5}{2.26\times10^{5}\times10^{-6}\,(C)\,2.26\times10^{5}\times10^{-6}} = 10^{-4}$

$10^{-1}C = \dfrac{5}{5\times10^{10}}$

$C = 10^{-9} = \boxed{1nF}$



c) $5D = 2.6$

$D = \boxed{52\%}$

$V_{ctrl} = \boxed{0.52\,V}$

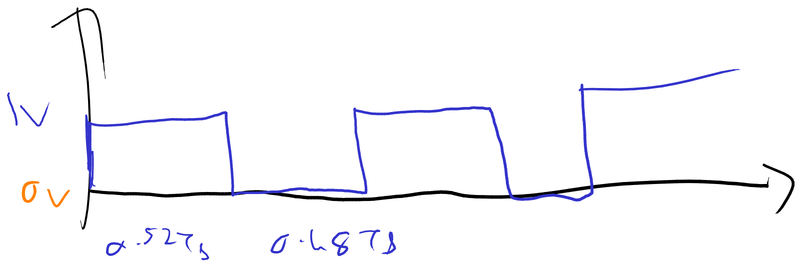
Figure 7: Circuit for Problem-7

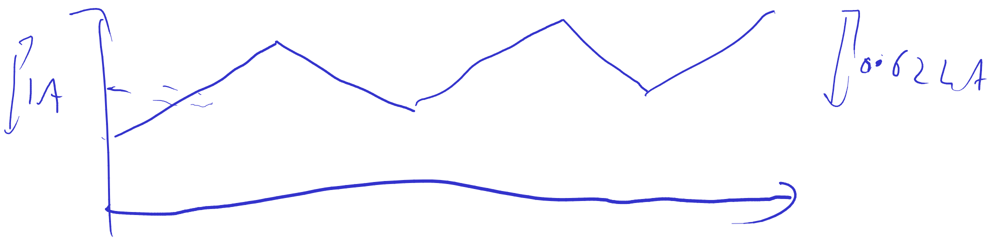
d) Find the value of peak to peak inductor ripple current and peak-to-peak output ripple voltage.

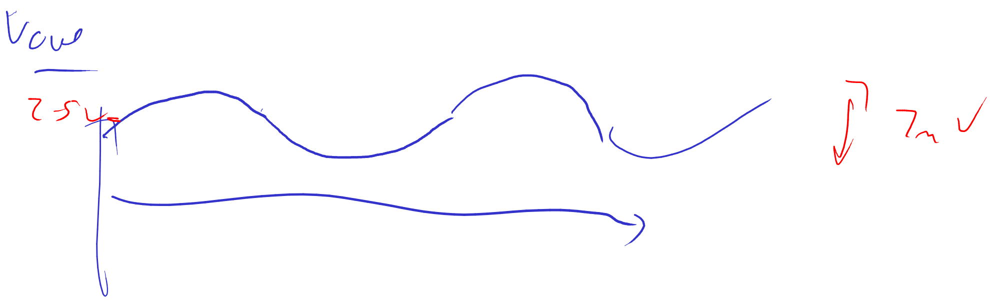
$\dfrac{(1-D)V_s\,(DT_s)}{L} = \dfrac{0.52\times0.48\times5\times10^{-6}}{2\times10^{-6}} = \boxed{0.624A}$

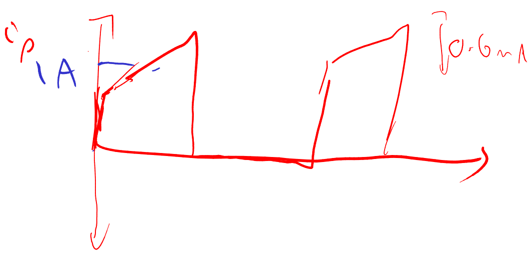
$\dfrac{\Delta i_L\,T_s}{8C} = \boxed{7.8\,mV}$

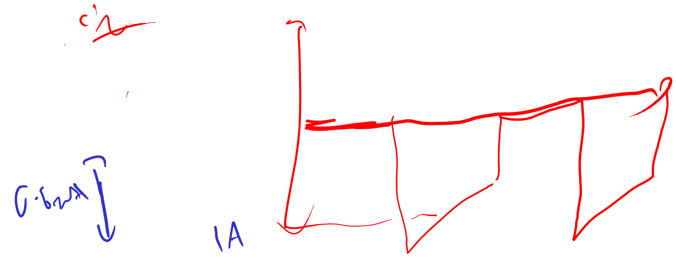
e) Draw the steady state waveforms for PWM voltage (V_{PWM}), switch currents (I_P and I_N), inductor current (I_L) and output voltage (Vout).


1V
0V
0.52Ts
0.48Ts


1A
0.624A

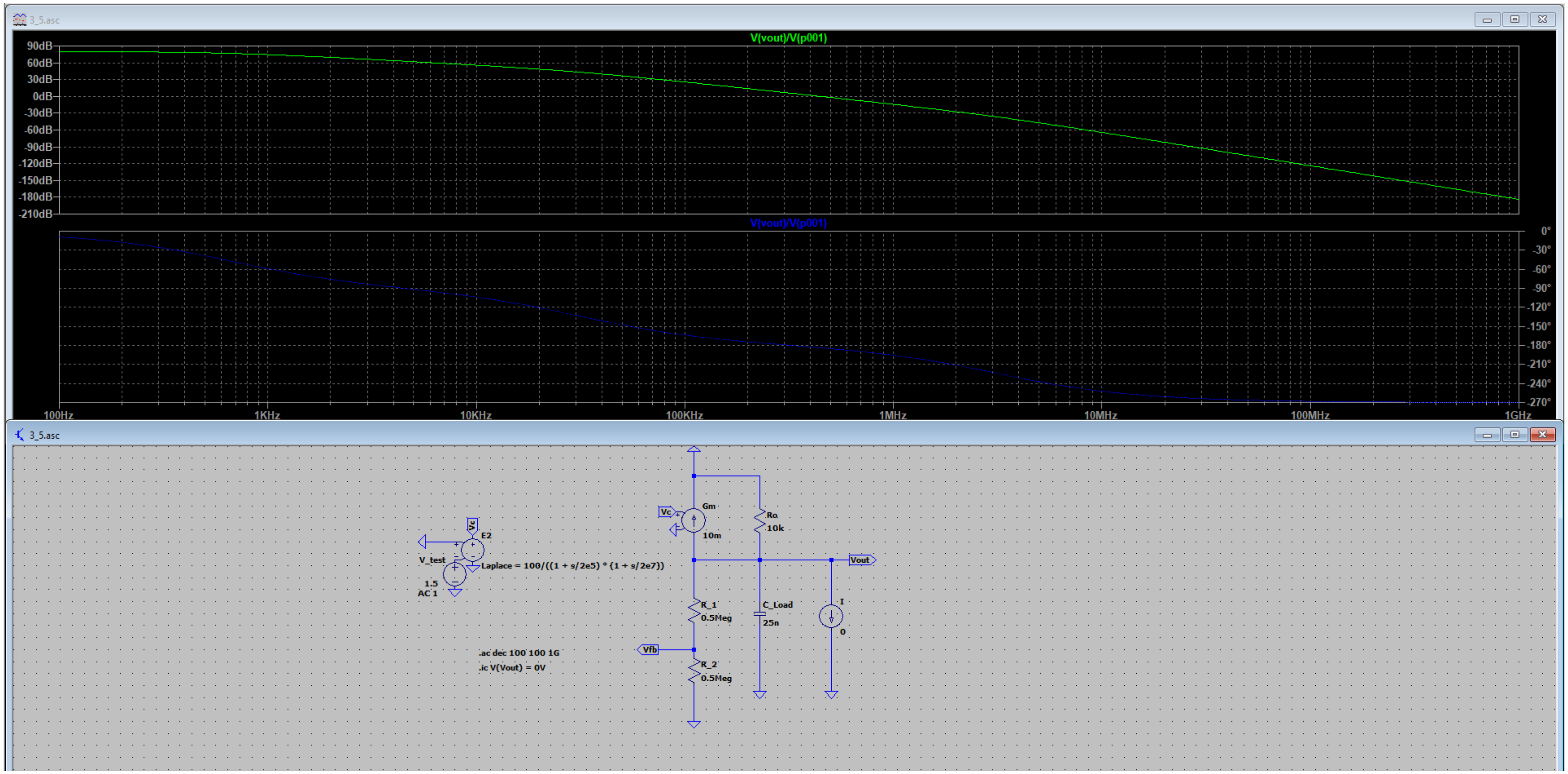

Vout
2.5V
7mV


ip
1A
0.6mA


0.6mA
1A

Problem 3

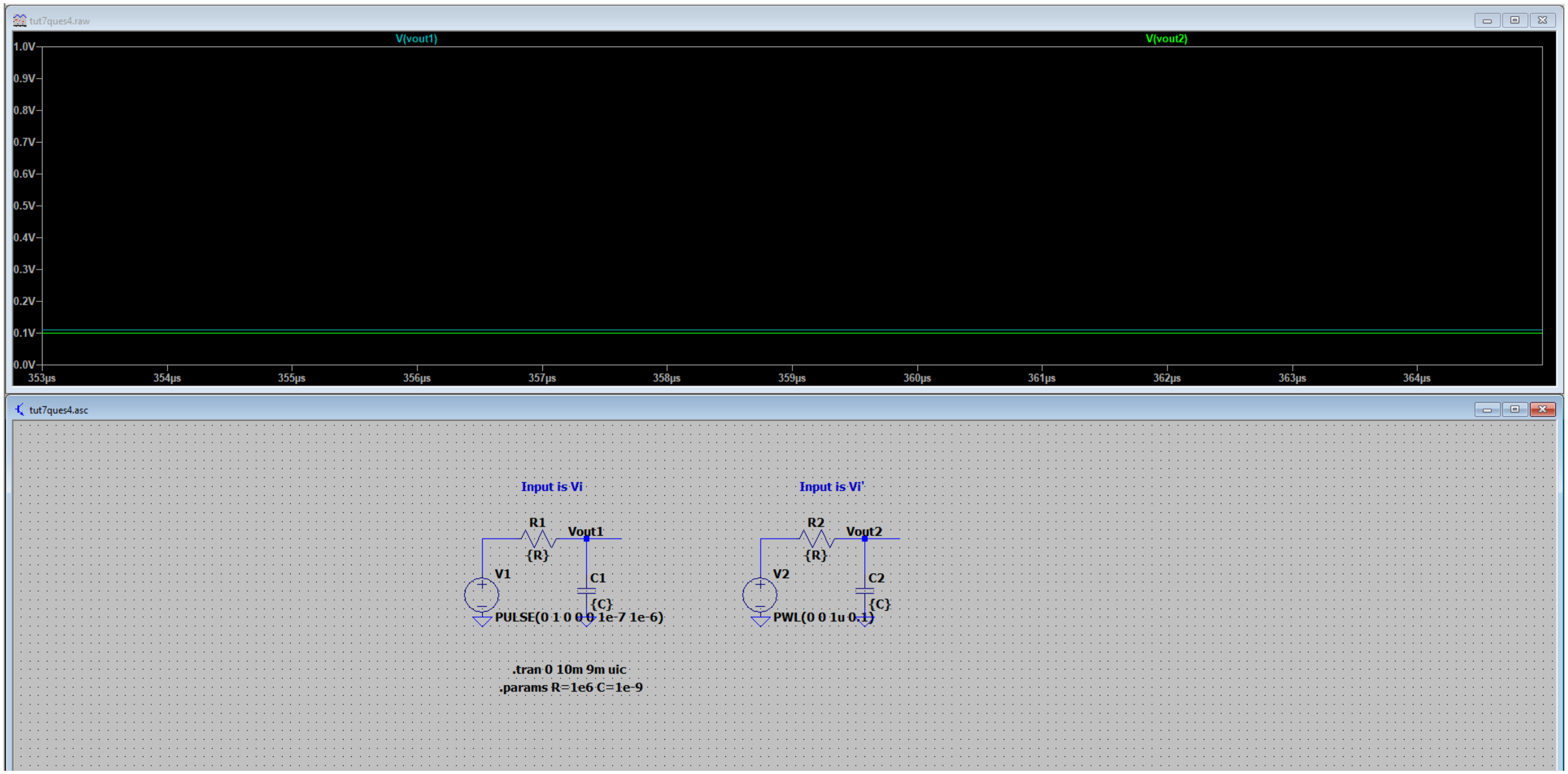
Problem 2 circuit is simulated below. Below simulation is for the loop gain. As calculated theoretically, 2.5 nF yields a phase margin of 0, so simulation matches theoretical prediction.



Problem 4

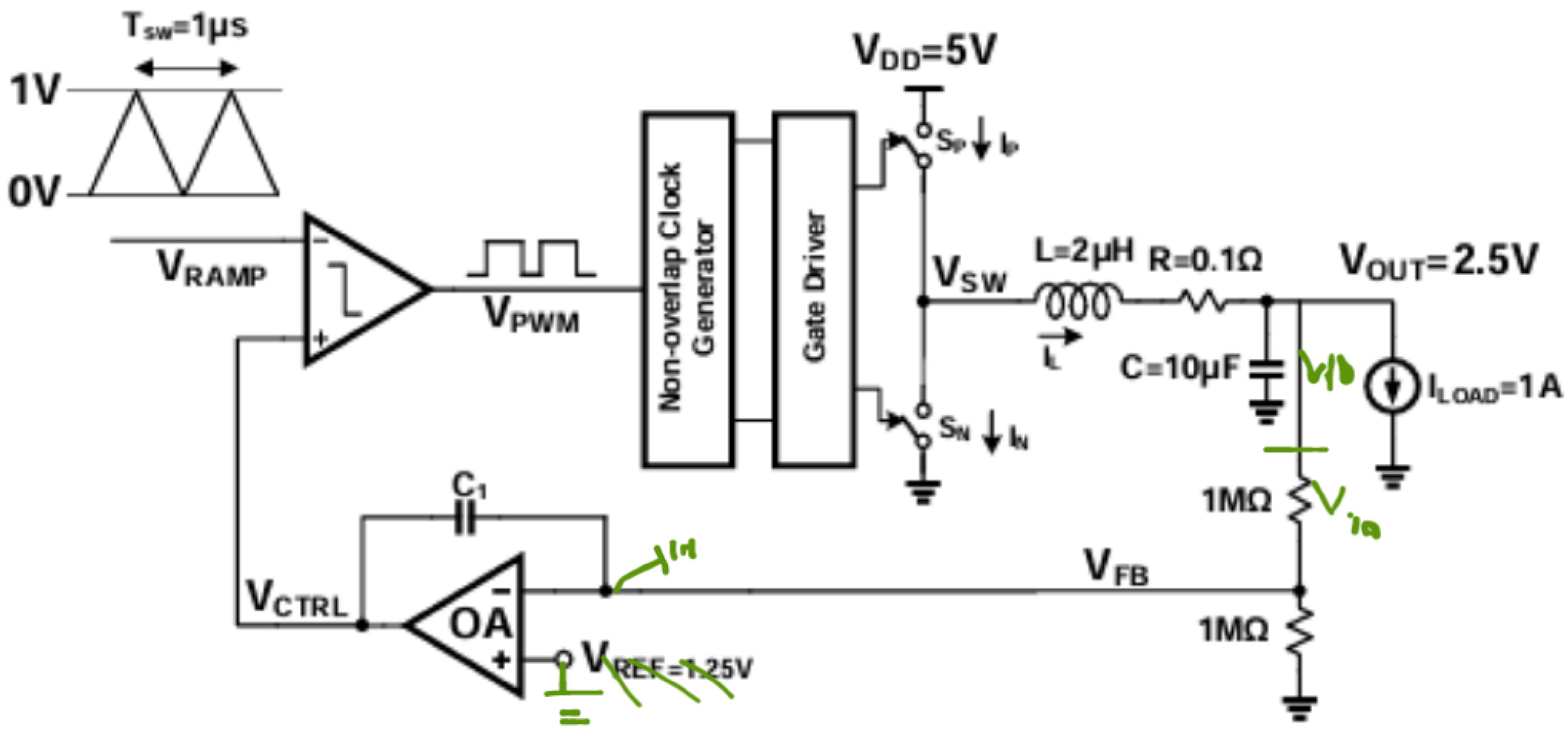
Vout1 is the output when input is vi
Vout2 is the output when input is vi’

Response of slow LTI system to vi is similar to vi’. Clearly, it is close to 0.1V in both cases.



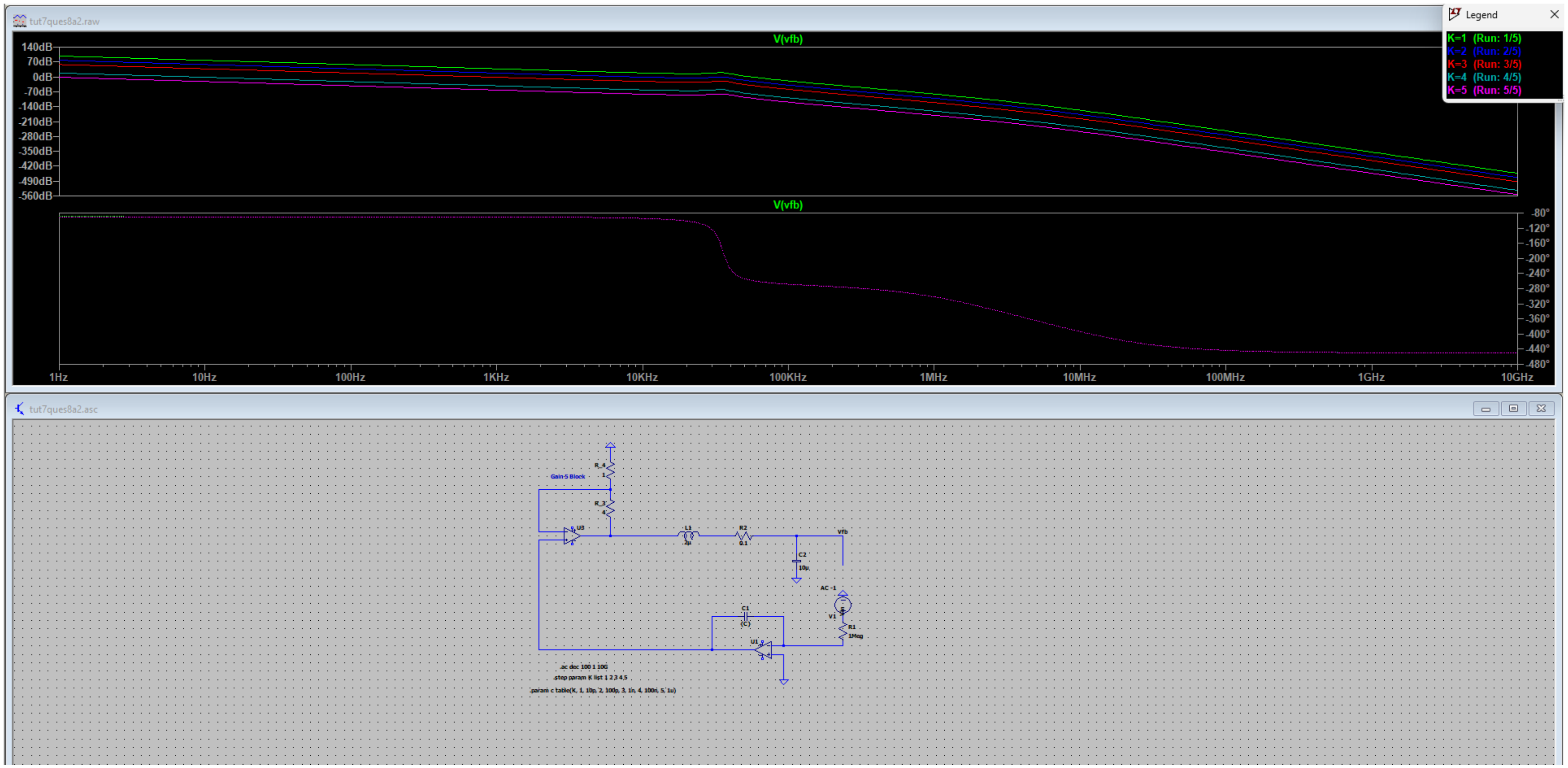
Problem 8

Below is the loop gain equation, where VDD = 0, Vref = 0, Iload = 0.

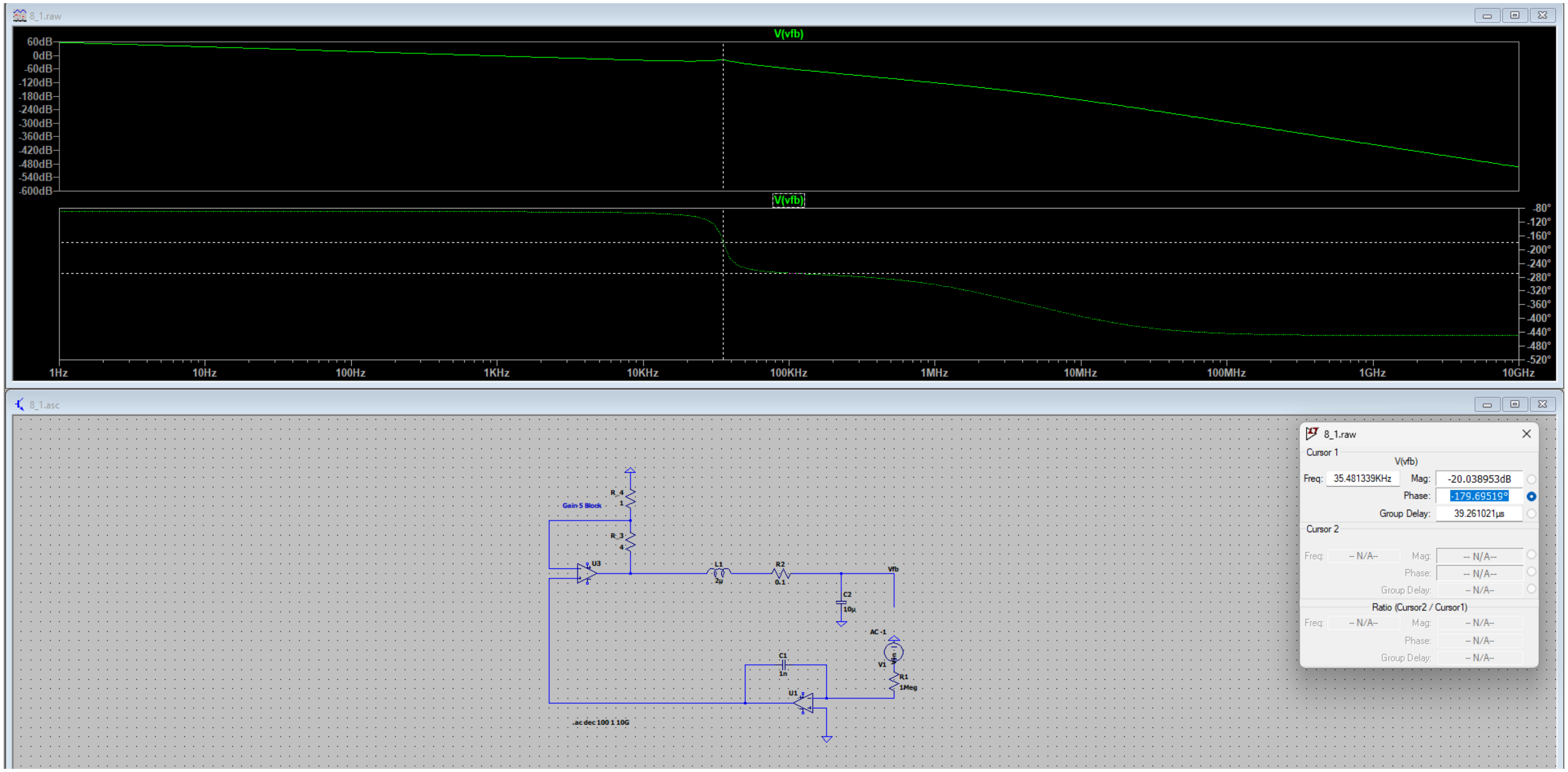


Problem 8 a)

Below is AC analysis for a range of Capacitor Values, 10p, 100p, 1n, 100n, 1u



Below is AC analysis at 1n, which achieves gain margin 20dB.



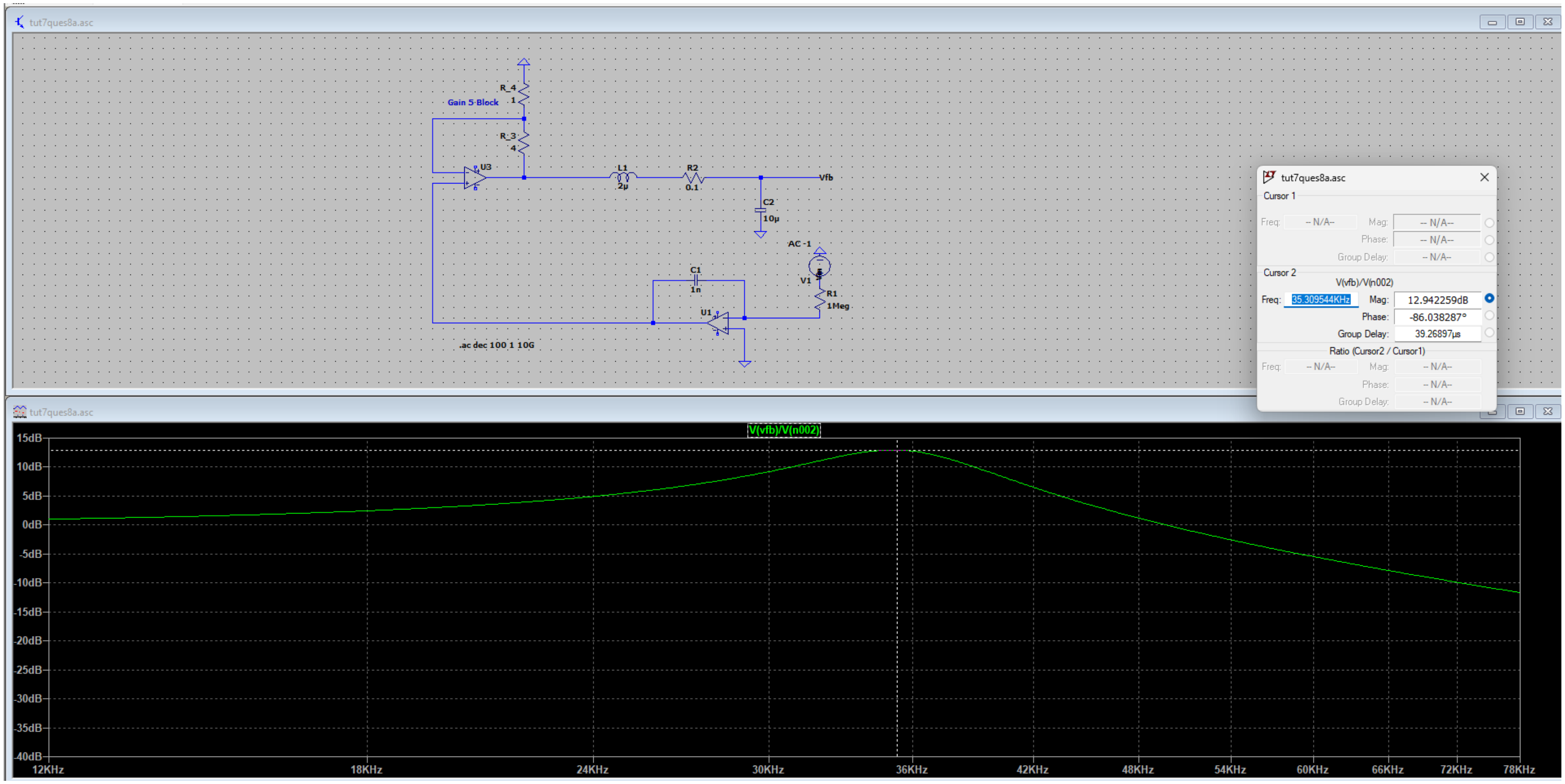
<u>Calculation of Q</u>

wn is natural frequency.

Consider the Transfer function of just the RLC circuit. There, the Gain is approximately 13dB. Now, Gain at w = wn is Q.

So, 20 * log10(Q) = 13.

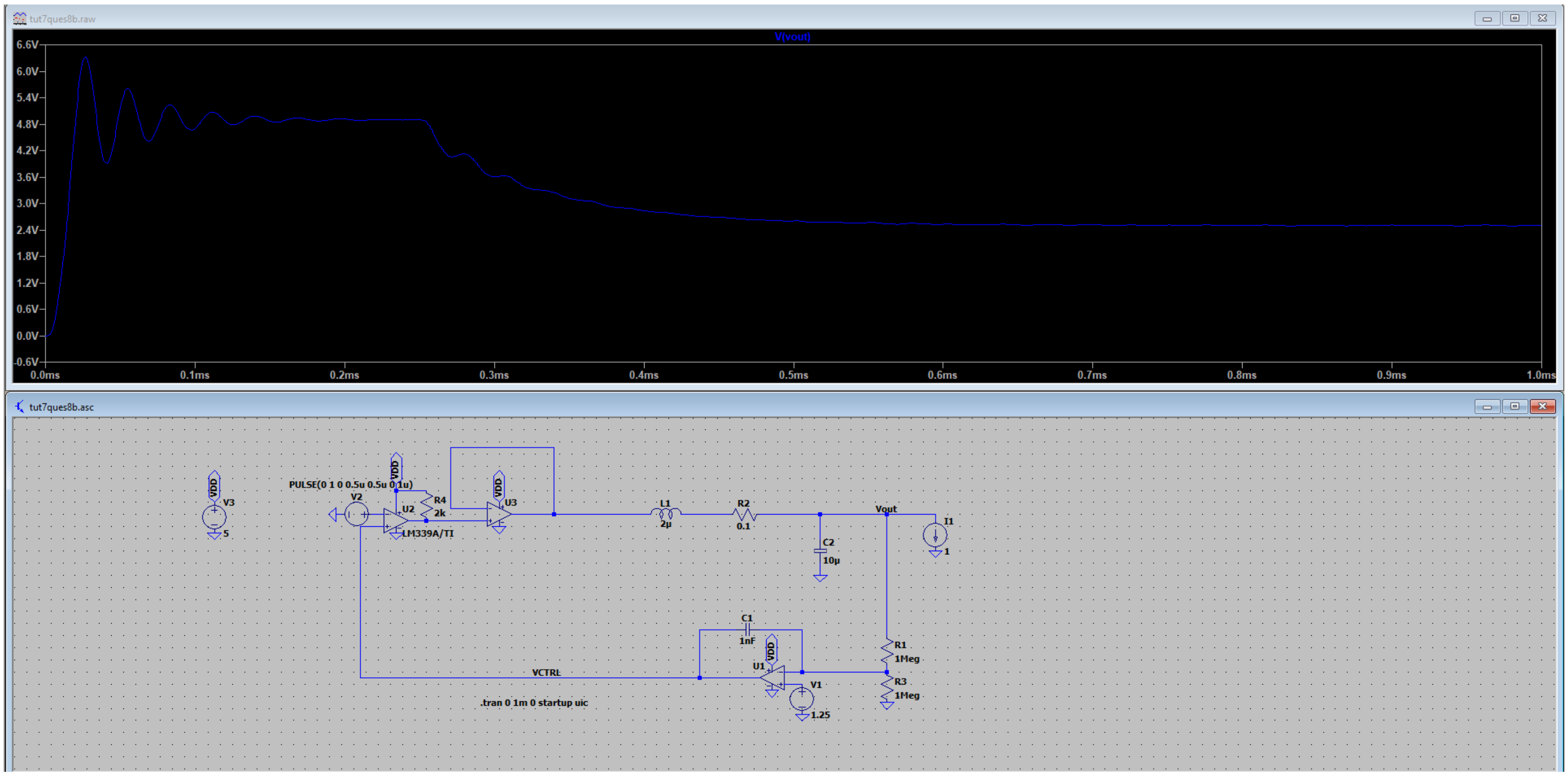
Therefore, **Q = 4.46**, which matches with theoretical calculations.



‘

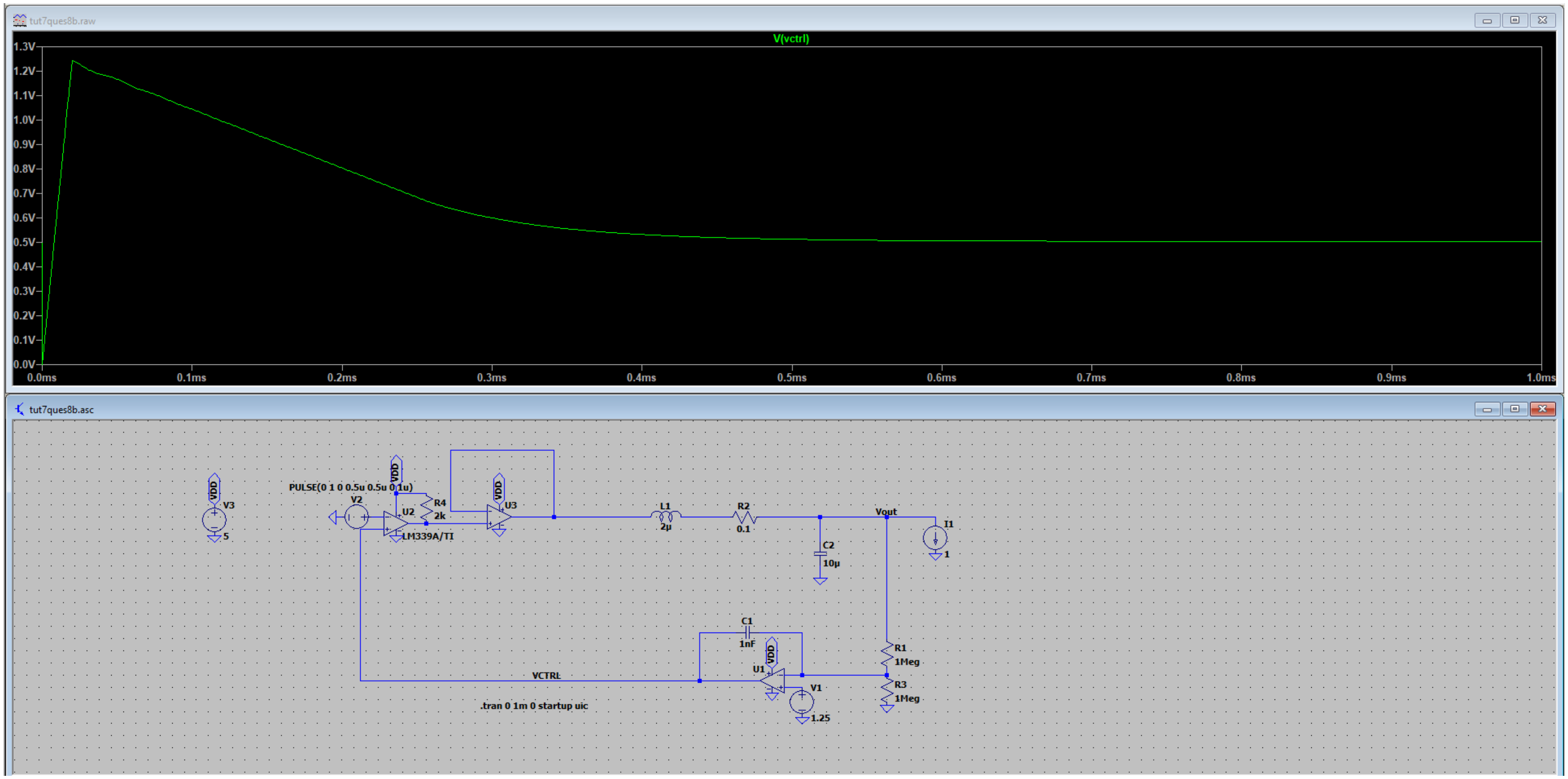
Problem 8 b)

Vout



We can observe that Vout has some initial condition, but finally settles down to 2.5 V as expected.

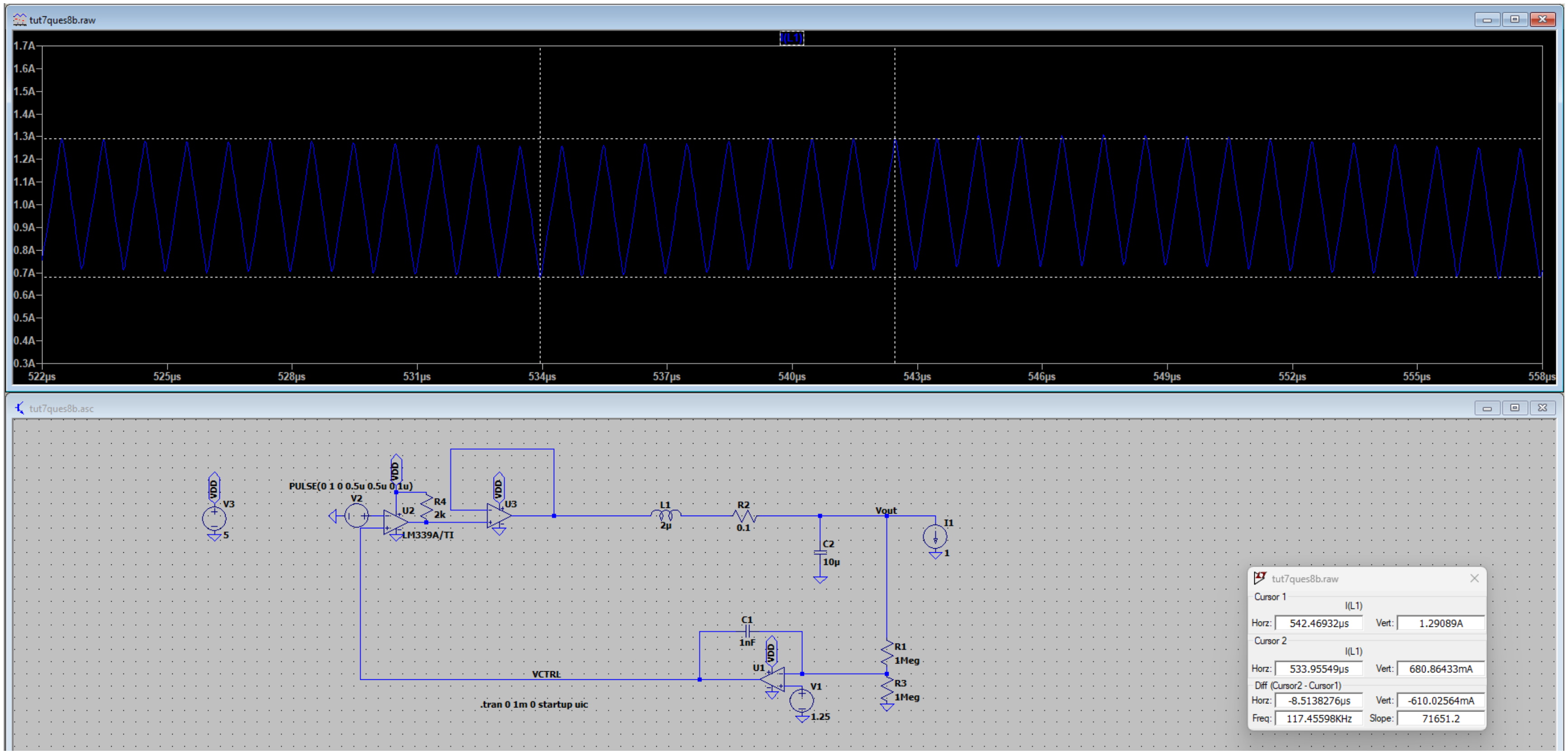
VCTRL



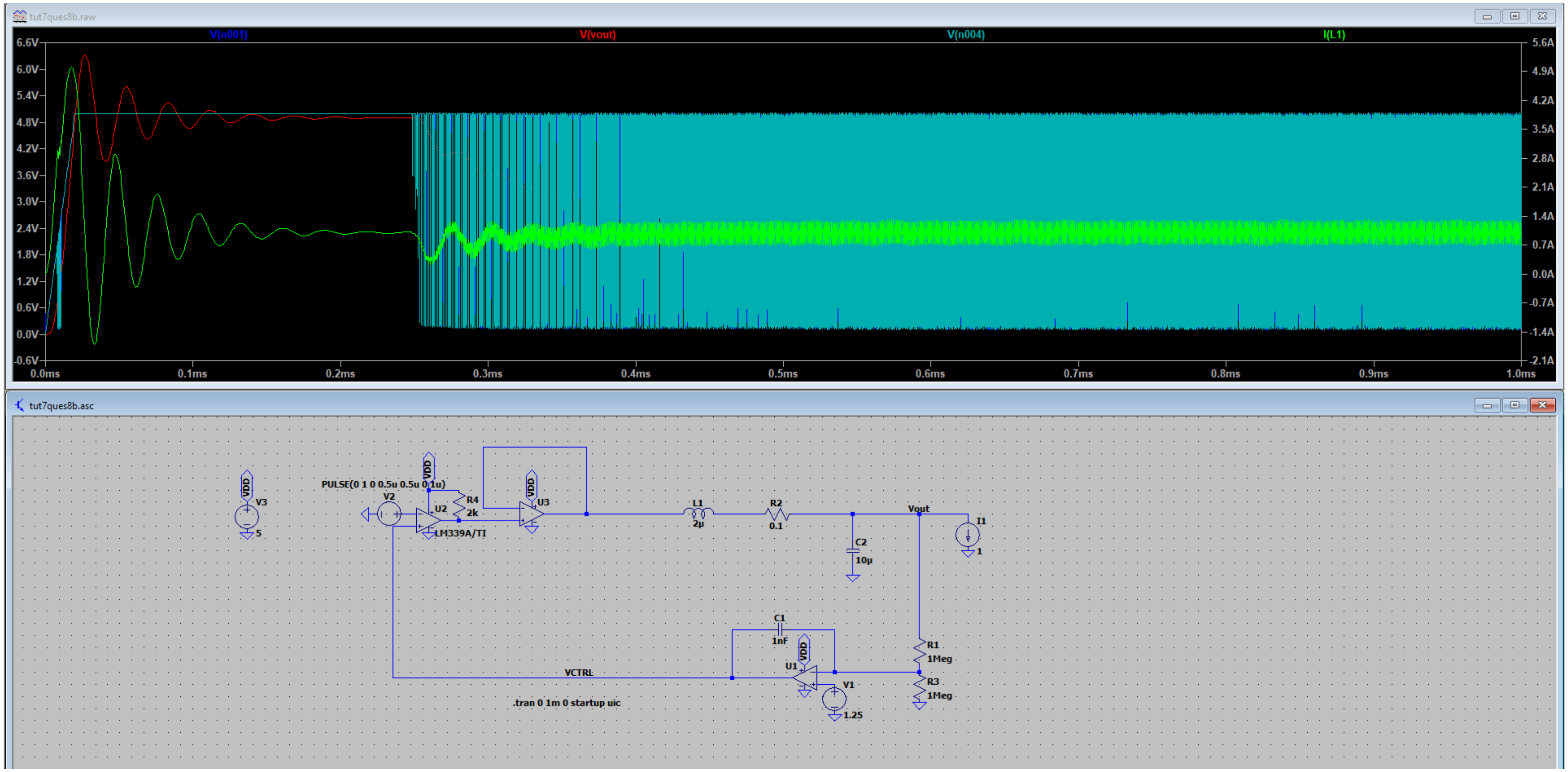
VCTRL also has some initial values, but settles down to 0.52V, as expected by theoretical calculation.

<u>Explanation:</u> c) As calculated theoretically, VCtrl = 0.52 V, Duty cycle is 0.52

d) Peak to Peak inductor ripple



Ripple current is found to be 1.29 A - 0.68 A = 0.6 A, which is similar to theoretical value e)



Theoretical predictions match with simulated values