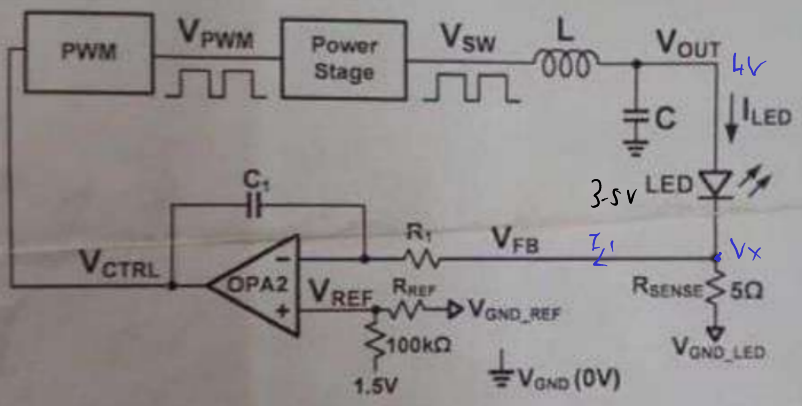
tion-4 (2 marks)

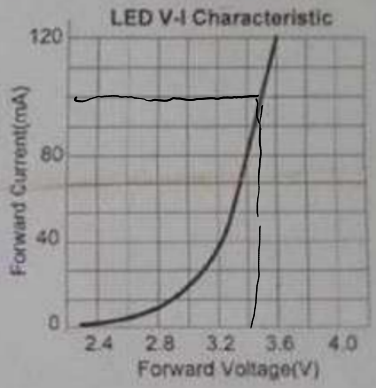
A bandpass filter was theoretically designed to operate at center frequency of 1kHz. When implemented on hardware, the center frequency was off from 1kHz due to tolerance in resistance and capacitance. How will you find the exact value of the center frequency without knowing or measuring the resistor and capacitor values?

Choose 1kHz freq, then measure V_{pp} at nearby frequencies. Change knob by at most $\frac{BW}{2}$, & smaller intervals

Question-3 (7 marks)

LED driver below was designed for the LED of V-I characteristic shown the figure.





a) Find the value of R_{REF} and V_{OUT} for the LED current (I_{LED}) of 100mA. Assume $V_{GND\_REF} = V_{GND\_LED} = 0V$ (3 marks)

b) Which of the following two resistors are most suitable to be used for R_{SENSE} and why? (2 marks)

Resistor Name	Resistance	Tolerance/Error	Maximum Power Rating
Resistor-A	5Ω	± 1%	60mW
Resistor-B	5Ω	± 0.5%	30mW

c) Suppose V_{GND} is the clean ground (0V) closer to reference ground (V_{GND_REF}) while LED ground (V_{GND_LED}) is not guaranteed to be 0V due to parasitic resistance. Which of two grounds (V_{GND} or V_{GND_LED}) should V_{GND_REF} be connected and why? (2 marks)

a) Assume $I_1 = 0$

$V_x = I_{LED} \times 5\Omega =$ **0.5V**

$V_{out} =$ **4V**

$V_{ref} = 0.5V$ $\Rightarrow$ $R_{ref} =$ **50k**

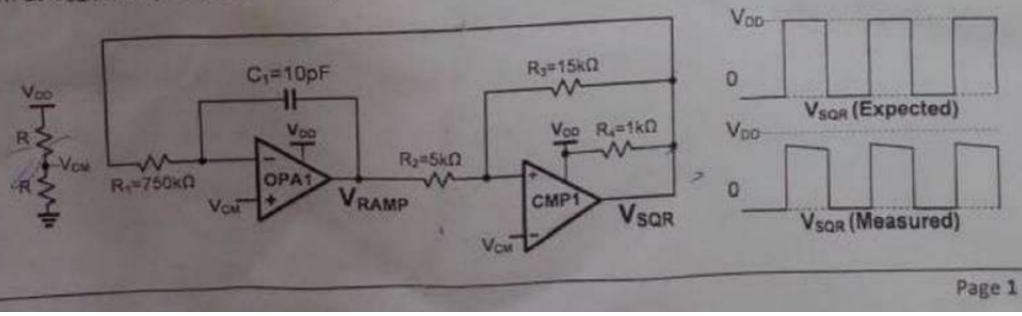
b) 100mA × 0.5V = 50mW

Use A

c) Vgnd-led

Question-2 (6 marks)

Following ramp generator was designed to operate at frequency of 100kHz with resistor and capacitor values as mentioned in the figure. Comparator CMP1 is an open drain/collector hence requires pull-up resistor R_4. Output waveform at V_{SQR} is expected to be a square wave of amplitude V_{DD}.



a) When measured on oscilloscope, the actual waveform at V_{SQR} had an amplitude lower than V_{DD} as shown in the figure. What could be the possible reason for attenuation in the amplitude and what are the two possible ways to fix this? (3 marks)

b) If resistor and capacitor values mentioned in the figure were selected at V_{DD}=5V, what would be the impact on ramp frequency and ramp amplitude when V_{DD} is reduced to 4V? (2 marks)

c) When measured on oscilloscope, it was observed that ramp frequency was not 100kHz but lower. What could be the possible reasons? (1 mark)

a)

- Pull up resistor draws current
- Due to slew rate of op amp

Fixes:

- Changing cap value until we get a square wave

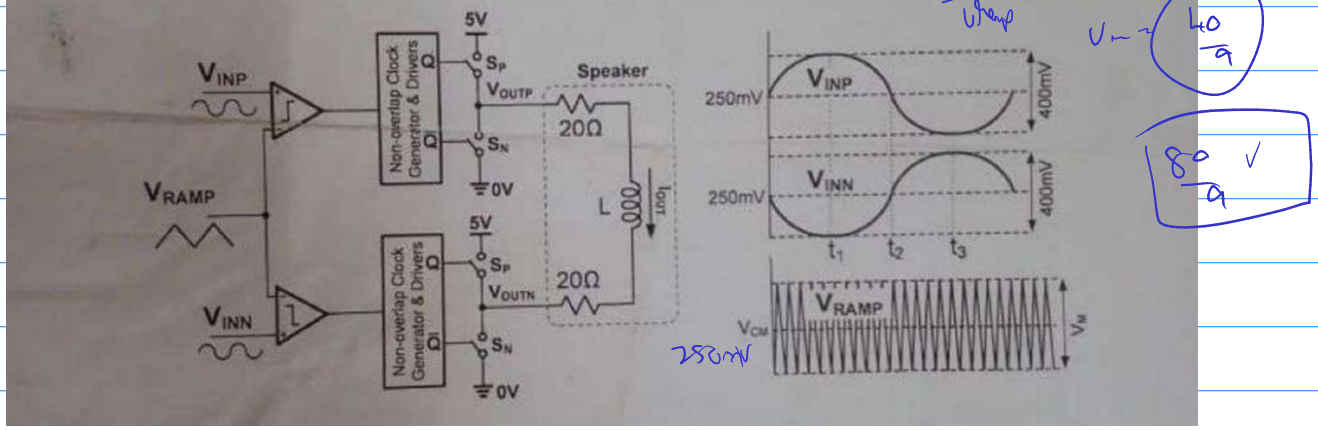
b) It will just be a ramp with Vpp lower. The slope (due to slew rate) of Vsqr will be lesser in magnitude

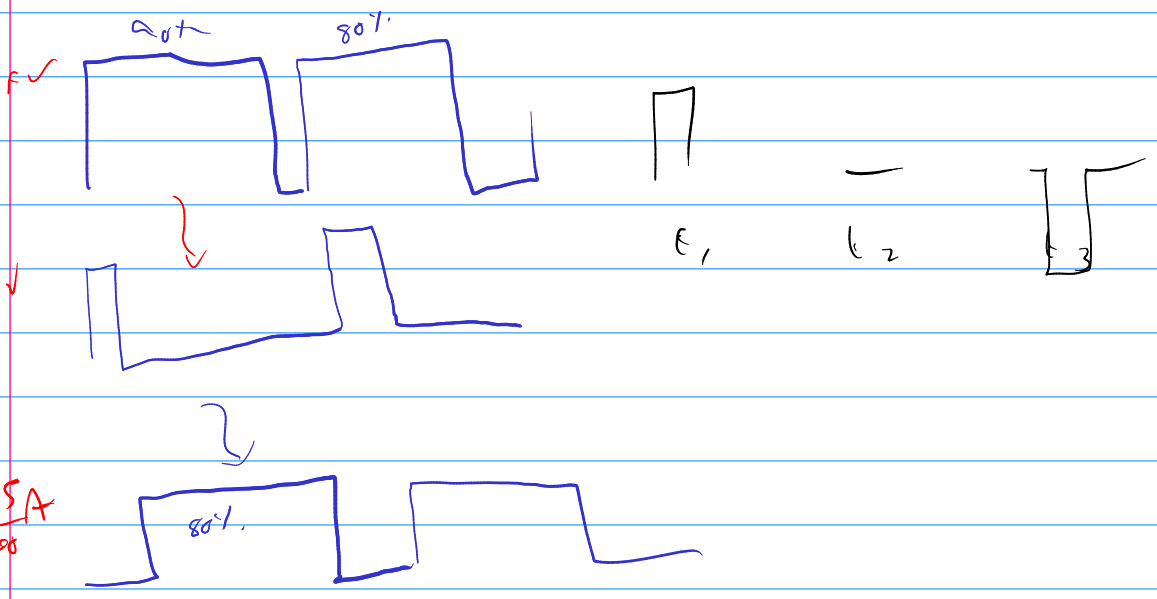
c) Cap could have some error, Cap can have parasitic resistance

Question-1 (15 marks)

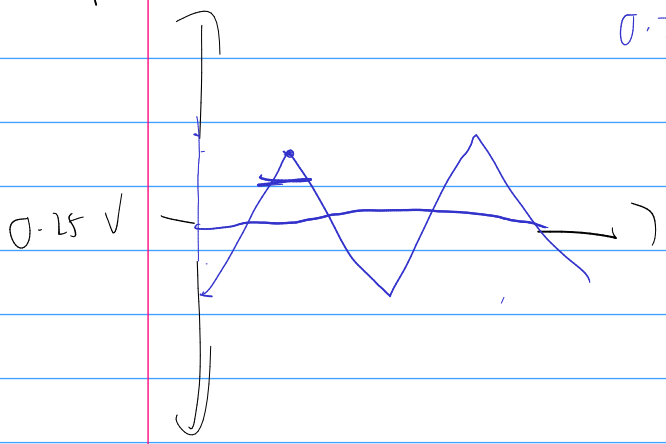
Following class-d amplifier is designed for a sinusoid input signal of 1kHz frequency and peak-to-peak amplitude of 400mV with 100kHz ramp signal of amplitude VM as shown in the Figure. If maximum and minimum duty cycle of PWM output is limited at 90% and 10%, respectively:

a) What should be the amplitude (V_M) of the ramp signal V_{RAMP_IN}? (1 mark)
b) Find the common mode voltage (V_{CM}) of the ramp signal V_{RAMP_OUT}. (1 mark)
c) Assuming inductor L is large enough to filter out PWM switching ripple, draw the waveform and find peak-to-peak value of the output current (I_{OUT}). (3 marks)
d) Find overall gain of the class-d amplifier. (2 marks)
e) Write the expression for differential PWM output (V_{PWMP}-V_{PWMN}) in terms of duty cycle (D). (2 marks)
f) Assuming switches S_P and S_N are ideal, draw the differential PWM waveform (V_{PWMP}-V_{PWMN}) at time instances t_1, t_2 and t_3. (6 marks)



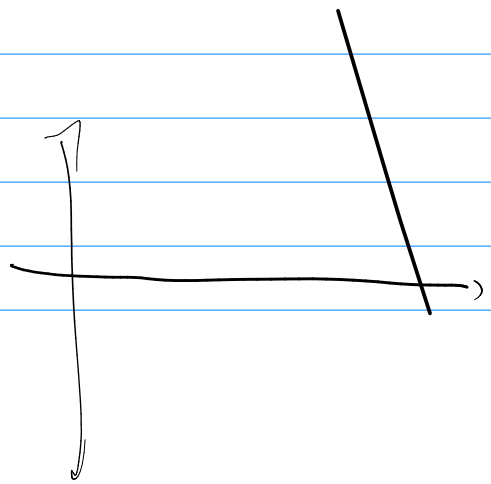


Ramp



$0.25 - \frac{V_{pp}}{2} + \left(\frac{V_{pp}}{2}\right) 90\%$ $\quad -0.25 \pm 0.2\,V$

$0.25 + V_{ripple} = 0.25 + 0.2$



Question-1 **(11 marks)**

Following class-d amplifier is designed for a triangular input signal of 10kHz frequency and peak-to-peak amplitude of 500mV with 10MHz ramp signal of amplitude V_M as shown in the Figure. If maximum and minimum duty cycle of PWM output is limited at 80% and 20%, respectively:

a) What should be the maximum peak-to-peak amplitudes V_{AN} and V_{AP} of the input signals V_{INN} and V_{INP}, respectively? *(1 mark)*

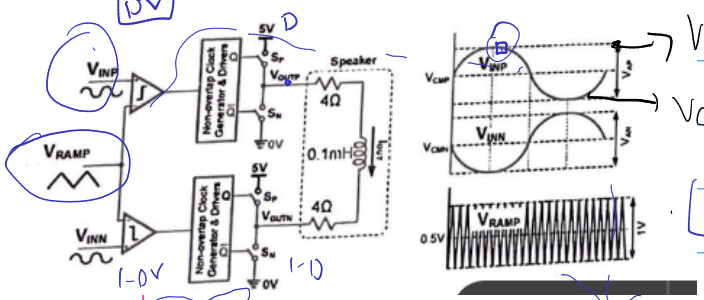
b) Find the common mode voltages V_{CMN} and V_{CMP} of the input signals V_{INN} and V_{INP}, respectively? *(1 mark)*

c) Ignoring ripple in I_{OUT} due to PWM switching, draw the waveform of output current I_{OUT} and find peak-to-peak value. *(2 marks)*

d) Find overall gain of the class-d amplifier. *(2 marks)*

e) Write the expression for average differential output voltage Avg.(V_{OUTP}-V_{OUTN}) in terms of duty cycle (D). *(2 marks)*

f) Assuming switches S_P and S_N are ideal, draw the instantaneous differential PWM waveform (V_{OUTP}-V_{OUTN}) when differential input (V_{INP}-V_{INN}) of dc +0.25V, 0V and -0.25V applied. *(3 marks)*



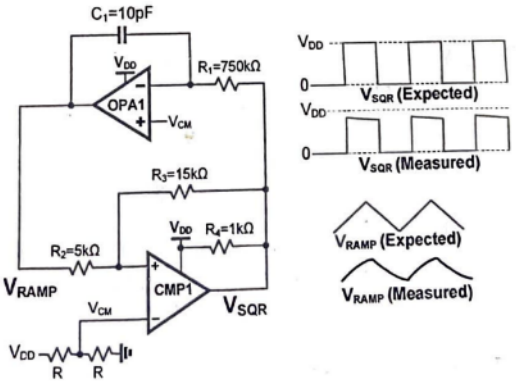
Following ramp generator was designed to operate at frequency of 100kHz with resistor and capacitor values as mentioned in the figure. Comparator CMP1 is an open drain/collector hence requires pull-up resistor R_4. Output waveform at V_{SQR} is expected to be a square wave of amplitude V_{DD} and V_{RAMP} is expected to be a triangular wave.

a) When measured on oscilloscope, the actual waveform at V_{SQR} had an amplitude lower than V_{DD} as shown in the figure. What could be the possible reason for attenuation in the amplitude and what are the two possible ways to fix this? *(2 marks)*

b) If resistor and capacitor values mentioned in the figure were selected at V_{DD}=5V, what would be the impact on ramp frequency and ramp amplitude when V_{DD} is reduced to 4V? *(2 marks)*

c) When measured on oscilloscope, it was observed that ramp frequency was not 100kHz but higher. What could be the possible reasons? *(1 mark)*

d) When measured on oscilloscope, ramp signal V_{RAMP} was not triangular but had some non-linearity as shown in the figure. What could be the reason for this non-linearity? *(1 mark)*

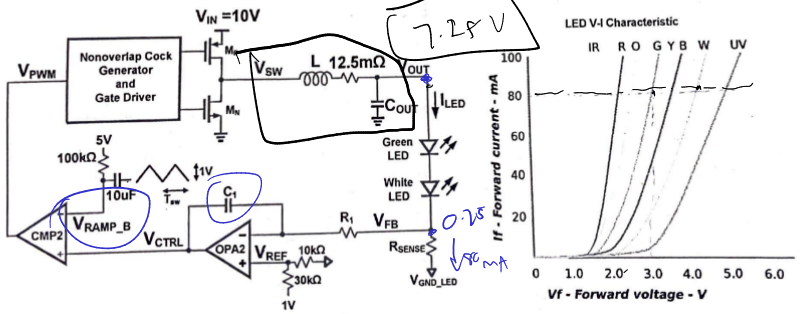


Question-3 (8 marks)

LED driver shown in figure below was designed to drive Green (G) and White (W) LEDs connected in series with their V-I characteristic shown the figure. If LEDs are driven with I_{LED}=80mA:

a) Find the value of R_{SENSE} *(1 mark)*
b) Find V_{OUT} *(1 mark)*
c) Find the value of V_{CTRL} *(1 mark)*
d) Draw the waveform at V_{RAMP_B} and V_{PWM} with dc and peak-to-peak voltage *(2 marks)*
e) Find the duty cycle of V_{PWM} *(1 mark)*
f) Which of the following three resistors is most suitable to be used as R_{SENSE} and why? *(2 marks)*

Resistor Name	Tolerance/Error	Maximum Power Rating
Resistor-A	± 1.2%	20mW
Resistor-B	± 0.5%	10mW
Resistor-C	± 1%	30mW



7.25 V

D = 72.5 %.

V_{ref} = 0.25 V

R_{sense} = 0.25 V / 80mA = 25/8 Ω

V_{ramp_b} = 5 V, 5.5 V, 4.5 V

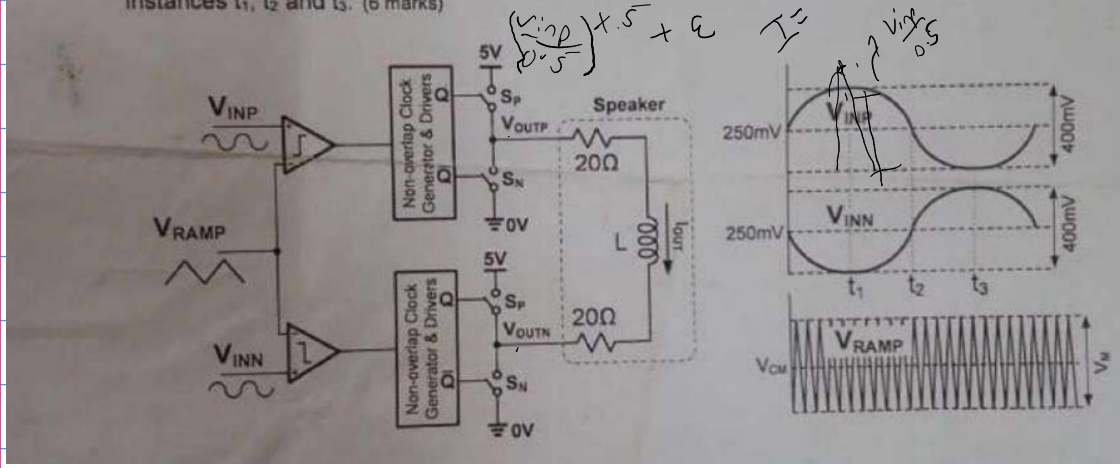
72.5 %

V_{ctrl} = 5.225 V

D = 72.5 %.

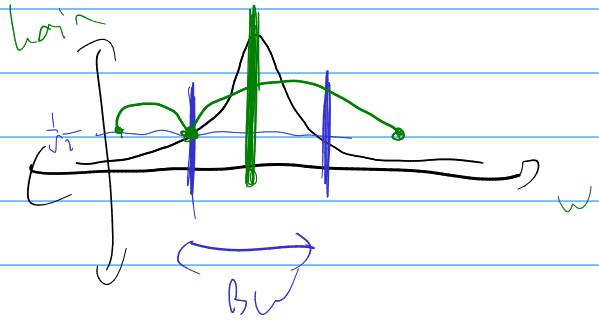
Following class-d amplifier is designed for a sinusoid input signal of 1kHz frequency and peak-to-peak amplitude of 400mV with 100kHz ramp signal of amplitude VM as shown in the Figure. If maximum and minimum duty cycle of PWM output is limited at 90% and 10%, respectively:

a) What should be the amplitude (V_M) of the ramp signal V_{RAMP_IN}? (1 mark)
b) Find the common mode voltage (V_{CM}) of the ramp signal V_{RAMP_OUT}. (1 mark)
c) Assuming inductor L is large enough to filter out PWM switching ripple, draw the waveform and find peak-to-peak value of the output current (I_{OUT}). (3 marks)
d) Find overall gain of the class-d amplifier. (2 marks)
e) Write the expression for differential PWM output (V_{PWMP}-V_{PWMN}) in terms of duty cycle (D). (2 marks)
f) Assuming switches S_P and S_N are ideal, draw the differential PWM waveform (V_{PWMP}-V_{PWMN}) at time instances t_1, t_2 and t_3. (6 marks)



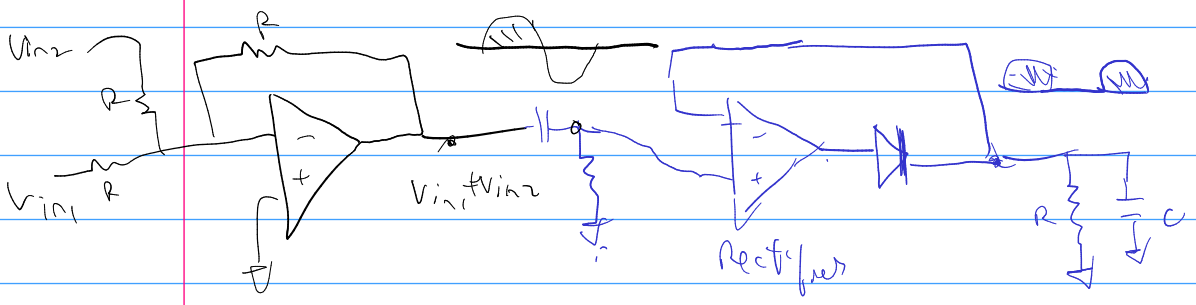
Question-4 (2 marks)

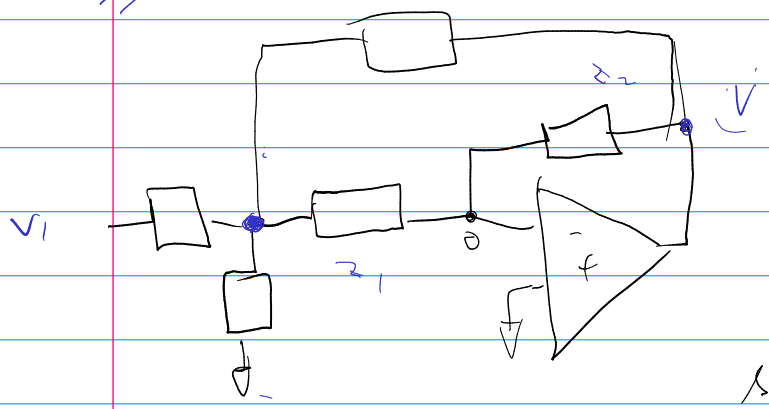
A bandpass filter was theoretically designed to operate at center frequency of 1kHz. When implemented on hardware, the center frequency was off from 1kHz due to tolerance in resistance and capacitance. How will you find the exact value of the center frequency without knowing or measuring the resistor and capacitor values?



Opt 7

Adder & Peak Detection



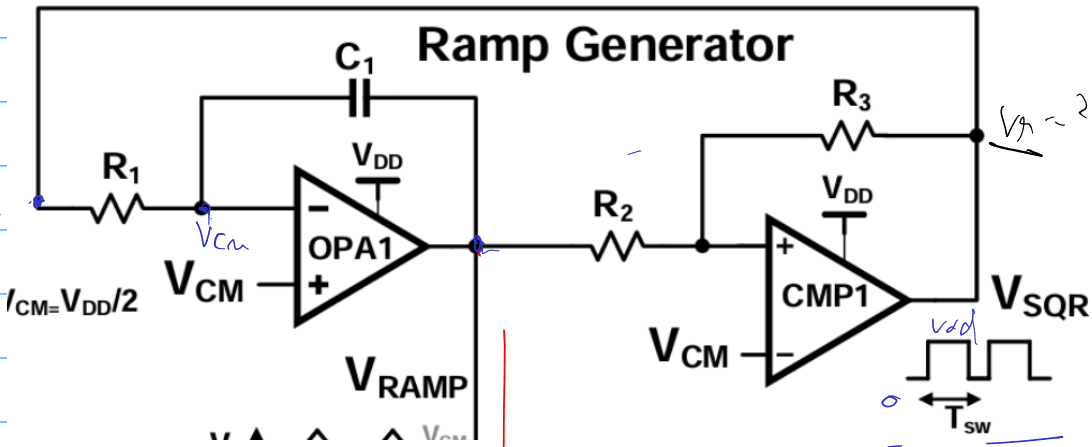


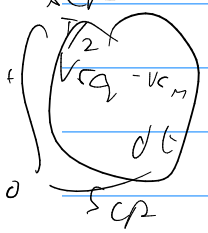
$$\frac{X}{Z_1} = \frac{-V}{Z_2}$$

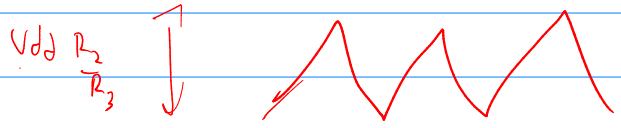
$$X = -\frac{Z_1}{Z_2} V$$

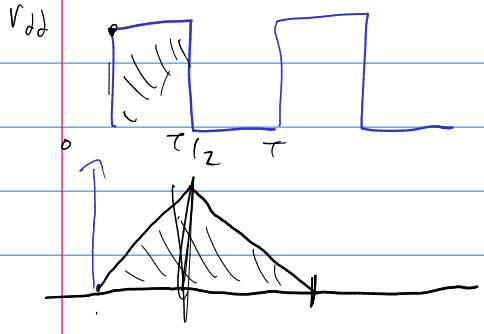
$$\frac{V_{CQ} - V_{CM}}{SC R_1} = \left(V_R - V_{CM}\right)$$

$$V_R = 2.5 + \frac{V_{CQ} - V_{CM}}{SCR}$$

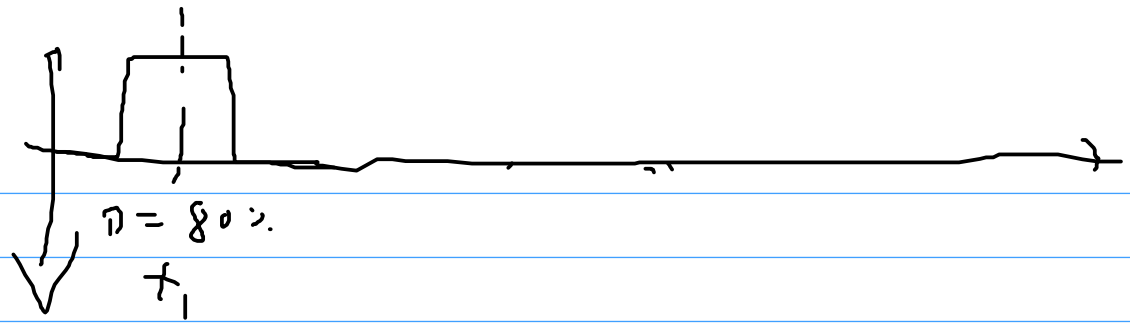


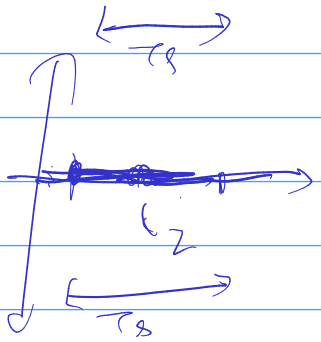


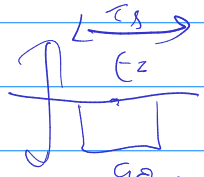




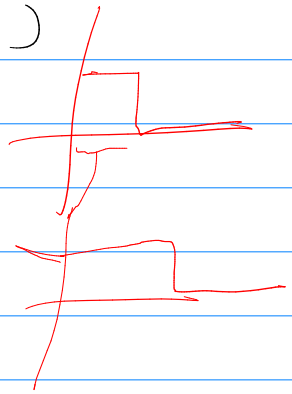
$$\frac{R_2 V_{dd}}{R_3} = \frac{1}{R_1 C_1} \times \frac{T}{2}$$

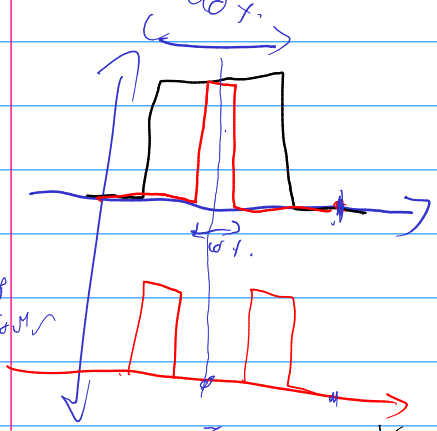


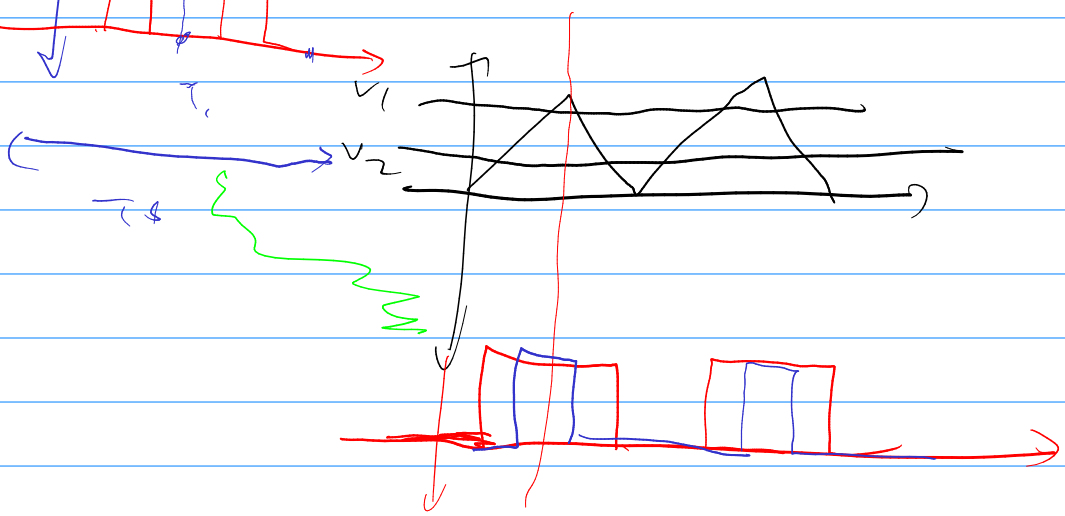


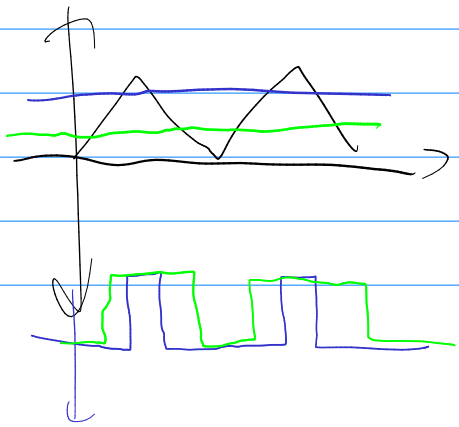


(20-1) V_{out} = 80 × (5)





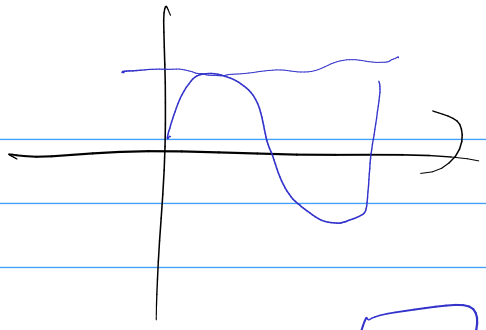




$D = 0.5 + 0.4 \sin \omega t$

$i_L = \dfrac{V_{dd}(2D-1)}{2R}$

$= \dfrac{V_{dd} \times 0.8}{2R}$



$\dfrac{2V_{dd}}{V_m} = 2D$

$(2D-1)\,V_{dd}$