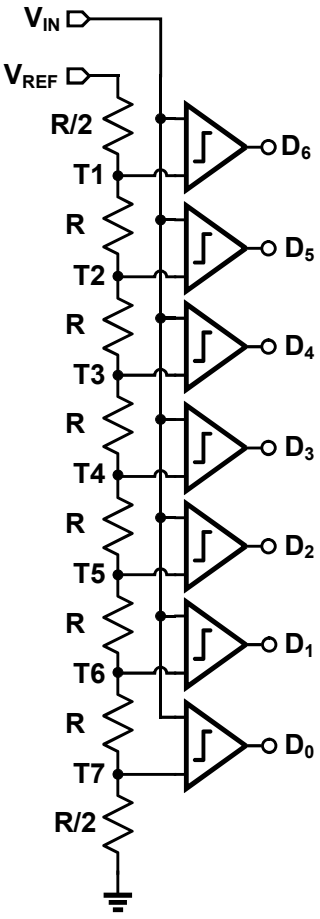
EE2019 – Analog Systems and Lab

Problem Set # 10

Question-1

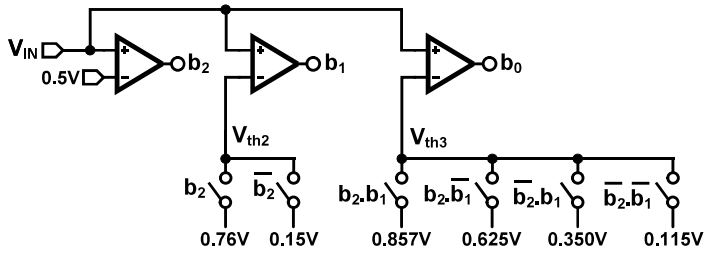
Consider a 3-bit flash ADC shown below. The comparators are ideal. Bits $D_0,\ldots,D_6$ are combined to give a digital output, *D*. Outputs of comparators are 0 or 1. V_{REF} = 1V and V_{IN} = 0.37V.

a) Find the digital output for the given input.
b) Sketch the digital output versus input voltage ([0,1V]) for the flash ADC.
c) Sketch the DNL profile of the ADC.
d) Let T1 and T2 be shorted, T3 and T5 be shorted, and T6 and T7 be shorted together. Sketch the digital output versus input voltage ([0,1V]) for the new flash ADC with shorted input reference voltage nodes.
e) Find the digital output for input V_{IN} = 0.37V with ADC described in (d).



Question-2

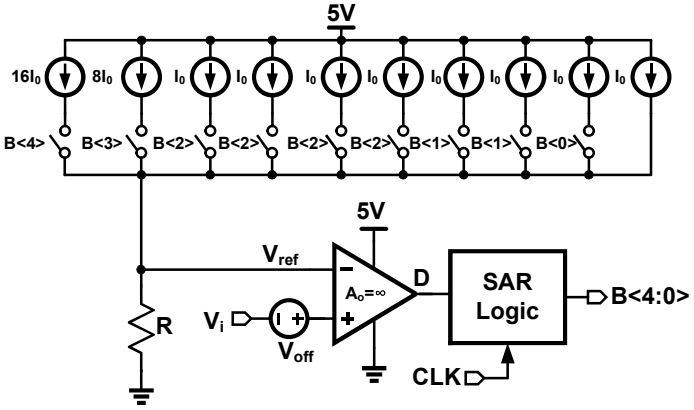
A 3-step flash ADC is shown below. Comparator outputs $b_{1,2,3}$ are 1 or 0. Switches are ideal with zero resistance for control voltage 1V. Switches are open with control voltage 0V.



a) Find ADC's output ($b_2b_1b_0$) if V_{IN} is 0.715 V.
b) Find comparator threshold voltages Vth2 and Vth3.

Question-3

In the circuit shown below, switched current sources are used with a resistor R to generate the reference voltage V_{ref} for comparison. The switches are ideal with zero ON resistance when control signal is high. The switch is turned OFF when control signal as 0V. The comparator has an input referred offset voltage V_{off}. V_i is the sampled input available for comparison. SAR logic is clocked using clock signal, CLK with time period T. SAR's outputs i.e., B<4:0> change every clock (CLK) period. Let B<4:0> has 5V has high voltage and 0V as low voltage. Also, I_0=31.25µA and R = 1kΩ. Let D=0 and B<4:0>=0 at t=0.



a) If V_i=0.743V and V_{off} = 0V, find D and B<4:0> every clock period till a final digital equivalent is found for the input.

If V_i=0.743V and V_{off} = -31.25µV, suggest a method to generate a correct digital equivalent of the analog input with available components in the circuit and without adding any extra circuit components.

Question-1

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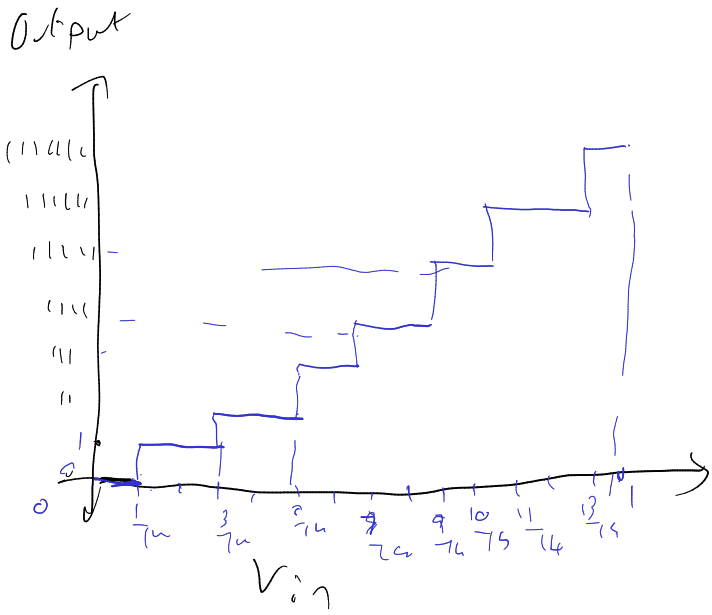

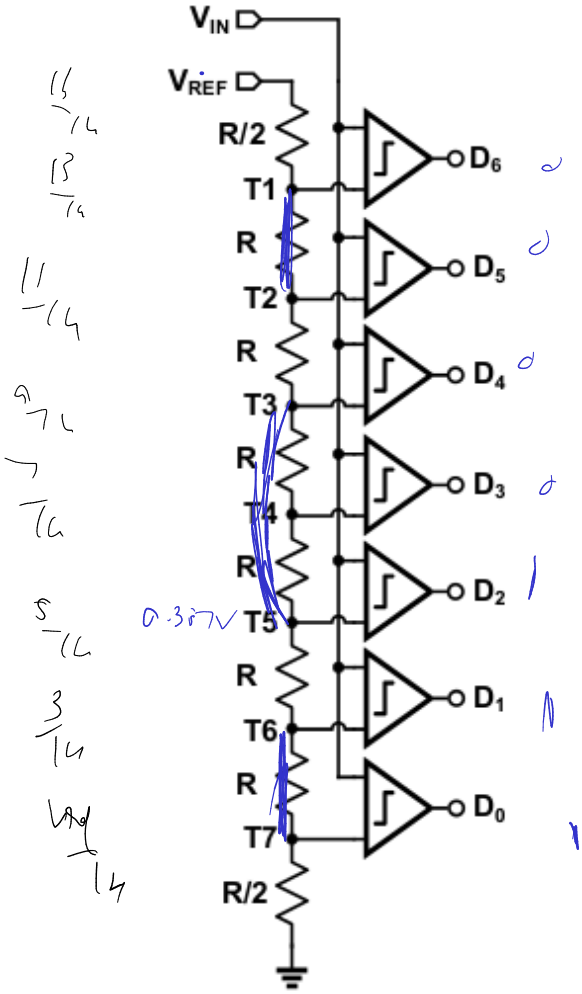

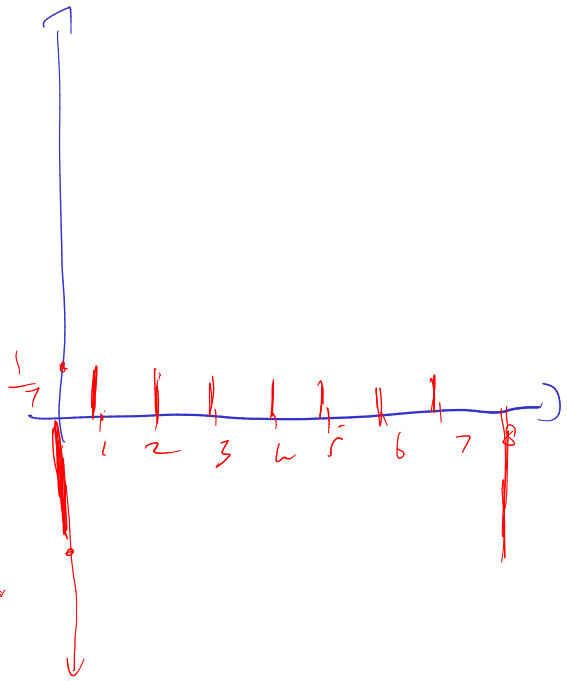

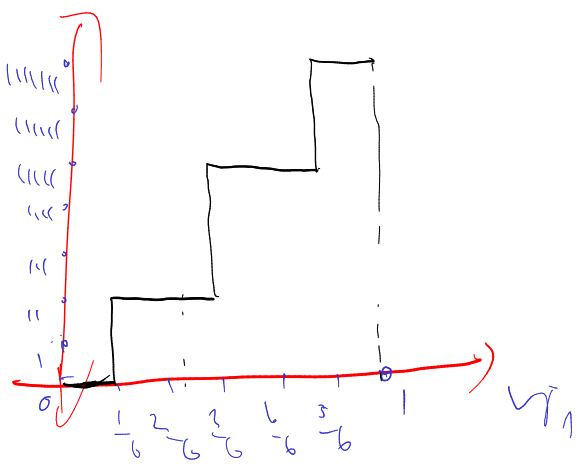

Question-2

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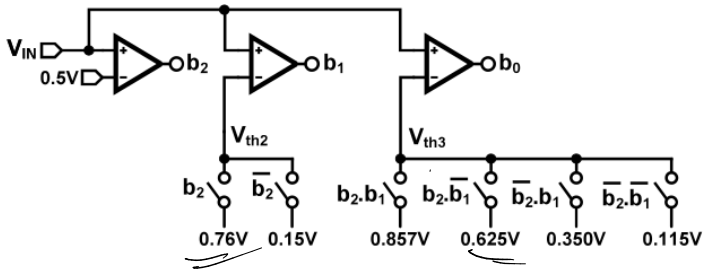
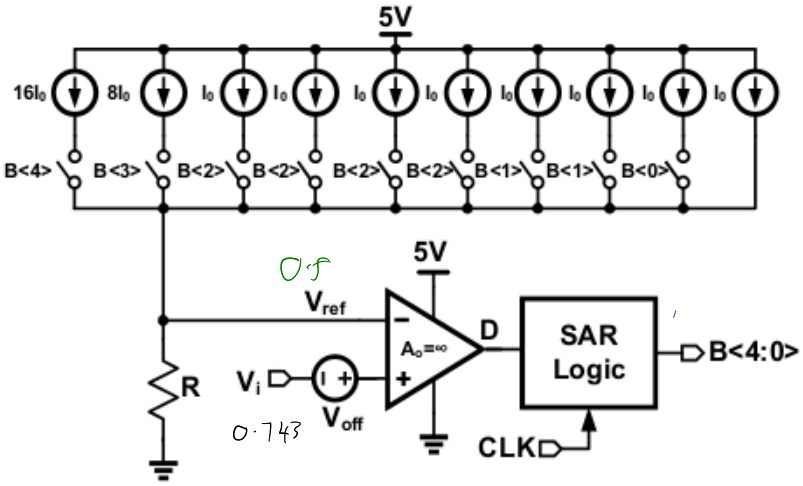


a) Find ADC's output ($b_2b_1b_0$) if V_{IN} is 0.715 V.
b) Find comparator threshold voltages Vth2 and Vth3.

0.76V, 0.625V

Question-3

In the circuit shown below, switched current sources are used with a resistor R to generate the reference voltage V_{ref} for comparison. The switches are ideal with zero ON resistance when control signal is high. The switch is turned OFF when control signal as 0V. The comparator has an input referred offset voltage V_{off}. V_i is the sampled input available for comparison. SAR logic is clocked using clock signal, CLK with time period T. SAR's outputs i.e., B<4:0> change every clock (CLK) period. Let B<4:0> has 5V has high voltage and 0V as low voltage. Also, I_0=31.25μA and R = 1kΩ. Let D=0 and B<4:0>=0 at t=0.

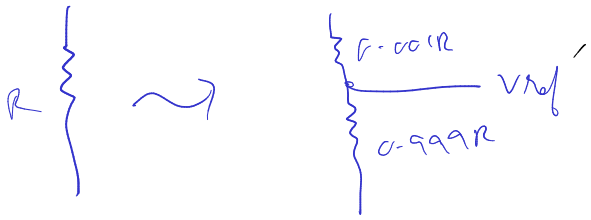


a) If V_i=0.743V and V_{off} = 0V, find D and B<4:0> every clock period till a final digital equivalent is found for the input.

If V_i=0.743V and V_{off} = -31.25μV, suggest a method to generate a correct digital equivalent of the analog input with available components in the circuit and without adding any extra circuit components.

	D	B	Vref
0	0V	00000	0
1	5V	10000	0.5
2	5V	11000	0.78125
3	0V	10100	0.65625
4	5V	10110	0.71875
5	5V	10111	0.75
6	0V	10110	0.71875

b) $V_t = V_i + V_{off}$



This will give same result