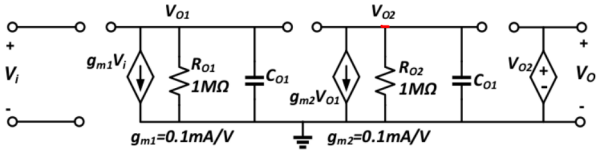
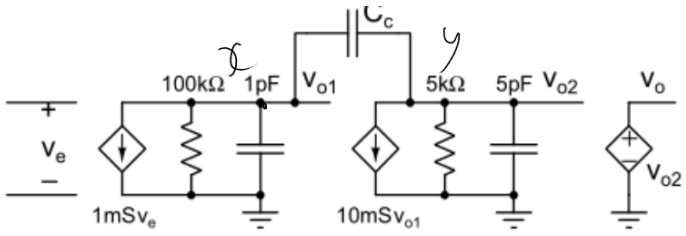
1

$$\frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$



$$\frac{g_{m1}g_{m2}R_{O1}R_{O2}}{(1+sR_{O1}C_{O1})(1+sR_{O2}C_{O2})}$$

2



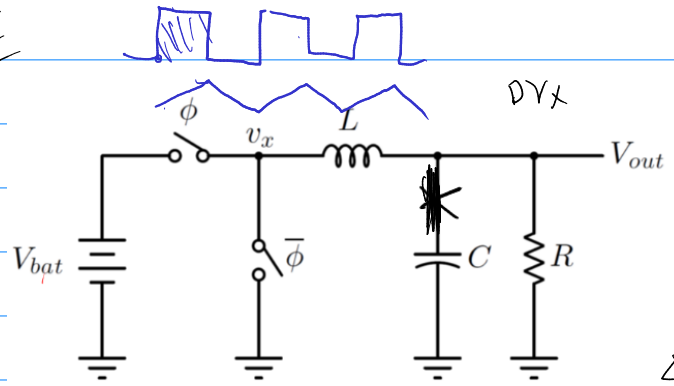
$$\frac{(g_{m1}g_{m2})\left(1-\frac{sC_c}{g_{m2}}\right)}{s^2[C_1C_2+C_cC_1+C_cC_2]+s\left[C_1+C_2+C_c\left[\frac{1}{R_1}+\frac{1}{R_2}+g_{m2}\right]\right]+\frac{1}{R_1R_2}}$$

$$f_1=\frac{1}{g_{m2}C_cR_1R_2}$$

$$f_2=\frac{g_{m2}C_c}{C_c[C_1+C_2]+C_1C_2}$$

3

PMC

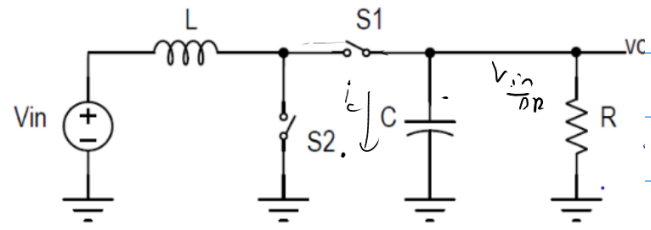


DYX

Buck Converter

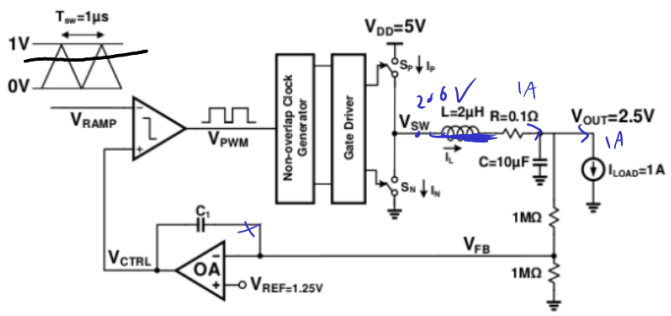
$$\Delta i=\frac{\alpha(1-\alpha)TV_{out}}{L}$$

$$\Delta V=\frac{1}{8}\frac{\Delta i T}{C}$$

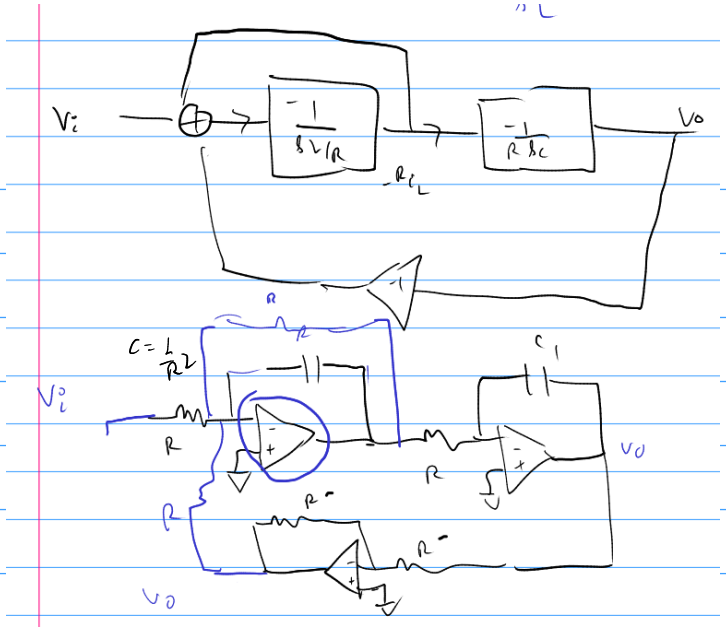


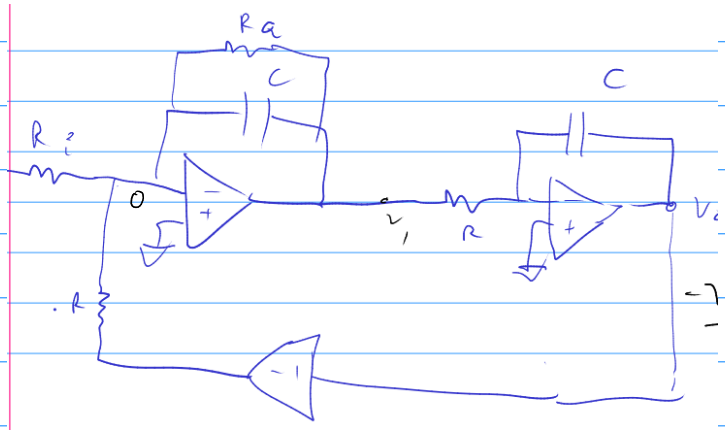
$$i_c=\frac{\int v_{dt}}{L}$$

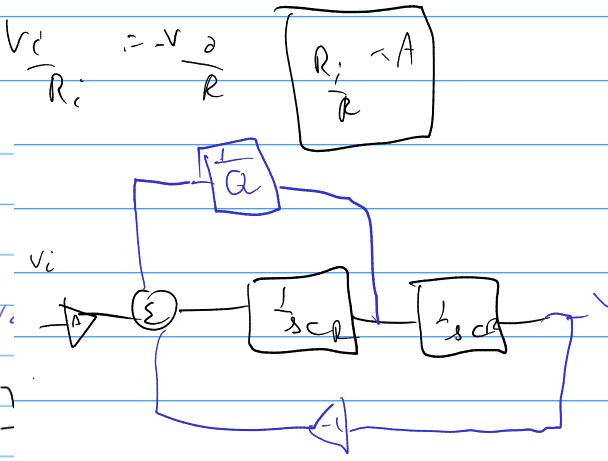
$$\Delta i=\frac{(1-D)V_{bat}DT_s}{L}$$



④ Filters







$$\text{DNL(i)} = \frac{V_{\text{out}}(i+1) - V_{\text{out}}(i)}{\text{ideal LSB step width}} - 1$$

$$INL(k) = \frac{T_a(k) - T_{ideal}(k)}{Ideal\ Step\ Size} = \sum_{i=0}^{k-1} DNL(i)$$

⑤ Oscillators

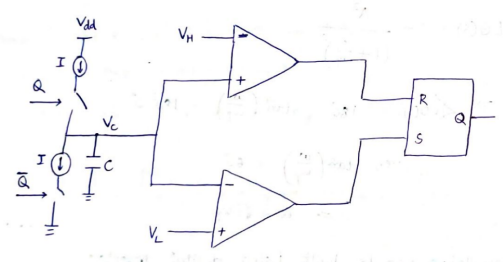
Wien bridge → lite

Ring

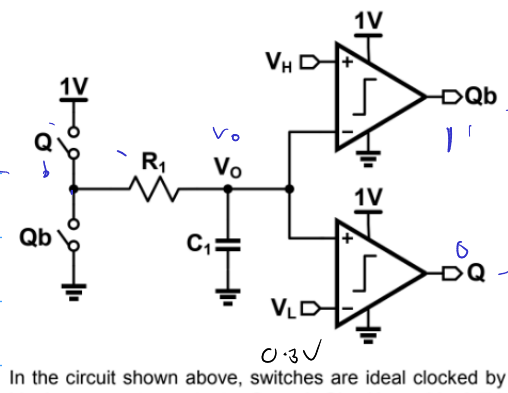
$\tau_d = \frac{T}{2}$

T odd

Relaxation



$$f = \frac{I}{2C(V_H - V_L)}$$



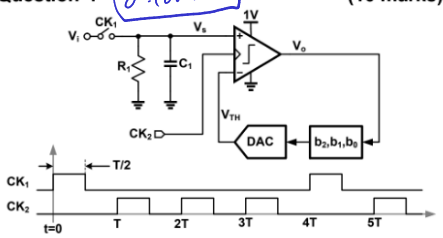
In the circuit shown above, switches are ideal clocked by ideal comparator outputs Q and Qb. Here, V_H=0.7V, V_L=0.3V, R_1=4kΩ, and C_1=8nF. In steady state, sustained oscillations are observed at V_O and Q/Qb and V_O has a dc voltage of 0.5V.

a) Find the frequency of sustained oscillations.

b) Find time domain expressions for a clock period at V_O. Plot waveforms for a clock period at V_O in steady state.

c) If V_L is changed to 0.15V, what is the new dc voltage across C_1?

Question-4 **(10 marks)**



Consider a 3-bit ADC as shown above. The input V_I is sampled using clock CK_1. The sampled input is compared with the threshold voltage V_{TH} at the rising edge of clock CK_2. The comparator outputs are stored in bits b_2,b_1,b_0. Digital-to-analog converter (DAC) converts digital bits to analog voltage V_{TH}. V_{TH} spans 0 to 1V. If V_I = 0.85V and R_1C_1=T/4, find digital bits at the end of each clock period. (Hint: You can start with V_{TH} = 0.5V. Switch is ideal.)

Question-5 **(5 marks)**

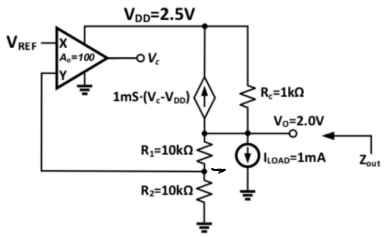
The LDO shown below is designed to regulate the output voltage, V_O=2.0V.

a) Determine the signs of opamp inputs (X & Y) for negative feedback operation.

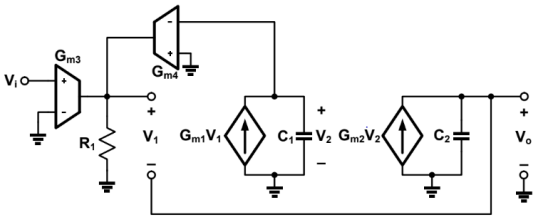
b) Find the value of V_{REF} and control voltage, V_C to regulate V_O at 2.0V.

c) Find the absolute error in V_O due to finite DC gain.

d) Determine the output impedance, Z_{out} looking into the output V_O.



Question-3 **(10 marks)**



For the closed loop feedback system shown above G_{m1} = 8 mA/V, G_{m2} = 40mA/V, G_{m3} = 1 mA/V, R_1 = 1kΩ, C_1 = 25 pF, C_2 = 160 pF,

a) Find loop gain and phase margin when G_{m4} = 0.

b) Find G_{m4} such that the closed loop $\frac{V_o(s)}{V_i(s)}$ is a second-order transfer function with Butterworth (maximally flat) response in signal band.

c) For G_{m4} value found in part (b), find loop gain and plot Bode magnitude and phase plots for the loop gain. Also, find the phase margin for loop.

$V_2 = (G_{m1} V_1)/sC_1$

$V_o = (G_{m2} V_2)/sC_2$

$V_o = \frac{G_{m1} G_{m2}}{s^2 C_1 C_2}[V_x - V_o]$

$V_x = R_1(G_{m3} V_i - G_{m4} V_2)$

$V_o = \frac{G_{m1} G_{m2}}{s^2 C_1 C_2}\left[R_1 G_{m3} V_i - \frac{R_1 G_{m4} s C_2}{G_{m2}} V_o - V_o\right]$

$1 + \frac{R_1 s C_2 G_{m4}}{G_{m2}} + \frac{s^2 C_1 C_2}{G_{m1} G_{m2}} = R_1 G_{m3} V_i$

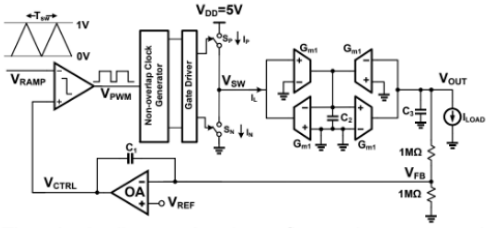
$\frac{V_o}{V_i} = \frac{R_1 G_{m3} s}{1 + \frac{R_1 G_{m4} C_2}{G_{m2}} s + \frac{C_1 C_2}{G_{m1} G_{m2}} s^2}$

$\omega_n = \sqrt{\frac{G_{m1} G_{m2}}{C_1 C_2}}$

$\frac{1}{\omega_0 Q} = \frac{R_1 G_{m4} C_2}{G_{m2}}$

$\frac{1}{Q} = \frac{1}{\omega_0} \frac{G_{m2}}{R_1 G_{m4} C_2} = \sqrt{\frac{G_{m2} C_1}{G_{m1} C_2}} \frac{1}{R_1 G_{m4}}$

Question-2 **(10 marks)**



The circuit diagram in above figure shows a type-I compensated buck converter with output voltage, V_{OUT} regulated at 4.5V for input supply, V_{DD}=5V and load current, I_{LOAD}=0.2A. The buck converter uses an active inductor with G_{m1}=5mA/V and C_2=2pF. Here, C_3=10μF and V_{REF}=2.25V. Assuming switches SP and SN are ideal.

a) Model the buck converter in continuous time domain and find the small signal loop gain transfer function.
b) Determine the value of capacitor C_1 to achieve the gain margin of >12dB and draw the Bode magnitude and phase plot.
c) Find the value of control voltage, V_{CTRL} and duty cycle, D to regulate the output voltage at 4.5V.
d) Find the value of peak-to-peak inductor ripple current and peak-to-peak output ripple voltage.

e) If Gm blocks consume 0.1mA from 5V supply voltage to have current gain of 1mA/V and the power consumption in all other blocks is negligible, find the power efficiency of the regulator.

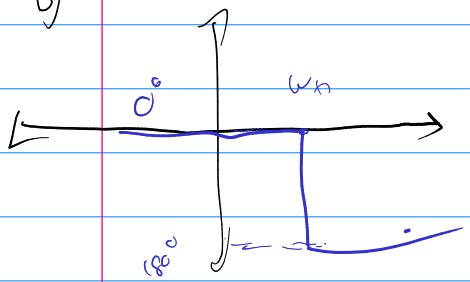
$\frac{1}{G_m^2 Z}$ $L = \frac{1}{G_m^2}$ $= 8 \times 10^{-8}$

$\frac{R}{sC} = \frac{R}{RsC+1}$ $\frac{\frac{R}{RsC+1}}{R + sL} = \frac{1}{1 + \frac{RsC+1}{R}sL}$

L C $R = V_{out}$ i_{load} $= 22.5\,\Omega$

$\frac{L}{sC}$ $= \frac{5}{s^2LC + 1 + \frac{sL}{R}}$ $\frac{1}{\omega_n \frac{L}{R}}$

b)



$\frac{5}{s^2LC + \frac{sL}{R} + 1}$ (sRC)

$\frac{5}{\left(s\frac{L}{R}\right)(sRC)}$ $= \frac{1}{\left(\frac{1}{LC}\right)\frac{L}{R}}$ (RC)

$= sRC$ $\frac{1}{RC}$

$= \frac{22.5 \times 10\mu}{1M}$ $\frac{5}{C}$ $= \frac{1}{4}$

$C = \frac{4 \times 22.5 \times 10\mu \times 5}{1M}$

$= 900\frac{\mu}{M} =$ 900pF

$=$ 1.8nF

Question-1 **(10 marks)**

A filter transfer function is given by

$$H(s) = \frac{10\left(1+\frac{s^2}{\omega_p^2}\right)}{1+\frac{s}{\omega_p Q_p}+\frac{s^2}{\omega_p^2}}$$

Here, $\omega_p = 10^9$ and $Q_p = \frac{1}{5}$.

a) Draw s-domain block diagram of the above filter using integrators and gain blocks.
b) Realize the above filter transfer function using ideal opamps, resistors, and capacitors.
c) If 1pF capacitors are used for all integrators, find all resistor values used in your design.
d) Draw Bode magnitude and phase plots for the filter transfer function.

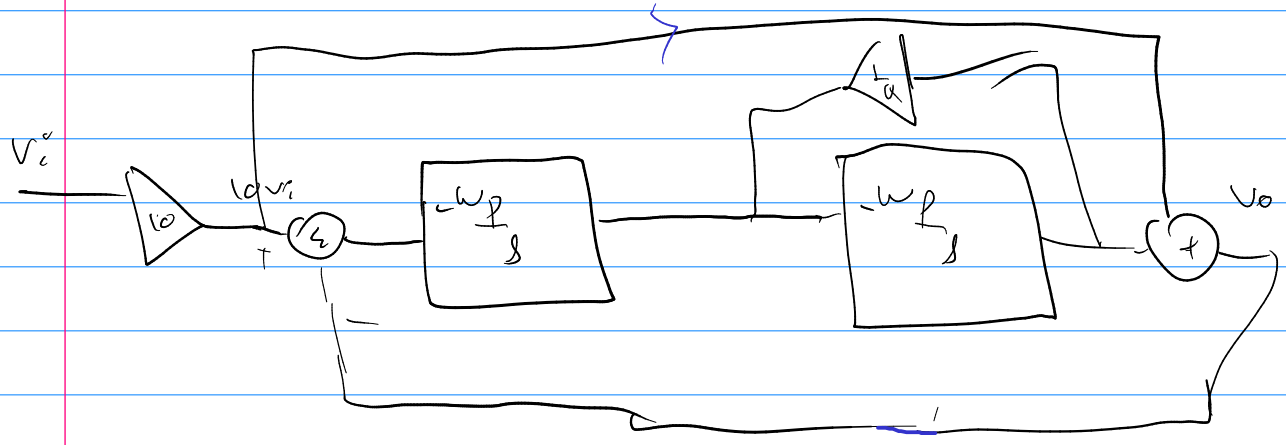
$10V_i + 10\frac{s}{\omega_p^2}V_i = V_o + V_o\frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p^2}V_o$

$10V_i\frac{\omega_p^2}{s^2} + 10V_i = V_o\frac{\omega_p^2}{s^2} + \frac{\omega_p V_o}{sQ_p} + V_o$

$10V_i - V_o = \frac{\omega_p V_o}{sQ_p} - \frac{\omega_p^2}{s^2}10V_i + V_o\frac{\omega_p^2}{s^2}$

$\frac{\omega_p}{s}\left[\frac{\omega_p(V_o - 10V_i)}{s} + \frac{1}{Q}V_o\right]$

$V_o = 10V_i - \frac{\omega_p}{s}\left[\frac{\omega_p}{s}(10V_i - V_o) + \frac{V_o}{Q}\right]$



Question-1 **(10 marks)**

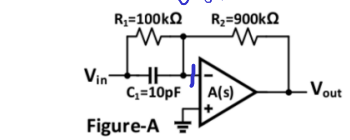


Figure-A

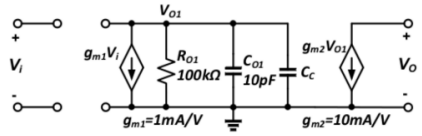


Figure-B

Closed loop amplifier shown in Figure-A needs to be designed for stable operation. Considering the op-amp (OA) model shown in Figure-B.

a) Find the loop gain transfer function.
b) Calculate the value of capacitor C_C to achieve the phase margin of 60 degrees.
c) Draw the bode magnitude and phase plot of the loop gain transfer function after the compensation. Clearly mention values of gain, phase and location of poles, zeroes and unity gain frequency.

$V_{out} = -AV_x$

$= 9000 \times 10^{-9} = 9\times10^{-6}$

$V_{out} - V_x + \frac{(V_{in} - V_x)}{9} + (V_{in} - V_x)s(1pF) = 0$

$V_{out} - 10V_x + 9V_{in} + V_{in}s\,9\times10^{-6} - V_x\,9\times10^{-6}s = 0$

$V_{out} + \frac{10}{A}V_{out} + 9\times10^{-6}sV_{out} = -9V_{in} - s9\times10^{-6}V_{in}$

$i_{out} = -g_{m2}V_{O1} = \frac{g_{m2}g_{m1}V_i}{\left(\frac{1}{R_{O1}} + s(C_C)\right)} = \frac{g_{m2}g_{m1}R_{O1}V_i}{(1+s(R_{O1}C_C))}$

$$\frac{R_1}{sC_1} = \boxed{\frac{R_1}{R_1 C_1 s + 1}} + R_2$$

$$R_1 + \frac{1}{sC_1}$$

$$V_{out} = I_{out} \times R_{out} = \left(g_m \frac{g_{m2} R_{o1}}{1 + s C R_{o1}} \right) \left[\frac{R_1}{R_1 C_1 s + 1} \right]$$

$$= \frac{10^5}{\left(1 + \frac{1}{10^6}\right)\left(1 + \frac{s}{p_1}\right)}$$

Dampod

$$\omega_y = \frac{1}{\sqrt{3}} 10^6$$

$$\frac{10^5}{\left(\frac{2}{\sqrt{3}}\right)\left(\frac{\omega_y}{p_1}\right)} = 1$$

$$\frac{10^5 \, 3 p_1}{2 \, 10^6} = 1$$

$$\frac{3}{2} \frac{p_1}{10} = 1$$

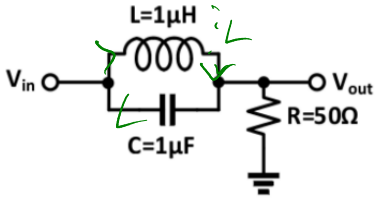
$$p_1 = \boxed{2e13} = \frac{1}{R_1 C_1}$$

$$C_{eq} = \frac{1}{R_1} \frac{3}{2\pi} = \frac{3}{20} \frac{1}{10^5}$$

$$\boxed{\approx 1.5 \, \mu F}$$

Question-4 **(10 marks)**

Design a Gm-C equivalent filter for the following RLC filter using state variable technique. Specify the values of all transconductances and capacitances used in the design.



$V_{out} - V_{in} = V_C$

$R\left(\frac{1}{sL}\right) i_L = V_C$

$R i_L = \frac{V_C}{\frac{sL}{R}}$

$R i_L = (V_C) sCR + V_{out}$

$R i_L = V_C sCR + V_{in} + V_C$

$V_C = \frac{R i_L - V_{in}}{1 + sCR}$

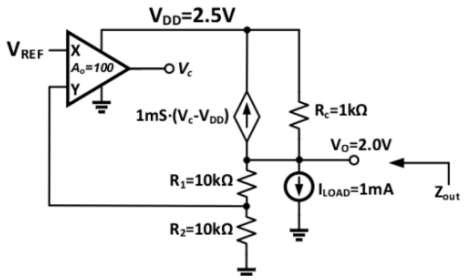
The LDO shown below is designed to regulate the output voltage, V_O=2.0V.

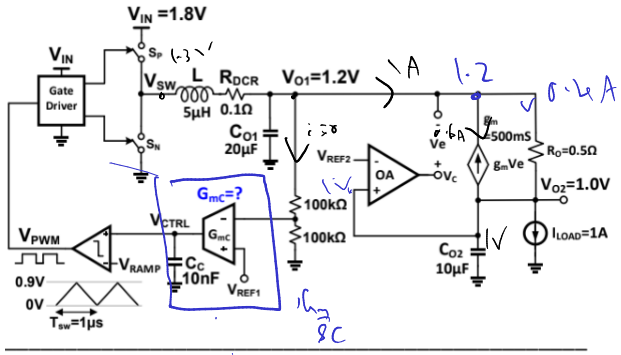
a) Determine the signs of opamp inputs (X & Y) for negative feedback operation.

b) Find the value of V_{REF} and control voltage, V_C to regulate V_O at 2.0V.

c) Find the absolute error in V_O due to finite DC gain.

d) Determine the output impedance, Z_{out} looking into the output V_O.





Above voltage regulator system consisting of a switching buck converter followed by a linear regulator is designed for following specifications: V_{IN}=1.8V, output of the switching buck converter, V_{O1}=1.2V, output of the linear regulator, V_{O2}=1.0V, load current of the linear regulator, I_{LOAD}=1A, ramp switching period=1µS, ramp amplitude=0.9V, inductor L=5µH, series resistance R_{DCR}=0.1Ω, capacitors C_{O1}=20µF, C_{O2}=10µF and integrator capacitor, C_C=10nF. Assuming ideal switches S_P and S_N where S_P a turned ON when V_{PWM} is high and S_N is turned ON when V_{PWM} is low.

a) Determine the steady state value of control voltage, V_{CTRL}, PWM duty cycle and linear regulator control voltage, V_C.
b) Find the loop gain unity gain frequency and value of integrator transconductance, G_{mc} to achieve the minimum gain margin of 20dB (i.e. loop gain magnitude = -20dB at 0 phase margin) for I_{LOAD}=0 to 1A.
c) Find peak-to-peak inductor ripple current ΔI_L and output ripple voltage ΔV_{O1}.
d) Determine the overall efficiency of the entire voltage regulator system.

Question-5 (10 marks)

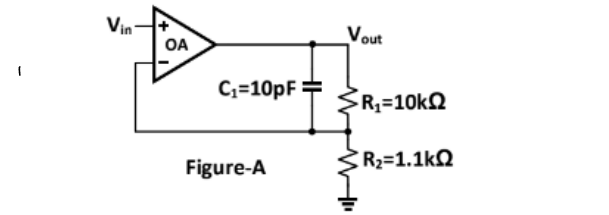


Figure-A

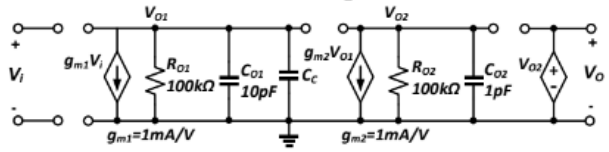
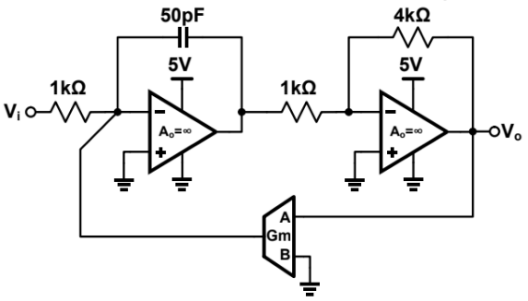


Figure-B

A closed loop amplifier shown in Figure-A needs to be designed for stable operation. Considering the op-amp (OA) model shown in Figure-B

a) Determine the loop gain transfer function and frequency of poles and zeros with C_C=0.
b) Calculate the value of capacitor C_C to achieve the phase margin of 60 degrees.
c) Draw the bode magnitude and phase plot of the loop gain transfer function after the compensation. Clearly mention values of gain, phase and location of poles, zeroes and unity gain frequency.
d) If R_1 remains fixed at 10kΩ while R_2 is changed to adjust the closed loop gain, find the value R_2 at which the amplifier becomes unstable (i.e. phase margin is dropped to 45 degrees).
e) Find the damping factor (ζ) with location of poles and zeroes of the closed loop transfer function, $V_{out}(s)/V_{in}(s)$ before and after the compensation.

Question-4 (5 marks)

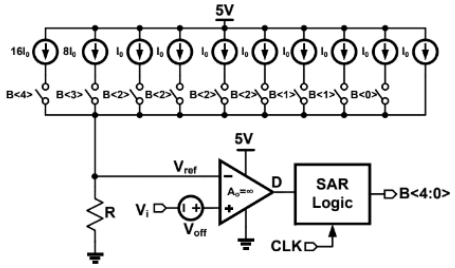


In the circuit shown above, Gm = 1mA/V.

a) Find the signs of terminals 'A' and 'B' such that the closed loop operation is stable.
b) Find the closed loop gain $V_o(s)/V_i(s)$. Find the unity gain frequency for the closed loop transfer function.

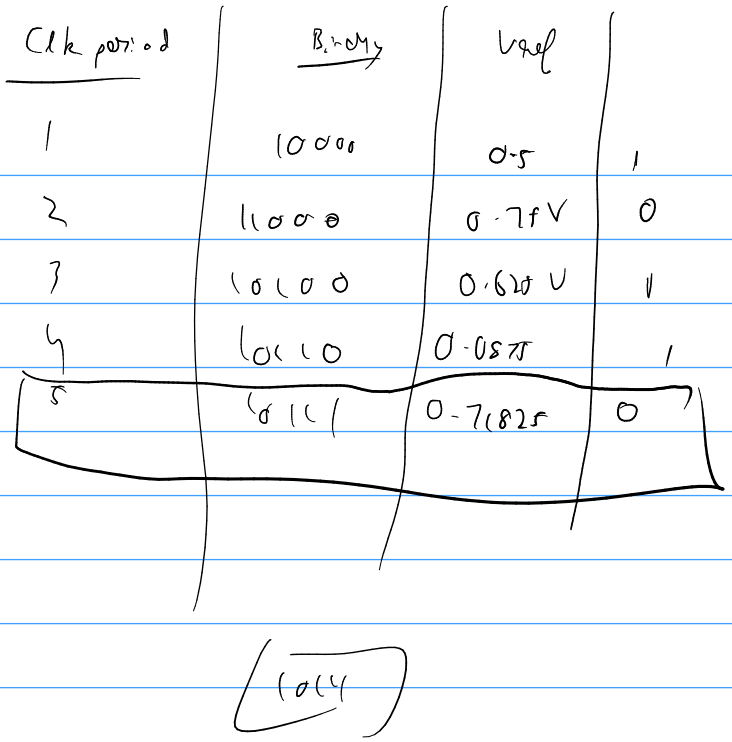
Question-3 **(5 marks)**

In the circuit shown below, switched current sources are used with a resistor R to generate the reference voltage V_{ref} for comparison. The switches are ideal with zero ON resistance when control signal is high. The switch is turned OFF when control signal as 0V. The comparator has an input referred offset voltage V_{off}. V_i is the sampled input available for comparison. SAR logic is clocked using clock signal, CLK with time period T. SAR's outputs i.e., B<4:0> change every clock (CLK) period. Let B<4:0> has 5V as high voltage and 0V as low voltage. Also, I_0=31.25μA and R = 1kΩ. Let D=0 and B<4:0>=0 at t=0.



a) If V_i=0.743V and V_{off} = 0V, find D and B<4:0> every clock period till a final digital equivalent is found for the input.

b) If V_i=0.743V and V_{off} = -31.25mV, suggest a method to generate a correct digital equivalent of the analog input with available components in the circuit and without adding any extra circuit components.



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