BASIC GATES

EXPLANATION

- AND Gate : Both inputs are high then output is high,for remaining combinations output is low

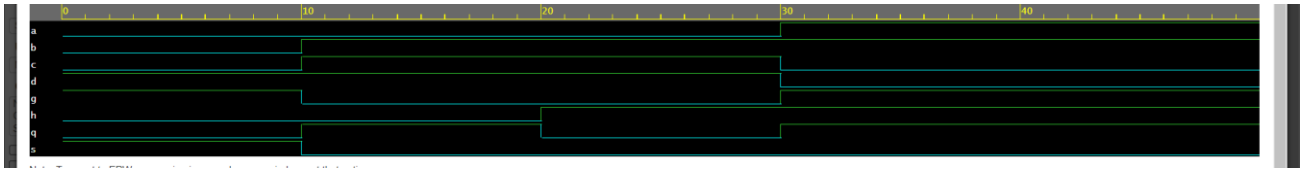
- OR Gate : Any one of the input is high output is high,for remaining combinations output is low
- . NOT Gate : Complemented input
- NAND Gate : Any one of the input is low output is high.
- NOR Gate : Any one of the input is high output is low.
- XOR Gate : Odd Number of the input is high output is high.
- XNOR Gate : Even Number of the input is high output is high.

RTL CODE:

```
module gates(a,b,c,d,s,g,h,q);
  output a,b,c,d,s,g;
  input h,q;
  assign a=h&q;  \\ and logic
  assign b=h|q;     \\ or logic
  assign c=h^q;       \\ xor logic
  assign d=~(h&q);    \\ nand logic
  assign s=~(h|q);     \\ nor logic
  assign g=~(h^q);     \\ xnor logic
endmodule
```

TEST BENCH

```
module test_beanch;
  reg h,q;
  wire a,b,c,d,s,g;
  gates g1(a,b,c,d,s,g,h,q);
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
  initial
    begin
      h=0;q=0;
    end
  initial
    begin
      #10 h=0;q=1;
      #10 h=1;q=0;
      #10 h=1;q=1;
    end
  initial
    begin
      #50 $finish();
    end
endmodule
```


0
10
20
30
40
a
b
c
d
g
h
q
s