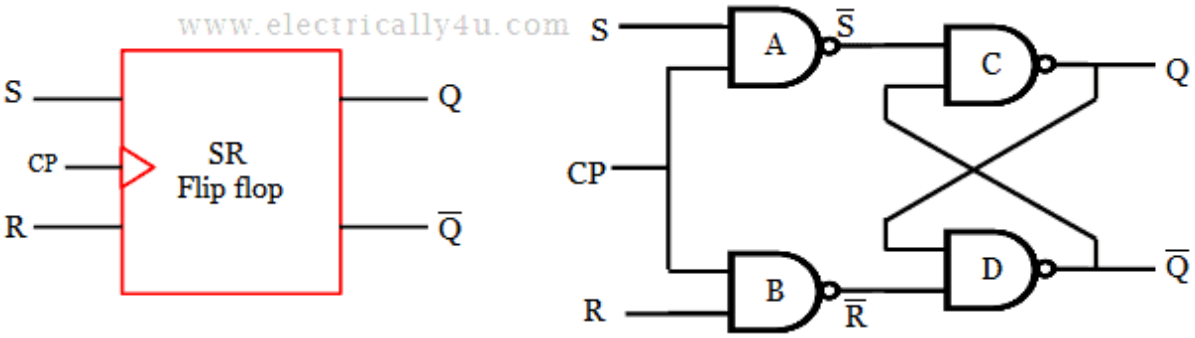
SR FLIP FLOP

It is a Flip Flop with two inputs, one is S and other is R. **S** here stands for Set and **R** here stands for Reset. Set basically indicates set the flip flop which means output 1 and reset indicates resetting the flip flop which means output 0. Here clock pulse is supplied to operate this flip flop, hence it is clocked flip flop.



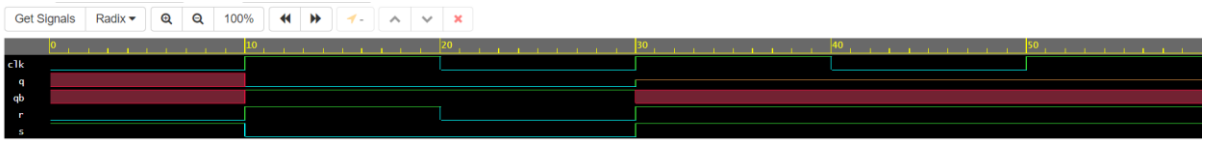
RTL CODE:

```
module tla(input clk,input s,input r,output reg q,output reg qb);
  always @(posedge clk) begin
    case({s,r})
      2'b00: q<=q;
      2'b01: q<=0;
      2'b10: q<=1;
      2'b11: q<=1'bz;
      endcase
  end
  assign qb=~q;
```

```
endmodule
```

TEST BENCH:

```
module test;
  reg clk;
  reg s;
  reg r;
  wire q,qb;
  tla t1(clk,s,r,q,qb);
  initial begin
    clk=0;
    forever #10 clk = ~clk;
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    s= 1; r= 0;
    #10 s= 0; r= 1;
    #10 s= 0; r= 0;
    #10 s= 1; r= 1;
  end
  initial begin
    #60 $finish();
  end
endmodule
```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.