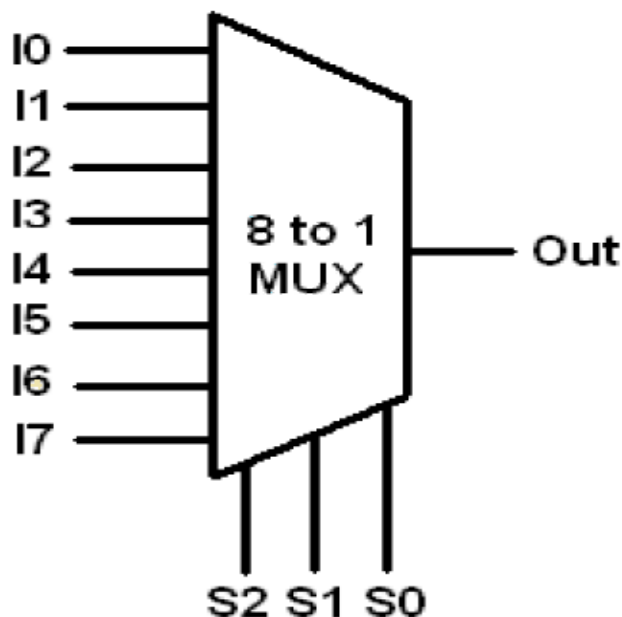


8:1 MUX

8:1 [multiplexer](#) circuit having 8 input lines $I_0, I_1, I_2, \dots, I_7$, one enable input (E), single output line (Y) and three select line (S_0, S_1, S_2).

8:1 mux having 3 select lines. So, we can select any one of the input (depend on the value of select line) by moving the dialer we can have a input at the output. Dialer move and select input depend on the value of select line.

The one more input of multiplexer is Enable input (E). The function of Enable input is to enable the circuit it means, if $E=1$ (enable input is high) circuit operate and the output of the circuit is depends on the value of select line. If $E=0$ (enable input is low) circuit not operate and output of the multiplexer is zero its not depend on the value of select line



RTL CODE:

```
module mux(input [7:0]i,input[2:0]s,output reg y);  
  
    always @( * )  
  
        begin
```

```
case({s})  
    3'b000: y=i[0];  
    3'b001: y=i[1];  
    3'b010: y=i[2];  
    3'b011: y=i[3];  
    3'b100: y=i[4];  
    3'b101: y=i[5];  
    3'b101: y=i[6];  
    3'b111: y=i[7];  
  
endcase  
  
end  
  
endmodule
```

TESTBENCH:

```
module test;  
  
    reg [7:0]i;  
    reg [2:0]s;  
    wire y;  
    mux a1(i,s,y);  
  
    initial begin  
        $dumpfile("dump.vcd");
```

```
$dumpvars(1);
```

```
end
```

```
initial begin
```

```
s[2]=0;s[1]=0;s[0]=0;i[0]=1;i[1]=0;i[2]=0;i[3]=0;i[4]=0;i[5]=0;i[6]=0;
```

```
#10 s[2]=0;s[1]=0;s[0]=1;i[0]=0;i[1]=1;i[2]=0;i[3]=0;i[4]=0;i[5]=0;i[6]=0;
```

```
#10 s[2]=0;s[1]=1;s[0]=0;i[0]=0;i[1]=0;i[2]=1;i[3]=0;i[4]=0;i[5]=0;i[6]=0;
```

```
#10 s[2]=0;s[1]=1;s[0]=1;i[0]=0;i[1]=0;i[2]=0;i[3]=1;i[4]=0;i[5]=0;i[6]=0;
```

```
#10 s[2]=1;s[1]=0;s[0]=0;i[0]=0;i[1]=0;i[2]=0;i[3]=0;i[4]=1;i[5]=0;i[6]=0;
```

```
#10 s[2]=1;s[1]=0;s[0]=1;i[0]=0;i[1]=0;i[2]=0;i[3]=0;i[4]=0;i[5]=1;i[6]=0;
```

```
#10 s[2]=1;s[1]=1;s[0]=0;i[0]=0;i[1]=0;i[2]=0;i[3]=0;i[4]=0;i[5]=0;i[6]=1;
```

```
#60 $finish();
```

```
end
```

```
endmodule
```

