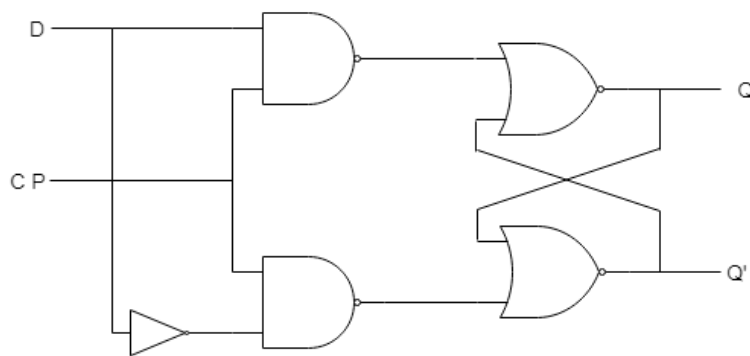


## D FILP FLOP

A flip flop can store one bit of data. Hence, it is known as a memory cell. [Flip-flops](#) are synchronous circuits since they use a clock signal. Using flip flops, we build complex circuits such as RAMs, [Shift Registers](#), etc.

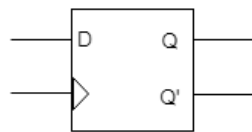
A D flip-flop stands for data or delay flip-flop. The outputs of this flip-flop are equal to the inputs.



(a) Logic diagram with Nand gates

Q D	Q (t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Transition table



(b) Graphic Symbol

fig. Clocked D flip flop

## RTL CODE:

```
module t1s(input clk,rst,d,output reg q,output reg qb);  
  always @(posedge clk)  
  begin  
    if(rst==1)begin  
      q<=0;  
      qb<=1;  
    end  
    else
```

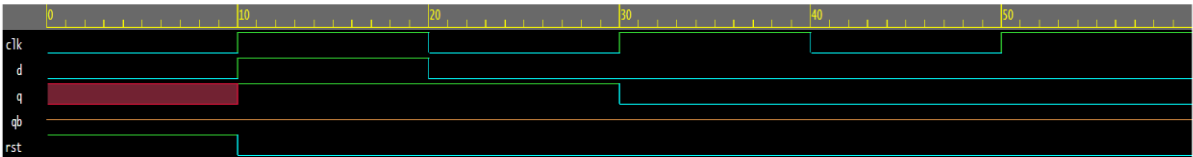
```

        begin
            q<=d;
            qb=!d;
        end
    end
endmodule

TEST BENCH:
module test;
    reg clk,rst,d;
    wire q,qb;
    t1s a(clk,rst,d,q);
    initial begin
        $dumpfile("dump.vcd");
        $dumpvars(1);
    end
    initial begin
        clk=0;
        forever #10 clk=~clk;
    end
    initial begin
        rst=1;d=0;
        #10 rst=0;d=1;
        #10 d=0;
    end
    initial begin
        #60 $finish();
    end
end

```

endmodule



Note: To revert to EPiWave opening in a new browser window, set that option on your user page.