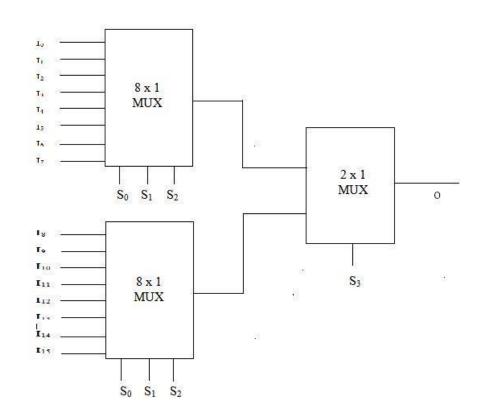
16X1 MUX USING 8X1 AND 2X1 MUX

The diagram will be same as of the block diagram of 16-to-1 line multiplexer in which 8-to-1 line multiplexer Selection lines will be S_0 – S_2 and S_3 will be connected to 2-to-1 line multiplexer Selection and First 8-to-1 line multiplexer Input lines will be I_0 – I_7 and Second8-to-1 line multiplexer Input lines will be I_8 – I_{15}



RTL CODE:

```
module mux(input i1,input i2,input s,output y);
assign y=s?i2:i1;
endmodule
```

```
module mux1(input [7:0]i,input [2:0]s,output reg y);
 always @(*) begin
  case(s)
   3'b000: y=i[0];
   3'b001: y=i[1];
   3'b010: y=i[2];
   3'b011: y=i[3];
   3'b100: y=i[4];
   3'b101: y=i[5];
   3'b110: y=i[6];
   3'b111: y=i[7];
  endcase
 end
endmodule
module mux_2(input [15:0]i,input [3:0]s,output y);
 wire y1,y2;
 mux1 m1(i[15:8],s[2:0],y1);
 mux1 m2(i[7:0],s[2:0],y2);
 mux m3(y1,y2,s[3],y);
endmodule
TESTBENCH:
module test;
```

```
reg [15:0]i;
 reg [3:0]s;
 wire y;
 mux_2 h1(i,s,y);
 initial begin
  $dumpfile("dump.vcd");
  $dumpvars(1);
 end
 initial begin
  i=16'b11110000111110000;
  s=4'b0000;
  #10 s=4'b0001;i=16'b0001100110010000;
  #10 s=4'b0010;i=16'b0000111100110011;
  #200 $finish();
 end
endmodule
```