MOD 2 COUNTER

RTL CODE:

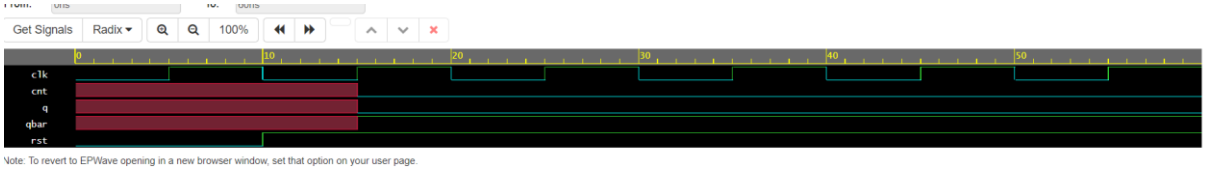
```
module test(input clk,rst,d,output reg q,output reg qbar);
  always@(posedge clk)begin
    if(rst)
      q<=0;
    else begin
      q<=d;
    end
    assign qbar=~q;
  end
endmodule
module syn(input clk,rst,output q,qbar,output cnt);
  wire d;
  test a1(clk,rst,d,q,qbar);
  assign d=qbar;
  assign cnt=q;

endmodule
```

TESTBENCH:

```
module tls;
  reg clk,rst;
  wire q,qbar,cnt;
  syn a1(clk,rst,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
```

```
  end
  initial begin
    clk=0;
    forever #5 clk=~clk;
  end
  initial
    begin
      repeat(5) begin
        rst=$random;
        #10;
      end
    end
  initial
    begin
      #60 $finish();
    end
endmodule
```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.