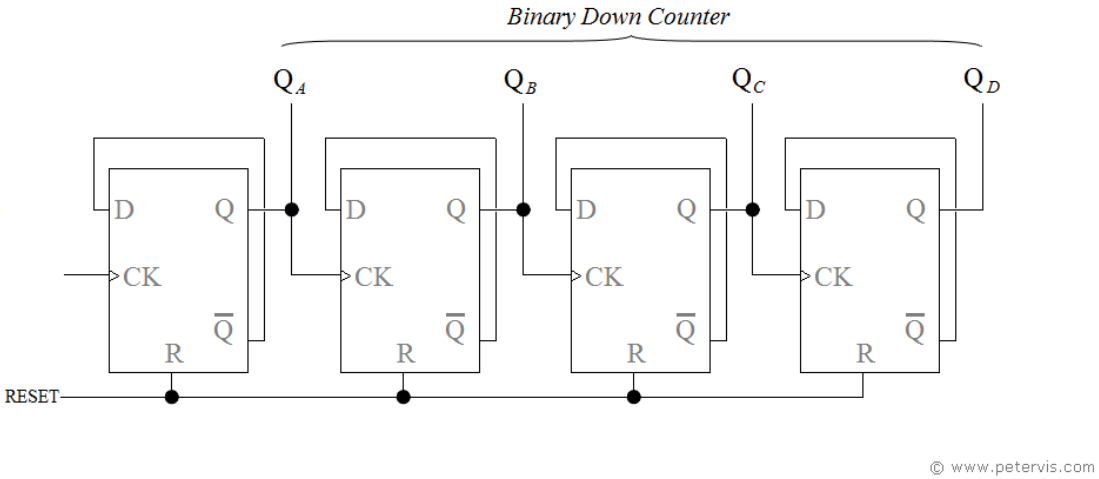
4-BIT ASYNCHRONOUS DOWN COUNTER



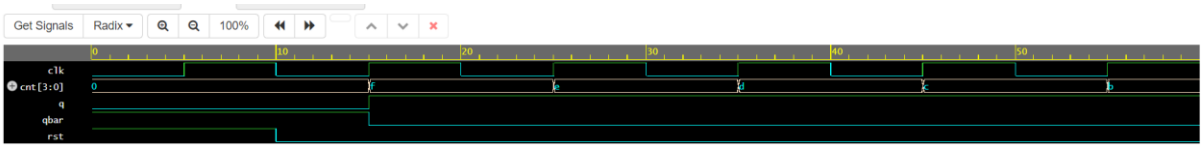
RTL CODE:

```
module test(input clk,rst,d,output reg q,output reg qbar);
  always@(posedge clk or posedge rst)begin
    if(rst)
      q<=0;
    else begin
      q<=d?1:0;
    end
    assign qbar=~q;
  end
endmodule
module syn(input clk,rst,output q,qbar,output [3:0]cnt);
  wire [3:0]d;
  wire q0,q0bar,q1,q1bar,q2,q2bar;
  test a1(clk,rst,d[0],q0,q0bar);
  test a2(q0,rst,d[1],q1,q1bar);
  test a3(q1,rst,d[2],q2,q2bar);
  test a4(q2,rst,d[3],q,qbar);
  assign d[0]=q0bar;
```

```
  assign d[1]=q1bar;
  assign d[2]=q2bar;
  assign d[3]=qbar;
  assign cnt={q,q2,q1,q0};
endmodule
```

TESTBENCH:

```
module tls;
  reg clk,rst;
  wire q,qbar;
  wire [3:0]cnt;
  syn h1(clk,rst,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    forever #5 clk=~clk;
  end
  initial begin
    rst=1;clk=0;
    #10 rst=0;
  end
  initial begin
    #60 $finish();
  end
endmodule
```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.