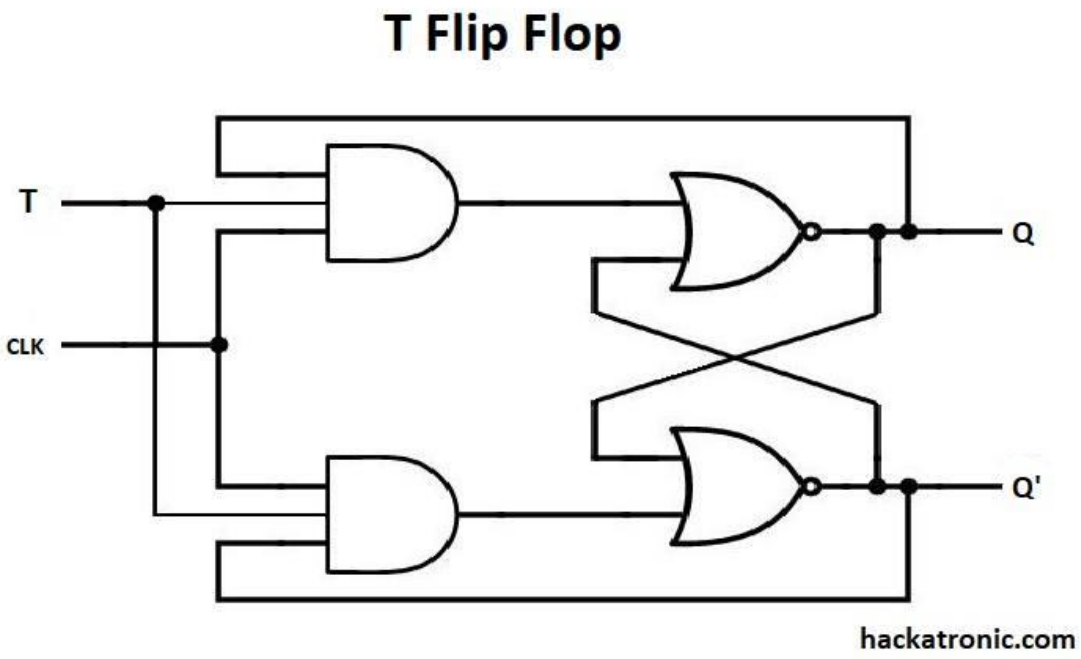
T -FLIP FLOP

T stands for ("toggle") flip-flop to avoid an intermediate state in SR flip-flop. We should provide only one input to the flip-flop called Trigger input Toggle input to avoid an intermediate state occurrence.

Then the flip - flop acts as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as ***Toggling***.

We can construct the T flip-flop by making changes in the ***JK flip-flop***. The T flip-flop has only one input, which is constructed by connecting the input of JK flip-flop. This single input is called T.

The Block diagram of the T flip-flop is given below where T defines the "Toggle" input, and CLK defines the "clock signal" input.



RTL CODE:

```
module tlas(input clk,input rst,input t,output reg q,output reg qb);
  always@(posedge clk)
```

```
    begin
      if(rst)
        q<=0;
      else
        begin
          case(t)
            1'b0:q<=q;
            1'b1:q<=~q;
          endcase
        end
      assign  qb=~q;
      end
endmodule
```

TEST BENCH:

```
module test;
  reg clk,rst,t;
  wire q,qb;
  tlas a1(clk,rst,t,q,qb);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    clk=0;
    forever #10 clk=~clk;
```

```
  end
  initial begin
    rst=0;t=0;
    #10 rst=1;t=0;
    #10 rst=0;t=1;
  end
  initial begin
    #60 $finish();
  end
endmodule
```