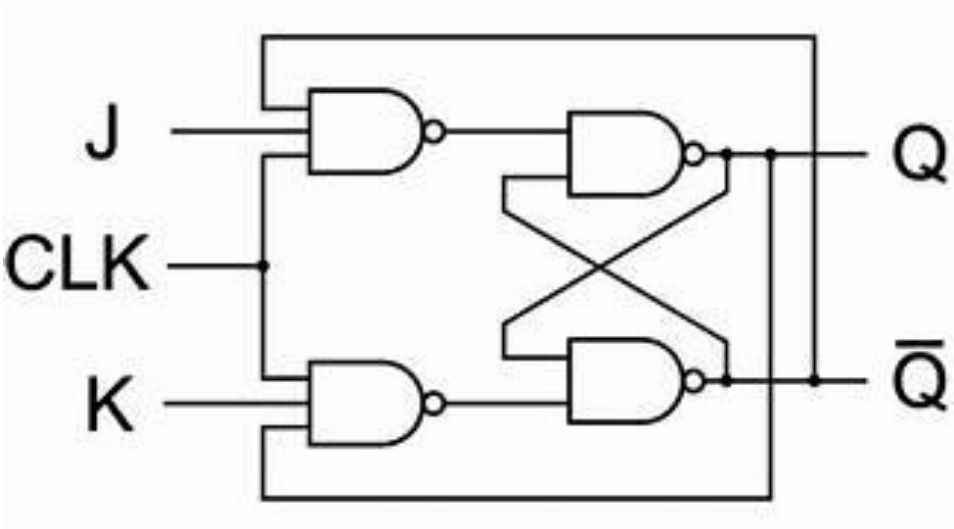
JK FLIP FLOP

Flip-flops are fundamental building blocks of sequential circuits. A flip flop can store one bit of data. Hence, it is known as a memory cell. Since they work on the application of a clock signal, they come under the category of synchronous circuits.

The J-K flip-flop is the most versatile of the basic flip flops. The JK flip flop is a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic 1. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”.



RTL CODE:

```
module tlsa(input clk,input rst,input j,input k,output reg q,output reg qb);
  always@(posedge clk)begin


    if(rst) begin
      q<=0;
    end
    else
      begin
        case({j,k})
          2'b00: q<=q;
          2'b01: q<=0;
```

```
        2'b10: q<=1;
        2'b11: q<=qb;
      endcase
    end
  assign qb=~q;
 end
endmodule
```

TESTBENCH:

```
module test;
 reg clk,rst,j,k;
 wire q,qb;
 tlsa a1(clk,rst,j,k,q,qb);
 initial begin
  $dumpfile("dump.vcd");
  $dumpvars(1);
 end
 initial begin
  clk=0;
  forever #10 clk=~clk;
 end
 initial begin
  repeat(5) begin
   rst=$random;j=$random;k=$random;
   #10;
  end
```

```
  end
  initial begin
    #60 $finish();
  end
endmodule
```