# 4 BIT UP-DOWN COUNTERS

## RTL CODE:

```
module up_down(input clk,rst,updown,output reg [3:0]cnt);
  always@(posedge clk)begin
    if(rst)
      cnt<=0;
    else if(updown==1 && cnt>=0 && cnt<16)
      cnt<=cnt+1;
    else if(updown==0 && cnt>=0 && cnt<16)
      cnt<=cnt-1;
    else
      cnt<=0;
  end
endmodule
```

**TEST BENCH:**

```
module test;
  reg clk,rst,updown;
  wire [3:0]cnt;
  up_down a1(clk,rst,updown,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    clk=0;
    forever #5 clk=~clk;
  end
  initial begin
    repeat(5)
      begin
        rst=$random;updown=$random;
```

```
        #10;
      end
  end
  initial begin
    #60 $finish();
  end
endmodule
```