# 4-BIT ASYNCHRONOUS UP COUNTER

## III. Operation of Counter

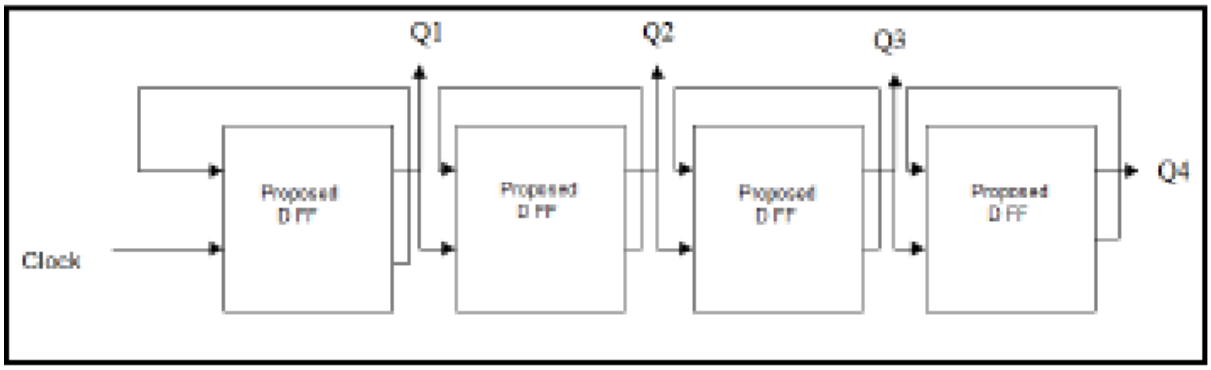



Fig. 3: Up Counter Using D Flip-Flop

## RTL CODE

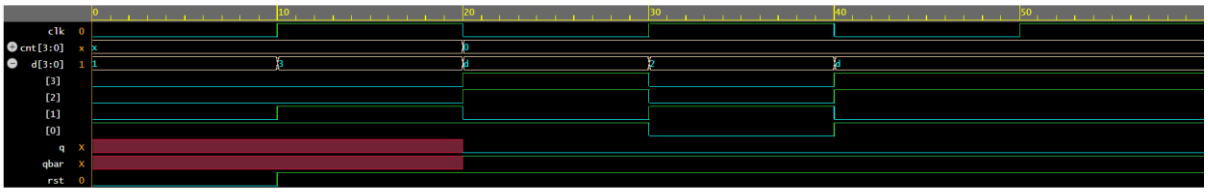
```
module tls( input clk,rst,d,output reg q,output qbar);
  always@(negedge clk)begin
    if(rst)
      q<=0;
    else
      q<=d;
  end
  assign qbar=~q;
endmodule
module asy(input clk,rst,[3:0]d,output q,qbar,output[3:0]cnt);
  wire q0,q0bar,q1,q1bar,q2,q2bar;
  tls a1(clk,rst,d[0],q0,q0bar);
  tls a2(q0,rst,d[1],q1,q1bar);
  tls a3(q1,rst,d[2],q2,q2bar);
  tls a4(q2,rst,d[3],q,qbar);
  assign d[0]=q0bar;
  assign d[1]=q1bar;
```

```
  assign d[2]=q2bar;
  assign d[3]=qbar;
  assign cnt={q,q2,q1,q0};
endmodule
```

**TESTBENCH**

```
module test;
  reg clk,rst;
  reg [3:0]d;
  wire q,qbar;
  wire [3:0]cnt;
  asy h1(clk,rst,d,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    clk=0;
    forever #10 clk=~clk;
  end
  initial begin
    repeat(5)begin
      rst=$random;d=$random;
      #10;
    end
  end
  initial begin
    #60 $finish();
```

```
  end
endmodule
```




Note: To revert to EPWave opening in a new browser window, set that option on your user page.