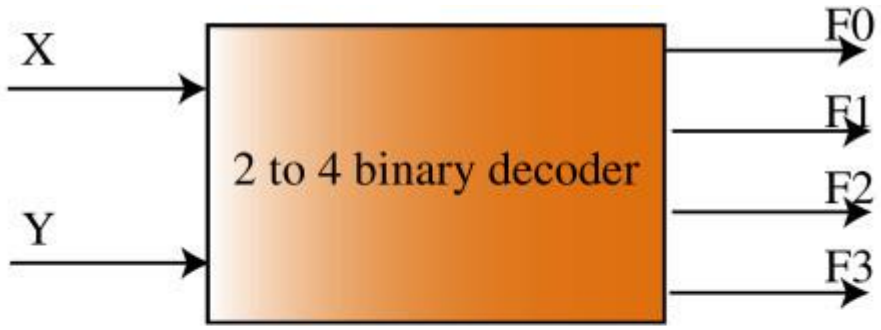
2:4 DECODER

A decoder is a combinational logic circuit that has 'n' input signal lines and 2^n output lines. In the 2:4 decoder, we have 2 input lines and 4 output lines. In addition, we provide '*enable*' to the input to ensure the decoder is functioning whenever enable is 1 and it is turned off when enable is 0. The truth table, logic diagram, and logic symbol are given below:



X	Y	F0	F1	F2	F3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

RTL CODE:

```
module tal(input en,input [1:0]a,output reg [3:0]y);
  always @(*)
    begin
      if(en)begin
        case(a)
```

```
        2'b00: y=4'b0001;
        2'b01: y=4'b0010;
        2'b10: y=4'b0100;
        2'b11: y=4'b1000;
      endcase
    end
    else
      y=4'b1111;
  end
endmodule
```

TESTBENCH:

```
module test;
  reg en;
  reg [1:0]a;
  wire [3:0]y;
  tal t1(en,a,y);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    a=2'b00;en=0;
    #10 a=2'b00;en=1;
    #10 a=2'b01;en=1;
    #10 a=2'b10;en=1;
```

```
    #10 a=2'b11;en=1;
  end
  initial begin
    #60 $finish();
  end
endmodule
```