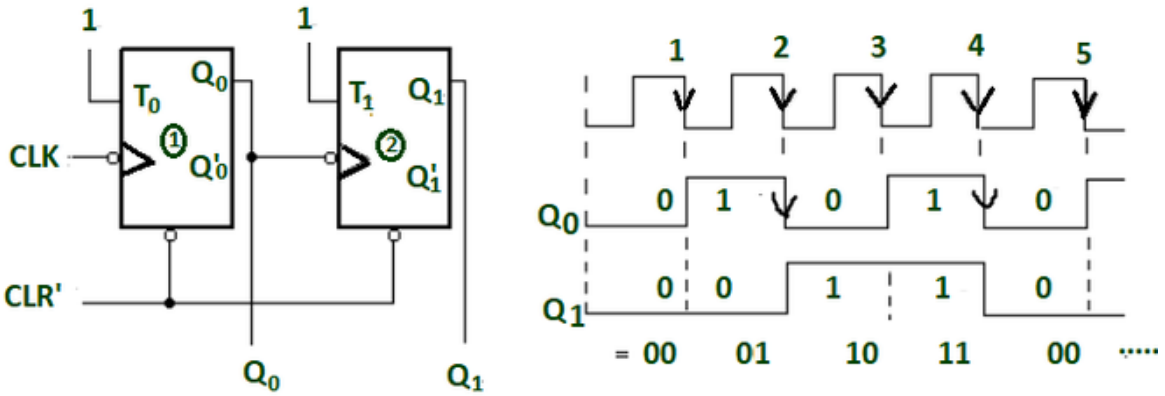
2 BIT ASYNCHRONOUS UP COUNTER



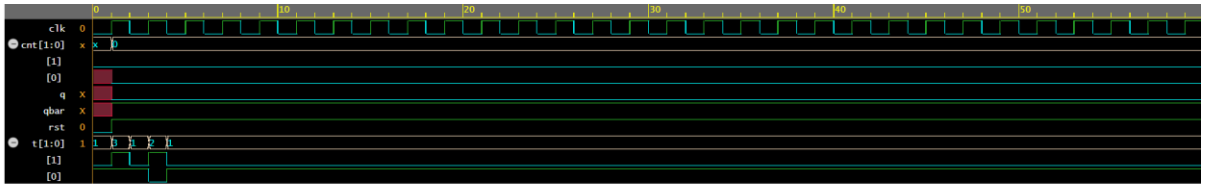
RTL CODE:

```
module ttf(input clk,rst,t,output reg q,output reg qbar);
  always@(posedge clk)begin
    if(rst)
      begin
        q<=0;
      end
    else
      begin
        q=t?~q:q;
      end
    assign qbar=~q;
    end
endmodule
module ansyy(input clk,rst,[1:0]t,output q,qbar,[1:0]cnt);
  wire a,b;
  ttf a1(clk,rst,t[0],a,b);
  ttf a2(b,rst,t[1],q,qbar);
  assign cnt={q,a};
```

```
endmodule
```

TESTBENCH:

```
module test;
  reg clk,rst;
  reg [1:0]t;
  wire q,qbar;
  wire [1:0]cnt;
  ansyy h1(clk,rst,t,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    clk=0;
    forever #1 clk=~clk;
  end
  initial begin
    repeat(5)begin
      rst=$random;t=$random;
      #1;
    end
  end
  initial begin
    #60 $finish();
  end
endmodule
```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.