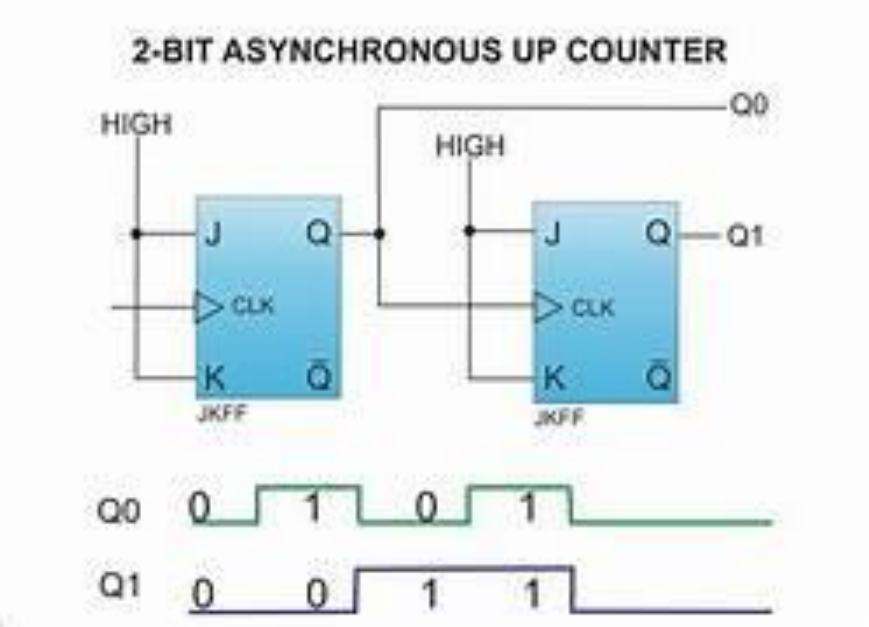
# 2 Bit Synchronous Counter




RTL CODE:

```
module ttf(input clk,rst,d,output reg q,output reg qbar);
  always@(negedge clk)begin
    if(rst)
      begin
        q<=0;
      end
    else
      begin
        q=d;
      end
    assign qbar=~q;
    end
```

```
endmodule
module ansyy(input clk,rst,[1:0]d,output q,qbar,[1:0]cnt);
  wire a,b;
  wire c,h,e,f;
  ttf a1(clk,rst,a,c,h);
  ttf a2(clk,rst,b,e,f);
  assign a=~c^e;
  assign b=f;
  assign cnt={c,e};
endmodule
```

**TESTBENCH:**

```
module test;
  reg clk,rst;
  reg [1:0]d;
  wire q,qbar;
  wire [1:0] cnt;
  ansyy a1(clk,rst,d,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
```

```
    clk=0;
    forever #10 clk=~clk;
  end
  initial begin
    repeat(5) begin
      rst=$random;d=$random;
      #10;
    end
  end
  initial begin
    #60 $finish();
  end
endmodule
```