

## LOOK A-HEAD CARRY ADDER

The drawback of '[Ripple carry adder](#)' is that it has a carry propagation delay that introduces slow computation. Since adders are used in designs like multipliers and divisions, it causes slowness in their computation. To tackle this issue, a carry look-ahead adder (CLA) can be used that reduces propagation delay with additional hardware complexity.

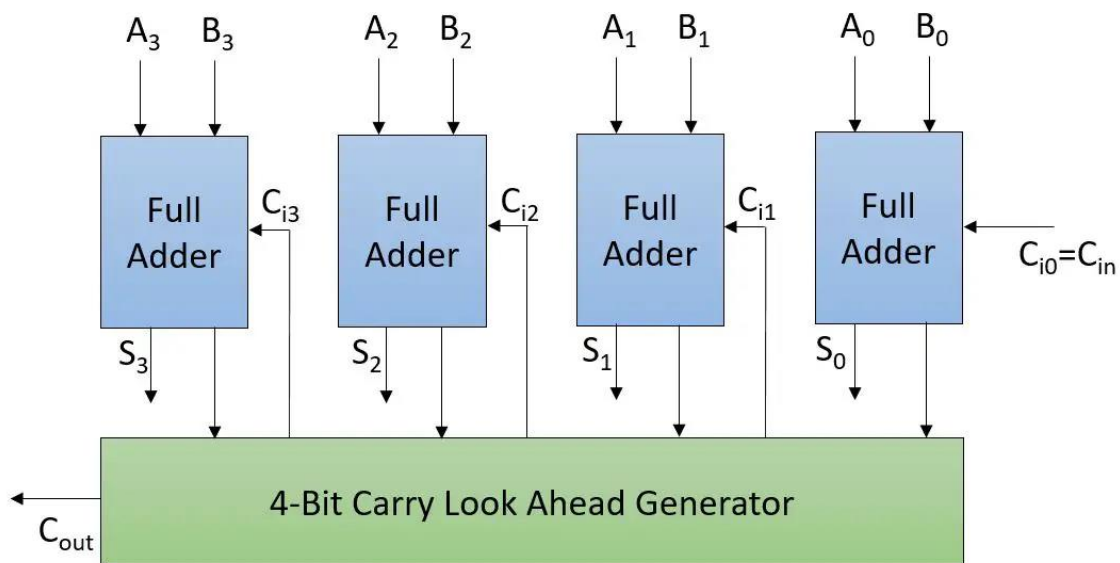
CLA has introduced some functions like 'carry generate (G)' and 'carry propagate (P)' to boost the speed.

**Carry Generate (G):** This function denotes how the carry is generated for single-bit two inputs regardless of any input carry.

As we have seen in the full adder, carry is generated using the equation as  $A \cdot B$ .

Hence,  $G = A \cdot B$  (similar to how carry is generated by full adder)

**Carry Propagate (P):** This function denotes when the carry is propagated to the next stage with an addition whenever there is an input carry.



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4-Bit Carry Look Ahead Adder

### RTL CODE:

```
module CarryLookAheadAdder(  
    input [3:0]A, B,  
    input Cin,
```

```

output [3:0] S,
output Cout
);

wire [3:0] Ci;

assign Ci[0] = Cin;
assign Ci[1] = (A[0] & B[0]) | ((A[0]^B[0]) & Ci[0]);
assign Ci[2] = (A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) &
Ci[0])));
assign Ci[3] = (A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) &
((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))));
assign Cout = (A[3] & B[3]) | ((A[3]^B[3]) & ((A[2] & B[2]) | ((A[2]^B[2])
& ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0]))))));

assign S = A^B^Ci;
endmodule

```

### TESTBENCH:

```

module TB;

reg [3:0] A, B;
reg Cin;
wire [3:0] S;
wire Cout;

CarryLookAheadAdder cla(A, B, Cin, S, Cout);

initial begin

```

```

$dumpfile("dump.vcd");
$dumpvars(1);
end

initial begin
    $monitor("A = %b: B = %b, Cin = %b --> S = %b, Cout = %b, Addition =
%0d", A, B, Cin, S, Cout);

    A = 1; B = 0; Cin = 0; #3;
    A = 2; B = 4; Cin = 1; #3;
    A = 4'hb; B = 4'h6; Cin = 0; #3;
    A = 5; B = 3; Cin = 1;

end

endmodule

```

