K-map for C:

Z8 Z4 \ Z2 Z1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

Exp No.:	DESIGN OF BCD ADDER
Date :	

AIM:

To design and implement BCD adder IC 7483.

APPARATUS REQUIRED:

S.No.	Component	Specification	Qty.
1.	IC	IC 7483	2
2.	EX-OR GATE	IC 7486	1
3.	AND GATE	IC 7408	1
3.	IC TRAINER KIT	-	1
4.	Patch Cords	-	Adequate

THEORY:

BCD ADDER:

BCD adder is a circuit that performs the addition of two BCD numbers in parallel. BCD additions are performed in 4-bit binary form so there is a possibility of increasing binary number greater than 9 that results wrong output. To avoid this, in BCD addition correction logic I included as described below,

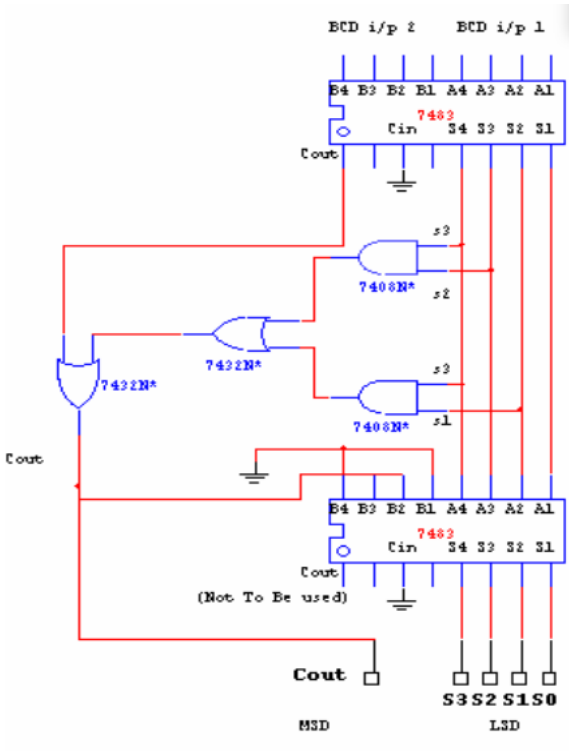
1. If the binary sum is equal or less than 9 with carry 0, then that binary sum is correct BCD sum.
2. I the binary sum is equal or less than 9 with carry 1, then that binary sum is an incorrect BCD sum. To get the correct BCD sum add 0110 with least significant binary sum digits.
3. If the binary number is greater than 9, then that binary sum is an incorrect BCD sum. To get the correct BCD sum add 0110 with binary sum digits.

BCD adder can be constructed with three blocks such as two binary adders and the correction logic circuit. Initially in the BCD adders, the four bit binary numbers are added using parallel binary adder and then, the binary output is checked to correct as BCD number. The correction logic generates the correction code based on the binary output values. When we get the incorrect binary output as per the condition described above, the correction code is added with the binary output to get the correct BCD number through second binary adder.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Apply the logical Input data and verify the corresponding output.

LOGIC DIAGRAM:BCD ADDER



TRUTH TABLE:

Binary sum					BCD sum					Decimal
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13

0	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**14**
0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**15**
1	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**16**
1	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**17**
1	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**18**
1	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**19**

RESULT:

Thus the BCD circuit were designed and implemented using IC 7483 and logic gates.