

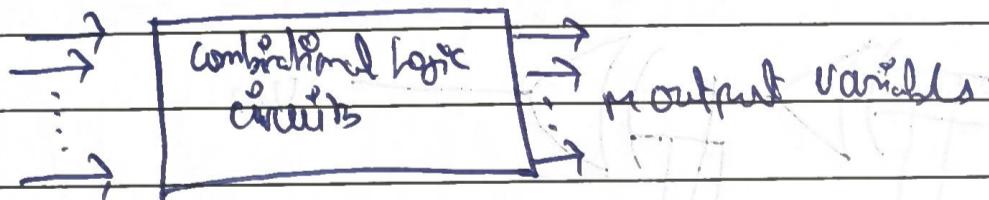
Unit-1

Topics to cover

- * Combinational Circuits ✓
- * K-Map ✓
- * Analysis and Design procedures ✓
- * Binary Adder ✓
- * Subtractor ✓
- * Decimal Adder ✓
- * Magnitude Comparison ✓
- * Decoder ✓
- * Encoder ✓
- * Mux ✓
- * Demux ✓

Combinational circuits

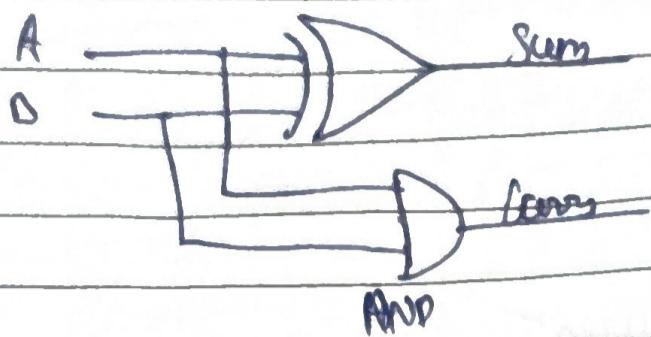
* It consists of basic logic gates, the output is determined by the current input not previous (Q₀ and Q₁)



Adders (Half Adders)

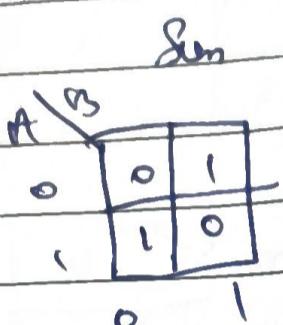
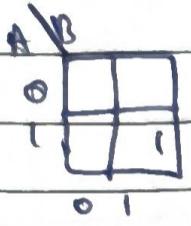
- * It adds two single bits
- * 2 inputs and 2 outputs (Sum, Carry)
- * Boolean Expression
 - o Sum = $A \oplus B$ (or Sum = $AB + \bar{A}\bar{B}$)
 - o Carry = AB

Diagrams



		Truth Table	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

R-map Carry



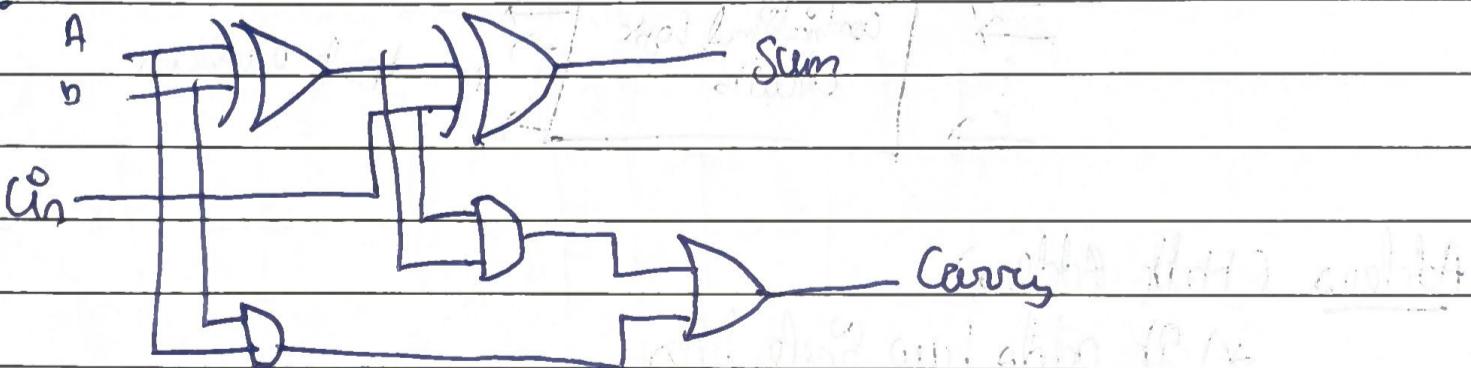
Full Adder:

- * It adds three bits
- * 3 inputs 2 outputs
- * Implemented by joining two half adders
- * Boolean expression

$$\text{Sum} = \text{Cin} \oplus (\text{A} \oplus \text{B})$$

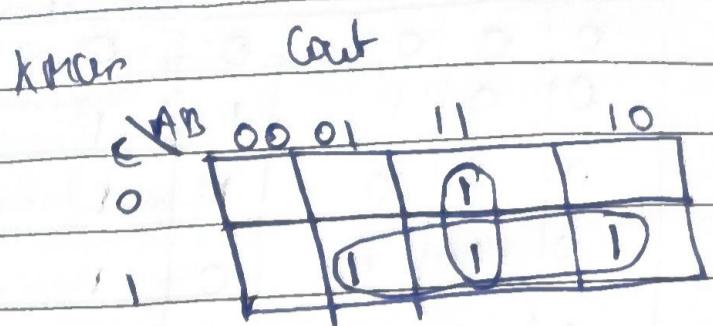
$$\text{Out} = \text{AB} + \text{Cin}(\text{A} + \text{B})$$

Diagram:



Truth table

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

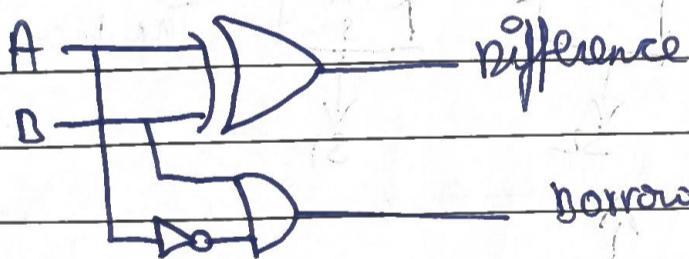


$$\text{Out} = AB + DC_{in} + AC_{in}$$

Draw k-map for sum too.

Subtractor

Half Subtractor

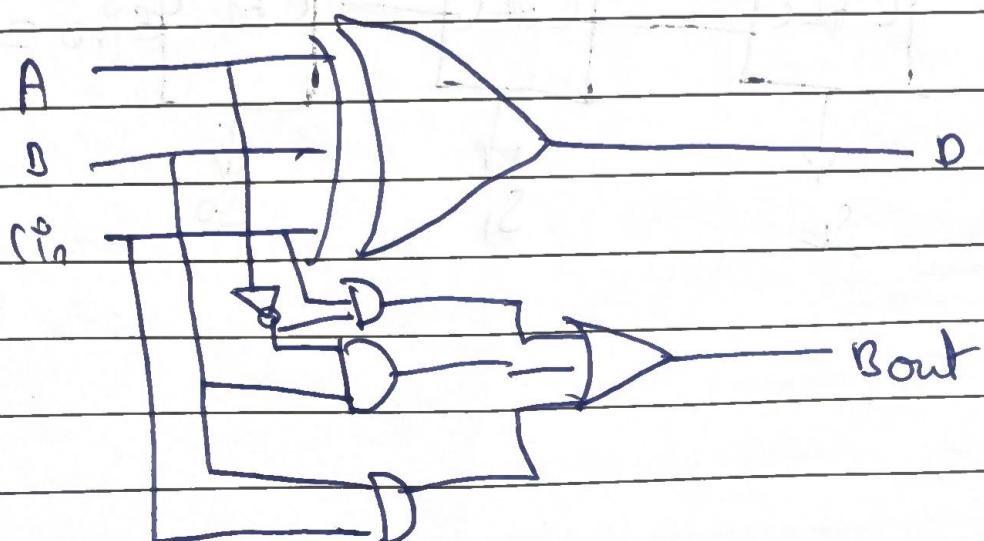


Truth table

A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

k-map (you know how to draw k-map!)

Full Subtractor

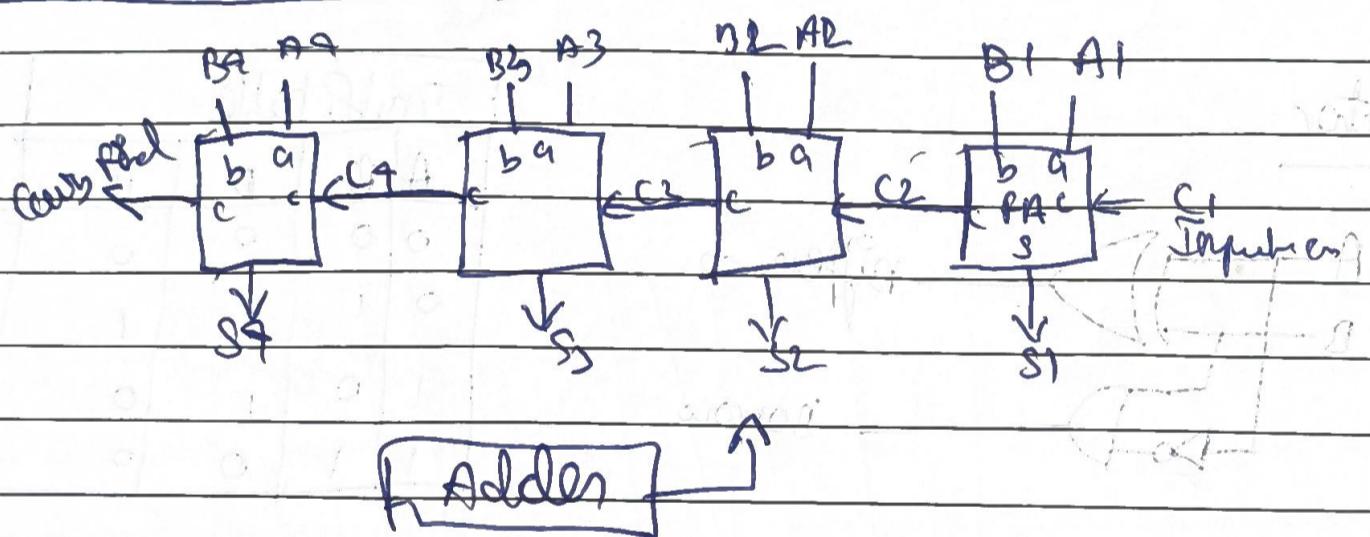


Truth table

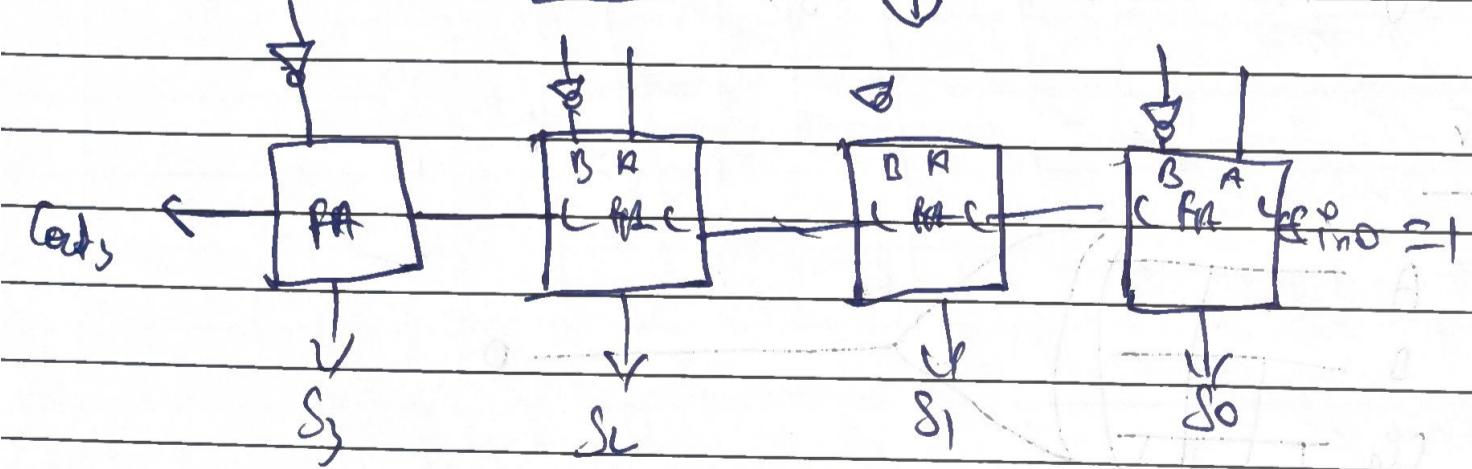
A	B	B_{in}	D	Sum
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Draw K map then

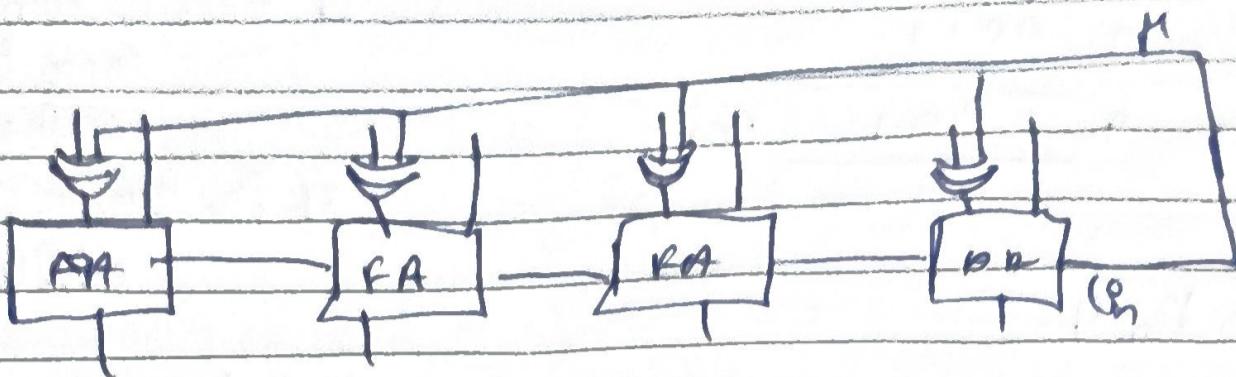
Parallel Adder - Subtractor



Subtractor



Both parallel binary adder and subtractor



M=0 Adder

M=1 Subtractor

BCD Adder

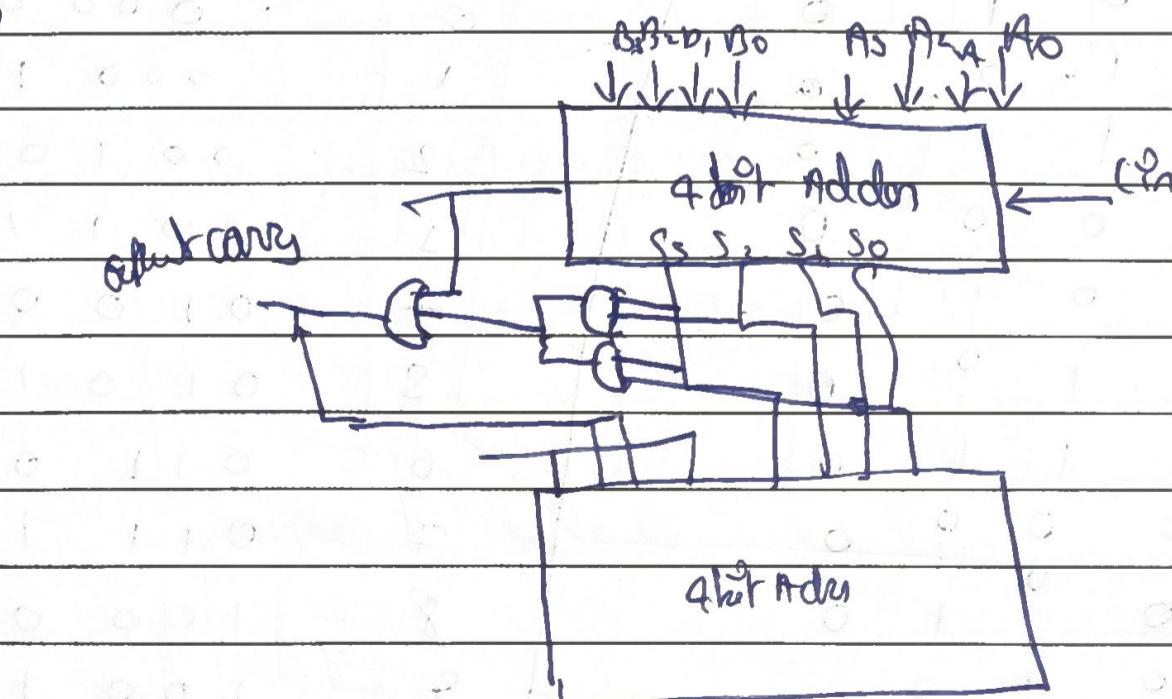
Binary coded decimal

* Adds two BCD numbers

* correction logic: If the 4 bit sum is greater than 9 or if a carry is generated, add 010₂ (6) for correction

* The logic circuit to detect sum > 9 uses output $V = S_3 S_2 + S_3 S_1$

Diagram



M	T	W	T	F	S
Page No.:	YOUVA				
Date:					

Adders and Sub

$$\begin{array}{r}
 6 \ 0110 \\
 3 \ 0011 \\
 \hline
 + 1001 \quad \text{Ans}
 \end{array}$$

rule: Add using normal

if 4 bit is zero

correction is
needed

if it is greater than 9
add (0110)6

But if it is greater than 9

$$\begin{array}{r}
 6 \ 0110 \\
 9 \ 1000 \\
 \hline
 14 \ 1110 \\
 - 0011 \\
 \hline
 0110
 \end{array}$$

use decimal to binary
converter

invalid BCD then add 6 for
correction

Truth table

S ₄	S ₃	S ₂	S ₁	S ₀	V	Inputs
0	0	0	0	0	0	000000
0	0	0	1	0	0	000100
0	0	1	0	0	1	001000
0	0	1	1	0	2	001100
0	1	0	0	0	3	010000
0	1	0	1	0	4	010100
0	1	1	0	0	5	011000
0	1	1	1	0	6	011100
1	0	0	0	0	7	101100
1	0	0	1	0	8	100000
1	0	1	0	1	9	100100
1	0	1	1	1	10	101000
1	1	0	0	1		110000
1	1	0	1	1		111000
1	1	1	0	1		111100

Received binary

0 8421 0

0 0000 213
0001 [1-1]

2 0010

3 0001 1

4 0100

5 0101

6 0110

7 0111 1

8 1000 0

9 1001 1

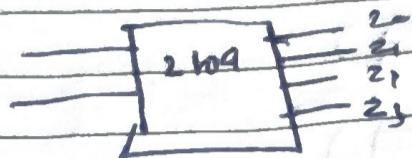
10

$$\begin{array}{r}
 26 - 101 \\
 23 - 0 \\
 \hline
 1-1
 \end{array}$$

Decoders and Encoders

Decoder:

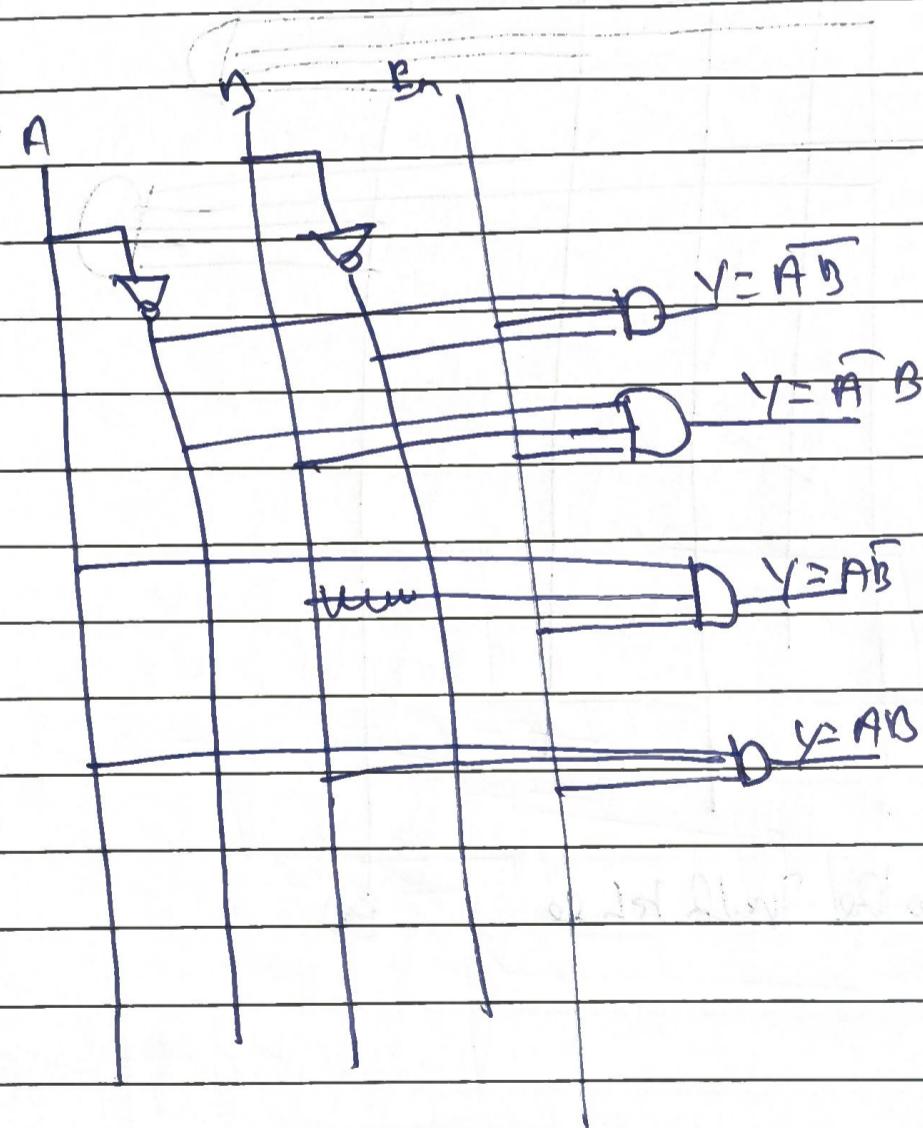
Combines N inputs and give 2^n outputs.



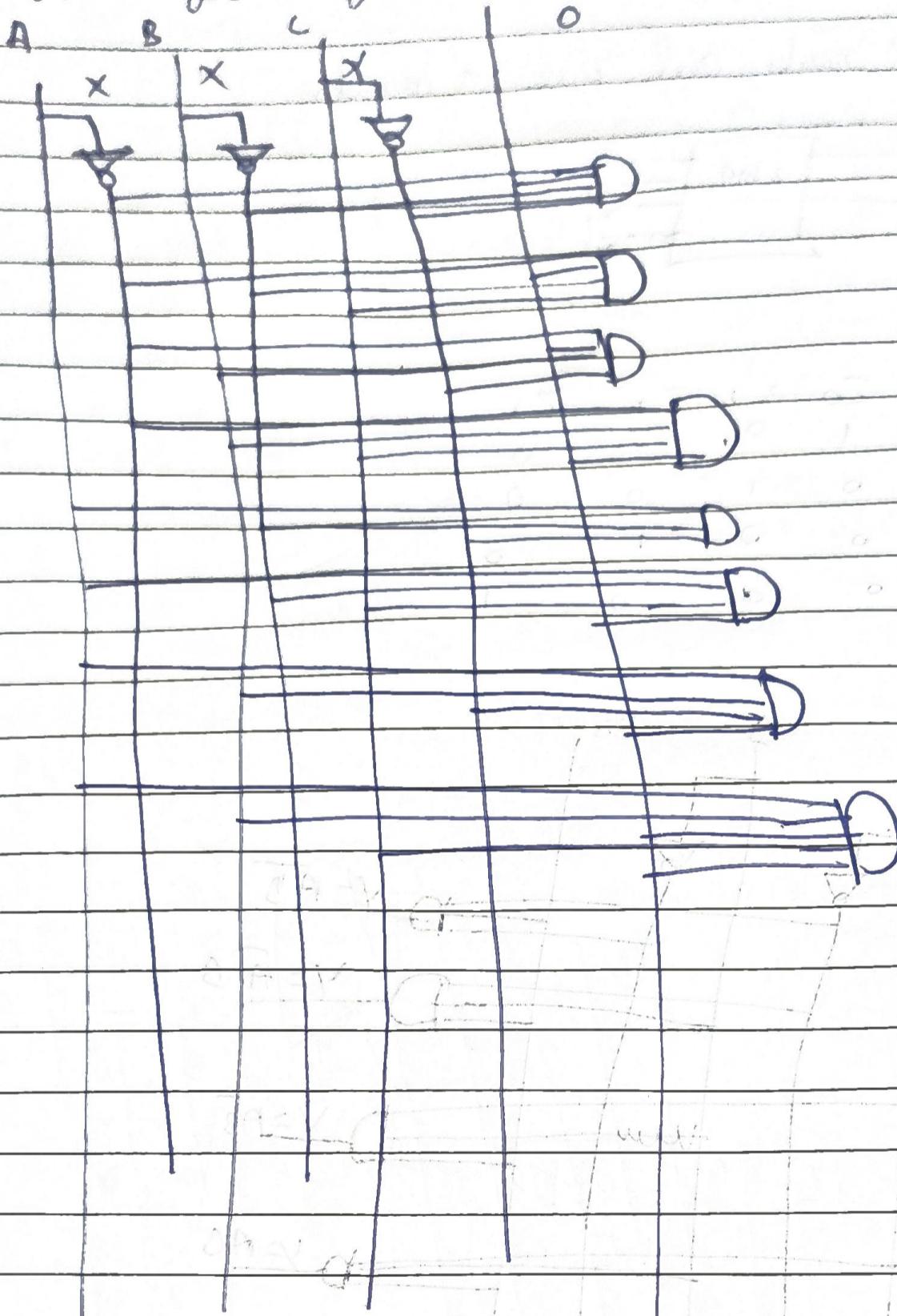
Truth table

A	B	Z_0	Z_1	Z_2	Z_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Logic diagram



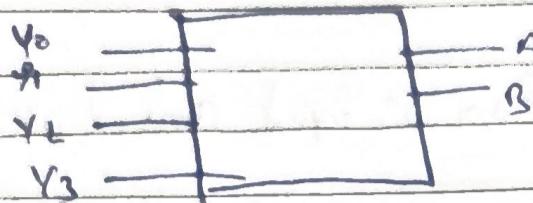
If it has three inputs then it has 8 output
and draw logic diagram SN



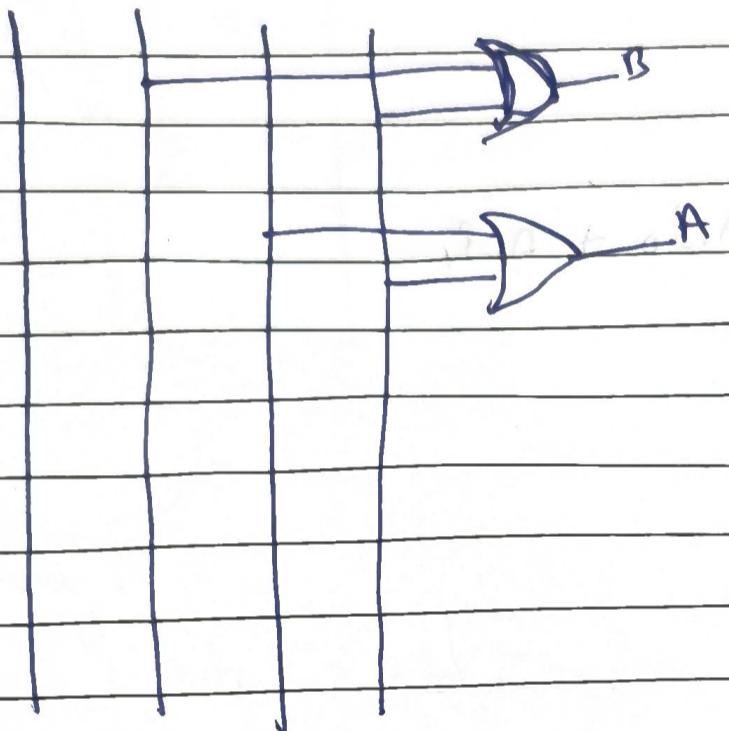
Draw according to the Truth table EN

Encoder

Take 2^n inputs and give n output



$Y_0 \quad Y_1 \quad Y_2 \quad Y_3$



Truth Table

Y_0	Y_1	Y_2	Y_3	A	B
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

So students drew for all types

Tip

Draw truth table for logic diagram accord

Priority encoder

In Truth Table

all below 1's don't care
and has an active

If it has 4 inputs draw
another line in table as 0
everywhere first

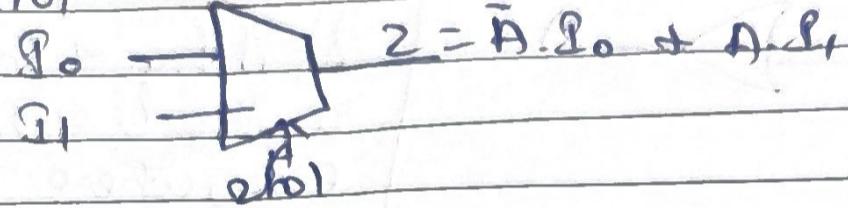
It has one valid bit

MUX-DEMUX

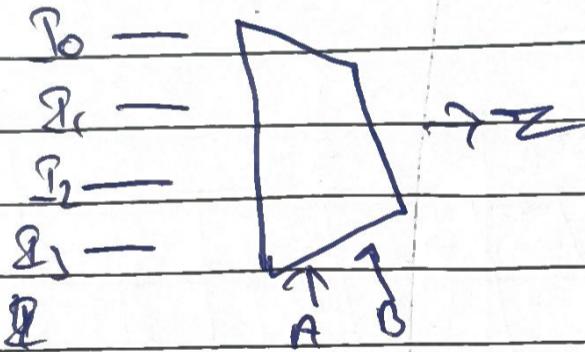
Multiplexer (Mux)

- * i) Selects binary information from 2ⁿ input and make them as single output
- * ii) control lines : n select lines control input selection
- * iii) 2 to 1 Mux
- * iv) 4 to 1 Mux and Out

2 to 1



4 to 1



A	B	Z
0	0	S ₀
0	1	S ₁
1	0	S ₂
1	1	S ₃

$$Z = \bar{A}\bar{B} \cdot S_0 + \bar{A}B \cdot S_1 + A\bar{B} \cdot S_2 + AB \cdot S_3$$

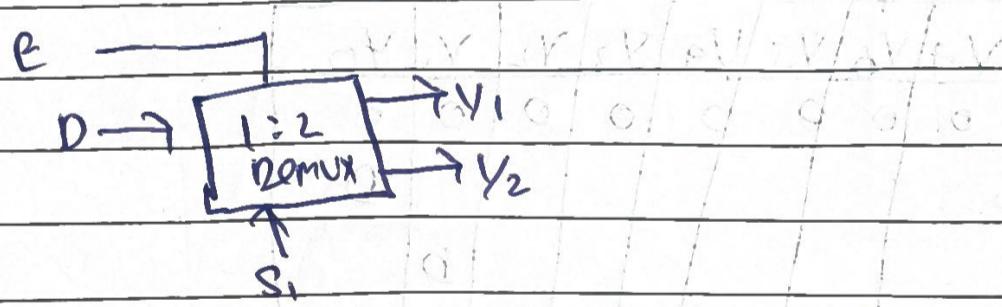
and it is also known as
as 1-bit selector device

8 to 1 Mux same as others but it has 3 input select and 8 outputs

A	B	C	Z
0	0	0	g ₀
0	0	1	g ₁
0	1	0	g ₂
0	1	1	g ₃
1	0	0	g ₄
1	0	1	g ₅
1	1	0	g ₆
1	1	1	g ₇

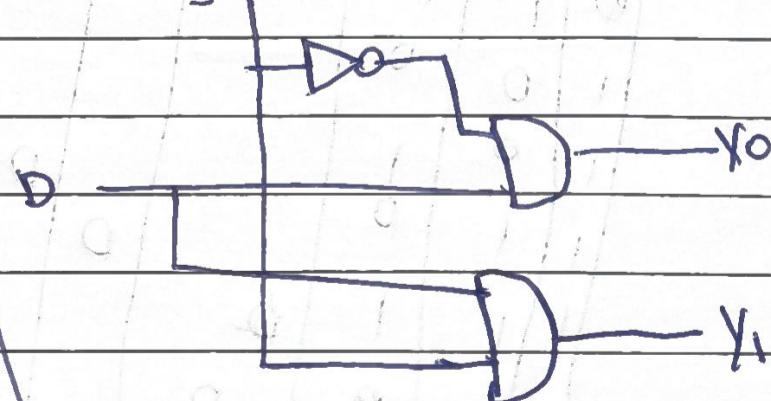
De Multiplexer

It has 2^2 outputs 2 select lines one input

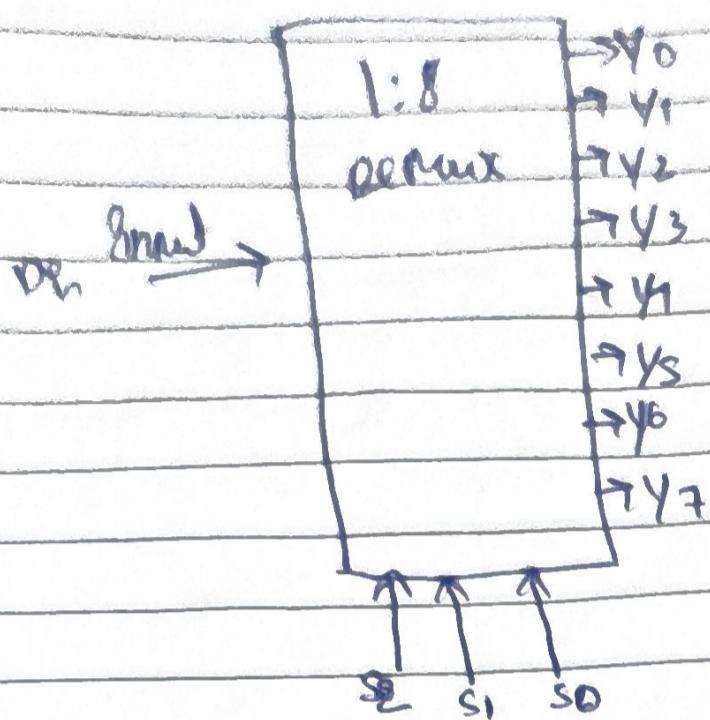


Select	Input	outputs	
S	D	Y ₁	Y ₀
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

Diagram's



Encoder bit has code in binary



Truth table 3

Digitalized Select inputs output

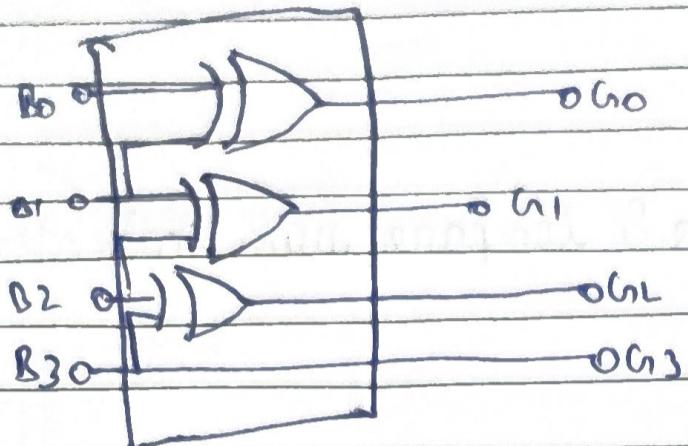
D S2 S1 S0 Y4 Y6 Y5 Y4 Y3 Y2 Y1 Y0

Data Input	Select Input			Output							
b	S ₂	S ₁	S ₀	Y ₄	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
D	0	0	0	0	0	0	0	0	0	0	0
D	0	0	0								b
D	0	0	1								b
D	0	1	0								D
D	0	1	1								D
D	1	0	0								D
D	1	0	1								D
b	1	1	0								0
b	1	1	1								0
b	1	1	1	0	0	0	0	0	0	0	0

Other are zero

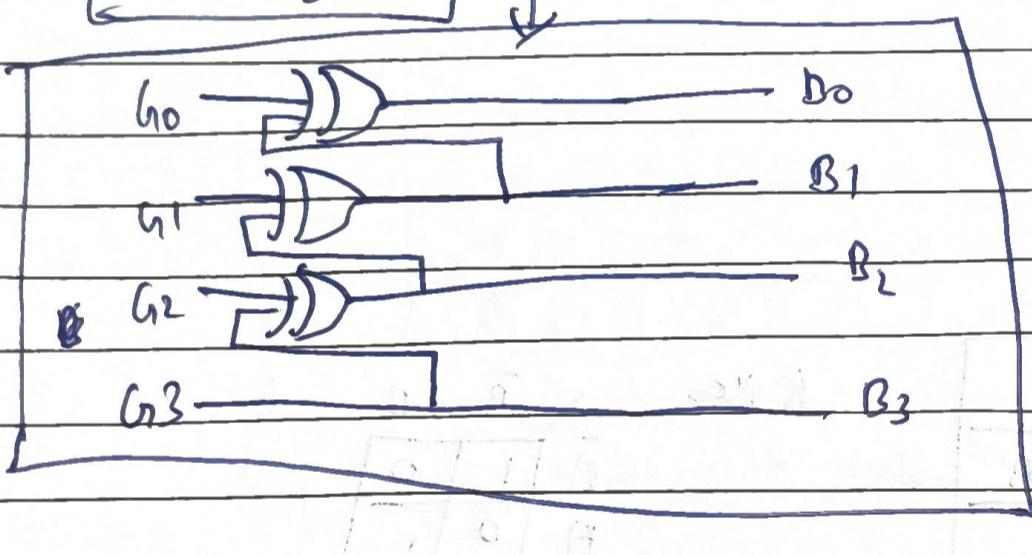
And draw whatever you want

Code Converters



Binary to gray

Gray to binary



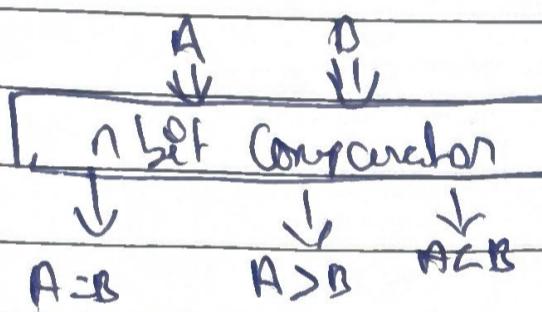
Magnitude Comparators

1-bit Comparator

$A=B$, $A>B$, $A<B$

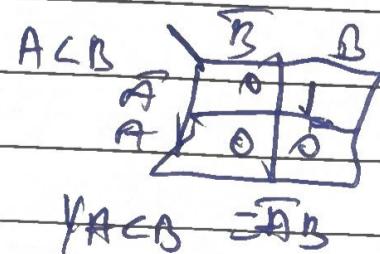
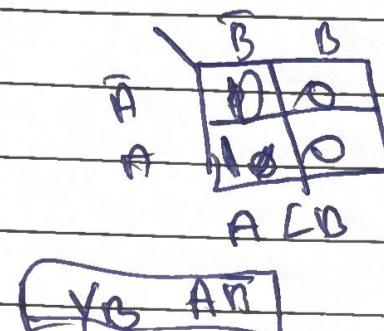
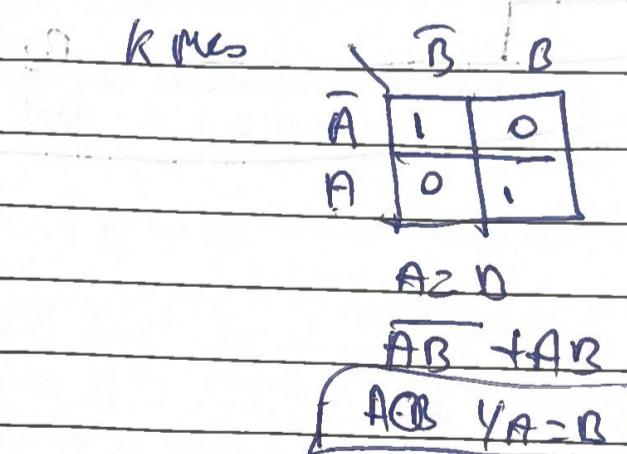
- * It takes binary elements and compare with each other.
- * That's all

Block diagram



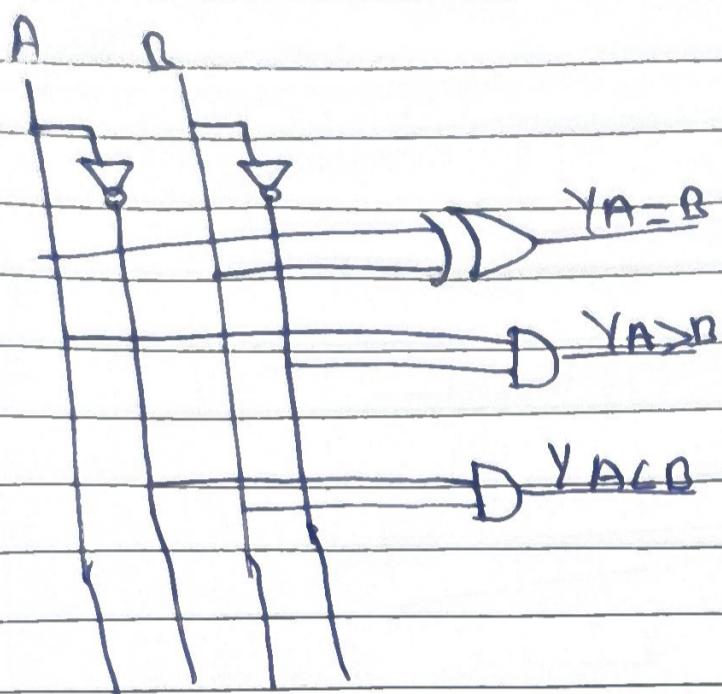
1 bit Comparator

Input			
$A \backslash B$	$Y_{A=B}$	$Y_{A>B}$	$Y_{A<B}$
0 0	1	0	0
0 1	0	0	1
1 0	0	1	0
1 1	1	0	0



S	T	W	F	S	S
Pragya Singh:					
15440				YOUVA	

Diagram:



2-bit Comparator

Inputs				outputs		
A_1	A_0	B_1	B_0	$A > B$	$A = B$	ALD
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	0
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

00 - 0

01 - 1

10 - 2

11 - 3

(They don't man

and :

we get

we get

$$(A > B) = A_1 \bar{B}_1 + A_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_0$$

$$(ALD) = \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 D_1$$

$$(A = B) = (A_0 \oplus B_0) (A_1 \oplus B_1)$$

The draw accordingly is

4 bit magnitude comparator

$$A = A_3, A_2, A_1, A_0$$

$$B = B_3, B_2, B_1, B_0$$

Output

$$(A=B) \Rightarrow X_3, X_2, X_1, X_0$$

$$X_3 = \overline{A_3} B_3 + B_3 A_3$$

$$X_2 = \overline{A_2} B_2 + A_2 \overline{B_2}$$

$$X_1 = \overline{A_1} B_1 + A_1 \overline{B_1}$$

$$X_0 = \overline{A_0} B_0 + A_0 \overline{B_0}$$

$$(A=B) = X_3 X_2 X_1 X_0$$

$$A > B = \overline{A_3} \overline{B_3} + X_3 \overline{A_2} \overline{B_2} + X_2 \overline{A_1} \overline{B_1} + X_1 \overline{A_0} \overline{B_0}$$

$$A < B = \overline{A_3} B_3 + X_3 \overline{A_2} B_2 + X_2 \overline{A_1} B_1 + X_1 \overline{A_0} B_0$$

use this and draw diagram thick cell

Karnaugh map Type I

so let's see problems related to them

II Reduce using mapping the expression $\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$

Soln :

There are 4 variables $(A+B)(A+B)(A+B)$

