Design and Implementation of a 700 MHz to 2.3 GHz CMOS Power Amplifier with 5 dBm Output Power

Master Thesis: Harman Malhotra
Supervisor: Sreekesh Lakshminarayanan
Start Date: 17th Jan. 2018 | Submission Date: 16th Jul. 2018
Fachgebiet Integrierte Elektronische Systeme | Prof. Dr.-Ing. Klaus Hofmann

TECHNISCHE UNIVERSITÄT DARMSTADT

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Abstract

This thesis describes the design and implementation of a 700 MHz to 2.3 GHz CMOS power amplifier with 5 dBm output power. The designed power amplifier uses just one inductor and is composed of three stages: A common gate stage as the input stage, a cascode stage as the core stage and a source follower buffer as the output stage. The design and layout was completed in the Cadence design environment using the 0.13 μm BiCMOS SG13GS technology from IHP. The fully layouted power amplifier was found to consume 210 x 165 μm^2 chip area. The performance of the layouted power amplifer was compared by using an on-chip inductor and an off-chip inductor as the drain inductor for the core stage. The used on-chip inductor was synthesized in ADS using the RFIC Inductor Toolkit from Mühlhaus and an S-parameter inductor model file from Coilcraft was used as the off-chip inductor. The power amplifier was found to have 5 dBm output power and 15.9 dB power gain in the off-chip inductor case. In the on-chip inductor case the output power and power gain were found to have dropped to 4 dBm and 15.09 dB respectively.

Zusammenfassung

Diese Arbeit beschreibt den Entwurf und die Implementierung eines 700 MHz bis 2,3 GHz CMOS-Leistungsverstärkers mit 5 dBm Ausgangsleistung. Der entworfene Leistungsverstärker verwendet nur eine Induktivität und drei Stufen: eine Common Gate-Stufe als Eingangsstufe, eine Kaskodenstufe als Kernstufe und einen Source-Follower-Puffer als Ausgangsstufe. Das Design und Layout wurde mit Hilfe der Cadence-Design-Umgebung in der 0,13 μm BiCMOS SG13GS-Technologie von IHP entwickelt und nimmt eine Chipfläche von 210 x 165 μm^2 ein. Die Leistung des Layout-Leistungsverstärkers wird von der On-Chip-Induktivität und der Off-Chip-Induktivität als Drain-Induktivität für die Kernstufe verwendet. Die verwendete On-Chip-Induktivität wurde in ADS unter Verwendung des RFIC Inductor Toolkits von Mühlhaus implementiert und der S-Parameter-Datei von Coilcraft, wie auf der Off-Chip-Induktivität verwendet. Die Simulationen zeigen, dass der Leistungsverstärker unter Verwendung der Off-Chip Induktivität eine Ausgangsleistung von 5 dBm und eine Leistungsverstärkung von 15,9 dB hatte. Mit On-Chip-Induktivität verringerten sich die Werte der Ausgangsleistung und der Leistungsverstärkung auf 4 dBm bzw. 15,09 dB.

Acknowledgements

First and foremost, I would like to thank Prof. Dr.-Ing. Klaus Hofmann for giving me the opportunity to write my thesis at the the department for Integrated Electronic Systems, Technische Universität Darmstadt. I would also like to thank my thesis supervisor M.Sc. Sreekesh Lakshminarayanan for his unending and constant support during the course of my thesis work. His knowledge in the field RF circuit design helped me in finding good solutions and motivated me to solve the problem at hand. Last but not the least, I would like to thank my family, friends and in particular Kevin Becker for helping me during my thesis.

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1 Introduction and Motivation

Chapter Overview: *This chapter gives an introduction into this thesis work and also spells out the motivation behind it.*

1.1 Why CMOS for RF design?

Traditionally, technologies like III–V or silicon bipolar have been used for RF design. These technologies offer a higher transit frequency (f_T) i.e., the frequency at which the small signal current gain drops to unity and hence, it seems logical enough to use them for RF design. CMOS technology however, has continued to benefit from both scaling and the enormous momentum of the digital market. This is why many high-speed and RF integrated circuits are likely to appear and continue to appear as CMOS implementations [24]. CMOS technology as suggested in the paper has the inherent ability of higher integration as compared to Bipolar technology and this makes it attractive for even RF designs. The higher level of integration has resulted in the production of low cost electonic devices that are easier to market. The integration potential of CMOS is hence, the primary driving force behind it's choice for this thesis work.

1.2 Problem Description

A power amplifier is one of the most important blocks in any radio frequency (RF) signal chain. From the transmitter point of view, the power amplifier (PA) is the most critical component since its performance strongly influences the overall system features in terms of bandwidth, output power, efficiency, and operating temperature [26]. It hence, becomes critical for any transceiver system to have an efficient and robust power amplifier that has sufficient power gain and output power to satisfy the system specifications.

The problem at hand was bipartite. The first part of the problem was to design a CMOS power amplifier with the laid out specifications. The target specifications were created inline with the requirements of the Fiber to the x (FTTx) transceiver chip currently under development at the department for Integrated Electronic Systems, Technische Universität Darmstadt.

Also, very few literature sources exist that compare the performance of RF blocks with on-chip and off-chip passives. The second part of the problem was hence, to compare the the performance of the designed CMOS power amplifier with an on-chip inductor and an off-chip inductor at the drain of the cascode stage. The comparison was made to find the optimal indutive solution for the designed power amplifier in terms of quality factor (Q-Factor) and self resonance frequency (SRF).

1.3 Literature Review

A through literature review was conducted at the start of the thesis. In Table 1.1, the findings from the same have been compiled.

Ref.	Freq (GHz)	Technology	Gain (dB)	S_{11} (dB)	S_{22} (dB)	OP1 (dBm)	Power (mW)
[10]	2.4-5.2	0.18μm,CMOS	18	NA	NA	14	NA
[30]	0.7-6.0	0.13μm, RF-CMOS	22	-10	-10	6	NA
[1]	0.5-8.5	0.6μm,CMOS	6.1	-10	-10	5	103.8
[20]	0.6-22	0.18μm,CMOS	7.3	-8	-9	4	52
[4]	0.5-5.5	0.6μm,CMOS	6.5	-9	-10	15.3	83.4
[15]	3.1-10.6	0.13μm,CMOS	17	-10	-10	3.5	NA
[21]	3.1-12.6	0.18μm, RF-CMOS	10.46	-10	-10	5.6	NA
[5]	3.0-5.0	0.18μm,CMOS	13.3	-7.5	-7	1.81	25.2
[22]	3.0-5.0	0.18μm,CMOS	15.5	-12.9	-13.3	9.13	25.46
[31]	3.0-5.0	0.18μm,CMOS	17.5	-10	-10	2.57	30
[32]	3.0-5.0	0.18μm,CMOS	15.2	-5	-6	11.2	25
[17]	3.1-4.8	0.18μm,CMOS	19	-10	-8	-4.2	25
[16]	57-65	0.25μm,SiGe BiCMOS	8.8	-6	-5	11.5	51.8
[19]	0-15	0.5μm,SiGe BiCMOS	12	-8	-8	4.4	23.76
[3]	3.0-5.5	0.8μm,SiGe BiCMOS	8.5	-6	-6	16.2	325
[8]	26-40	0.13μm,SiGe BiCMOS	13	-15	-15	19.4	525
[9]	79-97	0.13μm,SiGe BiCMOS	14.5	-10	-10	19.6	561
[28]	0.1-14	0.35μm, SiGe BiCMOS	9.8	-8	-8	22.8	NA

Table 1.1.: Literature Review: State of the art power amplifiers

2 Theory of Power Amplifiers

Chapter Overview: *This chapter throws light on the fundamental concepts involved in RF design. The various design parameters, central to any power amplifier design process have also been touched upon.*

2.1 S-parameters

The scattering parameters or S-parameters are one the key concepts of RF design. They are very well suited to represent both the reflection as well as the transfer function of any device. Thus, S-parameters can define the complete small signal charactersistics of a device excluding noise [12]. The S-parameters are based on power wave theory and use the variables a_m and b_n to represent the incident and reflected powers. A basic two port network has been shown in Fig.2.1 and would be used as the central point for this discussion.

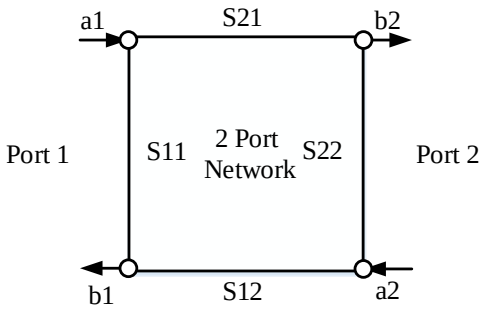


Figure 2.1.: S-parameters for a 2-port network

For any two port network an S-paramter matrix can be built up to highlight the interaction between each port. This matrix as shown below, basically shows the relationship between the incident and reflected power waves for each port.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

From the matrix, S_{11} which is also called as the input reflection coefficient can be written as,

$$S_{11} = \frac{b_1}{a_1} \tag{2.2}$$

S_{12} which is also called as the reverse transmission coefficient can be written as,

$$S_{12} = \frac{b_1}{a_2} \tag{2.3}$$

S_{21} which is also called as the forward transmission coefficient can be written as,

$$S_{21} = \frac{b_2}{a_1} \tag{2.4}$$

S_{22} which is also called as the output reflection coefficient can be written as,

$$S_{22} = \frac{b_2}{a_2} \tag{2.5}$$

Each of these S-parameter plays a very important role in the design process.

2.2 Wideband Impedance Matching

For RF circuits there is a need to attain wideband impedance matching because the transmission lines or RF traces in the case of an RFIC have a fixed characteristic impedance of 50 Ω. These lines or traces are used to carry the RF signal between two block in an RF signal chain. It is hence, very important to achieve optimal matching to reduce reflection based losses. The reflections can not only lead to losses but also have the potential to make an amplifier unstable. It hence, becomes doubly important to achieve good matching. In Fig.2.2, the basic idea behind impedance matching has been presented.

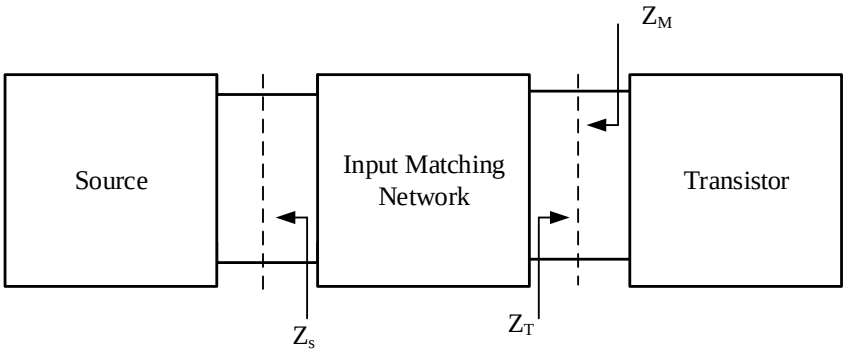


Figure 2.2.: The input matching network between source and transistor

The source impedance Z_S is fixed to 50 Ω. The input impedance of the transitor Z_T, incase of a CMOS is highly capacitive. Now, to limit the reflection based losses, an input matching network has been used that transforms Z_T to Z_S by using an intermediate impedance Z_M. The design of an impedance transformation/matching network becomes a challenge for wideband applications. Some fundamental matching networks have been shown in Fig.2.3.

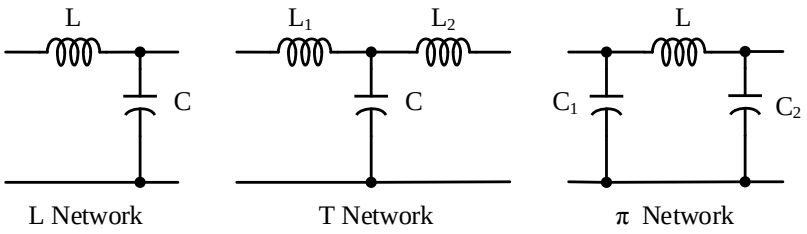


Figure 2.3.: Different impedance matching network topologies

These traditional matching networks use a combination of capacitors and inductors as L, T or π networks to attain lossless matching. These networks however, consume a huge amount of chip area and hence, other more integretable solutions are used for RFIC. Some of these solutions have been presented in later sections of this report.

2.3 Power Gain

Power gain is one of the most important design parameter for any power amplifier. The power gain can be defined in many ways for a two port network as shown in Fig.2.4. These various definitions exist because while calculating the gain, the extent of matching at the input and output ports has to be taken into account.

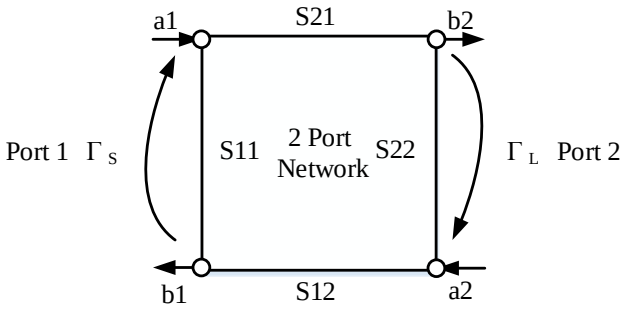


Figure 2.4.: a 2-port network for calculation of power gain

Before going into the different types of power gain, a few parameters have to defined,

- P_{in}: It is the power at the amplifier input in the unmatched source condition
- P_{AVS}: It is the power delivered to the source in the matched source condition
- P_L: It is the power delivered to the load in the unmatched load condition
- P_{AVN}: It is power delivered to the load in the matched load condition

Now, the three most fundamental definitions for power gain can be spelled out,

- Transducer Gain (G_T):

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.6}$$

- Operating power Gain (G_P):

$$G_P = \frac{P_L}{P_{in}} \tag{2.7}$$

- Available power Gain (G_A):

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{2.8}$$

Apart from these three, there exist two more important gain definitions that take into account the stability as a criterion to define the power gain. These two are as follows,

- Maximum Avaialble Gain (MAG):

$$MAG = G_{\mathrm{T,max}}|_{\mathrm{K}\geq 1} = \frac{S_{21}}{S_{12}} * (K - \sqrt{K^2 - 1}) \tag{2.9}$$

  The MAG is used to define the power gain for a power amplifier when it is unconditionally stable i.e., K$\geq$1.

- Maximum Stable Gain (MSG):

$$MSG = G_{\mathrm{T,max}}|_{\mathrm{K}<1} = \frac{S_{21}}{S_{12}} \tag{2.10}$$

  The MSG is used to define the power gain for a power amplifier when it is not unconditionally stable i.e., K<1.

2.4 Linearity and Compression

Linearity can be defined as the condition when the output changes in direct proportion to the input. Incase of a power amplifier the input and output powers are used to test out the linearity. There are two main parameters of a power amplifier that are dictated by it's linearity. These two parameters are known as the compression point and intermodulation products, the same have been discussed next.

2.4.1 1 dB Compression Point

In Fig.2.5, the plot for Input power (P_{in}) versus Output power (P_{out}) for a generic power amplifier has been shown. It is known fact that, the output power and hence, the gain cannot keep growing with the input power due to saturation. The point where the gain drops by 1 dB from the normal linear case is called the 1 dB compression point. The 1 dB compression point for P_{in} as well as P_{out} is a very important parameter.

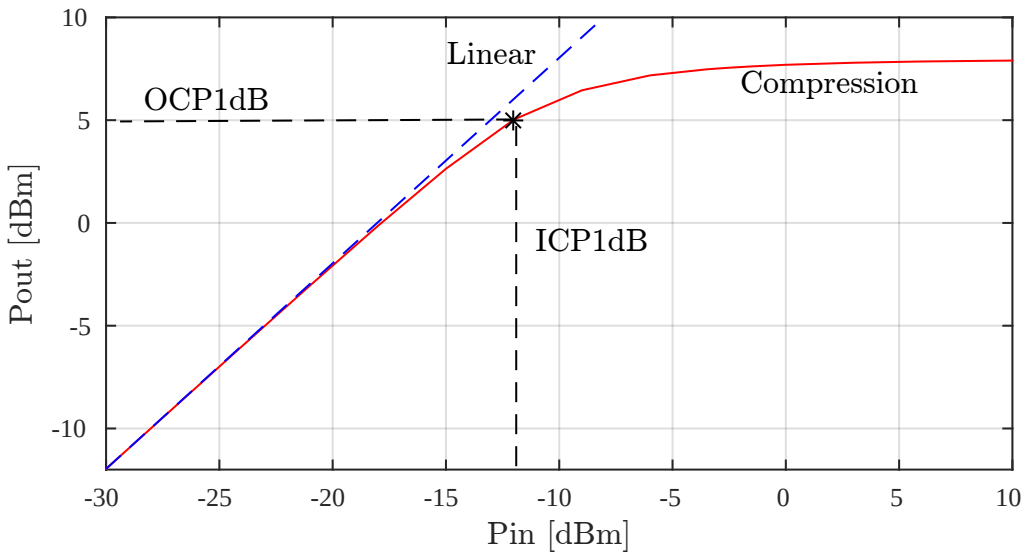


Figure 2.5.: 1 dB Compression Point

The 1 dB compression point at the output side is called the output 1 dB compression point also called the OCP1dB or OP1dB and can be viewed as the maximum deliverable output power from the power amplifier. The input 1 dB compression point or ICP1dB is the maximum input power that can be fed to the power amplifier, after this value compression occurs. The difference between ICP1dB and OCP1dB is equal to the power gain in dB.

$$PowerGain(dB) = OCP1dB - ICP1dB \tag{2.11}$$

2.4.2 Intermodulation

The power amplifier is an inherently nonlinear device due to which it gives rise to harmonics. The nonlinearity not only generates harmonics but also a mixture of frequencies that can be very hard to filter out unlike the harmonics. This undesired generation of a combination of frequency components that can interfere with the main signal being amplified is called intermodulation. The sums and differences of two very close in frequency signals, that cause interference are called as the intermodulation products. A two tone analysis is generally required to test out the impact of intermodulation on a power amplifier. In this test two very close frequency components f_1 and f_2 are fed to the power amplifier. The two, third order intermodulation (IM3) products written as $2*f_1-f_2$ and $2*f_2-f_1$ can cause the most amount of interference as these two are very close to the fundamental component being processed. The other products apart from being far from the fundamnetal component are also very weak in amplitude. The linearity of the power amplifier hence, becomes a direct function of the IM3 products and the third order intercept point as shown in Fig.2.6.

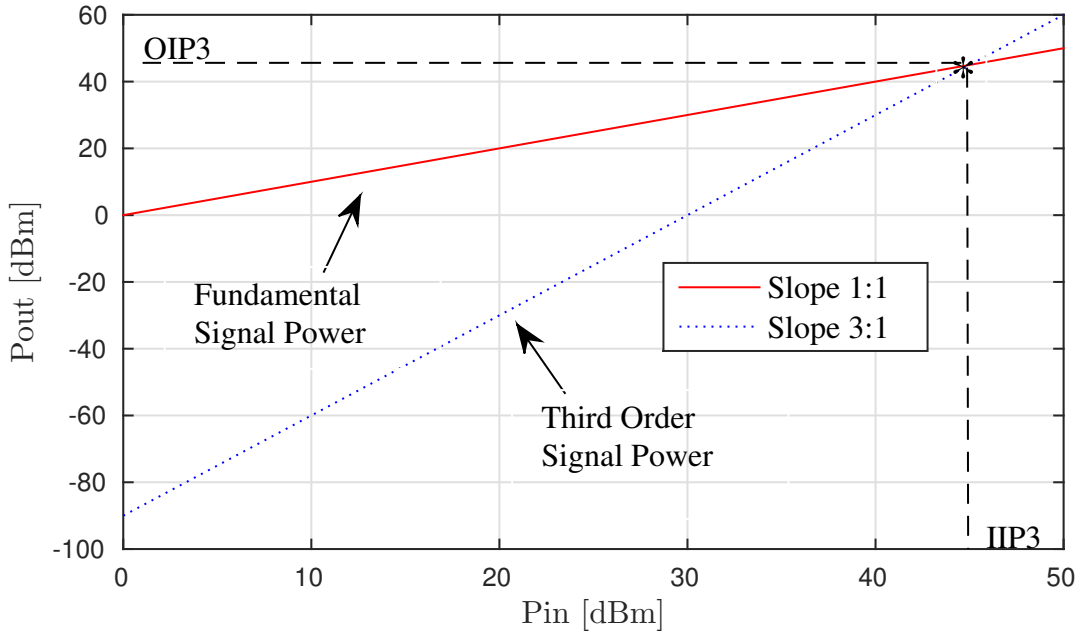


Figure 2.6.: Third Order Intercept Point IP3

The third order intercept point or IP3 is defined as the intersection point between the extrapolted curves of the fundamental frequency and the IM3 products [12]. The IP3 at the output and input side is called the output IP3 or the OIP3 and the input IP3 or the IIP3.

2.5 Efficiency

The efficiency for a power amplifier is defined as the ratio between the ouput RF power to the input DC power. The efficiency can hence, be written as

$$\eta = \frac{P_{\mathrm{RF,out}}}{P_{\mathrm{dc}}} \tag{2.12}$$

Another efficiency parameter called the power added efficiency (PAE) is used to take into account the sharp drop in gain at high frequencies. The PAE for a power amplifier is defined as,

$$PAE = \frac{P_{\mathrm{RF,out}} - P_{\mathrm{RF,in}}}{P_{\mathrm{dc}}} \tag{2.13}$$

Clearly, if the gain for a power amplifier is sufficiently high then, η = PAE.

2.6 Noise Figure

Noise can be defined as any unwanted signal that can interfere with the signal of interest to us. The major types of noise are as follows,

- Thermal Noise
- Shot Noise
- Flicker or 1/f Noise

For any circuit block the signal to noise ratio (SNR) can be used as a measure for the signal quality in the presence of noise. The SNR is defined as follows,

$$SNR = \frac{SignalPower}{NoisePower} \tag{2.14}$$

Another parameter called the Noise Factor (F) can be used to determine the impact of noise on a device. This parameter determines the noise increase due to a device exhibiting additional noise power N_a wrt noise power of the source N_1 [12]. Noise Factor is defined as,

$$F = \frac{TotalNoisePower}{NoisePowerofSource} = \frac{N_1 + N_a}{N_1} = 1 + \frac{N_a}{N_1} \tag{2.15}$$

Noise figure is just the logarithmic representation for noise factor. It is computed as follows,

$$NF = 10 * log_{10}(F) \tag{2.16}$$

The noise figure for a block in dB tells us the amount of SNR deprovement in dB that the introduction of this block brings about for the whole RF signal chain to which it is added. The noise figure hence, is the most popular choice to measure the noise contibution from any circuit block. Generally, there is a need to be able to compute the resulting noise figure from cascaded stages as shown in Fig.2.7.

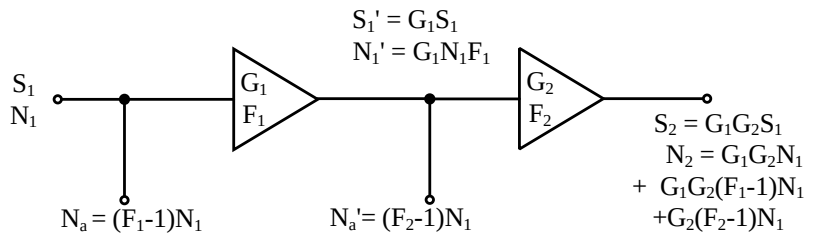


Figure 2.7.: Noise Figure: Two cascaded stages (from Ellinger, 2008, p.97)

The net noise figure can be calculated using the formula of Friis. The net noise figure for a two stage cascade can be written as,

$$F_{21} = F_1 + \frac{F_2 - 1}{G_1} \tag{2.17}$$

where, F_1 and F_2 is the noise figure for each of the stage individually and F_{21} is the resulting noise figure from the cascaded stage arrangement. The formula suggests that, if the gain of the first stage of a signal chain is high enough, it would nullify the noise figure contribution from other stages. The equivalent circuit for the cascade, taking Eq.2.17 into account has been shown in Fig.2.8.

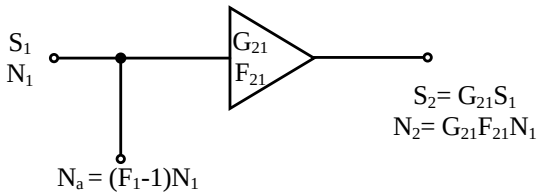


Figure 2.8.: Noise Figure: Equivalent circuit (from Ellinger, 2008, p.97)

2.7 Power Amplifier Classes

The portion of input signal for which the power amplifier conducts has a major bearing on it's properties. Based on the conduction portion, the power amplifier can be divide into a numer of classes. A basic common source power amplifier, as shown in Fig.2.9 can be used to highlight these classes.

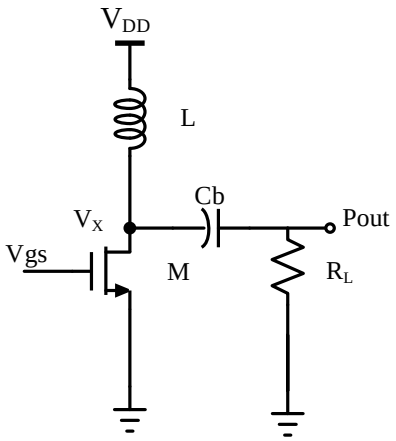


Figure 2.9.: A basic common source power amplifier

2.7.1 Class A

Class A is the most fundamental class. It is the class of operation for which the power amplifier conducts for the entire input signal cycle i.e., for both the negative as well as the positive half cycles. Since, the power amplifier is always in the on state the resulting V_{DS}, as shown in Fig.2.10 in the ideal case is a full sine wave.

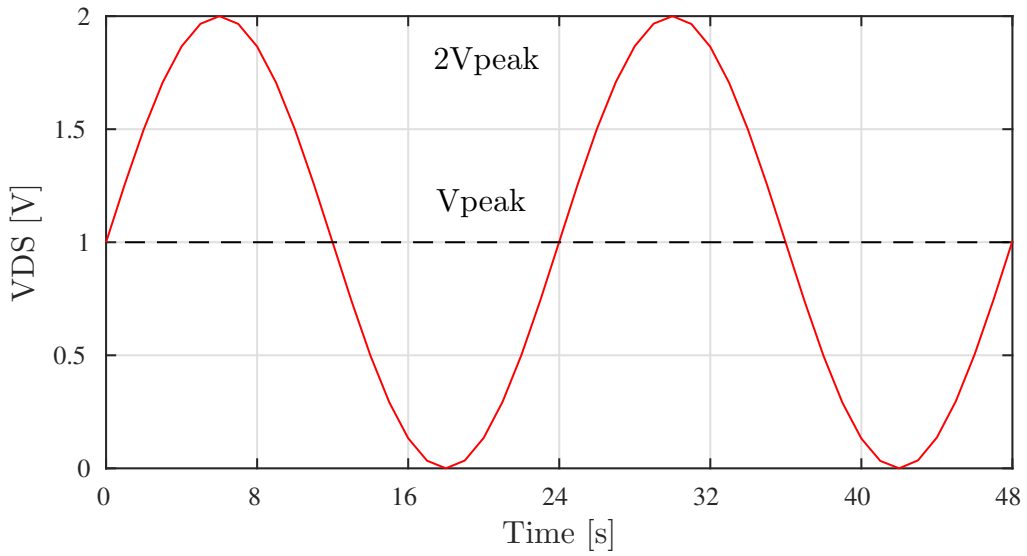


Figure 2.10.: Class-A amplifier drain voltage

Also, since there is no clipping the drain current too has a full swing. In the ideal case the I_{DS}, as shown in Fig.2.11 is a full sine wave.

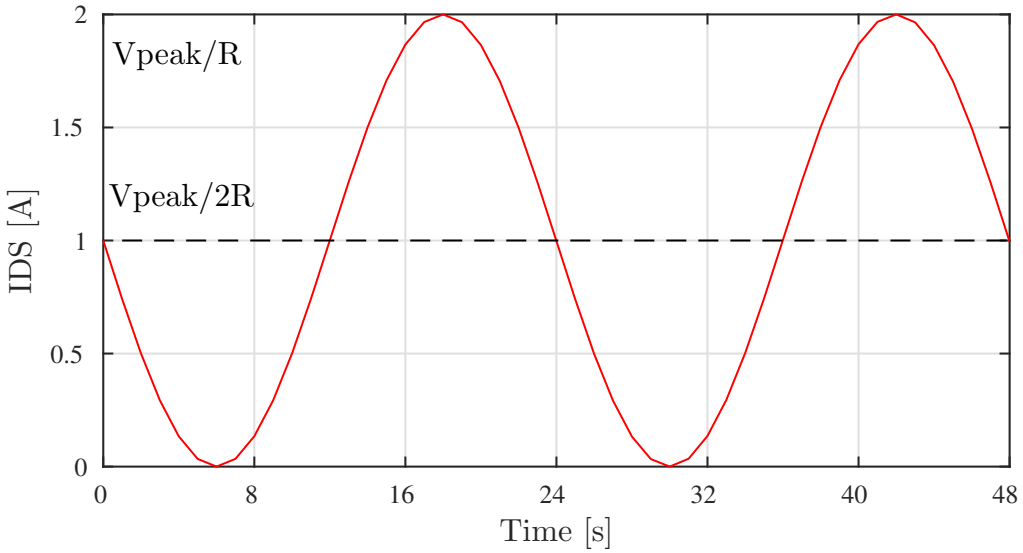


Figure 2.11.: Class-A amplifier drain current

Since, class A power amplifier is always conducting it is the most linear of all power amplifiers. The class A power amplifier also boasts of the highest output power and power gain. The only problem with it is that it's power consumption is very high. Also, it can never have an efficiency greater than 50%.

2.7.2 Class B

Another widely used power amplifier is the class B power amplifier. It conducts for only 50% of the input signal. This still results in V_{DS}, as shown in Fig.2.12 being a full sine wave in the ideal case.

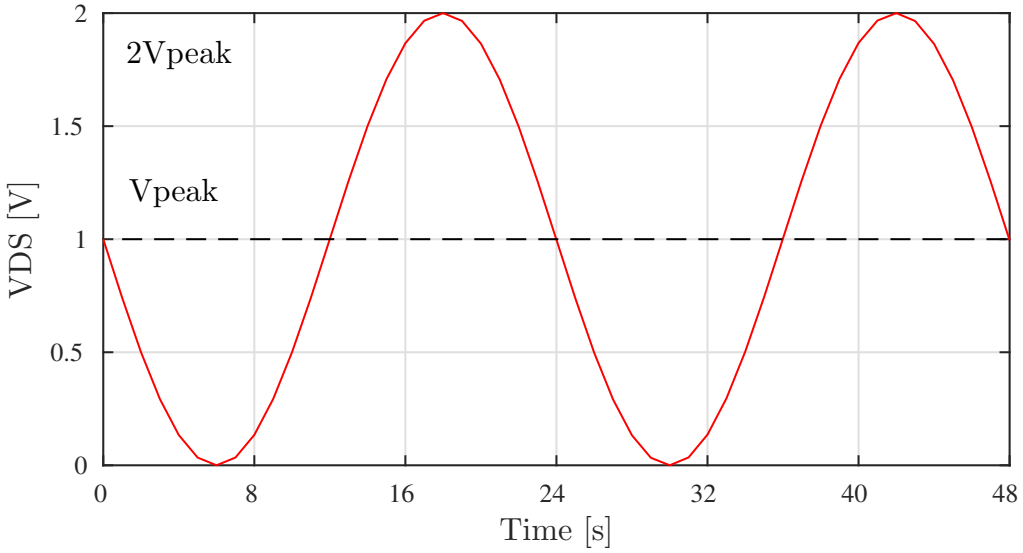


Figure 2.12.: Class-B amplifier drain voltage

The drain current I_{DS} is however, clipped. In Fig.2.13, the clipped I_{DS} is shown. The I_{DS} swings only for half of the input signal and also to half of the peak value as compared to a class A power amplifier.

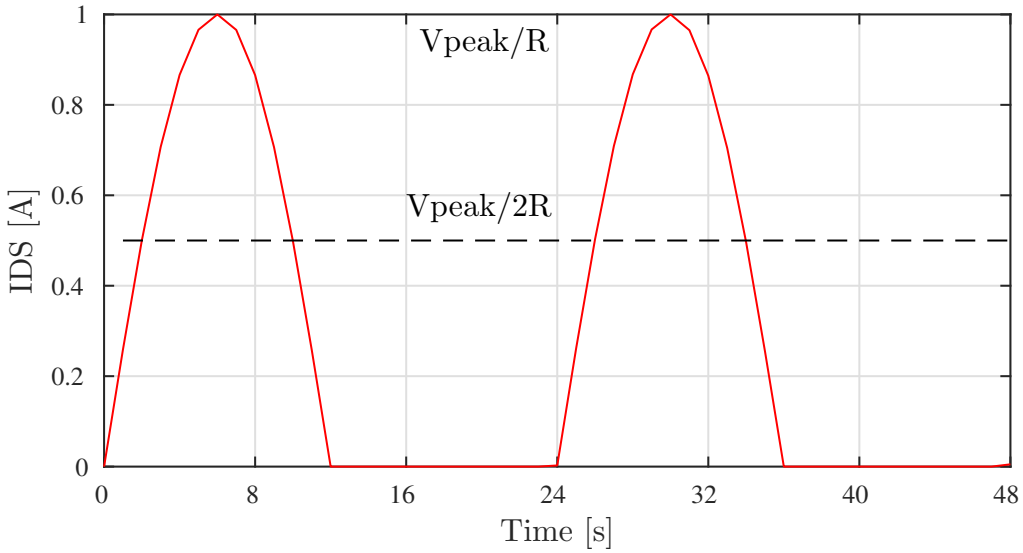


Figure 2.13.: Class-B amplifier drain current

The clipping makes the class B power amplifier more nonlinear as compared to it's class A counterpart. Also, the output power drops and the power gain is 6 dB lower than the MAG reachable using a class A power amplifier. The efficiency for a class-B amplifier is however, higher than a class A amplifier. In the best case the efficiency can be as high as 78.5%.

2.7.3 Class AB

The class AB power amplifier conducts for a signal duration between that for class A and class B. Also, the performance of a class AB power amplifier is better than a class B power amplifier but lower than that for a class A power amplifier.

2.7.4 Other Classes

There are other classes of operation for a power amplifier apart from the ones discussed. These are as follows,

- Class C
- Class D
- Class E
- Class F

Each of these classes has it own set of advantages and limitations. Class C for example allows the power amplifier to attain an efficiency of upto 100% by compromising on the gain. The class D, E and F are a seperate class of power amplifiers called the switched power amplifiers. These amplifiers reduce the static power consumption by emplyoing a switching action and in the process are able to attain a much higher power efficiency. The power gain is however, lost as a tradeoff.

3 Power Amplifier Design

Chapter Overview: *This chapter talks about the power amplifier design cycle and the techniques involved in the same. The chapter starts off with laying down the target specifications for the power amplifier and a brief review of the equations involved in the power amplifier design process. This is followed by highlighting the design approach undertaken. Next, the two implemented power amplifier topologies: common gate power amplifier and shunt feedback power amplifier would be discussed on the schematic level. The chapter ends with a comparative analysis of the two implemented topologies. All schematic designs have been done using Cadence Virtuoso in the 0.13 µm BiCMOS SG13GS technology.*

3.1 Design Specifications

The CMOS power amplifier has been designed to meet the following specifications:

- Frequency Range: 700 MHz – 2.3 GHz
- DC Power $<$ 300 mW
- Output P1dB $\geq$ 5 dBm
- OIP3 $>$ 20 dBm
- NF $<$ 6 dB
- S_{11} $<$ -10 dB
- S_{12} $<$ -30 dB
- Gain $>$ 18 dB
- S_{22} $<$ -14 dB
- Gain Flatness $<$ 2 dB

Some additional constraints got introduced due to the need for on-chip integration of the power amplifier. One of these was that the number of inductors were to be limited to only one. Also, an analyis was required to find out the most suitable inductor interms of Q-factor and self resonace frequency for the power amplifier. A comparative analysis has to be done in this regard between the power amplifier performance with an on-chip inductor and an off-chip inductor.

Last but not the least, the designed power amplifier had to be unconditionally stable. The K-factor and B1f have been used as criteria to measure the stability of the power amplifier.

3.2 Power Amplifier Design Equations

Now that the target design specifications have been discussed, the design process could be started with. The first step in this regard would be to review a few fundamental design equations that are the corner stone of any power amplifier design. A basic common source power amplifier as shown in Fig.3.1 will be used initially to lay the groundwork for this section. Also, the section has been divided into points to make it easier for the reader to follow.

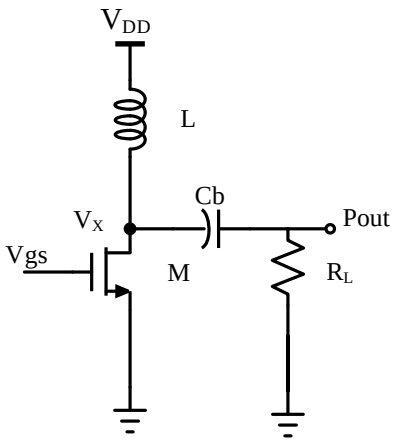


Figure 3.1.: A basic common source power amplifier

- The output power 'P_{out}' delivered to any load resitor R_L by the power amplifier can be written as,

$$P_{\text{out}} = \frac{{V_{\text{peak}}}^2}{(2 * R_{\text{L}})} \tag{3.1}$$

  where, the voltage at point V_x swings between 0 and 2*V_{peak}.

- To deliver for example., 100 mW (20 dBm) of power to a 50 Ω load resistor, the required value for V_{peak} can be obtained using Eq.3.1. This value comes out to be roughly 3.16 V. This means that to deliver 100 mW of output power, $V_{DD} > V_{peak\ to\ peak}$ i.e., $V_{DD} > 6.325$ V is required. This requirement can however, be relaxed by using an inductor because in the ideal case, it would allow a voltage swing from 0 to 2*V_{DD} at point V_x. Also, the required load current represented as I_L corresponding to the voltage swing can be calculated as follows,

$$I_{\text{L}} = \frac{V_{\text{peak}}}{R_{\text{L}}} = \frac{3.16}{50} = 63.2mA \tag{3.2}$$

- If the drain voltage is a sinusoid then in the ideal case the peak to peak voltage swing at point V_x would be equal to 2*V_{DD}. This would mean,

$$P_{\text{out}} = \frac{{V_{\text{DD}}}^2}{2 * R_{\text{L}}} = 108.9mW \tag{3.3}$$

  Hence, a power of 108.9 mW can be delivered to a 50 Ω load with a V_{DD} of 3.3 V. Also, for V_x to reach V_{DD}, the inductor must provide a current equal to,

$$\frac{V_{\text{DD}}}{R_{\text{L}}} = \frac{3.3}{50} = 66mA \tag{3.4}$$

This current would lead to DC power being drawn from the supply, this value can be calculated as follows,

$$\frac{{V_{\mathrm{DD}}}^2}{R_{\mathrm{L}}} = \frac{(3.3)^2}{50} = 217.8mW \tag{3.5}$$

- Now if V_x has to swing from 2*V_{DD} to V_{DD} to near zero, the drain current I_d for transistor M also has to go down to zero . This means that V_x can only reach 2*V_{DD} if transistor M turnsoff. In order, to prevent the transistor from turning off,

$$V_{\mathrm{x}} \geq (V_{\mathrm{gs}} - V_{\mathrm{th}}) \tag{3.6}$$

where, (V_{gs} - V_{th}) is the difference between the gate-source voltage and the threshold voltage for transistor M. This difference is also reffered to as the overdrive voltage for a transistor.

- This for a cascode power amplifier as shown in Fig.3.2 would mean,

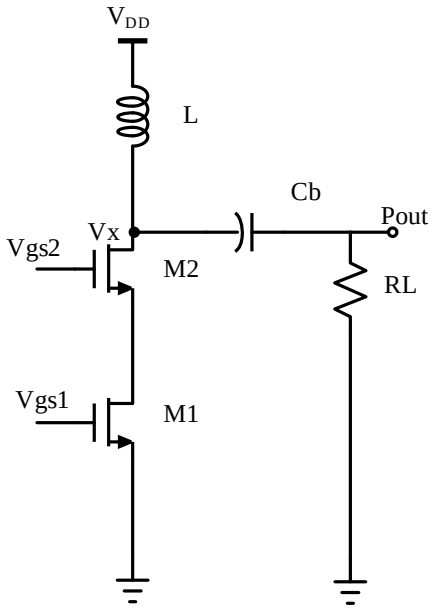


Figure 3.2.: A cascode power amplifier

$$V_{\mathrm{x}} \geq (V_{\mathrm{gs1}} - V_{\mathrm{th1}}) + (V_{\mathrm{gs2}} - V_{\mathrm{th2}}) \tag{3.7}$$

The voltage swing at point V_x is hence, limited by the overdrive voltages for both M_1 and M_2.

- To compensate for this reduction in the voltage swing the current swing has to be increased. As an example, let's assume that due to the cascode power amplifier the output voltage swing gets reduced to a $V_{\text{peak to peak}}$ of 4 V from 6.6 V. This means that the new deliverable output power would be,

$$P_{\mathrm{out}} = \frac{{V_{\mathrm{peak}}}^2}{2 * R_{\mathrm{L}}} = \frac{(2)^2}{2 * 50} = 40mW(16dBm) \tag{3.8}$$

Now, to obtain the initial target value of 100 mW (20 dBm) with this reduced voltage swing the optimum value for R_L has to be recalculated as follows,

$$R_{\text{opt}} = \frac{V_{\text{peak}}}{2 * P_{\text{out}}} = \frac{4}{2 * 100 * 10^{-3}} = 20\Omega \tag{3.9}$$

This hence, calls for either sacrificing the P_{out} or designing an output impedance transformation network. This impedance transformation done to obtain a desired amount of output power is called Loadpull Analysis.

- We could also try and reduce the overdrive voltage to allow for a larger voltage swing at V_x. This can be done by increasing the widths for transistors M_1 and M_2. For example, to reduce the overdrive voltage by say 50% the width for M_1 would have to be bumped up 4 times. This would however, make the power amplifier more non linear and would also increase C_{gs} and C_{db} both of which can have unwanted effects on the performance of the power amplifier in the frequency range of interest.

- Last but not the least, to achieve an output power of 5 dBm (3.16 mW), the output voltage swing required can be calculated using Eq.3.1. The resulting value for V_{peak} comes out as 0.5621 V, which can rounded of to 0.57 V. Hence, an output volage swing of approximately 1.15 V $V_{\text{peak to peak}}$ becomes a principle design target for this thesis work.

The basic math involved in any power amplifier design as well as suited for this thesis work has been shown above. Focus will now be shifted over to the actual design process staring off with the design approach undertaken.

3.3 Design Approach

The design approach undertaken for the power amplifier involves splitting the entire power amplifier block into three sub-blocks, which are as follows:

- Input Stage
- Core Stage
- Output stage

In Fig.3.3, the three sub-blocks have been shown. The input stage is primarily responsible for providing wide band input matching to 50 Ω i.e., meeting the specification for S_{11}. The second sub-block, the core stage accounts for the power gain and output power for the power amplifier. This stage is hence, responsible for fulfilling the Gain, Output P1dB and OIP3 specifications. Last but not the least, the output stage has to satify the ouput matching criteria to 50 Ω over the entire frequency range of interest.

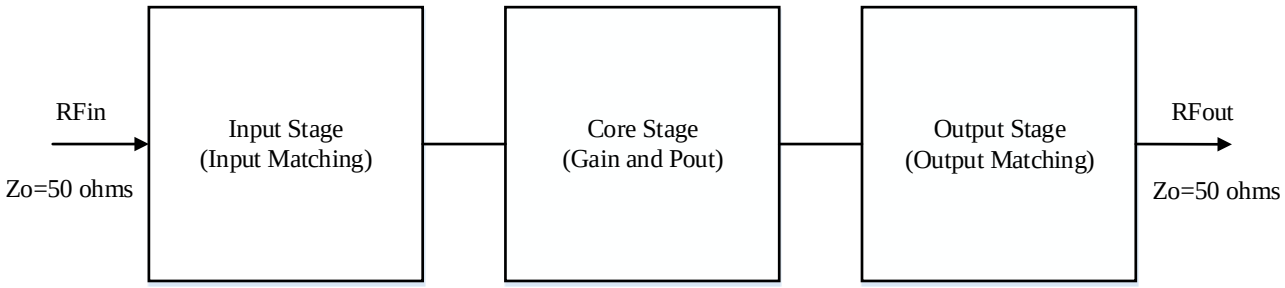


Figure 3.3.: Power amplifier: 3 block model

As suggested in section 3.1, the maximum number of usable inductors are limited to one for the power amplifier design process. This could pose a huge challenge while designing the input and output stages, as most of the wide band matching techniques use a combination of inductors and capacitors as L, T or π networks. Novel approaches had to be implemented in this regard to satisfy the input and output match criteria.

3.3.1 Core Stage and Biasing

The design process for the power amplifier started with the design of the core stage. This stage as suggested in section 3.3 is responsible for the gain and output power. These two parameters constitute the two most important design specifications for any power amplifier. The two most popular choices as the core stage of a power amplifer are,

- Common Source stage
- Cascode stage

Each of the two topologies has it's advantages and limitations. In [7], a comparison of the common source topology and cascode topology for the design of a 60 GHz amplifier in the 65 nm CMOS process has been carried out. The two topologies have been compared on the basis of gain, input-output isolation and stability. Although the analysis in the paper has been done for 60 GHz, results are available for all frequencies below 100 GHz. The paper hence, gives many uselful results for the frequency range that is of interest to us. These can be summed up as follows,

- Gain: The cascode topology offers atleast 5 dB higher gain than it's common source counterpart
- Input-Output isolation: The cascode topology also offers atleast 15 dB higher isolation than the common source topology
- Stability: The increased input-output isolation makes the cascode topology stabler

These advantages seem to be swinging the balance in favour of the cascode topology. The common source stage however, offers the advantage of simpler design and smaller overdrive voltage requirements. This reduced overdrive voltage inturn would allow the drain voltage to have a larger swing. This increased voltage swing allows the amplifier to deliver a higher amount of output power as explained in section 3.2. The higher voltage swing is a very important design requirement for any power amplifier with a small supply voltage as available with a standard CMOS process. The 0.13 μm BiCMOS SG13GS technology, however offers a supply voltage of 3.3 V. The advantage of a higher voltage swing with the common source topology is therefore, overshadowed by the larger available supply voltage and the ability of the cascode stage to allow the power amplifier in using the 3.3 V supply for increased headroom and improved linearity much more effectively as suggested in [33].

Apart from this, the cascode structure also provides protection against oxide breakdown and hot carrier degradation, while providing large output impedance and good isolation property as explained in [30]. These points along with the comparative analysis done in [7] makes the cascode topology ideally suited for this thesis work. In Fig.3.4, the designed cascode stage has been shown.

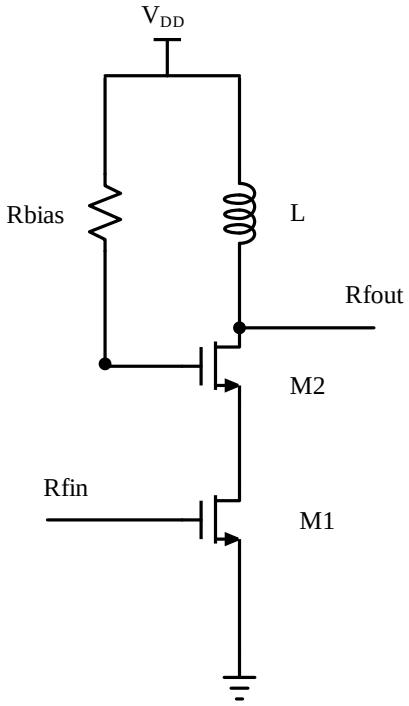


Figure 3.4.: Power amplifier: Cascode Stage

Apart from the choice of topology for the core stage, another important parameter that would decide the amount of deliverable output power and power gain is the bias point selection. As suggested in section 2.7.1, a power amplifier biased in Class A region of operation can achieve 6 dB higher power gain than it's Class B counterpart. Biasing in Class A region also yields designs with higher bandwidths and higher linearity. These features are very attractive as they would allow the power amplifier to achieve higher values for both Output P1dB and OIP3. The only clear disadvantage of Class A region selection is the higher power consumption that it brings in. This is not particulary a problem for this design because the power budget stands at 300 mW.

Once a decision on the required region of operation was taken, simulations were done using the Spectre Circuit Simulator available with Cadence Virtuoso to decide the optimum gate source voltages for both M_1 and M_2, while keeping the drain source current I_{ds} high enough to provide at least 5 dBm of output power. The simulation results produced the following values as the optimal bias point,

- V_{gs}(M1): 1.2 V
- V_{gs}(M2): 3.3 V
- I_{ds}: 22 mA

The bias point selection concludes the design of the core stage of the power amplifier. Next, the other stages involved in the power amplifier design will be discussed.

3.3.2 Output Stage: Source Follower

As suggested in section 3.3, the output stage is responsible for providing wide band output matching over the entire frequency range of interest. Limiting the number of inductors makes this target even more challenging to achieve. An LNA design has been brought about in [23] using a source follower as the output stage. The LNA has been designed for a frequency range of 3.1 GHz to 10.6 GHz and the source follower provides the required output isolation over the entire frequency range.

Another LNA with a source follower as the output stage has been undertaken in [6]. The LNA operates over the frequency range of 3 GHz to 10 GHz while providing an S_{22} < -8 dB over the entire wideband range of frequencies. These implementations with a source followers can be used as a good starting point while undertaking the design of the output stage.

The output stage used in either of the implementations cannot be however, directly used for the power amplifier, as none of them meets the S_{22} design specification. Moreover, it is a known fact that the source follower has a maximum voltage gain of unity, which means it has the potential of providing compression for RF designs. Compression can supress both the output power as well as the power gain which are two of the most critical parameters for a power amplifier. In Fig.3.5, the adapted output stage suitable for the power amplifier has been shown.

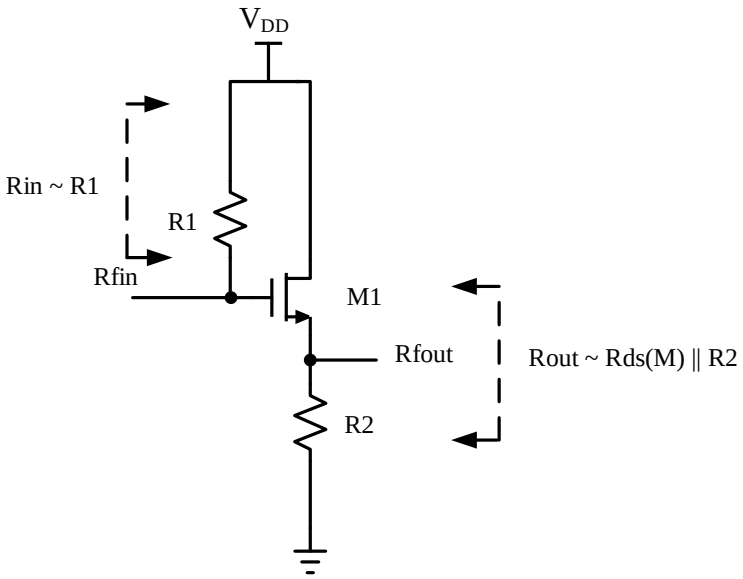


Figure 3.5.: Power amplifier: Output Stage

The output stage can be viewed as a two port network with,

- Input Impedance roughly equal to R_1 Ω
- Output Impedance roughly equal to a parallel combination of R_2 and R_{ds}(M1) i.e., (R_2 || R_{ds}) Ω

The value for R_1 was chosen from load pull analysis. This value was choosen to allow for the required current swing to obtain an output power of 5 dBm. The choice of R_2 however, involves a tradeoff between S_{22} and the achievable output power and power gain. The resistance R_2 is in principle a degeneration resistor and increasing it's value improves the output impedance of the buffer but reduces the I_{ds} through

the buffer, which in turns limits the transconduactance(g_m) of the output stage. This reduction in g_m increases the compression from the output stage and reduces the output power and power gain of the overall power amplifier.

On one hand increasing the value of R_2 improves the value for S_{22} while increasing the compression, decreasing the value does exactly the opposite. Decreasing the value for R_2 deproves the value for S_{22}, while reducing the compression introduced by this stage. In Fig.3.6, the trade-off involved has been shown. The value of R_2 has been swept between 25 Ω and 250 Ω. The resulting values for compression and S_{22} in dB have been plotted on the left and right y-axis respectively.

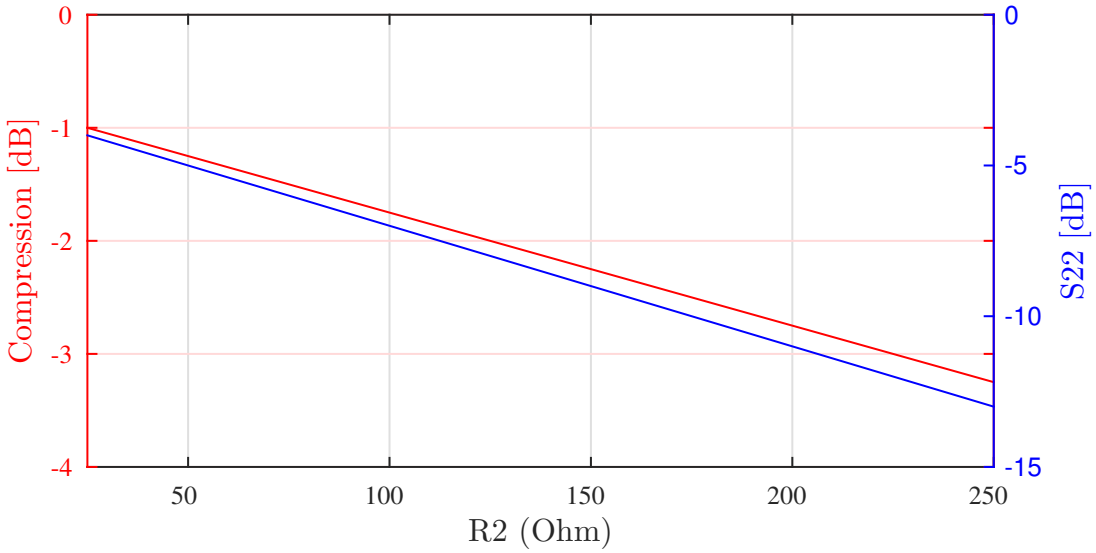


Figure 3.6.: Output Stage tradeoff: Compression vs S22

From the plot it is clear that,

- There indeed exists a direct trade-off between the compression introduced by the output stage and S_{22}
- The target specification of -14 dB for S_{22} would be difficult to achieve as it would introduce a compression of approximately -3.5 dB

It therefore makes sense to reduce the target specification for S_{22} down to -10 dB which would translate into a compression of roughly -2.5 dB. Another intresting point noted from the simulations conducted in cadence virtuoso is that, as the effective width for transistir M_1 is increased it relaxes the tradeoff a little. This means that by simultaneously changing the values for the effective width of M_1 and R_2, an S_{22} of -10 dB with roughly -1.5 dB compression is possible. This way an an almost 2 dB improvement over the initial compression of -3.5 dB can be made.

3.4 Shunt Feedback Power Amplifier

The shunt feedback power amplifier would be discussed in this section. It was the first of the two power amplifier topologies implemented. The core stage and output stage for the power amplifier have already been discussed in the previous sections. The input stage will be the focal point of discussion now.

3.4.1 Input Stage

Unlike the output stage, many inductor-less topologies are available for achieving wide-band input matching. A number of these toplogies would be discussed and a design decision would be taken to choose the best possible topology for the power amplifier being designed.

The first wide-band topology that would be discussed is the direct resistor termination.In Fig.3.7, the basic idea behind the topology has been shown. By using a resistance R of 50 Ω, the input impedance can be set to roughly 50 Ω for a wide-band range of frequencies. Hence,

$$R_{\text{in}} = R \tag{3.10}$$

The obvious advantage of this topology is it's simplicity. The Resistive termination technique however, suffers from poor noise performance due to the deleterious effect of real resistor at input port [13].

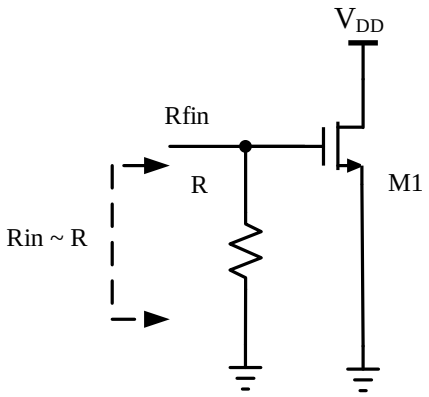


Figure 3.7.: Input stage: Direct resistor termination

A through analysis of the potential noise figure contribution from the resistor R has been done in [27]. The analysis suggests that there are two reasons for the large noise figure contribution from this resistor, these reasons are as follows,

- Firstly, the added resistor contributes its own noise to the output, which equals the contribution of the source resistance
- Secondly, the resistor introduces attenuation for the input signal, which worsens the noise performance of the block

The analyis is concluded by suggesting that the large noise penalty resulting from these effects makes this architecture unattractive. A similar analysis has been made for the designed power amplifier.In Fig.3.8, the analysis has been shown. The resistance R is swept from 50 Ω to 250 Ω, while the noise figure for the power amplifier and the resulting S_{11} have been plotted on the left and right y-axis respectively.

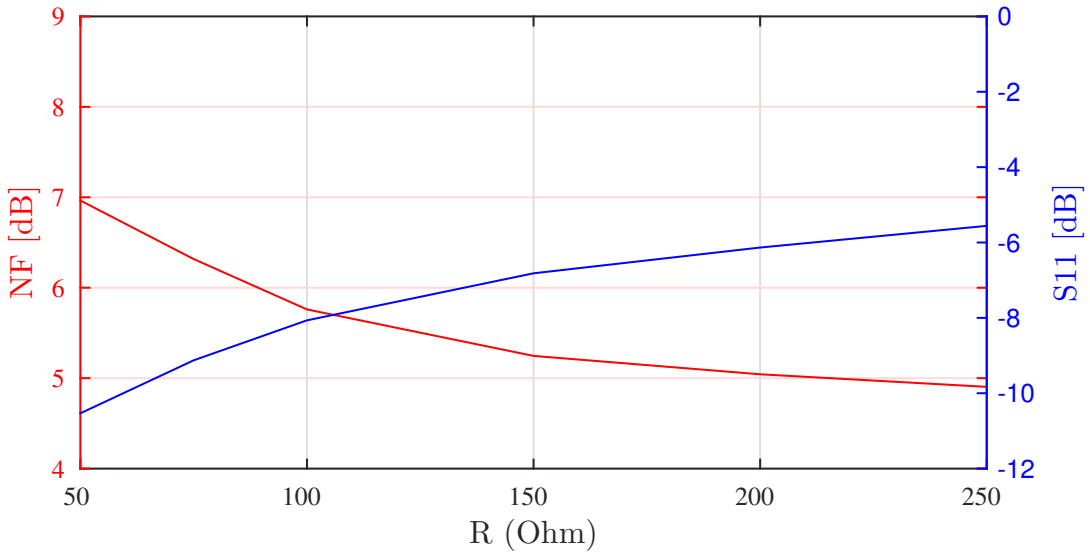


Figure 3.8.: Direct resistor termination: Noise Figure vs S11 analysis

It is clear form the results that the desired S_{11} of atleast -10 dB would also bring along a noise figure contibution of roughly 7 dB. Also, incase a lower noise figure is desired let's say 5 dB, the resulting S_{11} would have to be just -5 dB. This topology hence, cannot be used for the power amplifier being designed.

Another widely used wide-band topology for input matching is the shuntfeedback.In Fig.3.9, the shunt feedback topology has been shown. The topology has been discussed at lenght in [17] .The basic idea behind this topology as suggested in the paper is that, the feedback network can be designed in such a way that it provides the required match at the input end. This topology has the added advantage of achieving flat gain response.

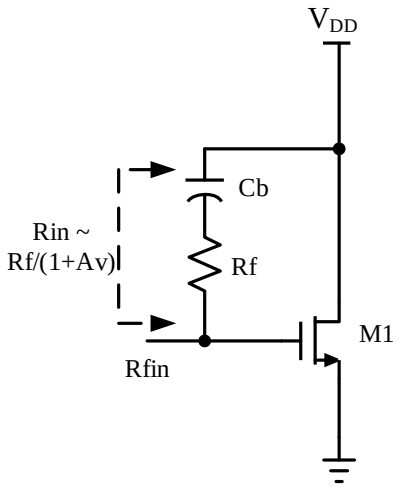


Figure 3.9.: Input stage: Shunt-feedback

The resulting input impedance R_{in} from this topology can be expressed as,

$$R_{in} = \frac{R_f}{(A_v + 1)} \tag{3.11}$$

where, A_v is voltage gain from the amplifier for which the input matching network is being designed.

The real challenge with topolgy comes into the picture when an attempt to select R_f is made. The paper suggests that a small R_f can provide excellent matching but the gain of the amplifier drops due to significant signal feedback through this path. On the other hand, a large R_f can provide good gain but reduces the effect of feedback. Through careful simulations, the optimum value of R_f can be achieved for the best matching and gain conditions.

An attempt has been made to find the optimum value for R_f to satisfy both the gain and S_{11} criteria simultaneously. The resistance R_f has been swept from 0 Ω to 800 Ω, while the resulting S_{21} and S_{11} for the power amplifier have been plotted on the y-axis simulatneously. The results from the analysis have been presented in Fig.3.10.

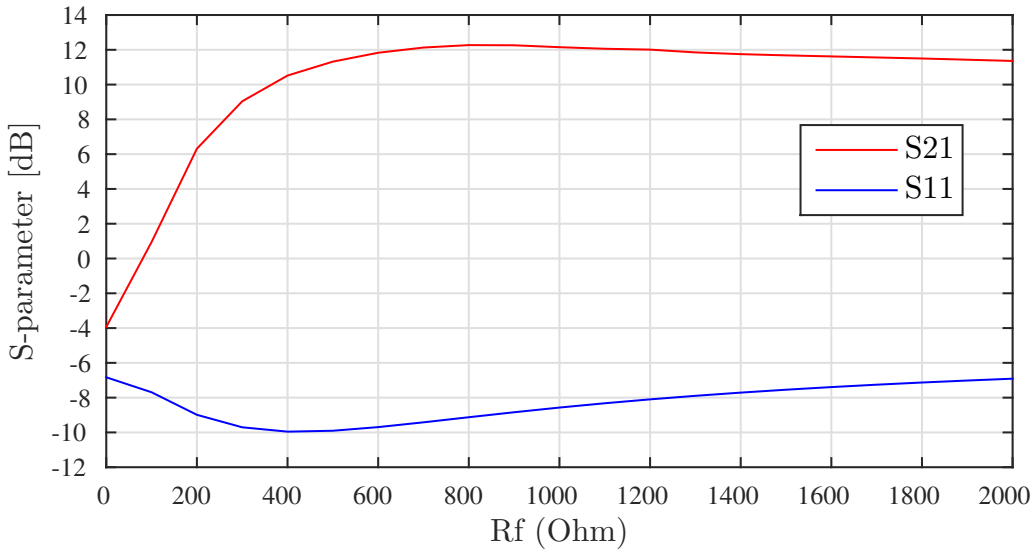


Figure 3.10.: Shunt feedback input stage: S21 vs S11 analysis

The results show that if R_f is chosen to meet the criterion for S_{11} < -10 dB, the resulting gain would be roughly 10.7 dB. Also, the maximum gain of 12.27 dB can be achieved by relaxing the S_{11} specification down to -9 dB from -10 dB. Other interesting results from the analysis were that the noise figure never went above 4.61 dB and the gain flatness always remained under 2 dB. These results are much better than those obtained in the case of direct resistor termination based input matching network. A potential problem area was however, highlighted by the analysis. This is the reduction in input-output isolation due to the huge feedback introduced from the output side of the power amplifier to the input side when R_f was choosen to be under 500 Ω. This huge feedback while reducing S_{12} can ultimately result in reducing the stability of the power amplifier. The design of an unconditionally stable power amplifier is one of the primary goals of every designer and hence, this topology was not used for the design process.

Although, both the direct resitor termination based input matching network as well as the shunt-feedback based input matching network cannot be individually used to achieve the desired parameters, a combination of both of them can perhaps produce the desired results by achieving a good compromise in terms of all design parameters. In Fig.3.11, the proposed combined matching network is shown. The idea behind this network is pretty straight-forward, it focuses on utilizing the positives from each of the two topologies, while eliminating the disadvantages.

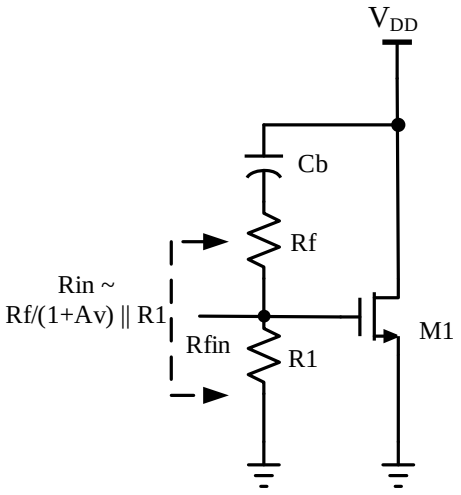


Figure 3.11.: Input stage: Combined

The input impedance from the proposed matching network can be roughly expressed as,

$$R_{\text{in}} = \frac{R_{\text{f}}}{(A_{\text{v}} + 1)} || R_1 \tag{3.12}$$

which is basically a parallel combination of the input impedance obtained from the direct resistor termination topology and the shunt-feedback topology. The effectiveness of this topology also lies in the R_{in} equation. Both resistors and R_f and R_1 now share the responsibility of achieving input wideband matching to 50 Ω, this allows the selection of relatively larger values for each of the resistors as compared to cases where they were used individually. After a number of simulation runs the following values were decided upon,

- $R_f = 900$ Ω
- $R_1 = 100$ Ω

These values allowed the achievement of wideband input matching while keeping the noise figure and input-output isolation incheck. Next, the full impementation for the shunt feedback power amplifier will be discussed.

3.4.2 Full Implementation and Simulation Results

The shunt feedback power amplifier was the first fully designed power amplifier topology. It was composed of the following three stages,

- Input Stage: Implemented using the combined input stage shown in Fig.3.11
- Core Stage: Implemented using the cascode topology discussed in section 3.3.1
- Output Stage: Implemented using the source follower discussed in section 3.3.2

The full implementation for the designed power amplifier has been shown in Fig.3.12. The three stages as shown, were connected together with the following additional elements,

- C_{b1} and C_{b2} as the blocking capacitors to isolate the dc biasing of each stage
- A voltage divider created using the resistances R_2 and R_3 to provide the required gate bias voltage for the transistor M_1

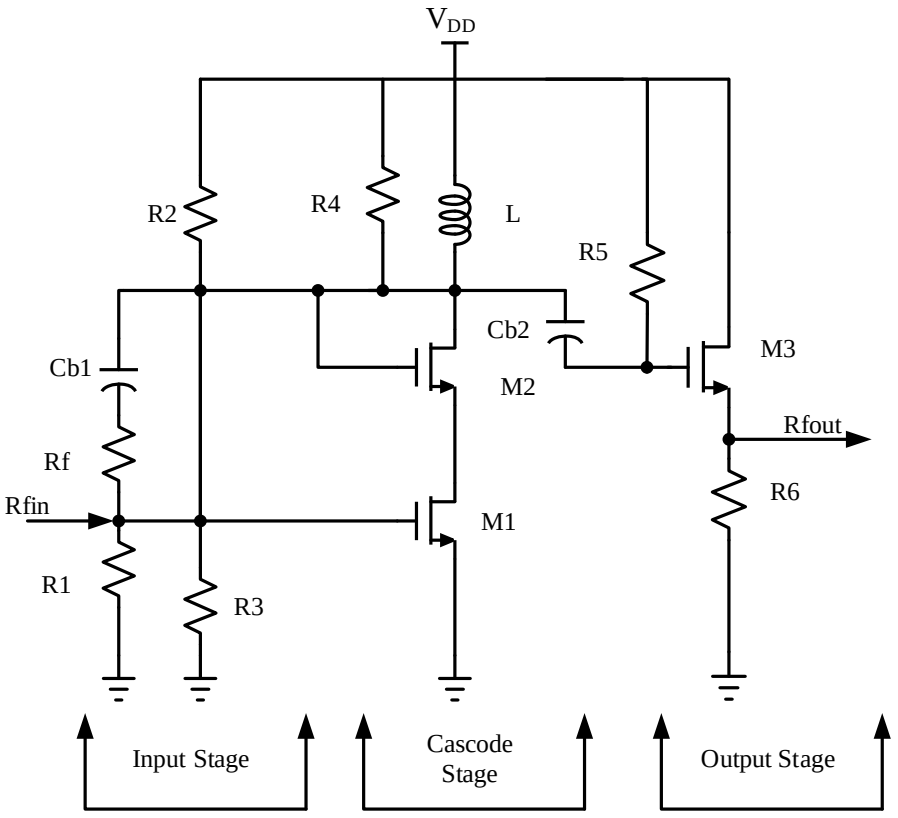


Figure 3.12.: Full Implementation: Shunt feedback power amplifier

The implementation was followed by simulating the power amplifier to analyse it's performance. The power amplifier was simulated and analysed using the Spectre Circuit Simulator available with Cadence Virtuoso. Simulations were conducted for not only the typical case but also to account for the variations in the process,

voltage and temperature parameters (PVT variations). The corner analysis was done to cover the following variations,

- Process:
  - MOS: All combinations of slow, typical and fast PMOS and NMOS (ss, sf, tt, fs, ff cases)
  - Resistors: Worst Case, Typical Case and Best Case (wcs, typ, bcs cases)
  - Capacitors: Worst Case, Typical Case and Best Case (wcs, typ, bcs cases)
- Voltage: 3.0 V, 3.3 V, 3.63 V (10% variation)
- Temprature: 25 °C , 50 °C , 85 °C

The simulation results for the typical as well as PVT corners have been summed up in Table 3.1. The parameters that get fulfilled have been higlighted in blue and the ones that fail have been highlighted in red.

Parameter	Target-Specs.	Typical-Case	Corner-Simulations	
			Min	Max
Frequency [GHz]	0.7-2.3	0.7-2.3	0.7-2.3	0.7-2.3
DC Power [mW]	<300	153.4	122.3	188.1
OP1dB [dBm]	>5	5.043	4.275	5.992
OIP3 [dBm]	>20	17.5	16.78	17.84
NF [dB]	>6	4.967	4.879	5.396
S_{11} [dB]	<-10	-10.28	-11.19	-9.654
S_{12} [dB]	<-30	-46.53	-47.54	-45.45
S_{21} [dB]	>18	10.93	9.022	11.76
S_{22} [dB]	<-14	-10.11	-12.03	-8.694
Gain Flatness [dB]	<2	1.932	1.489	2.465

Table 3.1.: Shunt feedback power amplifier corner simulation results

The table shows some interesting results that can be concluded as follows,

- Output Power (OP1dB): The 5 dBm target value gets fulfilled with the shunt feedback power amplifier
- Gain (S_{21}): A value of roughly 11 dB, which is 7 dB lower than the target specification has been achieved with the shunt feedback power amplifier
- Output Matching (S_{22}): The target specification of -14 dB for S_{22} has not been met
- Other Parameters: All the other parameters are more or less in the desired range
- Corner Variations: Each parameter shows a very nominal deviation across all PVT corners

In the next section each of the failed corners will be discussed at lenght and the reasons for each failure will be laid out. Also, the possible circuit changes needed to fix these failed corners will be discussed.

3.4.3 Shortcomings

The shunt feedback power amplifier's performance was discussed in the previous section. The amplifier meets one of the primary design requirement of 5 dBm output power but fails to meet the gain criterion. Apart from this, the S_{22} target value has also not been met. The primary reasons for criterion not being met are,

- Output Stage Compression: As discussed in section 3.3.2, this stage produces a compression of -1.5 dB, which limits the gain of the power amplifier
- Lack of active input stage: Although, the used input stage satisfies the S_{11} design requirements over the entire frequency range on interest, it contributes nothing towards the gain

The above mentioned reasons can be attributed to the limited gain obtained from the shunt feedback power amplifier in the typical case. The gain further drops to just 9 dB in the worst case scenario as seen from the corner simulation results in table 3.1.

To offset this 7 dB reduction in gain an active input stage is desired. An active stage has to be selected in such a way that, on one hand it strengthens the power amplifier in terms of gain and on the other hand it does not disturb the input matching.

Now that a potential solution for the gain problem has been found, attention can be focused to the problem of output matching. As explained in section 3.3.2, in order to reduce the amount of potential compression introduced by the output stage from -3.5 dB to -1.5 dB, the S_{22} target specification was pushed down from -14 dB to -10 dB. This new target value is fully met by the designed power amplifier over the entire frequency range on interest.

In the following section the design and performance of a new, improved power amplifier topology will be discussed.

3.5 Common Gate Power Amplifier

The need for higher power gain calls for the implementation of a new power amplifier, the same will be discussed here at lenght. The new power amplifier will be called the common gate power amplifier based on the active input common gate stage that it uses.

3.5.1 Input Stage

In section 3.4.3 it has been suggested that an active input stage that has the dual capability of providing wideband input matching to 50 Ω as well as contributing towards the power gain is desired. The common gate stage comes in as an obvious choice in this regard. As suggested in [29], the common gate input stage is attractive as compared to other topologies as it features wideband input impedance matching. Also, it offers good linearity, stability, and low power consumption. The input impedance of a common-gate stage can be approximated to $1/g_m$, where g_m is the transconductance of the transistor used. The g_m of a transistor is rather constant over a large bandwidth, and hence, it allows for a wideband input match to 50 Ω .

In Fig.3.13, the input common gate is shown. The input impedance for the common gate stage as explained, is,

$$R_{in} = \frac{1}{g_m} \tag{3.13}$$

where, g_m as already stated is the transconductance for transistor M.

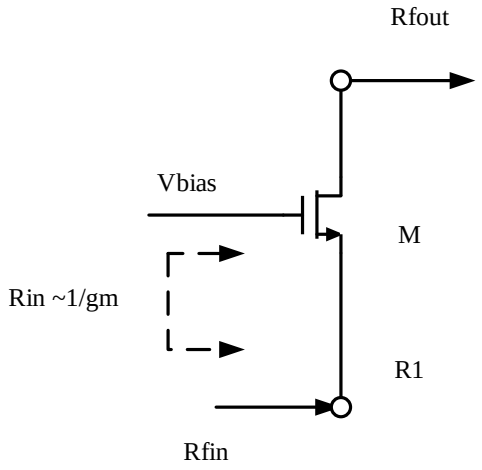


Figure 3.13.: Input stage: Common gate

A g_m of 20 m℧ would translate directly to an impedance of 50 Ω. This value of g_m is very realistic and can be easily achieved. It is hence, quite straight forward to achieve wideband matching with a common gate stage. Also, the common gate amplifier has no current gain but has a good voltage gain, this translates into a moderate power gain which can be expressed as,

$$PowerGain = g_m * R_L \tag{3.14}$$

where, R_L is the load impedance used with the common gate stage. The common gate stage hence, satisfies both the selection criteria of wideband matching as well as contributing towards the power gain.

3.5.2 Full Implementation and Simulation Results

The common gate input stage was integrated along with the core and the output stage to complete the full implementation for the common gate power amplifier. The full implementation is composed of the following three stages,

- Input Stage: Implemented using the common gate input stage discussed in section 3.5.1
- Core Stage: Implemented using the cascode topology discussed in section 3.3.1
- Output Stage: Implemented using the source follower discussed in section 3.3.2

The full implementation for the designed power amplifier has been shown in Fig.3.14. The three stages as shown, were connected together with the following additional elements,

- C_1 and C_2 as the blocking capacitors to isolate the dc biasing of each stage
- Voltage dividers created using the resistances R_1-R_2 and R_5-R_6 to provide the required gate bias voltages for the common gate transistor M_1 and the transistor M_2 from the cascode stage

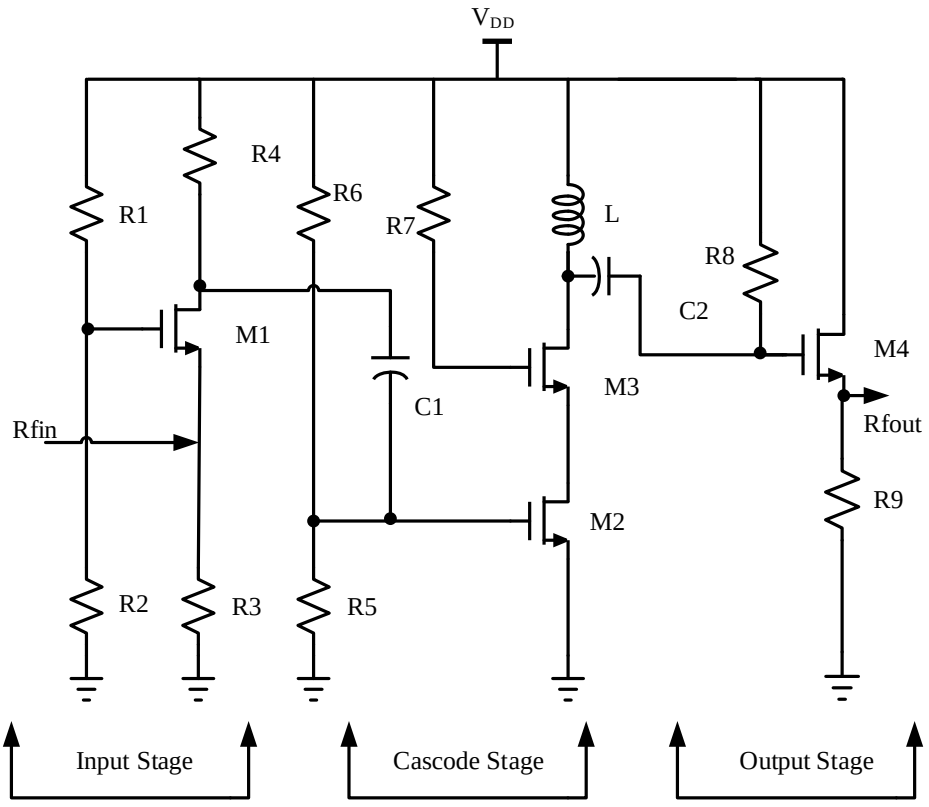


Figure 3.14.: Full Implementation: Common gate power amplifier

The implementation was followed by simulating the power amplifier to analyse it's performance. The power amplifier was simulated and analysed using the Spectre Circuit Simulator available with Cadence Virtuoso. The simulations results for the power amplifier have been summed up in Table 3.2. The parameters that

get fulfilled have been higlighted in blue and the ones that fail have been highlighted in red.

Parameter	Typical-Case
Frequency [GHz]	0.7-2.3
DC Power [mW]	126
OP1dB [dBm]	5.03
OIP3 [dBm]	16.27
NF [dB]	5.965
S_{11} [dB]	-12.02
S_{12} [dB]	-51.76
S_{21} [dB]	16.02
S_{22} [dB]	-10.12
Gain Flatness [dB]	1.947

Table 3.2.: Common gate power amplifier typical corner simulation results

The table throws up some interesting results that can be concluded as follows,

- Output Power (OP1dB): The 5 dBm target value gets fulfilled with the common gate power amplifier
- Gain (S_{21}): A minimum value of 16.02 dB has been achieved with the common gate power amplifier
- Noise Figure (NF): The common gate power amplifier touches a noise figure of roughly 6 dB
- Other Parameters: All the other parameters are more or less in the desired range

This topology like the shunt feedback power amplifier meets the output power requirement of 5 dBm. Also, this topology improves upon the power gain obtained from the shunt feedback power amplifier by 5 dB. This has resulted in the minimum power gain jumping up to 16.02 dB, although this is still 2 dB lower than the power gain specification, it is still a really good value for a CMOS power amplifier using just one inductor. The design specification for the gain was hence, lowered by 2 dB to 16 dB.

A major flaw for this implementation is however, it's noise figure of roughly 6 dB, which is the design specification for post layout simulations. The reason behind the high noise figure for a common gate input stage has been highlighted in [29]. The high noise contribution is due to the input matching condition, which restricts a certain value of transconductance to be used, that leads to low gain, and hence, high NF. Also, according to the Friis's formula highlighted in section 2.6, the input stage dominates the overall noise figure for an RF block, hence, the high noise figure from the input common gate stage results in an overall high noise figure for the power amplifier.

3.5.3 Noise Matching and Corner Simulation Results

As highlighted in the previous section, the designed common gate power amplifier exhibits 5 dB higher power gain than it's shunt feedback counterpart. This gain however, comes at the cost of 1 dB increase in the noise figure. The resulting noise figure stands at 5.965 dB which is almost the specified target noise figure from the post layout simulations. A worsening of anywhere between 1 dB to 2 dB for the noise figure can have been expected after the power amplifier is layouted, therefore, a mechanism to improve upon the noise figure has to be implemented.

A basic concept that can be useful in this regard is that, for every two port network, there is an optimum noise source admittance Y_{opt} that allows it to achive the minimum possible noise figure called NF_{min} [12]. The aim in this regard is to move the center of the noise circles to the center of the Smith chart so that Y_{opt} coincides with the source admittance Y_s. This is precisely the concept of noise matching i.e., to design an input matching network that allows the centers of the noise circles to move towards the center of the Smith chart. Also, to achieve the maximum gain the center of the gain circles needs to be moved towards the center of the Smith chart. These two tasks are more or less always conflicting which means that the maximum gain and minimum noise figure cannot, in general, be achieved simultaneously [14]. An indepth analysis is, hence, required to find a good trade-off between reducing the noise figure and not losing out too much on the gain. The same has been made in this section.

In Fig.3.15, the gain circles for gain varying from 14 dB to 17 dB have been plotted with a sweep of 1 dB, along with the gain circles, noise circles for a noise figure of 3 dB, 4 dB and 5 dB have also been plotted.

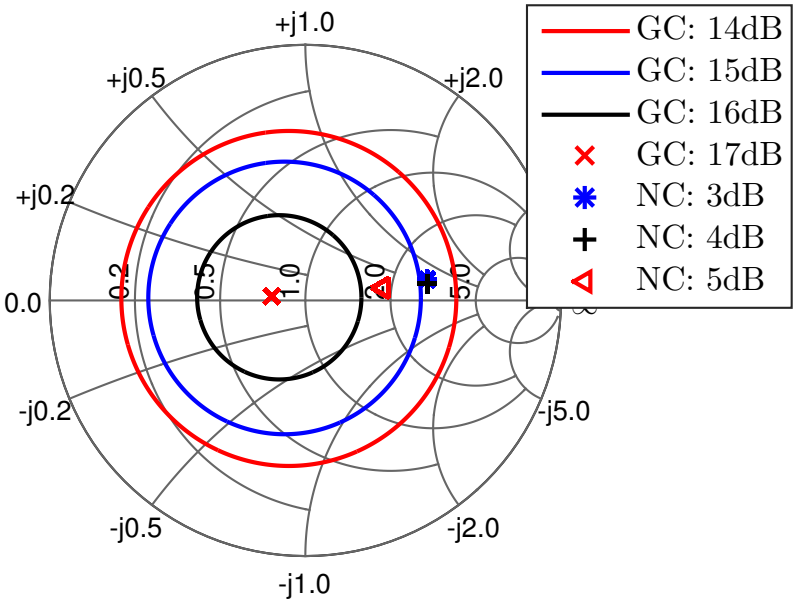


Figure 3.15.: Noise circles and gain circles without noisematching

From the plot it can be concluded that,

- For the designed power amplifier a noise figure of approximately 5 dB can be achieved without losing out on the gain
- If a noise figure of 4 dB is desired it would mean sacrificing the gain by 1 dB
- An even lower noise figure would demand a further reduction in gain, e.g., for 3 dB noise figure the gain would have to be sacrificed by roughly 2 dB

The noise matching has hence, been done for a noise figure of 5 dB, because for a power amplifier the power gain is a much more important parameter than it's noise figure. In Fig.3.16, only the gain circles for 15 dB and 16 dB along with noise circle of 5 dB have been highlighted (it is basically a zoomed in version of Fig.3.15). The smithchart plot shows that, to achieve a noise figure of 5 dB, the Γ_s required is $0.3\angle 8.3°$. This translates into Z_s of (91.68+j8.726) Ω.

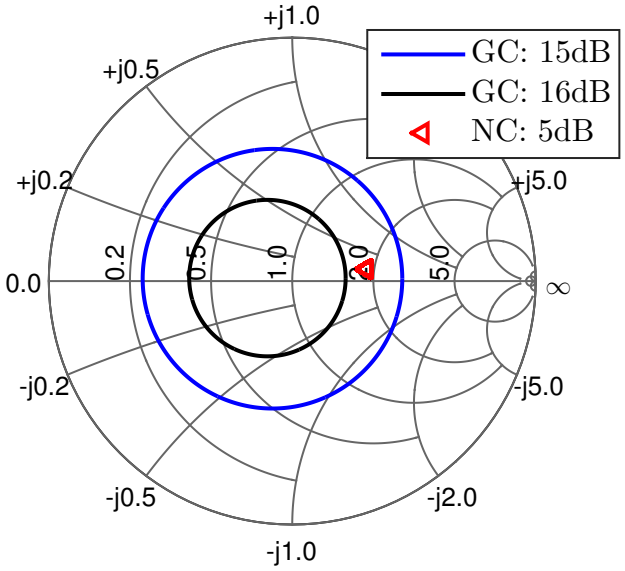


Figure 3.16.: Noise circle: 5dB and gain circles without noisematching

To perform matching to Z_s of (91.68+j8.726) Ω a capacitor would be first required to transform the imaginary part of Z_s. To calculate the value for the desired capacitor the following method has been used, $X_c = 8.726$ Ω at 2.3 GHz, also,

$$X_c = \frac{1}{2 * \pi * f * C} \tag{3.15}$$

where, f is the frequency at which the analysis has been conducted and
C is the capacitor value desired to achieve matching

This results into a capacitor of 7.925 pF, hence, an 8 pF capacitor has been used, which is represented as C1 in Fig.3.17.

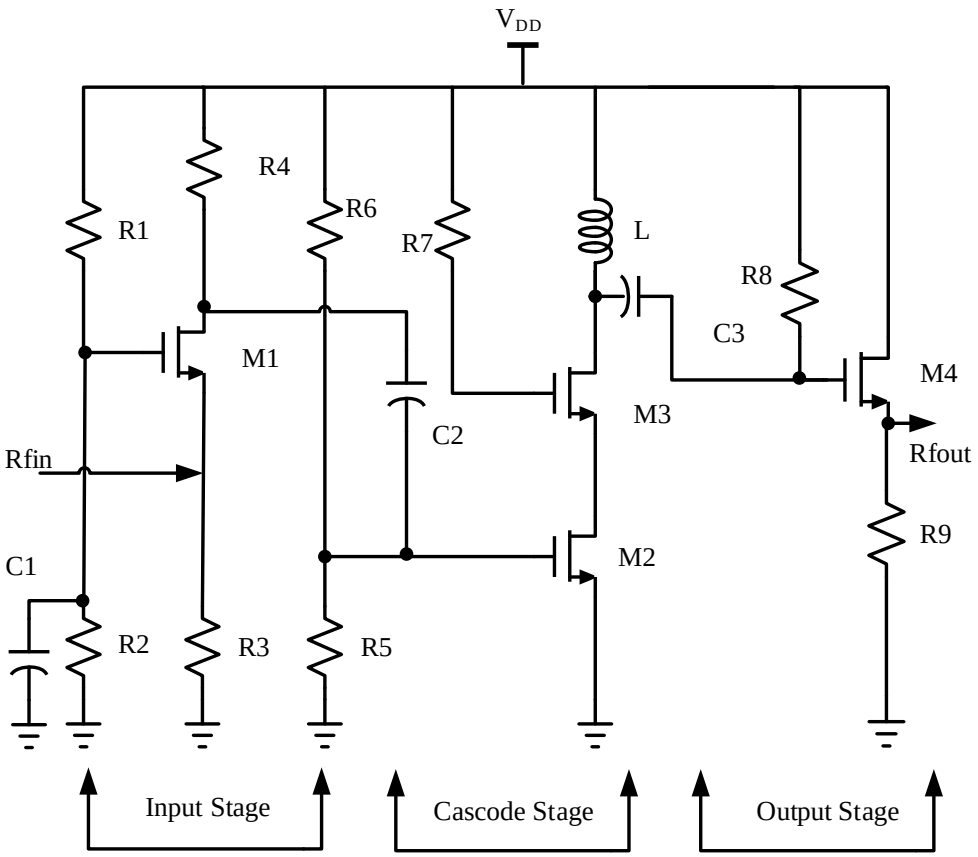


Figure 3.17.: Common gate power amplifier with noisematching

The matching for the real part has however, not been implemented as it would have required an inductor and the same could not be used due to area limitations on the chip. It is also clear from the following simulations and plots that matching to only the imaginary part of Z_s yields good enough results.

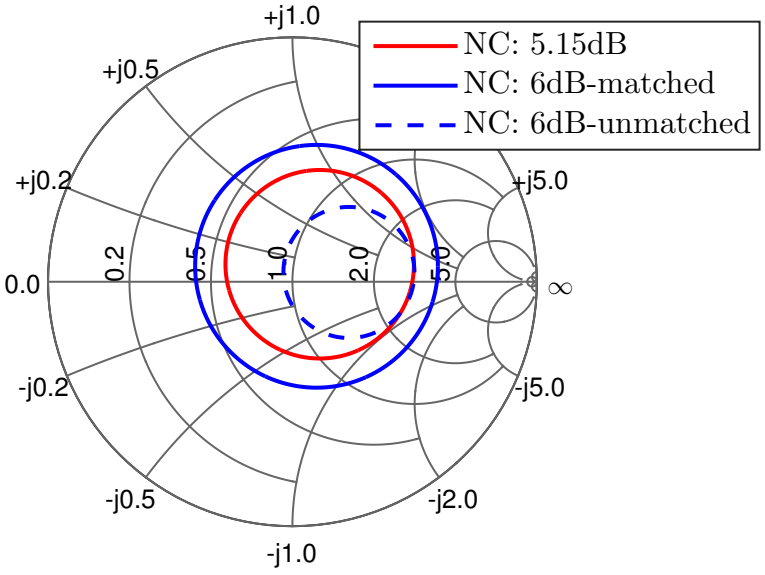


Figure 3.18.: Noise circles: 5.15 dB and 6 dB

In Fig.3.18, the noise circle for a noise figure of 5.15 dB (the achieved noise figure post matching) has been shown along with that for a noise figure 6 dB, in both the pre-noise matching and post-noise matching cases. From the plot it can be concluded that,

- Noise matching has lowered the noise figure for the power amplifier by rougly 0.85 dB to 5.15 dB
- The center of the noise circles post-matching have moved much closer to the center of the smith chart

These were precisely the two major targets laid out for noise matching. Next, a comparison between the achieved noise figure post noise matching (NF) and the minimum possible noise figure (NF-min) over the entire frequency range of design has been made. The results have been shown in Fig.3.19. It can be seen that the two differ roughly by a maximum of 0.2 dB at 700 MHz, which is a very nominal difference.

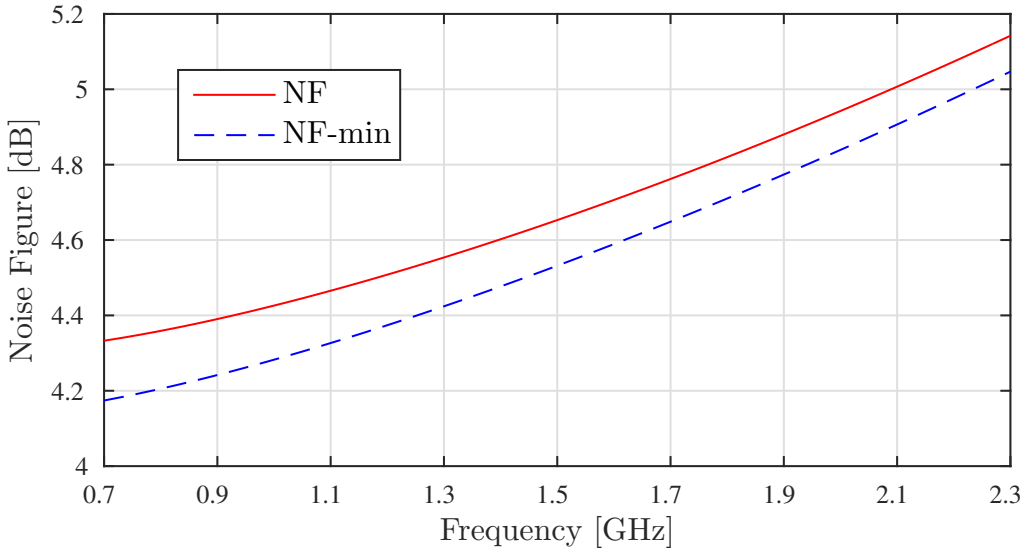


Figure 3.19.: Comparative Analysis: NF and NF-min post noise matching

After the noise figure for the power amplifier was brought down to a low enough value, it's performance was analysed. The power amplifier was simulated and analysed using the Spectre Circuit Simulator available with Cadence Virtuoso. Simulations were conducted for not only the nominal case but also to account for the variations in the process, voltage and temprature parameters (PVT variations). The corner analysis was done to cover the following variations,

- Process:
  - MOS: All combinations of slow, typical and fast PMOS and NMOS (ss, sf, tt, fs, ff cases)
  - Resistors: Worst Case, Typical Case and Best Case (wcs, typ, bcs cases)
  - Capacitors: Worst Case, Typical Case and Best Case (wcs, typ, bcs cases)
- Voltage: 3.0 V, 3.3 V, 3.63 V (10% variation)
- Temprature: 25 °C , 50 °C , 85 °C

The simulations results for the typical as well as PVT corners have been summed up in Table 3.3. The parameters that get fulfilled have been higlighted in blue and the ones that fail have been highlighted in red.

Parameter	Target-Specs.	Typical-Case	Corner-Simulations	
			Min	Max
Frequency [GHz]	0.7-2.3	0.7-2.3	0.7-2.3	0.7-2.3
DC Power [mW]	<300	126	103.5	151.6
OP1dB [dBm]	>5	5.07	3.261	5.81
OIP3 [dBm]	>20	16.44	14.49	17.52
NF [dB]	>6	5.142	4.932	5.319
S_{11} [dB]	<-10	-11.06	-12.99	-9.571
S_{12} [dB]	<-30	-53.25	-53.71	-52.72
S_{21} [dB]	>18	16.04	13.29	17.84
S_{22} [dB]	<-14	-10.34	-11.88	-9.197
Gain Flatness [dB]	<2	2.099	1.957	2.389

Table 3.3.: Common gate power amplifier corner simulation results

The table shows the following interesting results,

- Output Power (OP1dB): The 5 dBm target value gets fulfilled with the common gate power amplifier even post noise matching
- Gain (S_{21}): The gain value of 16 dB post noise matching has not been lost
- Noise Figure (NF): The noise figure has been brought down to 5.142 dB post noise matching
- Other Parameters: All the other parameters are more or less in the desired range and show nominal variations across all corners

Next, a comparative analysis for the two designed power amplifier toplogies would be done with the aim of choosing the appropriate implementation for layout.

3.6 Comparative Analysis

A comparison between CGPA and SFPA amplifier has been made and presented in 3.4. The parameters in one implementation that are better than those in the other implementation have been higlighted in blue.

Parameter	Shuntfeedback-PA	Commongate-PA
Frequency [GHz]	0.7-2.3	0.7-2.3
DC Power [mW]	153.3	126
OP1dB [dBm]	5.043	5.07
OIP3 [dBm]	17.5	16.44
NF [dB]	4.967	5.142
S_{11} [dB]	-10.28	-11.060
S_{12}[dB]	-46.53	-53.25
S_{21} [dB]	10.93	16.04
S_{22} [dB]	-10.11	-10.34
Gain Flatness [dB]	1.932	2.099

Table 3.4.: Comparision: Shuntfeedback-PA vs Commongate-PA

The comparative analysis can be summed up as follows,

- DC Power Consumption: Both topologies are under 50% of the available power budget
- Output Power (OP1dB): Both topologies satisfy the 5 dBm output power target at the schematic level
- Gain (S_{21}): The common gate power amplifier offers 5 dB higher power gain than the shunt feedback power amplifier
- Input and Output Matching (S_{11} and S_{22}): Both topologies meet the input output wide band matching criteria

Both topologies are more or less the same performance wise. The common gate power amplifier however, trumps the shunt feedback power amplifier because of a 5 dB higher power gain. This is the main driving force behind the decision to layout the common gate power amplifier.

4 Power Amplifier Layout

Chapter Overview: *This chapter highlights the layouting of the power amplifier and the techniques involved in the same. The layout for the power amplifier has been done using the Cadence Virtuoso Layout Suite in the 0.13 µm BiCMOS SG13GS technology. Apart from the layout, the post layout performance of the power amplifier has also been analysed with an ideal inductor, on-chip inductor and off chip inductor. The chapter concludes with a comparison between the power amplifier performance with the on-chip inductor and off-chip inductor.*

4.1 Layout

This section talks about the techniques involved in the layouting of the power amplifier. For an RF circuit, the signal integrity is a very important criterion, to satisfy this criterion all parasitics must be kept as small as possible and the RF signals routes must be kept as straight and as small as possible. RF signal lines and the overall circuit are very sensitive to cross-talk and interference and hence, sufficient measures need to be taken to isolate the layout from other circuit blocks. Also, to supress the impact of parasitic attenuation, RF signals lines should be routed using adequately thick metal lines. Other important techniques that should be implemented are the use of perpendicular RF traces to DC traces and the use of gradual tapering when connecting wide metal lines to thinner lines. RF circuits in general consume a very large amount of DC power and to satisfy the same, very thick supply and ground lines are required and they too should be layouted using higher or top metals that have very high current densities and introduce minimal attenuation.

The the fully layouted common gate power amplifier has been presented in Fig.4.1. The major highlights from the layout can be summed up as follows,

- The RF signal lines have been layouted in the ground-signal pattern to shield them from external interference
- A metal-1 layer has been used as the ground plane under the RF lines which have been layouted using metal-2 to have maximum positive impact from the ground-signal pattern
- Attention has also been paid to keep the RF signal routes sufficiently thick to minimize the potential parasitic attenuation

Generally, for an RF layout proximity matching is more important than individual instance matching. Techniques like common-centeroid and interdigitated layout yield less benefits for an RF layout as compared to an analog layout. Keeping this in mind the transistors have hence, been layouted using the multi-fingered approach. Multi-fingered approach brings along the following benefits,

- It decreases the amount of routing required as compared to the common centeroid or the interdigitated layout techniques
- This reduction in routing not only makes the layout less complex but also reduces the impact of parasitics

- Another advantage of the multifingered approach is that it reduces the C_{gs} and R_{gs} for the transistors being layouted

It is also clear from the layout that the, RF lines have been kept at 90° orientation to the DC lines and gradual tapering has been used wherever required. The designed power amplifier consumes approximately 123 mW of DC power, which translates into an overall current consumption of 38 mA. To satisfy the current requirements for each of the three power amplifier stages, the following steps have been taken during the layout,

- The supply lines and ground lines have been implemented with topmetal-1 which offers a current density of 15 mA/μm

- Since, the cascode stage consumes roughly 21 mA of current and this current flows via the inductor, this route has hence, been implemented using topmetal-2 which offers a current density of 16 mA/μm

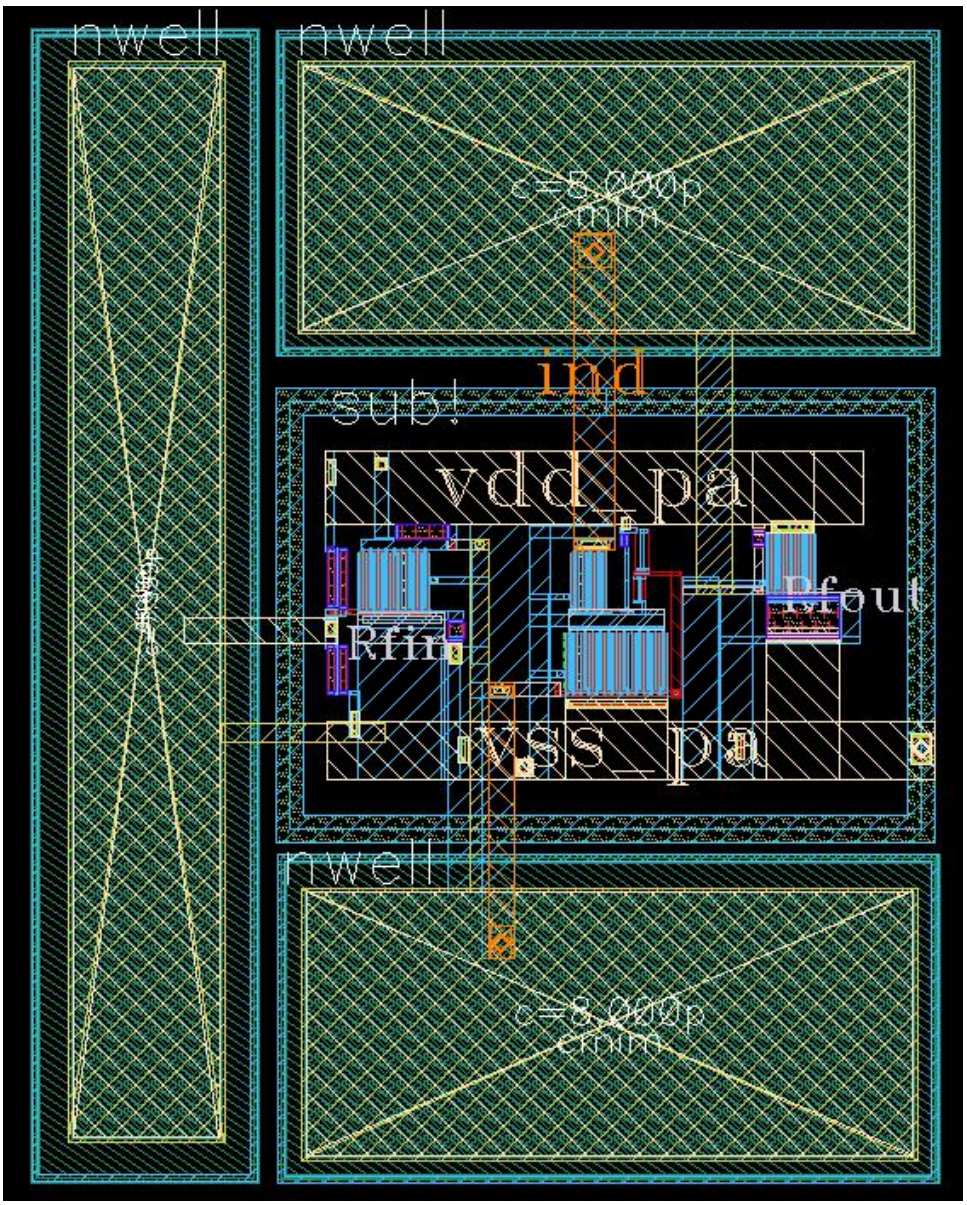


Figure 4.1.: Common gate power amplifier layout

Another important point for RF layouts is the need of isolation. To make sure that the layouted power amplifier is sufficiently isolated from the other layouted blocks on the chip, the following measures have been implemented

- A 3 contact, 10μm wide guard ring has been placed around the power amplifier with the aim of isolating it from the other circuit blocks
- This guard ring acts as a deterrence against cross-talk and interference both from and to the power amplifier
- Also, each capacitor used in the layout has been placed in a seperate n-well for better isolation

The overall power amplifier layout has a size 210 x 165 μm^2, which is inline with the primary requirement of on-chip integration for the designed power amplifier.

4.2 Post Layout Simulation Results with an Ideal Inductor

For the post layout simulations, the same test bench as used in section 3.5.2 has been used. The only difference is that, now the extracted version of the layout obtained using the Quantus QRC tool available with Cadence Virtuoso has been used.

The post layout simulation results for the power amplifier in the nominal case with an ideal inductor have been summed up in Table 4.1. The parameters that get fulfilled have been higlighted in blue and the ones that fail have been highlighted in red.

Parameter	Nominal Case
Frequency [GHz]	0.7-2.3
DC Power [mW]	122.7
OP1dB [dBm]	5.001
OIP3 [dBm]	17.1
NF [dB]	6.724
S_{11} [dB]	-18.72
S_{12} [dB]	-76.09
S_{21} [dB]	16.06
S_{22} [dB]	-10.02
Gain Flatness [dB]	1.972

Table 4.1.: Post layout simulations: Common gate power amplifier with ideal inductor

The results from the table can be concluded as follows,

- DC Power : The power amplifier still consumes only around 40% of the overall power budget in the post layout case with an ideal inductor
- Output Power (OP1dB): The 5 dBm target value is still met in the post layout case with an ideal inductor
- Gain (S_{21}): The gain does not drop down from 16 dB in the post layout case with an ideal inductor

- Noise Figure (NF): Noise figure breaches the 6 dB threshold in the post layout case with an ideal inductor

- Input-Output Isolation (S_{21}): The input-output isolation improves by 20 dB in the post layout case, this is a major boost for the amplifier's stability

- Input-Output Matching (S_{11} and S_{11}): The input and output matching targets of -10 dB have been met sucessfully in the post layout case with an ideal inductor

The results from the post layout case with an ideal inductor are good enough to move on to the inductor comparative analysis. The same would be covered in the next section.

4.3 Inductors for Power Amplifiers

As mentioned in section 3.1, an analyis is required to find out the most suitable inductor interms of Q-factor and self resonace frequency for the designed common gate power amplifier. An attempt has been made in this section to carry out the same. This section also talks a little about inductors in general and the two types of inductors available. Each type of inductor is then plugged into the designed common gate power amplifier and results from the post layout simulation have been discussed both individually as well as a comparitive analysis.

4.3.1 Main Characteristics of an Inductor

An inductor, also called a coil, choke or reactor, is a passive two-terminal electrical component that stores energy in a magnetic field when electric current flows through it [2]. For a real inductor the coil winding resistance, distance between the windings and the distance between the substrate and inductor windings introduce unwanted parasitic capacitance and resistance. A figure of merit is hence, required to determine how good an inductor implementation really is. The Quality Factor (Q-factor) has been used as this figure of merit that basically tells us how inductive the inductor really is, even in the presence of parasitics.

There are many different formulas that can be used to detemine the Q-factor for an inductor. The principle formula however is,

$$Q_{\text{ind}} = \frac{wL}{R} \tag{4.1}$$

where, ω is the frequency of interest in radians, L is the inductance value and R is the parasitic resistance that gets introduced during the inductor fabrication.

For the presented analysis however, the following modified version of the principle formula has be used,

$$Q_{\text{ind}} = \frac{Img[Z_{11}]}{Re[Z_{11}]} \tag{4.2}$$

where Z stands for the impedance parameter, Re and Img stand for the real and imaginary parts of Z_{11}.

The Quality factor of the inductor is clearly a function of frequency. It can hence, be plotted against frequency to check how effective an inductor would be at a particular frequency value. A plot of Q-factor versus frequency has been presented in Fig.4.2.

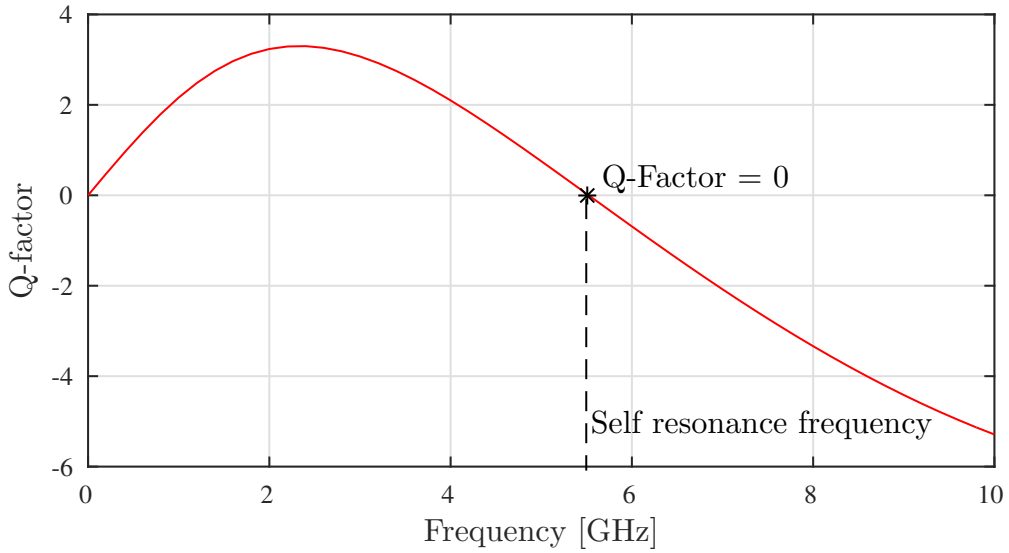


Figure 4.2.: Inductor: Q-Factor and SRF

It can be concluded from the plot that there is a point where the inductor's quality factor drops to 0. Beyond this point the inductor starts mimicing a capacitor. This frequency value at which the inductor's Quality factor drops to zero is called the Self Resonace Frequency (SRF) for an inductor. It is a direct function of the amount of parasitic capacitance that creeps in during the inductor's fabrication process or due to the inductor's topology. Hence, attention needs to be paid not only to the Q-factor but also the SRF while selecting an inductor.

4.3.2 Types of Inductors

The two basic types of inductors available to designers are,

- On-chip Inductor
- Off-chip Inductor

Each of them has a set of advantages and limitations which can be summed up in the following table,

Parameter	On-chip Inductor	Off-chip Inductor
Quality Factor	2 – 10	20 – 100
Area Consumption	High	Low
Customizable	Yes	No
Package Parasitics	Nil	Moderate to High
Overall Performance	Low to Moderate	Moderate to High
Integration Potentail	Low to Moderate	Moderate to High

Table 4.2.: On-chip Inductor vs off-chip Inductor

It is quite clear from Table 4.2, that the the off-chip inductor is superior interms of performance to it's on-chip counterpart. The one major advantage of the on-chip inductor however, is it's customizability. We can almost always create an on-chip inductor for a specific quality factor and self resonace frequency for

a particular frequency of operation. This is genearlly needed because the inductor library offered by the foundry does not usually cover the requirements that a PA imposes [25]. But since the proof of the pudding is in its eating, it is prudent to take a call on the most suitable inductor implementation from the simulation results.

Some attempts have been made in the past to compare on-chip and off chip passive elements for RF circuits. In [11], a complete and systematic analysis approach for on-chip versus off-chip passives has been presented. The performance of a common emitter Bipolar-LNA module for 5GHz WLAN is compared with both on chip and off chip inductors on the base, emitter and collector nodes. Another analysis has been carried out in [18]. In the paper, the performance of an a 2.4-GHz CMOS driver amplifier for bluetooth application has been analysed with on-chip and off-chip inductors connected to the drain node. These two papers have been used as a starting point for this analysis and would also come in handy at the time of the final overall performance comparison.

4.3.3 Post Layout Simulation Results with an On-chip Inductor

The analysis to compare the performance of the designed common gate power amplifier will be started off by discussing the on-chip inductor case first. The used on-chip inductor was synthesized in ADS using the RFIC Inductor Toolkit from Mühlhaus. The primary focus while synthesizing the inductor was kept on the self resonace frequency (SRF), hence, the 'Octagon diff' design toplogy was chosen. This toplogy has the potential to offer a very high SRF as it doesn't involve the use of a ground shield or stacked approach. The use of a ground shield or stacked approach increases the Q-factor but adds parasitic capacitance that kills the SRF. Also, sufficient attention was paid while dimensioning the inductor to keep the parasitic effects, primarly the parasitic capacitance at bay. The layout for the synthesized inductor has been shown in Fig.4.3. The inductor has an overall size of 450 x 448 μm^2.

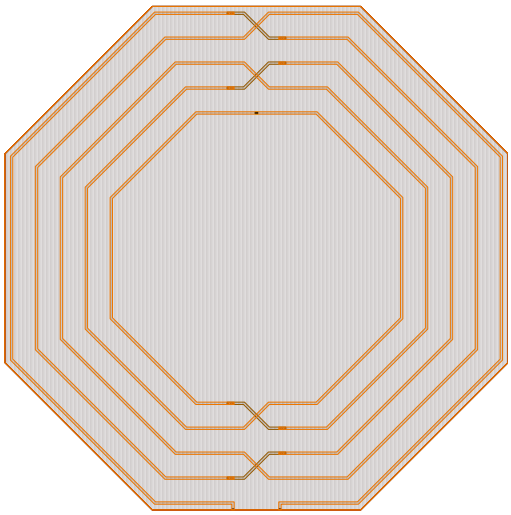


Figure 4.3.: The synthesized on-chip inductor using ADS

ADS also gives the option of analysing the inductor during synthesis itself. This allows the designer to select the best possible implementation in terms of Q-factor, SRF and area consumption. In Fig 4.4, the Q-factor for the synthesized inductor has been plotted.

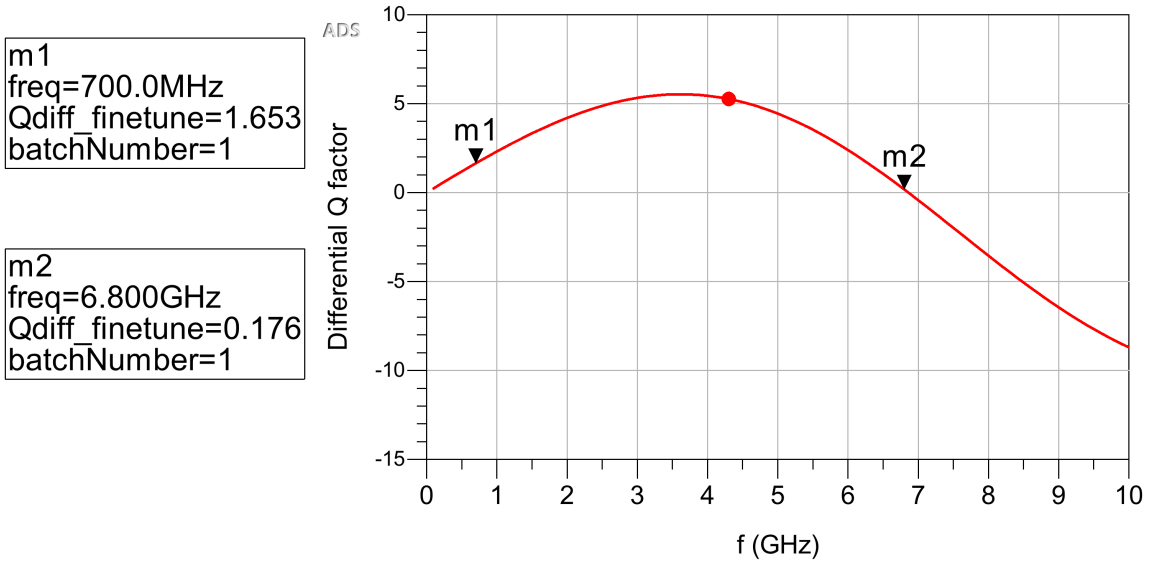


Figure 4.4.: On-chip inductor: Q-Factor vs Frequency

The Q-factor for the synthesized inductor lies between 1.65 and 4.87 over the frequency range of interest. The inductor also boasts of an SRF of almost 6.9 GHz which is very important to have a reliable design from the point of view of manufacturability. This high SRF is the hence, the primary highlight of the inductor. This SRF however, comes at a cost. In Fig.4.5, the attained inductance value at the three principle frequencies of 0.7 GHz, 1.5 GHz and 2.3 GHz has been shown. The inductor was designed with a central frequency of roughly 4.2 GHz to attain a high enough SRF which has resulted in anywhere between 2 nH to 3 nH lower inductance than expected. These values are however, still decent enough to carry out the performance analysis.

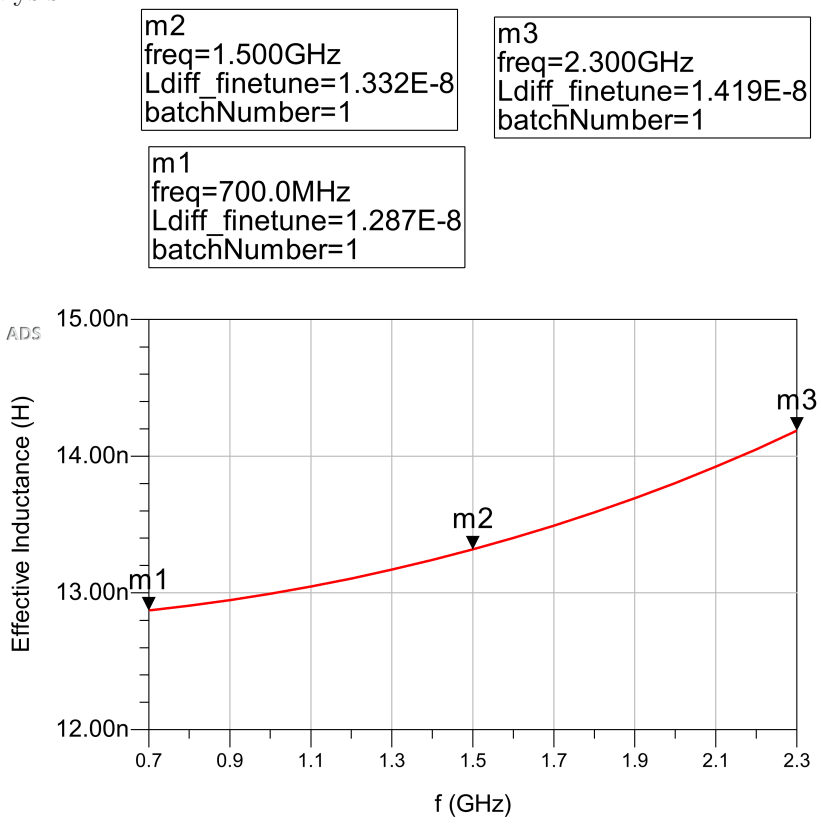


Figure 4.5.: On-chip inductor: Inductance vs Frequency

For the post layout simulations the same test bench as used in section 3.5.3 has been used. The only difference like in the ideal inductor case is that, that now the extracted version of the layout obtained using the Quantus QRC tool available with Cadence Virtuoso has been used. The simulations results for the typical corner have been summed up in Table 4.3. The parameters that get fulfilled have been highlighted in blue and the ones that fail have been highlighted in red.

Parameter	Typical-Case
Frequency [GHz]	0.7-2.3
DC Power [mW]	124.5
OP1dB [dBm]	4.013
OIP3 [dBm]	13.94
NF [dB]	6.692
S_{11} [dB]	-18.92
S_{12}[dB]	-73.91
S_{21} [dB]	15.09
S_{22}[dB]	-10.34
Gain Flatness [dB]	2.147

Table 4.3.: Post layout simulation results: Common gate power amplifier with on-chip inductor

The results from the table can be concluded as follows,

- Output Power (OP1dB): The power amplifier fails to meet the 5 dBm design target in the post layout case with an on-chip inductor
- Gain (S_{21}): The gain drops by roughly 1 dB to 15.09 dB in the post layout case with an on-chip inductor
- Output 3rd intercept point (OIP3): The OIP3 falls by over 3 dBm in the post layout case with an on-chip inductor
- Other Parameters: All other parameter are more or less in the desired range

There are two primary reasons for this perfomance drop,

- Q-Factor: The on-chip inductor has a very low quality factor that never exceeds 4.87
- Actual Inductance: The inductance value has been compromised by atleast 2 nH to attain a high enough SRF

Next, the perfomance of the designed power amplifier with an off-chip inductor will be analysed.

4.3.4 Post Layout Simulation Results with an Off-chip Inductor

Now that the post layout simulations results for the common gate power aplifier with an on-chip inductor have been presented and discussed, attention can be focused to the off-chip inductor. To simulate the power amplifier performance with an off-chip inductor the s-parameter file for '0302CS-16NXJE_': 16 nH inductor available from Coilcraft was used. The inductor was first analysed on it's own to see it's Q-factor and SRF. The results from the analysis have been plotted in Fig.4.6.

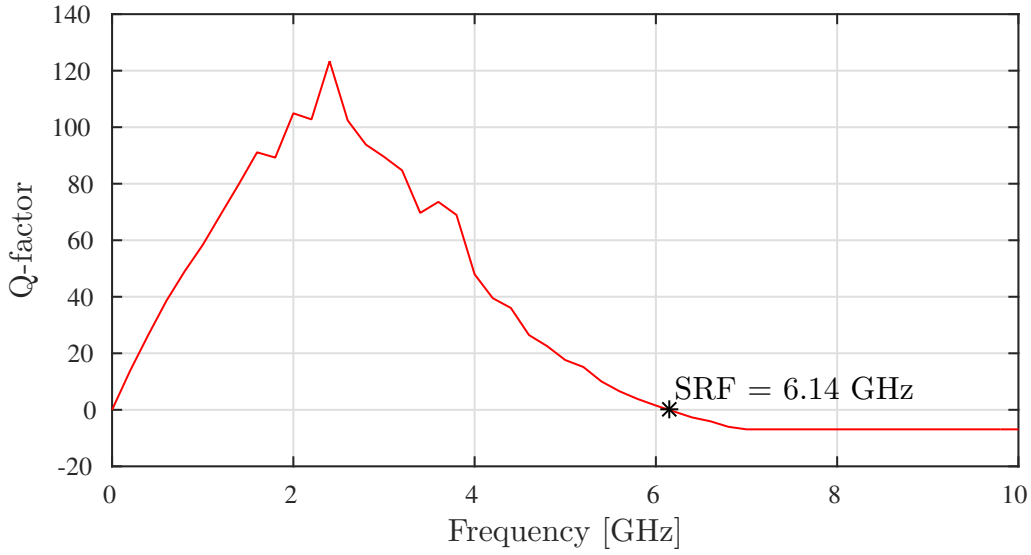


Figure 4.6.: Off-chip inductor: Q-Factor vs Frequency

The inductor has a good SRF of 6.14 GHz. Also, it is quite clear from the plot that this off-chip inductor offers a much higher quality factor than it's on-chip counterpart. The Quality factor for the inductor at the three principle frequencies of interest has been summed up in Table.4.4

Frequency [GHz]	Q-Factor
0.7	43.78
1.5	85.52
2.3	113.1

Table 4.4.: Q factor for off-chip inductor

The only thing now left to do is to simulate and analyse the performance of the designed commong gate power amplifier with the off-chip inductor. Exactly like in the previous cases, for the post layout simulations, the same test bench as used in section 3.5.3 has been used. The only difference is that, that now the extracted version of the layout obtained using the Quantus QRC tool available with Cadence Virtuoso has been used. The simulations results for the typical as well as PVT corners have been summed up in Table 4.5. The parameters that get fulfilled have been highlighted in blue and the ones that fail have been highlighted in red.

Parameter	Target-Specs.	Typical-Case	Corner-Simulations	
			Min	Max
Frequency [GHz]	0.7-2.3	0.7-2.3	0.7-2.3	0.7-2.3
DC Power [mW]	<300	134.7	108.8	163.6
OP1dB [dBm]	>5	5.013	3.915	5.759
OIP3 [dBm]	>20	17.14	15.84	18.06
NF [dB]	>6	6.848	6.667	7.153
S_{11} [dB]	<-10	-19.36	-20.5	-17.99
S_{12} [dB]	<-30	-75.070	-75.44	-74.16
S_{21} [dB]	>18	15.9	13.99	17.16
S_{22} [dB]	<-14	-10.02	-11.04	-9.298
Gain Flatness [dB]	<2	2.191	2.035	2.544

Table 4.5.: Post layout simulation results: Common gate power amplifier with off-chip inductor

The results from the table can be concluded as follows,

- DC Power : The power amplifier still consumes less 50% of the overall power budget in the post layout case with an off-chip inductor
- Output Power (OP1dB): The 5 dBm target value has been met in the post layout case with an off-chip inductor
- Gain (S_{21}): The gain drops down to 15.9 dB from 16 dB in the post layout case with an off-chip inductor, this is a however, a very tiny drop
- Noise Figure (NF): Noise figure again breaches the 6 dB threshold in the post layout case with an off-chip inductor
- Input-Output Isolation (S_{12}): The input-output isolation remains better than -75 dB in the post layout case with an off-chip inductor
- Input-Output Matching (S_{11} and S_{11}): The input and output matching targets of -10 dB each have been kept fulfilled in the post layout case with an off-chip inductor
- Corner Variations: Each parameter shows a very nominal deviation across all PVT corners

Next, each power amplifier design parameter has been individually plotted for the off-chip inductor case. The first parameter shown in Fig.4.7 is the 1-dB output and input compression points. The 1-dB output compression point can also be seen as the maximum deliverable output power from the power amplifier. Inline with the design specification, a value of 5 dBm has been achieved.

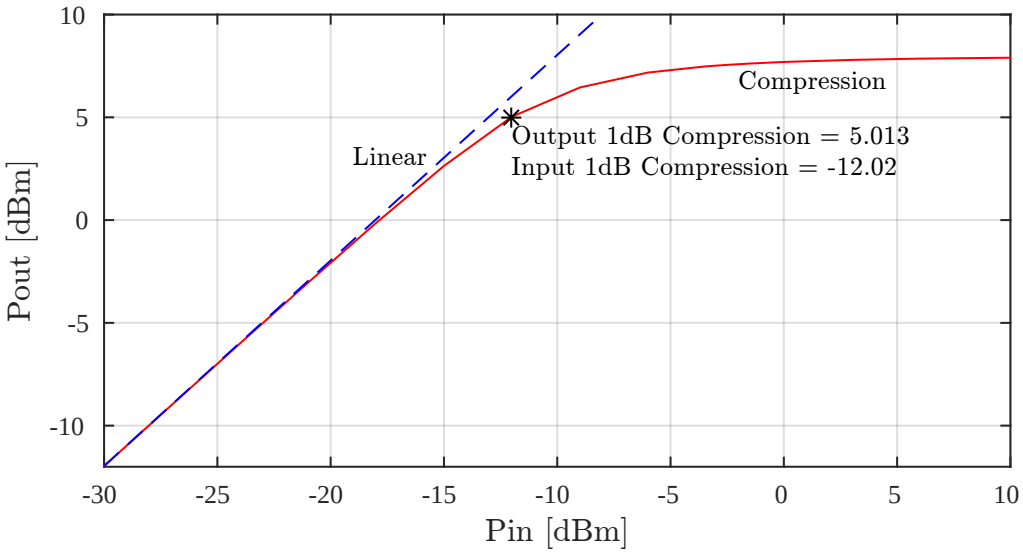


Figure 4.7.: Power amplifier 1 dB compression point

Next, in Fig.4.8, the output third order intercept point (OIP3) for the power amplifier has been shown.

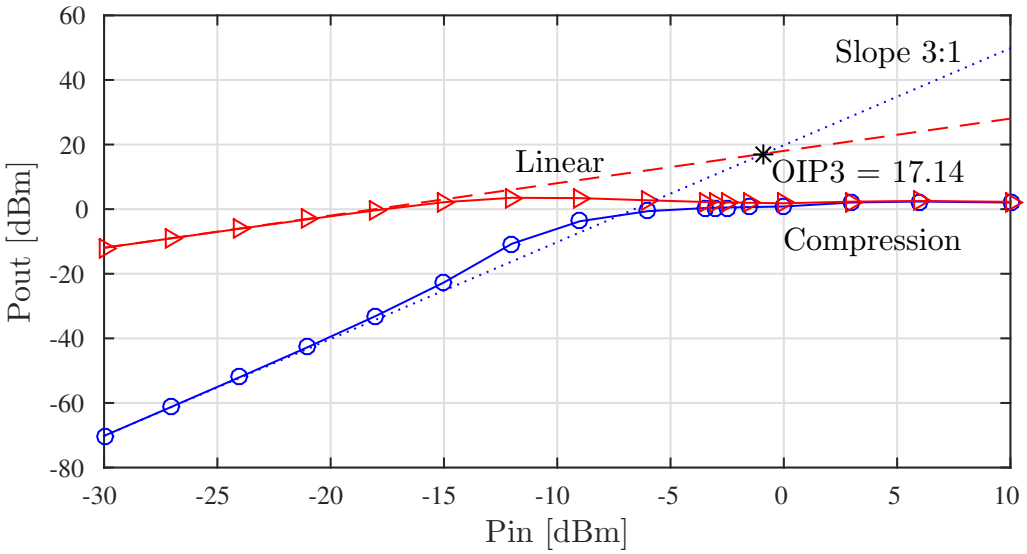


Figure 4.8.: Power amplifier 3rd order intercept point

The OIP3 achieved is indicative of the linearity of a power amplifier. Although, the designed power amplifier does not reach the target specification of 20 dBm, a value of above 17 dBm can be considered fairly good.

The OIP3 is followed by plots for the S_{11} and S_{22} for the designed power amplifier. These parameters highlight the extent of input and output matching to 50Ω. In Fig.4.9 the s-parameters have been plotted against the frequency range of interest. It can be seen that both the s-parameters fullfill the design target of -10 dB. Also in Fig.4.10, the S_{11} and S_{22} for the designed power amplifier have been plotted on the smith chart.

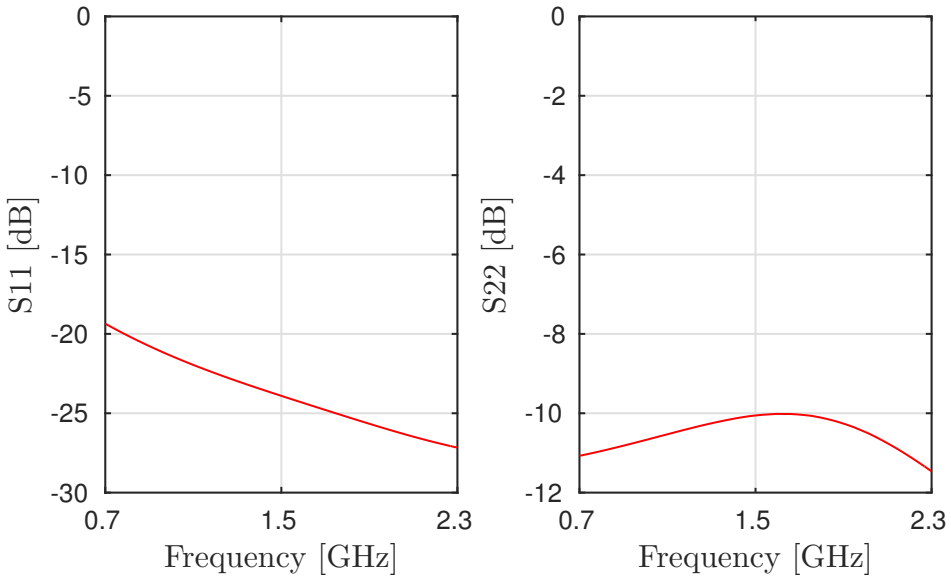
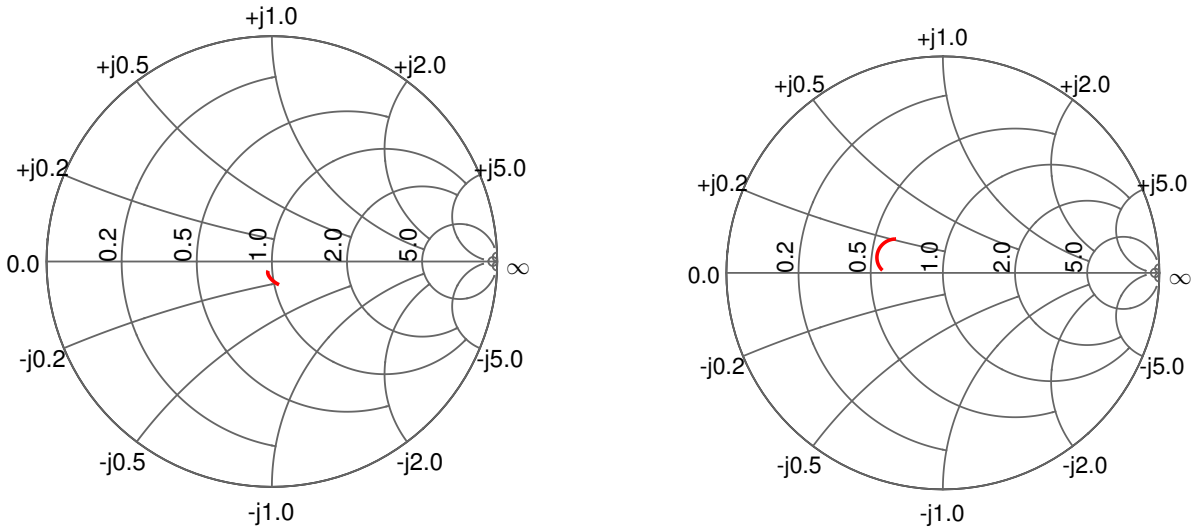


Figure 4.9.: Power amplifier: S_{11} and S_{22}



(a) S_{11} (b) S_{22}

Figure 4.10.: Power amplifier: S_{11} and S_{22} plotted on smith chart

The smith chart plots for S_{11} and S_{22} show that,

- S_{11} is capacitive: This is due to capacitor C1 shown in Fig.3.17, which is used to achieve noise matching. The capacitor helped in pushing the noise figure down by roughly 0.85 dB but has a bearing on the input impedance as shown in the smith chart plot for S_{11}.

- S_{22} is inductive: This is due to the drain inductor L used with the cascode stage. This inductor has a major influence on the ouput impedance of the power amplifier.

In Fig.4.11, the power gain (S21) and the input-output isolation (S12) have been shown. The power amplifier achieves a minimum gain of 15.9 dB with a gain flatness of roughly 2 dB, which is inline with the redesigned target specification for gain. Also, a high gain can render a power amplifier unstable. For the power amplifier to be unconditionally stable it has to have excellent input-output isolation.

A minimum value of -75 dB has been achieved for this parameter which ensures that the power amplifier is highly stable.

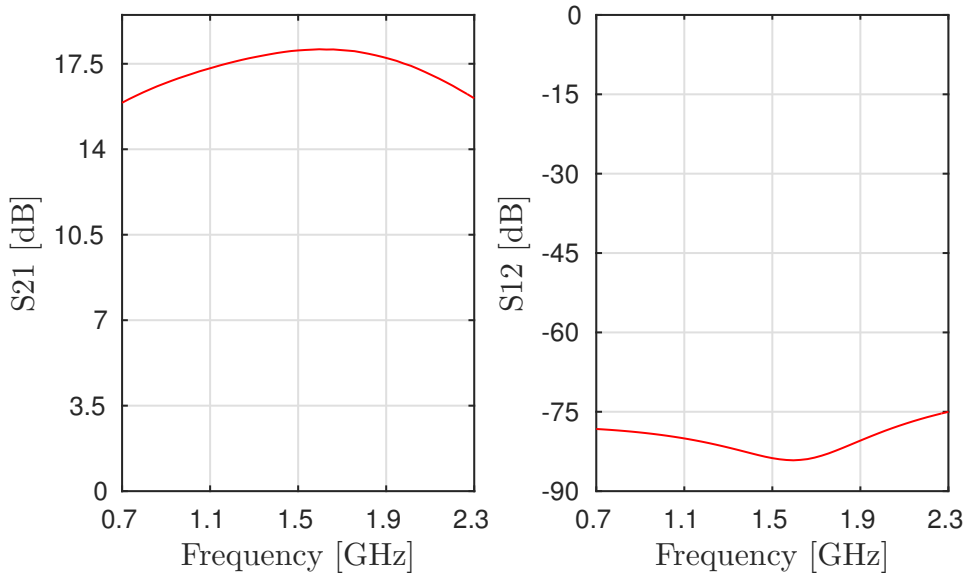


Figure 4.11.: Power amplifier: S21 and S12

Next in Fig.4.12, the resulting noise figure for the designed power amplifier has been shown. The power amplifier does not satisfy the criterion of 6 dB noise figure but a value of 6.85 dB is still quite good considering the fact that the power amplifier would be placed at the end of the RF signal chain, which would make it's contribution to the overall noise figure for the RF signal chain almost negligible.

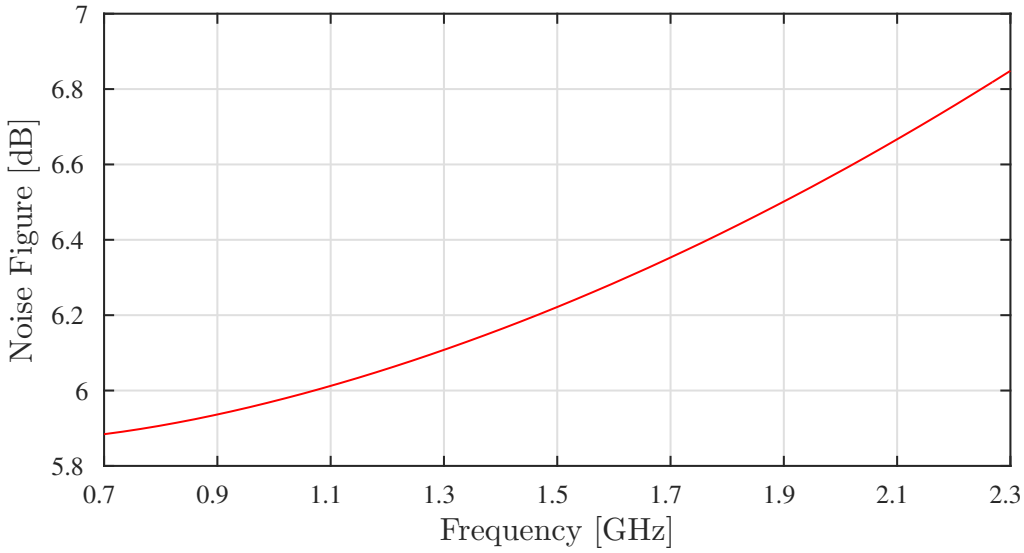


Figure 4.12.: Power amplifier: Noise figure

Last but not the least, the value for the power amplifier stability parameters the K-factor and the B1f have been shown in Fig.4.13. From the figure it is clear that,

- K-factor > 1
- B1f > 0

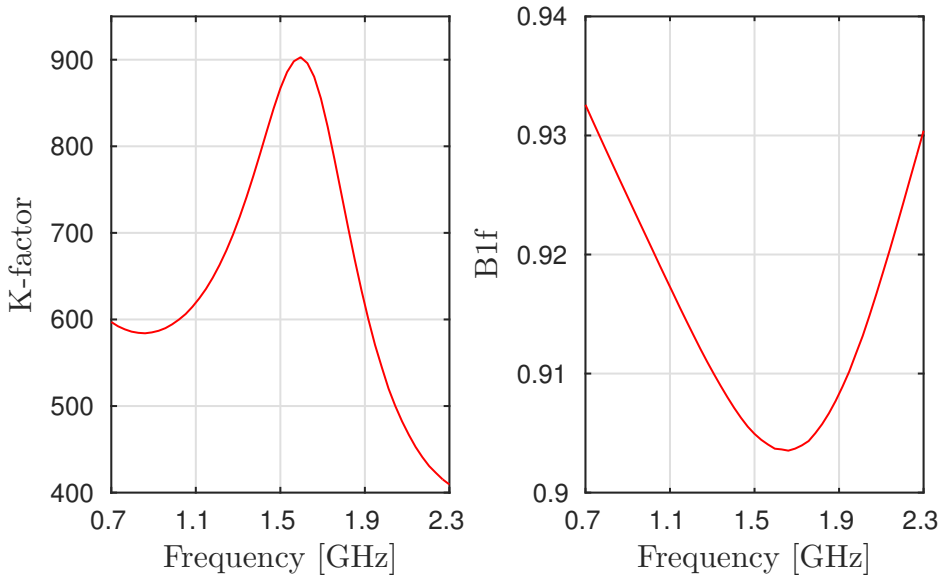


Figure 4.13.: Power amplifier stability parameters: K-factor and B1f

These values for the K-factor and B1f prove that the designed power amplifier is unconditionally stable.

4.3.5 Power Amplifier Results Comparison: On-chip Inductor vs Off-chip Inductor

Now that the performance for the power amplifier has been discussed for both the on-chip inductor as well as the off-chip inductor case, it makes sense to do an overall parameter by parameter comparison to decide upon the most apt inductor type for the power amplifier. In Table.4.6 the same has been done. The parameters in one implementation that are better than those in the other implementation have been higlighted in blue.

Parameter	On-chip-Inductor	Off-chip-Inductor
Frequency [GHz]	0.7-2.3	0.7-2.3
DC Power [mW]	124.5	134.7
OP1dB [dBm]	4.013	5.013
OIP3 [dBm]	13.94	17.14
NF [dB]	6.692	6.848
S11 [dB]	-18.92	-19.36
S12 [dB]	-73.91	-75.07
S21 [dB]	15.09	15.9
S22 [dB]	-10.34	-10.02
Gain Flatness [dB]	2.147	2.191

Table 4.6.: Power amplifier performance comparision: on-chip-Inductor vs off-chip-Inductor

The comparative analysis from the table can be concluded as follows,

- Output Power (OP1dB): The 5 dBm target value has been met with the off-chip inductor only, with the on-chip inductor the output power drops by 1 dBm
- Gain (S_{21}): The off-chip inductor tops the on-chip inductor interms of gain by roughy 1dB

- Other Parameters: All other parameter are more or less the same with either inductor type

The S-parameter results for the power amplifier with both on-chip and off-chip inductors have been plotted next. These plots would give us an insight into the performance variation introduced by the inductor type as a function of frequency. The first plot shown in Fig.4.14, shows a comparison between the S_{11} for both cases. This is followed by Fig.4.15 and Fig.4.16, that draw comparisons between the S_{12} and the S_{22} for the on-chip and off-chip cases.

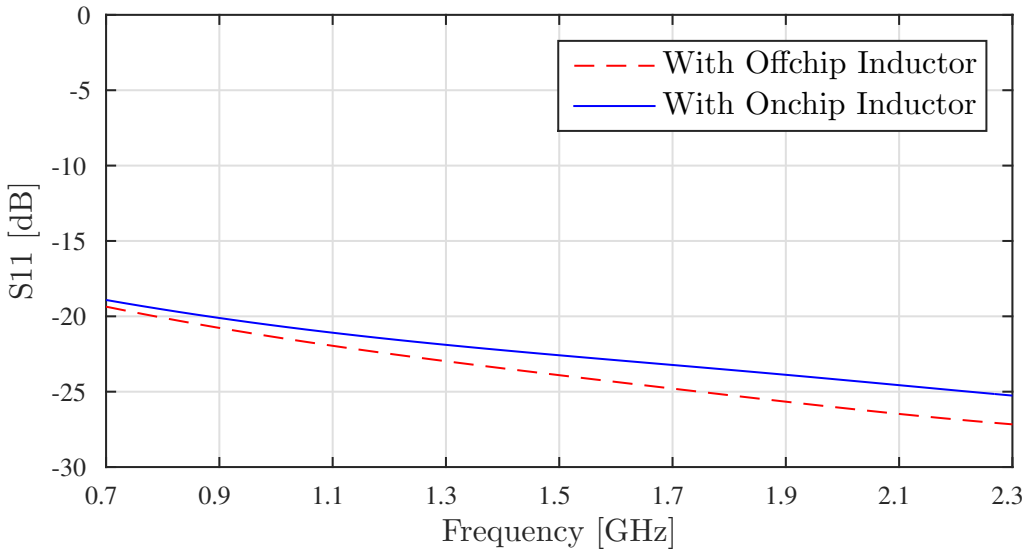


Figure 4.14.: S11: On-chip Inductor vs Off-chip Inductor

It is clear from the above plot that the S_{11} criterion gets fulfilled for both the on-chip aswell as the off-chip inductor case. Next, in Fig.4.15 the S_{12} with on-chip and off-chip inductor has been compared. It can be seen in the plot that both the values are more or less the same and show the same trend across the entire frequency range of interest.

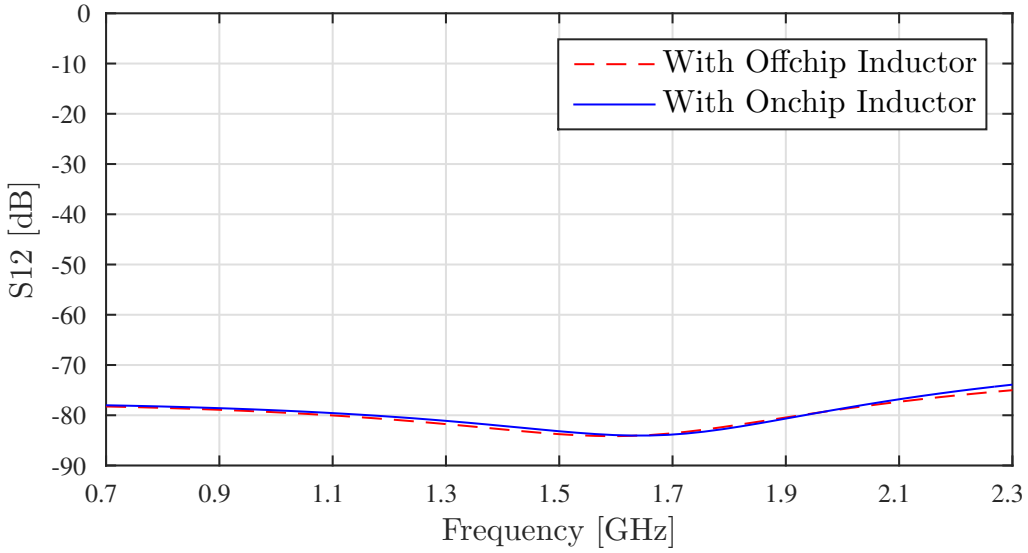


Figure 4.15.: S12: On-chip Inductor vs Off-chip Inductor

Another interesting plot would be Fig.4.16 because it compares the output matching criterion for the power amplifier with an on-chip and off-chip inductor. The scaled down S_{22} design specification of -10 dB is met for both the cases. The slighltly better value with the on-chip inductor is due to the higher parasitic resistance that the on-chip inductor has.

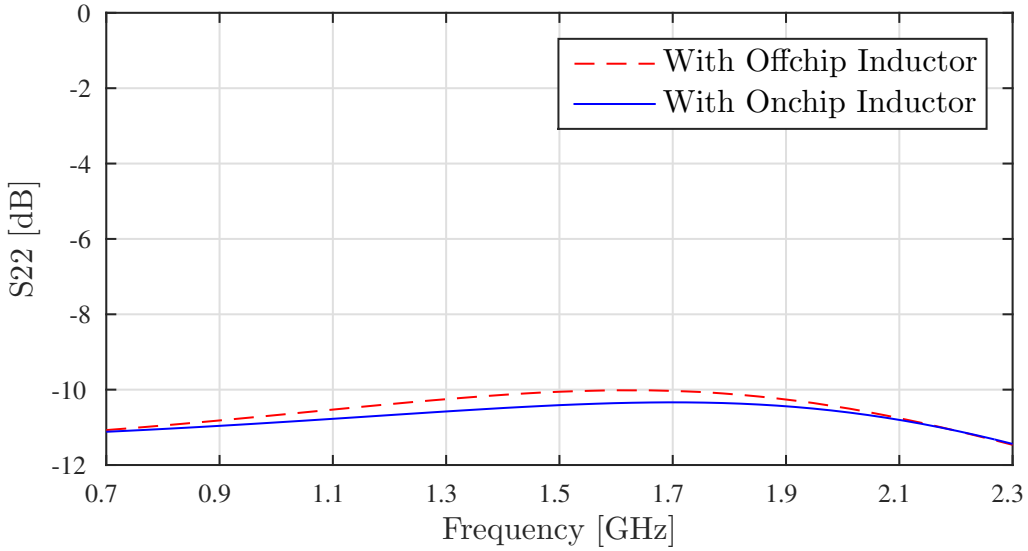


Figure 4.16.: S22: On-chip Inductor vs Off-chip Inductor

Last but not the least, the S_{21} attained by the common gate power amplifier with on-chip and off-chip inductor has been compared in Fig.4.17. The power amplifier with the off-chip inductor has a minimum S21 value of almost 16 dB, which is 1 dB higher than in the case of an on-chip inductor. This is hence, one area along with the output power where the the off-chip inductor clearly tops the on-chip inductor.

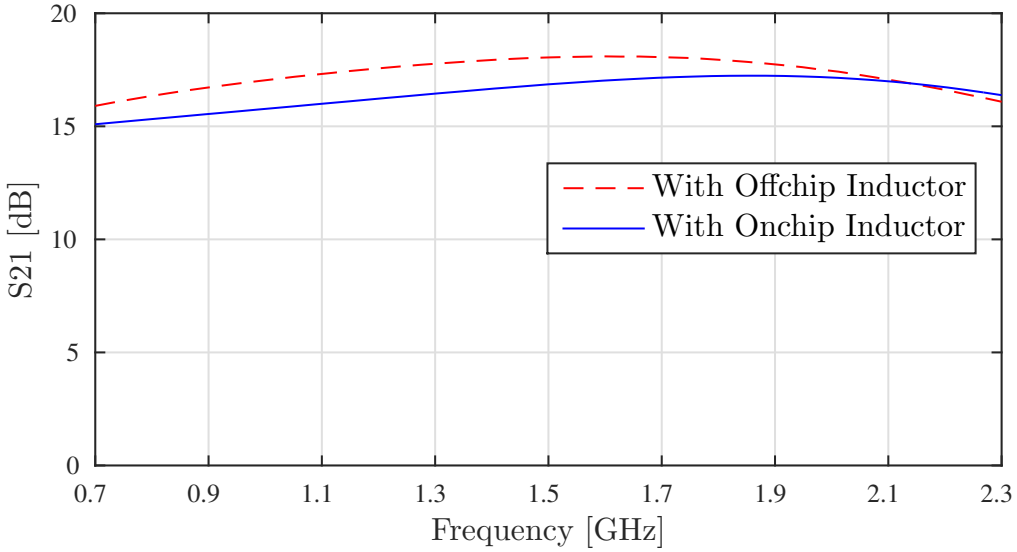


Figure 4.17.: S21: On-chip Inductor vs Off-chip Inductor

Better performance with an off-chip inductor is due to it's higher quality factor. The off-chip inductor offers a Q-factor of more than 43 over the entire frequency range of interest, this means that the actual inductance is much higher than the parasitic resistance that has the capability to limit the output volatge swing for the power amplifier.

It is exactly the opposite for the on-chip inductor where the the quality factor lies between 1.65 to 4.87, this means that the parasitic resistance has a much larger value here. This parasitic resitance component eats into the ouput voltage swing for the power amplifier and hence, limits not only the power gain but also the maximum deliverable output power.

The 1 dB loss in power gain and 1 dBm loss in output power are inline with the results shown in [11] and [18]. In [11], the transducer gain for the LNA drops from 21.6 dB in the off-chip inductor at all nodes case to just 16.2 dB in the on-chip chip inductor at all nodes case. A similar trend can be seen in [18], here the power gain for the analysed CMOS driver amplifier drops from 17.8 dB to 16.2 dB at 2.4 GHz. The output power however, shows a much sharper drop at the same frequency i.e., it drops from 6.8 dBm to 3.2 dBm. From these results it can be safely said that the off-chip inductor should be the obvious choice for the designed power amplifier.

4.4 Power Amplifier Performance Analysis

Now that the CMOS power amplifier has been designed and layouted, an overall performance analysis for it can be done. Also, at various points during the design process the target specifications for the power amplifier were redesigned due to one limitation or the other. The initial target specifications, the re-designed specifications and achieved specifications in the off-chip inductor case for the power amplifier have been organized in Table 4.7.

Parameter	Target-Specs.	Redesigned-Specs.	Achieved-Specs.
Frequency [GHz]	0.7-2.3	Unchanged	0.7-2.3
DC Power [mW]	300	Unchanged	134.7
OP1dB [dBm]	5	Unchanged	5.012
OIP3 [dBm]	20	Unchanged	17.14
NF [dB]	6	Unchanged	6.848
S_{11} [dB]	-10	Unchanged	-19.36
S_{12} [dB]	-30	Unchanged	-75.07
S_{21} [dB]	18	16	15.9
S_{22}[dB]	-14	-10	-10.02
Gain Flatness [dB]	2	Unchanged	2.191

Table 4.7.: Power amplifier performance analysis

The results from the table can be concluded as follows,

- Output Power (OP1dB): The 5 dBm target specification was not required to be changed and has been met.
- Gain (S_{21}): The gain specification was brought down by 2 dB to keep the noise figure in check as explained in section 3.5.3. The redesigned specification has been met gracefully.
- Output Matching (S_{22}): The target S_{22} was reduced down to -10 dB to limit the amount of compression from the output stage. The same has been explained about in section 3.3.2.
- All other specifications were more or less met without the need for a redesign.

Now, that a basic analysis of the overall power amplifier performance has been done, it makes sense to list out the reasons for the reduced performance. The same as been done in the next section.

4.5 Reasons for Reduced Performance

An attempt has been made in this section to attribute reasons to the CMOS amplifiers reduced performance. The discussion would be centered around power gain and output power. These two parameters have been chosen since, these are the two most important design parameters involved in any power amplifier design process.

4.5.1 Output Stage Tradeoff

As discussed in section 3.3.2, the output stage chosen for the designed power amplifier brings along a strong tradeoff between the attainable output matching and the compression it introduces. More light has been thrown on this trade off in this section. In Fig.4.18, the compression introduced by the output stage has been plotted on the y-axis in dB while the input power has been plotted on the x-axis in dBm.

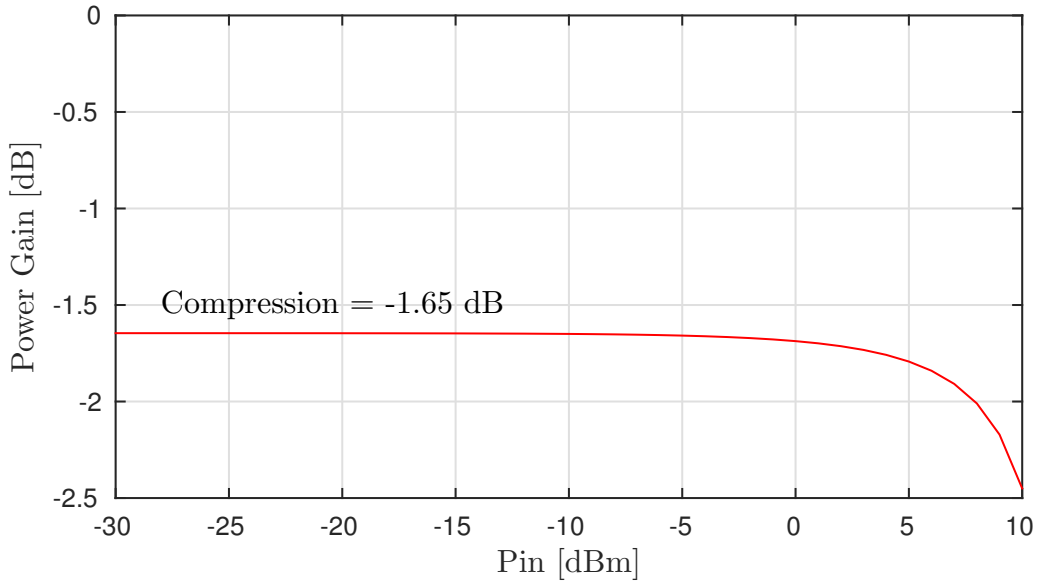


Figure 4.18.: Output stage: Power gain

This result confirms the fact that the output stage indeed introduces compression. This is because the source follower itself can never have a voltage gain greate than unity. The value of -1.65 dB is also very close to the value of -1.5 dB, discussed in section 3.3.2 for which the power amplifier has been designed. In Fig.4.19, the power amplifier output stage has been shown once again. Uptill now the tradeoff discussion for this stage has been centered around the value of the resistance R_2, another variable that can influence the performance of the output stage and hence, of the power amplifier is the effective width of MOS M_1. This will be now be the center of attention.

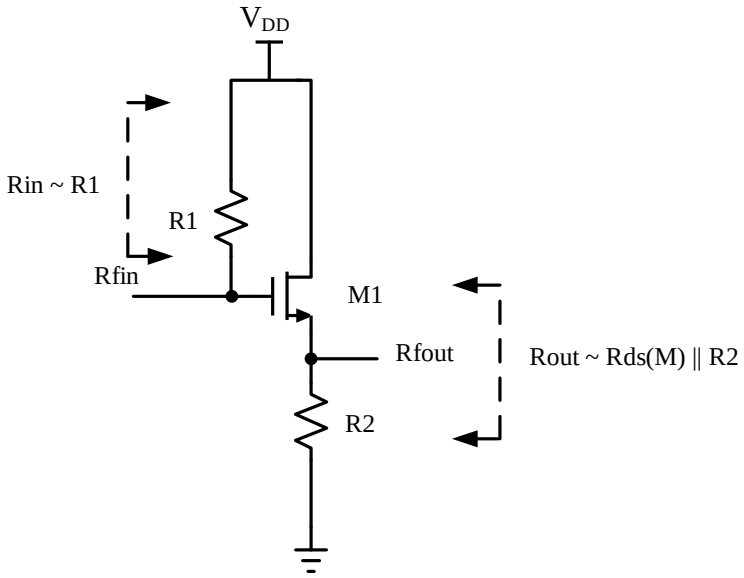


Figure 4.19.: Power amplifier: Output Stage

In Fig.4.20, the overall performance of the power amplifier has been analysed as a function of it's output stage. On the left y-axis the S_{21} and on the right y-axis the S_{22} both in dB for the power amplifier have been plotted. On the x-axis the MOS multiplication factor has been swept from 12 to 20 in steps of 1 each. The MOS multiplication factor basically decides the effective width of MOS M_1. As an example, if the MOS multiplictaion factor is equal to 10, then the effective width of MOS M_1 is 10*10 μm.

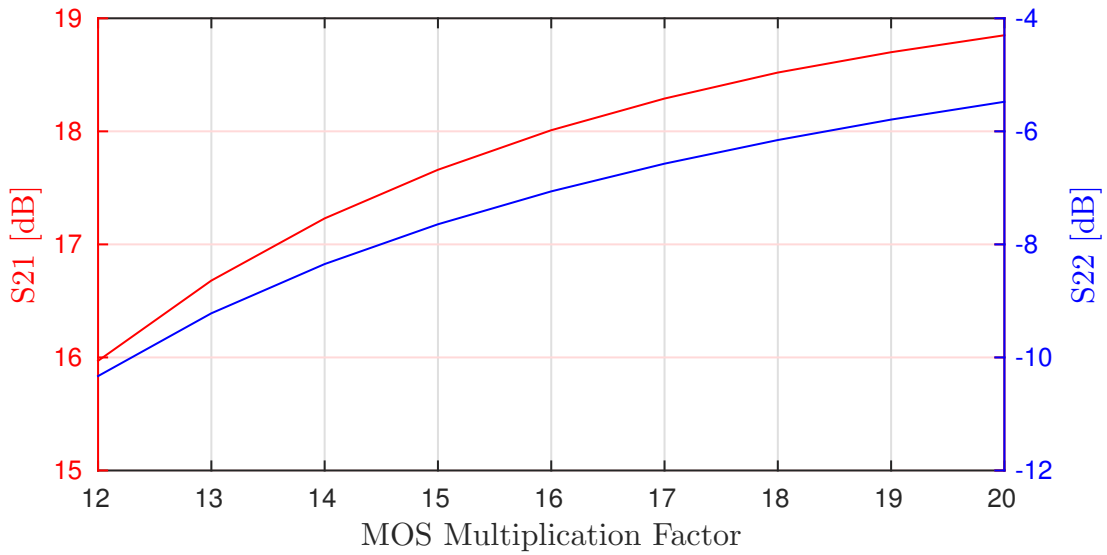


Figure 4.20.: Power amplifier: Power gain vs S22 tradeoff

From the plot it can be concluded that,

- To push the gain of the power amplifier beyond 16 dB, the S_{22} will have to be sacrificed
  - For example, for 19 dB gain the S_{22} drops to just -4.4 dB

- The resetting of the design specification for S_{22} from -14 dB to -10 dB, as done in section 3.4.3 makes absolute sense

Last but not the least, in Fig.4.21 the maximum deliverable output power versus the effective MOS width has been analysed. On the y-axis the the output power in dBm has been plotted and on the x-axis like in the previous case the MOS multiplication factor has been swept from 12 to 20 in steps of 1 each.

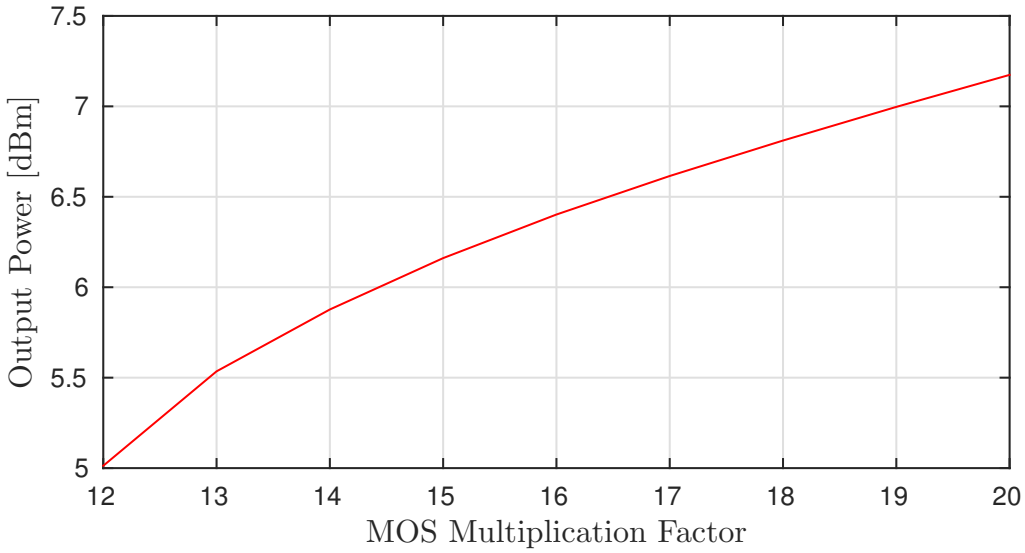


Figure 4.21.: Power amplifier: Output power vs S22 tradeoff

The major takeaway from this plot is that in case the output power needs to be pushed up, the output matching will have to be lost out on. The power amplifier can for example, deliver upto 7.25 dBm of output power but this would mean the S_{22} dropping to under -4.5 dB. These two analyses show that the output stage is not optimal in terms of gain and output power, but still the primary goal of 5 dBm output power and a decent enough gain of 16 dB has been reached. This stage is also inductorless, which is a major boost to the integration potential of the designed power amplifier. As suggested in the beginning no more than one inductor could be used for the design process, this output stage hence, gives an excellent compromise between the chip area saving and the overall power amplifier performance.

4.5.2 Noise Figure vs Gain Tradeoff

In section 3.5.3, noise matching to bring down the noise figure (NF) for the designed common gate power amplifier was done. The matching resulted in reducing the noise figure by roughly 0.85 dB to 5.14 dB. This improvement apart from the 5 dB higher power gain resulted in the decision to layout the common gate power amplifier. The matching process however, brought to light another very interesting tradeoff involved in the design of any power amplifier. This is the noise figure vs gain tradeoff. In Fig.4.22, the tradeoff for the designed power amplifier has been reshown.

Like mentioned previously, to attain a lower noise figure the gain would have to be compromised and vice versa. For a gain of 17 dB (1 dB higher than the redesigned specification) a noise figure of 7 dB (for the schematic design) would have to be accepted. This tradeoff for CMOS technology is much more stringent than for technologies like III–V or silicon bipolar. This is because the conduction channel incase of a MOS device is very near to the surface and the surface defects make the impact of noise much more dominant on a MOS transistor than on a Bipolar transistor. Apart from the structural reasons, the number of inductors being limited to one has resulted in increased noise contribution from the resistances. These discussed factors resulted in increasing the NFmin at the bias point of choice for the design. Once, the NFmin increases the room to reduce the NF to a certain value without losing out on the gain shrinks. This is also the primary reason that the NF threshold of 6 dB was breached.

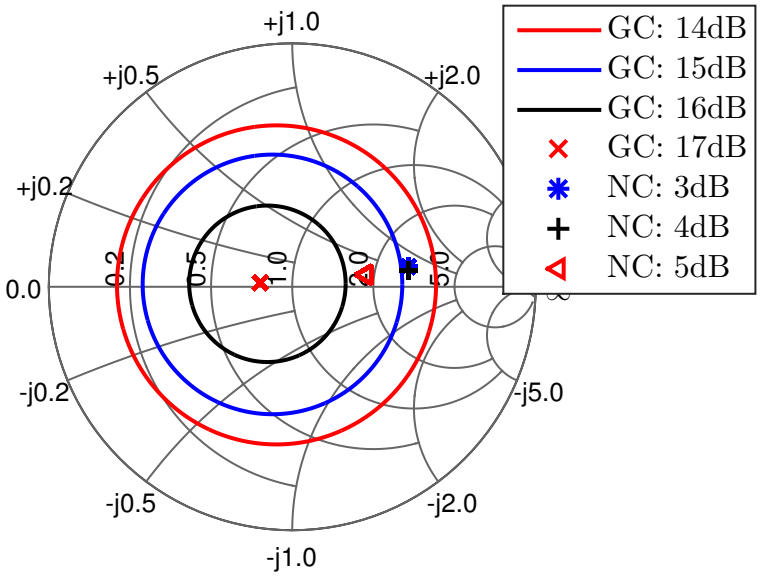


Figure 4.22.: Power Amplifier: Noise Figure vs Gain tradeoff

4.6 State of the Art Comparison

In Table 4.8, a comparison of the designed CMOS common gate power amplifier with an offchip inductor has been made with the state of the art power amplifiers.

Ref.	Freq (GHz)	Technology	Gain (dB)	S_{11} (dB)	S_{22} (dB)	OP1 (dBm)	Power (mW)
[10]	2.4-5.2	0.18μm,CMOS	18	NA	NA	14	NA
[30]	0.7-6.0	0.13μm, RF-CMOS	22	-10	-10	6	NA
[1]	0.5-8.5	0.6μm,CMOS	6.1	-10	-10	5	103.8
[20]	0.6-22	0.18μm,CMOS	7.3	-8	-9	4	52
[4]	0.5-5.5	0.6μm,CMOS	6.5	-9	-10	15.3	83.4
[15]	3.1-10.6	0.13μm,CMOS	17	-10	-10	3.5	NA
[21]	3.1-12.6	0.18μm, RF-CMOS	10.46	-10	-10	5.6	NA
[5]	3.0-5.0	0.18μm,CMOS	13.3	-7.5	-7	1.81	25.2
[22]	3.0-5.0	0.18μm,CMOS	15.5	-12.9	-13.3	9.13	25.46
[31]	3.0-5.0	0.18μm,CMOS	17.5	-10	-10	2.57	30
[32]	3.0-5.0	0.18μm,CMOS	15.2	-5	-6	11.2	25
[17]	3.1-4.8	0.18μm,CMOS	19	-10	-8	-4.2	25
[16]	57-65	0.25μm,SiGe BiCMOS	8.8	-6	-5	11.5	51.8
[19]	0-15	0.5μm,SiGe BiCMOS	12	-8	-8	4.4	23.76
[3]	3.0-5.5	0.8μm,SiGe BiCMOS	8.5	-6	-6	16.2	325
[8]	26-40	0.13μm,SiGe BiCMOS	13	-15	-15	19.4	525
[9]	79-97	0.13μm,SiGe BiCMOS	14.5	-10	-10	19.6	561
[28]	0.1-14	0.35μm, SiGe BiCMOS	9.8	-8	-8	22.8	NA
This Work	0.7-2.3	0.13μm,CMOS	15.9	$<$ -18	$<$ -10	5.012	134.7

Table 4.8.: Comparative Analysis: State of the Art vs This Work

5 Conclusion and Outlook

Chapter Overview: *This chapter talks about the major takeaways from the thesis work. Also, a small account of things that can follow this thesis has been given.*

5.1 Conclusion

In this thesis work two wideband CMOS power amplifiers using only one inductor have been designed and implemented. The CMOS technology was chosen due to it's huge on-chip integration potential. The major results from this work can be concluded a follows,

- The first implementation, a shunt feedback power amplifier (SFPA) was found to deliver 5 dBm output power with a power gain of 11 dB and with good input and output matching over the entire frequency range of 700 MHz to 2.3 GHz. It was implemented only on the schematic level as the obtained power gain was found to be too low.
- The second implementation, a common gate power amplifier (CGPA) was designed and was again found to deliver 5 dBm output power but with 16 dB power gain. The achieved S_{11} and S_{22} across the 700 MHz to 2.3 GHz band were better than -10 dB each.
- Due to it's higher power gain, the CGPA was layouted. The layouted amplifier was found to consume 210 x 165 μm^2 chip area. Also, in the post layout case it's perfomance was analysed using an onchip and an offchip inductor.
- With the offchip inductor the power amplifier was found to still deliver 5 dBm output power with 15.9 dB power gain.
- The power gain and output power however, dropped to 15.09 dB and 4 dBm respectively, in the onchip inductor case.

The designed CGPA with off-chip indutor hence, met the principle design targets of 5 dBm output power and one indutor design. It's power gain however, fell short by 2 dB as compared to the target specification. The achieved 15.9 dB power gain is still nevertheless, a really good value for a wideband CMOS power amplifier using just one inductor.

5.2 Outlook

There is always room to optimize and extend results produced as a part of any research work. This section identifies two major areas in this regard, which could not be worked upon due to lack of time. These two areas are as follows,

- Studying the impact of parasitics introduced from the packaging interface of the off-chip inductor: As pointed out in [11], parasitics from packaging interface (such as bonding wires, I/0 pads) have the potential to degrade performance. The paper also suggests that packaging technologies present larger process variations than IC technologies. It hence, makes complete sense in first modeling these

packages as s-parameter files through full field EM simulations and then studying their impact on the performance of the designed power amplifier.

- Measuring the performance of the fabricated power amplifier: It is a known fact that the performance of any fabricated circuit block shows deviations. It would hence, be prudent to get the designed power amplifier taped out and then to evaluate it's performance.

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