Literature Survey

FPGA Logic Block Verification using HDL and Schematic-Level Simulation

1. Introduction

Field Programmable Gate Arrays (FPGAs) are widely used in modern digital systems due to their flexibility and reconfigurability. As FPGA designs become more complex, verification before hardware implementation becomes critical. Verification ensures that the logic design functions correctly and meets timing requirements.

2. Evolution of FPGA Verification Techniques

Early FPGA verification relied mainly on functional simulation using HDL. Modern verification combines behavioral simulation, gate-level simulation, formal verification, and hardware-in-the-loop testing to improve reliability.

3. HDL-Based Functional Verification

Hardware Description Languages such as Verilog and VHDL are used to model digital circuits. Functional simulation verifies logical correctness using testbenches, assertions, and coverage analysis. This stage detects errors early in the design cycle.

4. Schematic-Level (Gate-Level) Verification

After synthesis, HDL code is converted into a gate-level netlist. Gate-level simulation verifies logical equivalence, propagation delay, setup and hold time, and timing constraints. It ensures the synthesized hardware matches the HDL design.

5. Verification Tools

Common tools include ModelSim, Xilinx Vivado, and Quartus Prime. These tools provide waveform analysis, debugging features, and timing reports to support complete FPGA verification workflows.

6. Formal Verification

Formal verification mathematically proves correctness by checking all possible input conditions. Techniques include property checking and equivalence checking. It is especially important in safety-critical systems.

7. Challenges in FPGA Verification

Verification challenges include state explosion, timing closure issues, synthesis mismatches, and large simulation resource requirements. Researchers address these issues using coverage-driven and constrained random verification techniques.

8. Applications

FPGA verification is applied in DSP systems, communication systems, processor design, embedded systems, and safety-critical applications such as aerospace and automotive control systems.

9. Conclusion

FPGA logic block verification requires a layered approach combining HDL simulation, schematic-level simulation, and formal verification. This ensures reliability, reduces debugging time, and improves overall system performance.