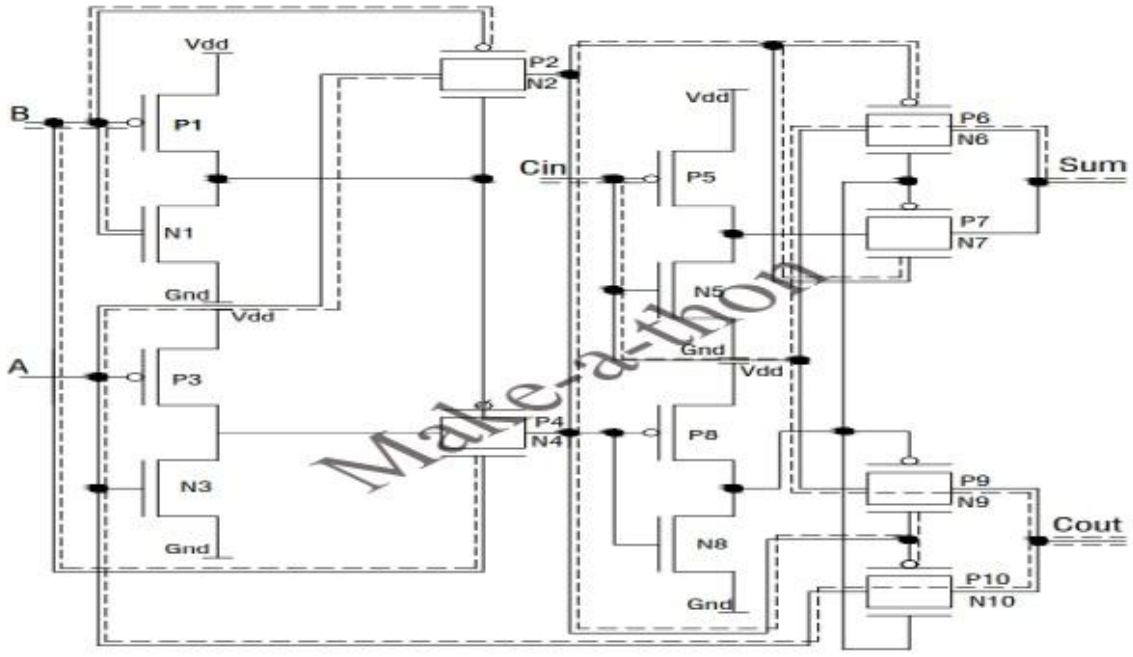
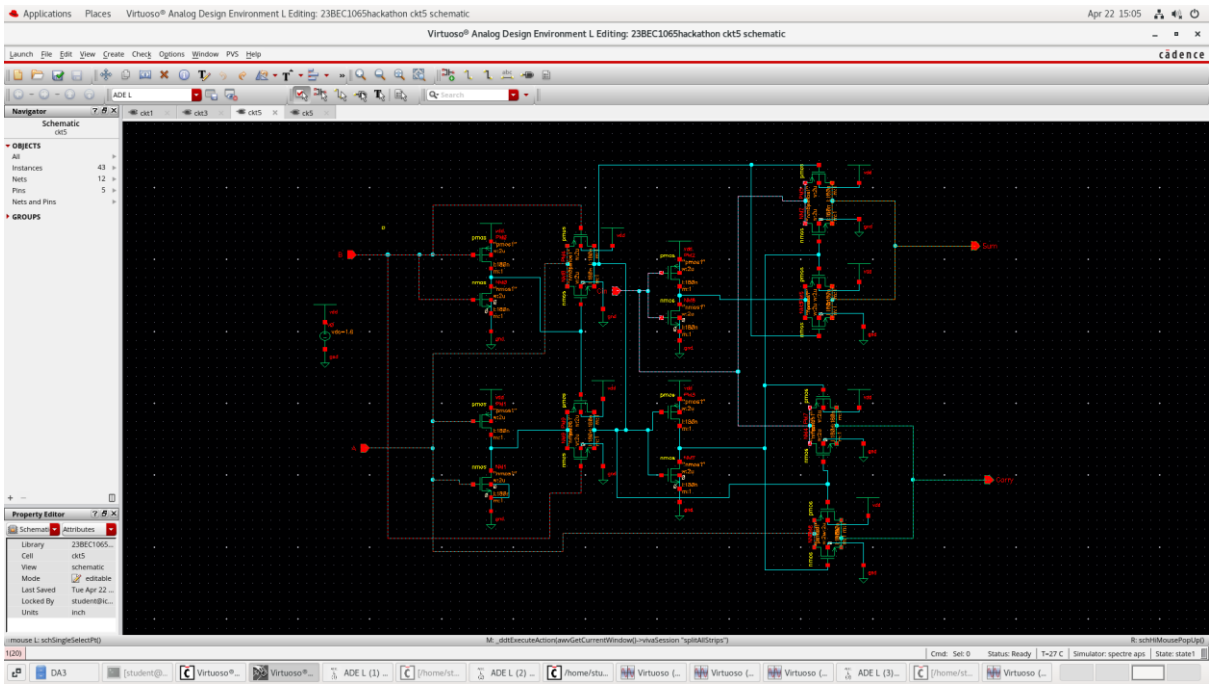
Adder 5

Circuit to be implemented

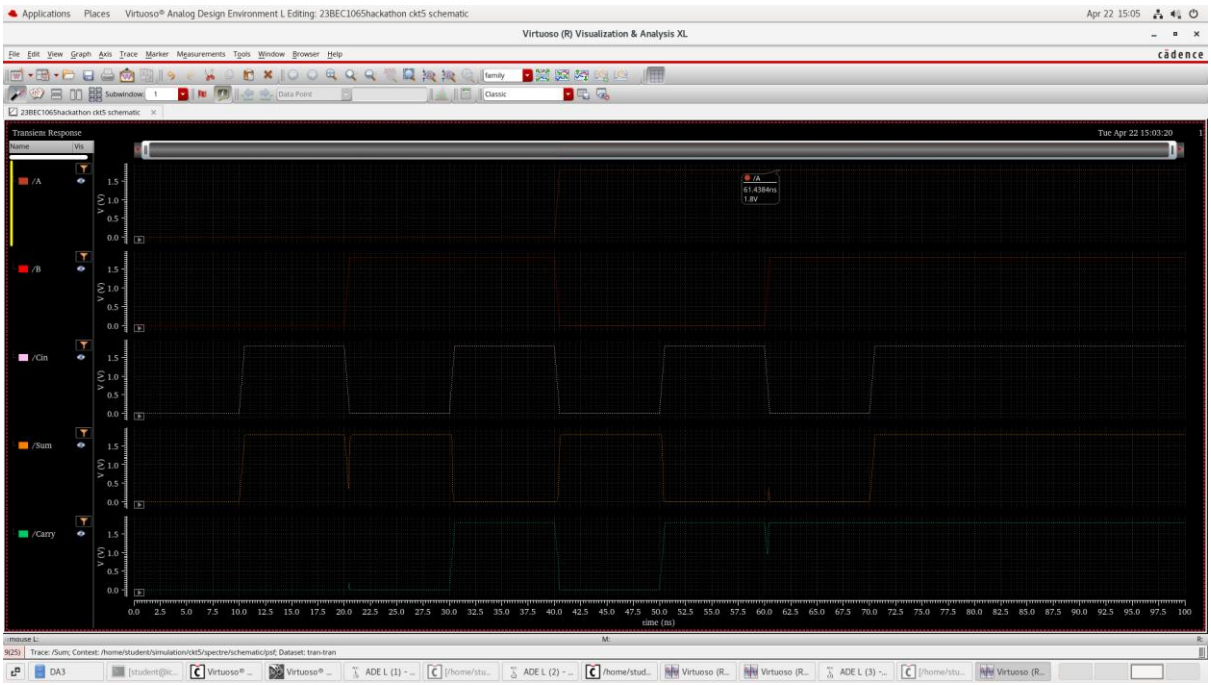


Implementation in cadence

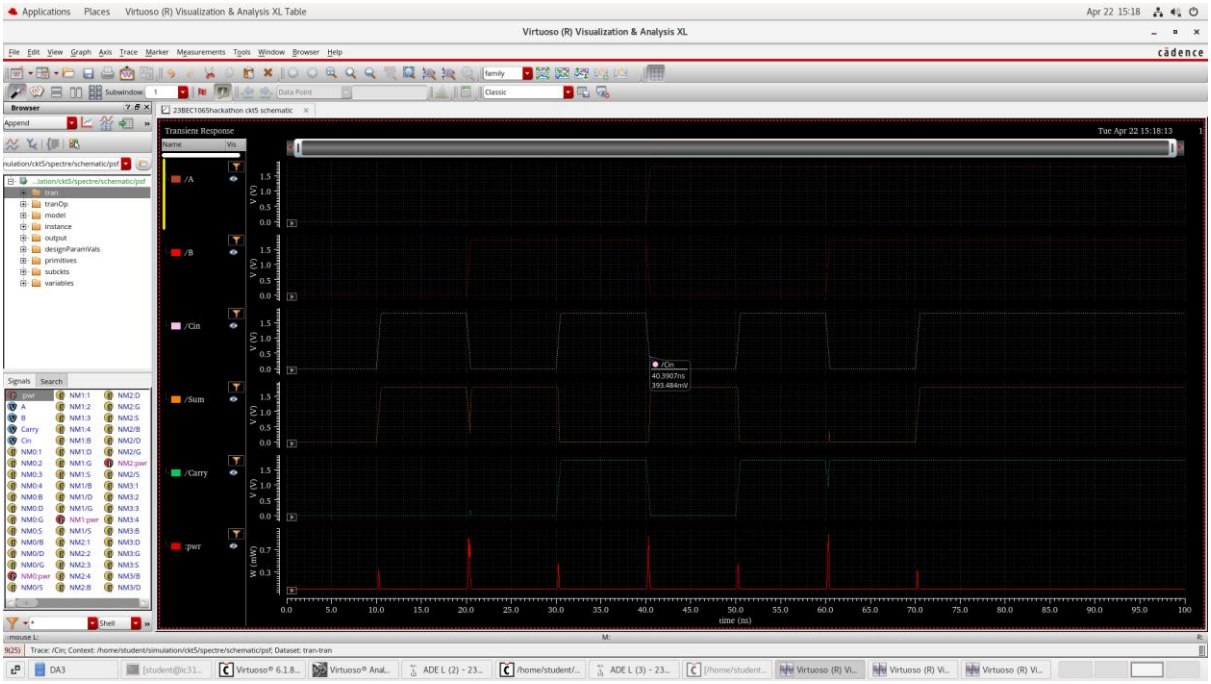
Before sizing



Timing diagram

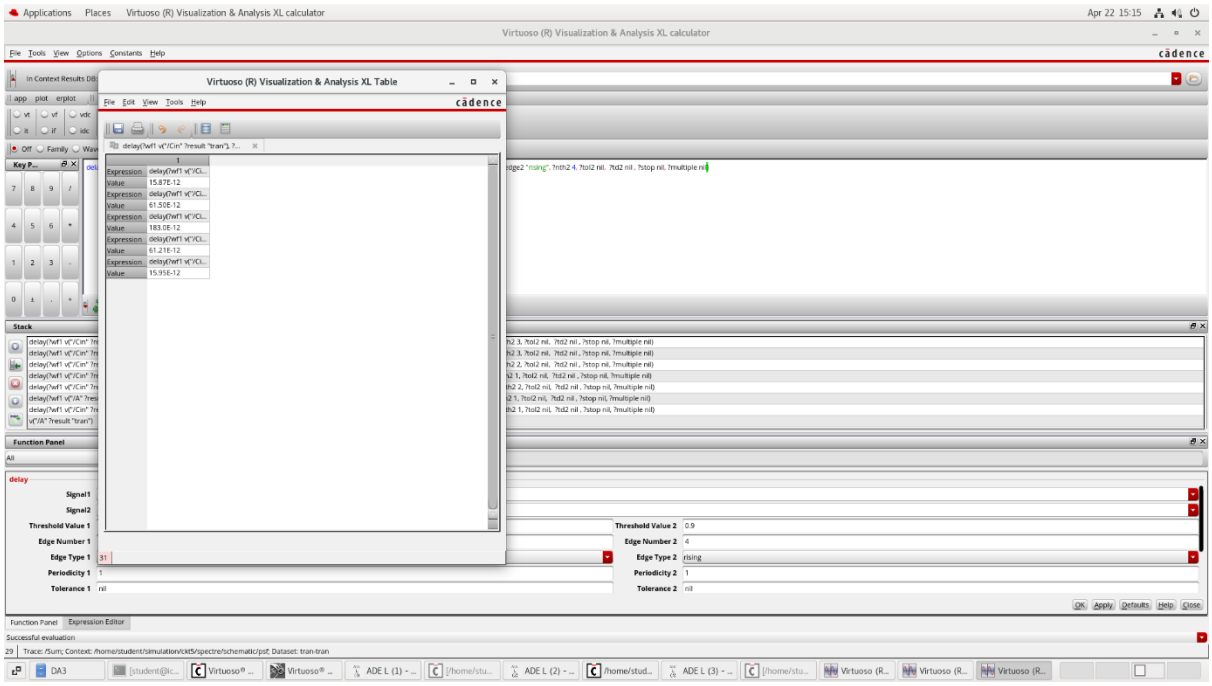


Power

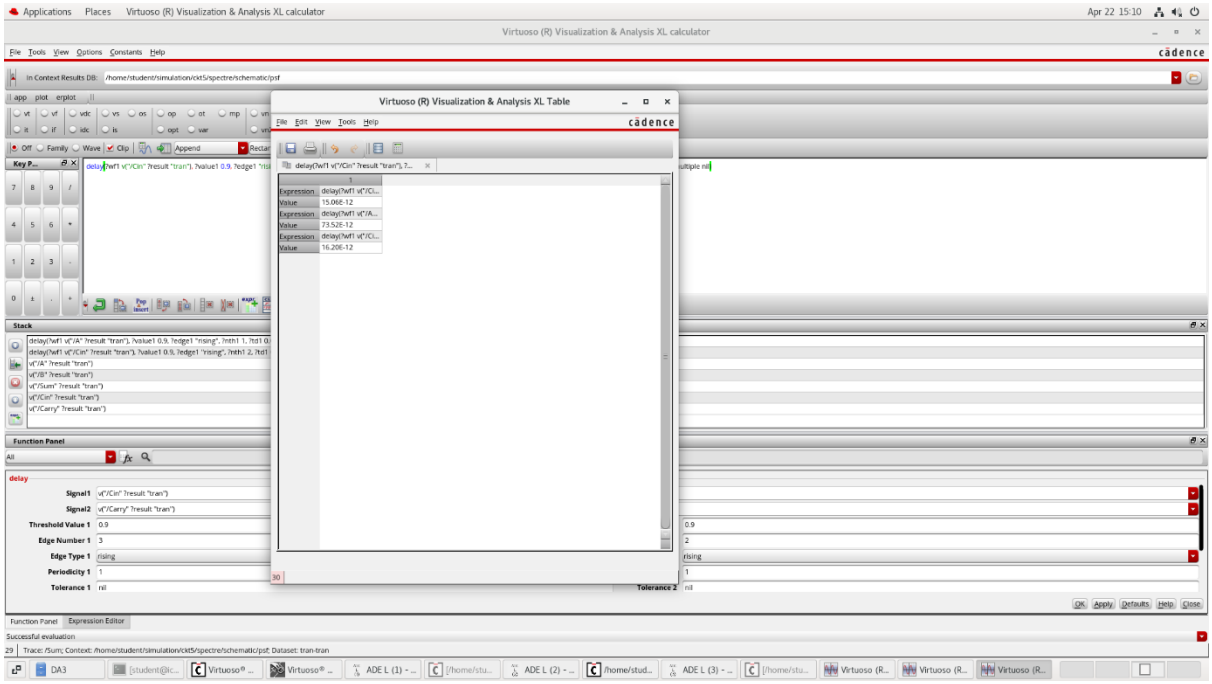


Delay value

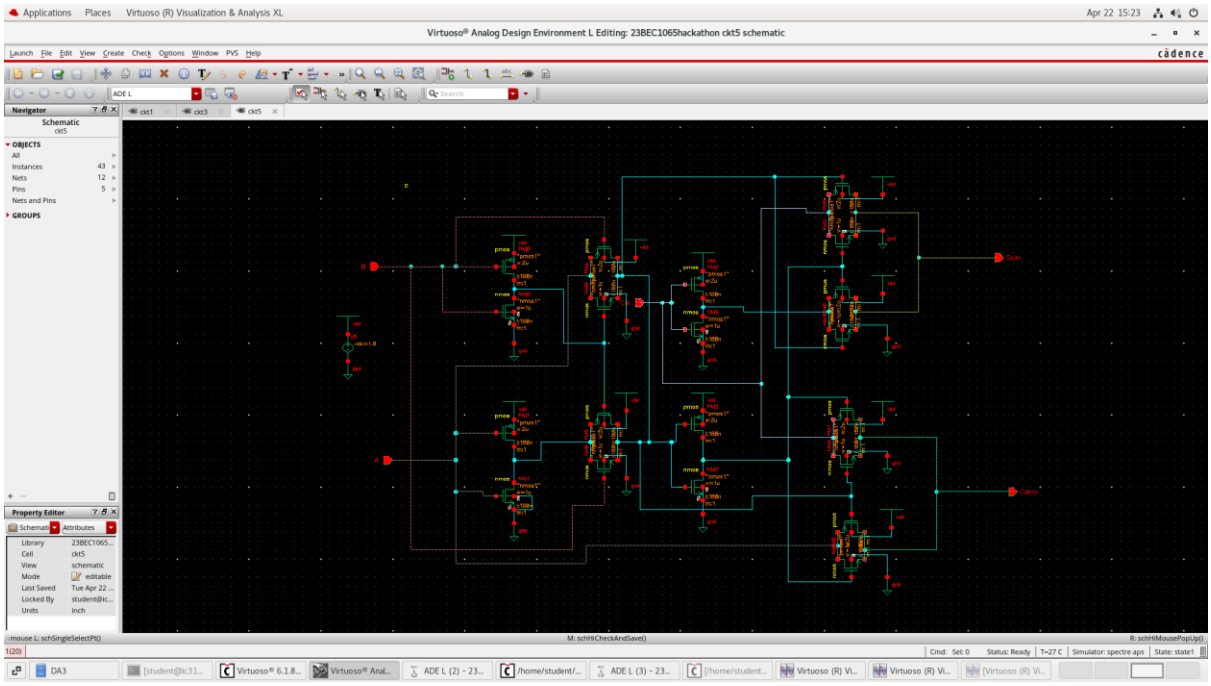
Sum



Carry

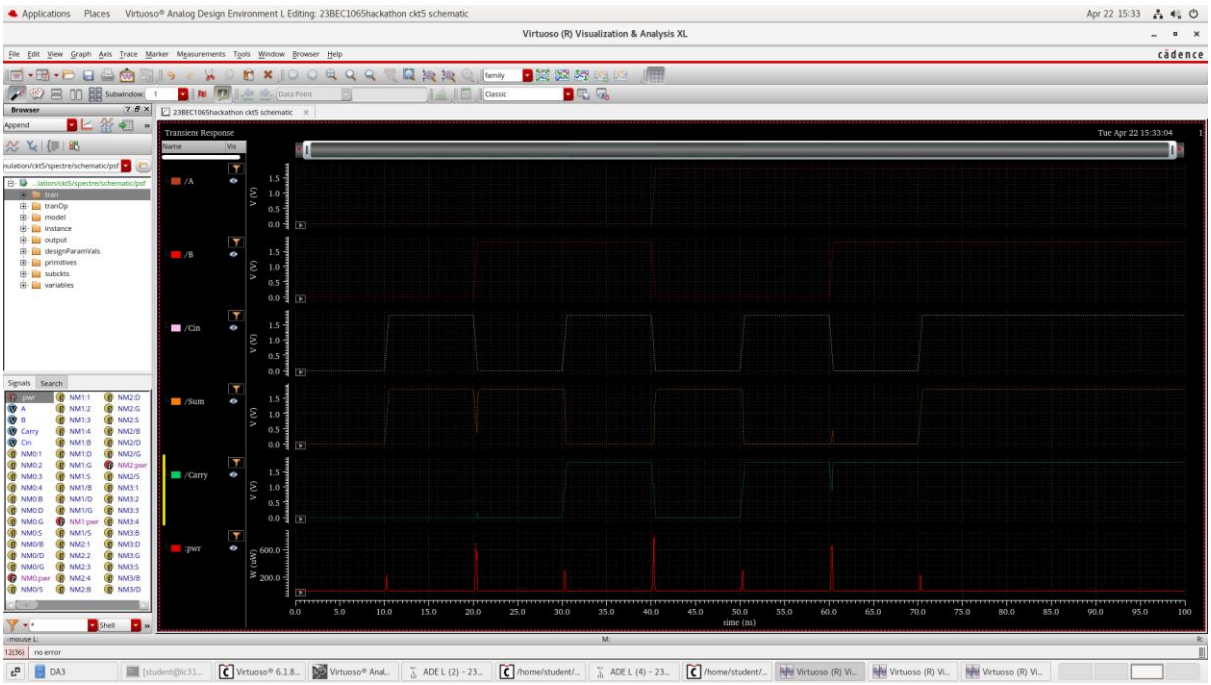


after sizing



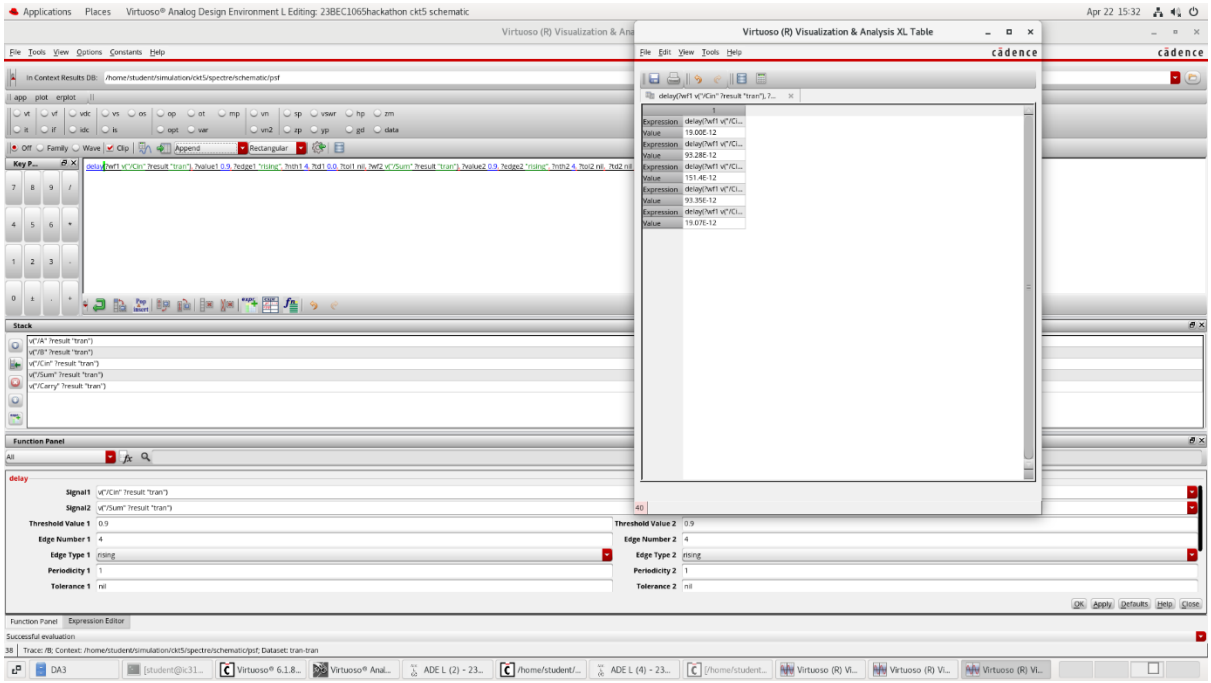
Timing diagram

Power

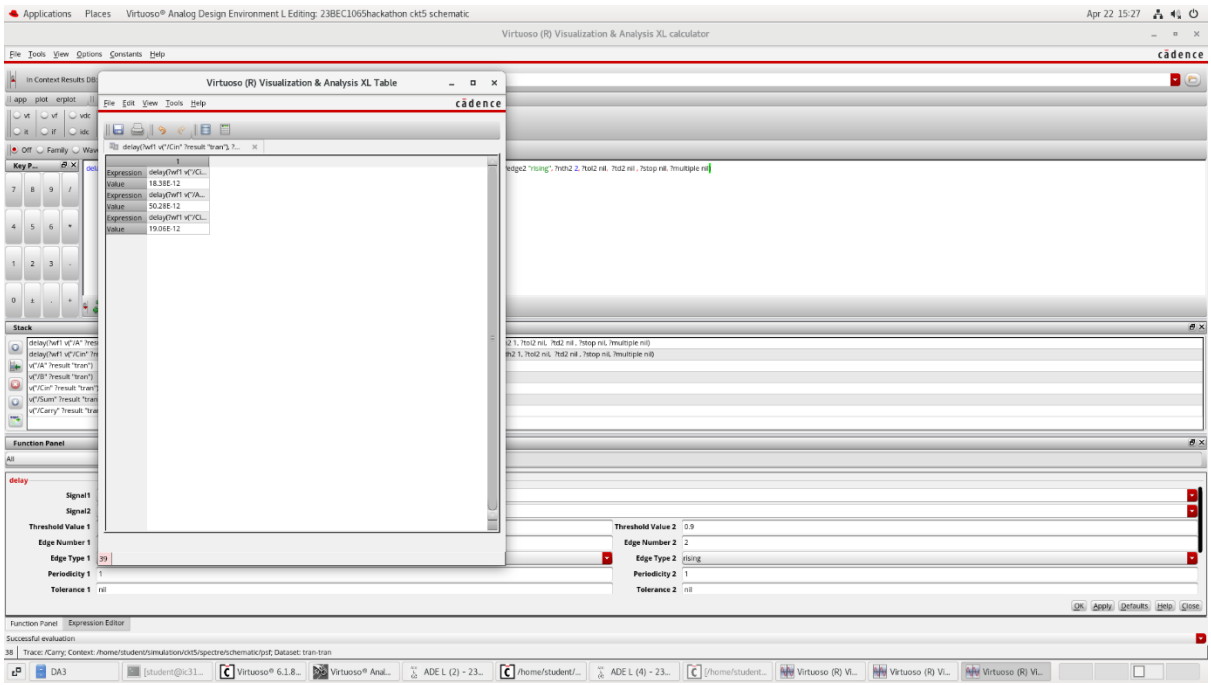


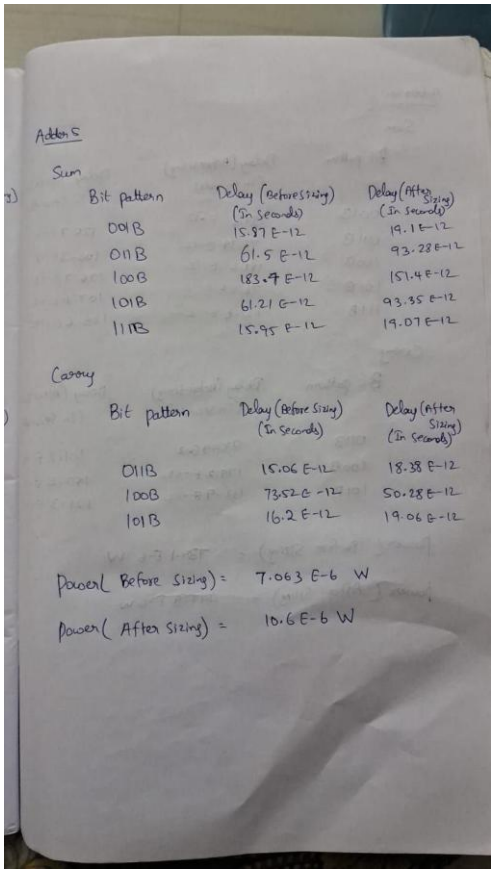
Delay value

Sum



Carry


Virtuoso (R) Visualization & Analysis XL Table
Virtuoso (R) Visualization & Analysis XL calculator
cadence


Adder
Sum
Bit pattern
Delay (Before sizing) (In Seconds)
Delay (After sizing) (In Seconds)
001B
15.87 E-12
19.1 E-12
011B
61.5 E-12
93.28 E-12
100B
183.7 E-12
151.4 E-12
101B
61.21 E-12
93.35 E-12
111B
15.95 E-12
19.07 E-12
Carry
Bit pattern
Delay (Before Sizing) (In Seconds)
Delay (After Sizing) (In Seconds)
011B
15.06 E-12
18.38 E-12
100B
73.52 E-12
50.28 E-12
101B
16.2 E-12
19.06 E-12
Power(Before Sizing) = 7.063 E-6 W
Power(After Sizing) = 10.6 E-6 W