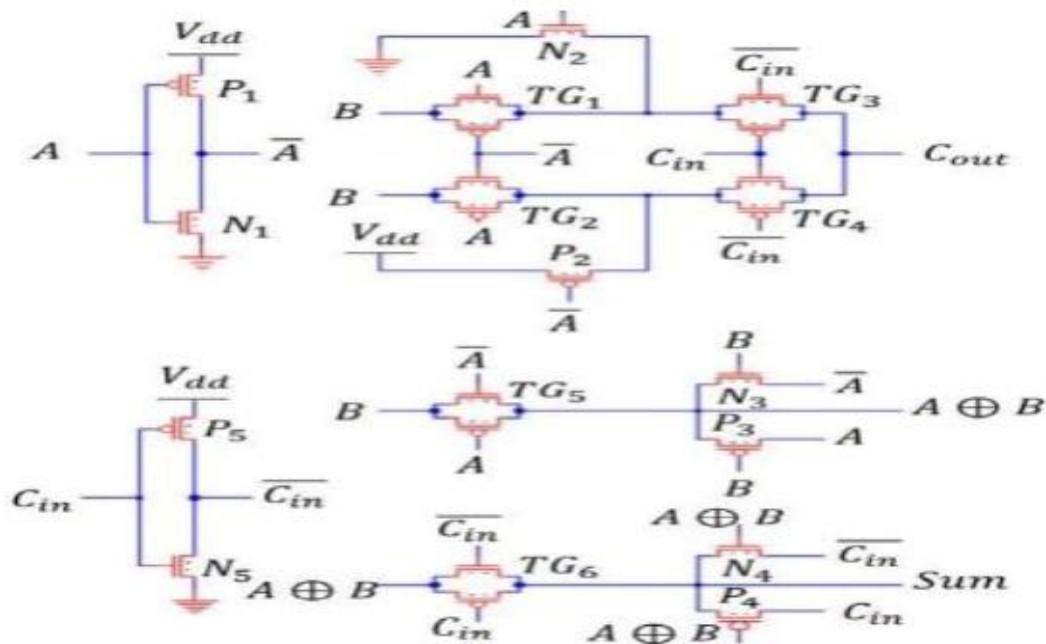


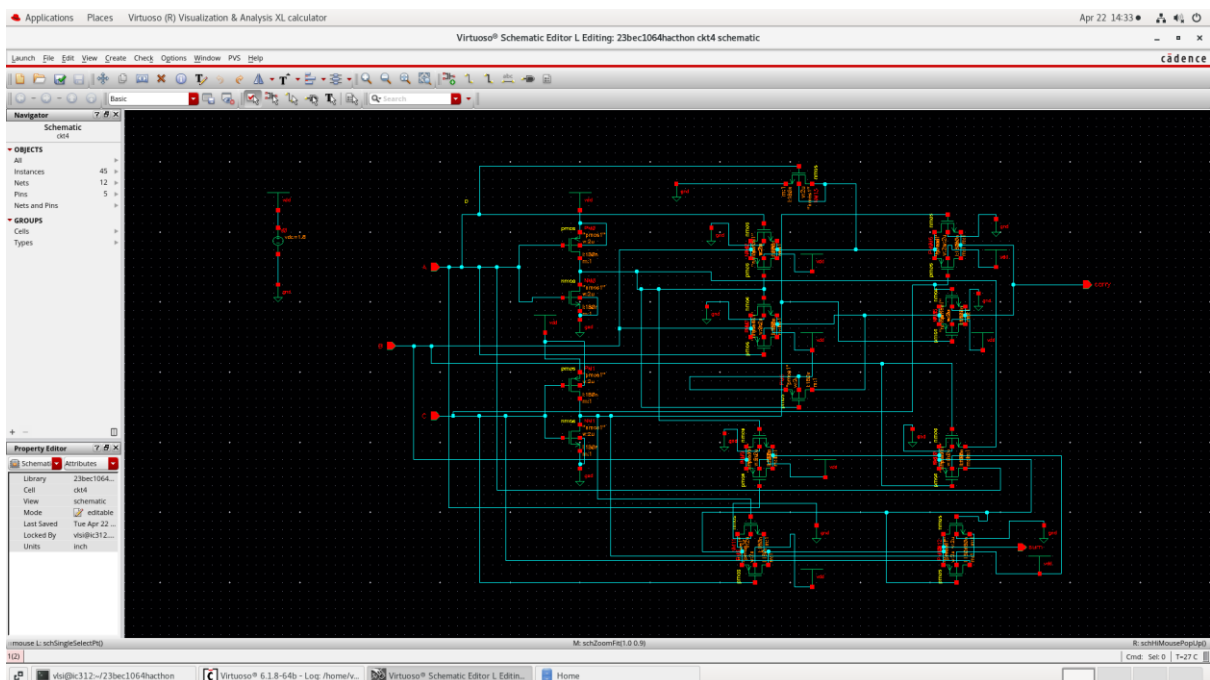
Adder 4

Circuit to be implemented



Implementation in cadence

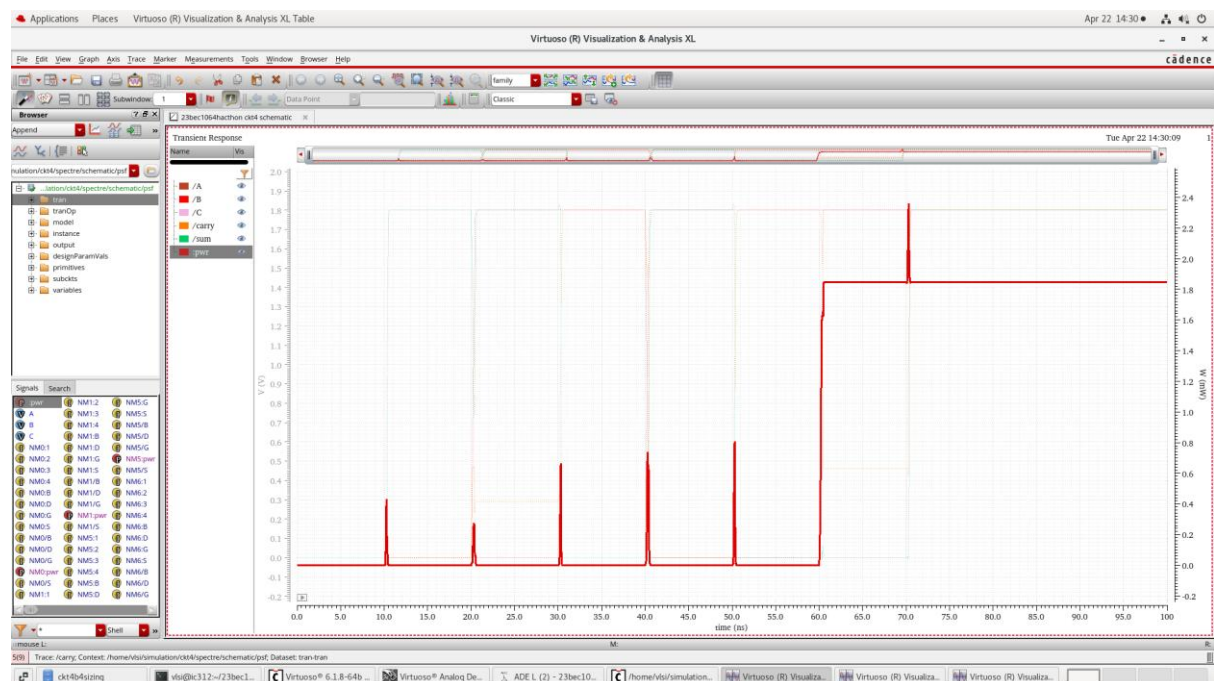
Before sizing



Timing diagram

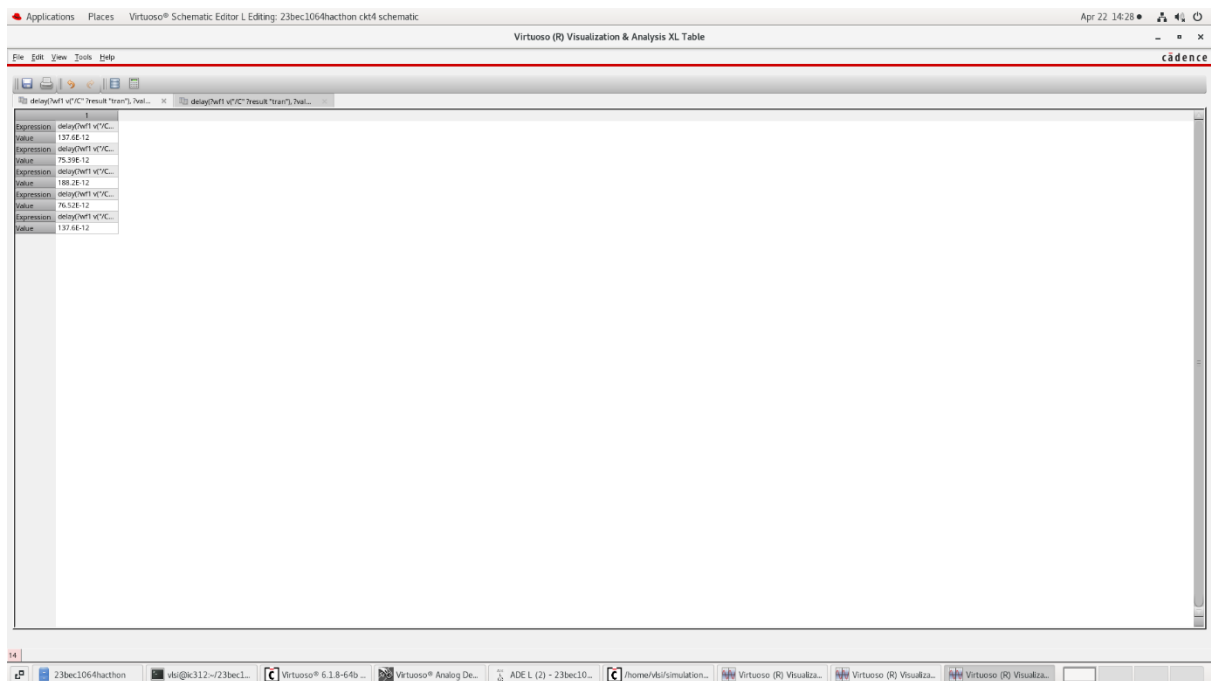


Power



Delay value

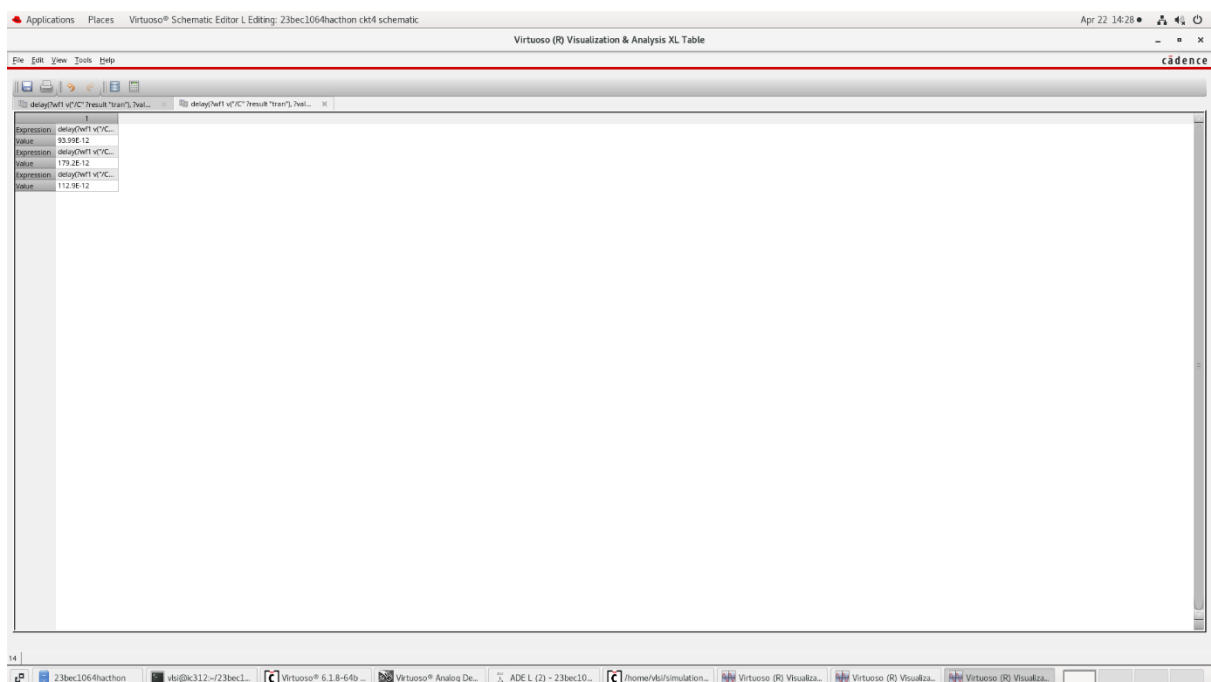
Sum



The screenshot shows the Cadence Virtuoso interface with a table titled "Virtuoso (R) Visualization & Analysis XL Table". The table contains the following data:

Expression	Value
delay(wt1 v1C) result train1, 7val...	137.44-12
delay(wt1 v1C) result train1, 7val...	75.318-12
delay(wt1 v1C) result train1, 7val...	110.28-12
delay(wt1 v1C) result train1, 7val...	76.128-12
delay(wt1 v1C) result train1, 7val...	137.44-12

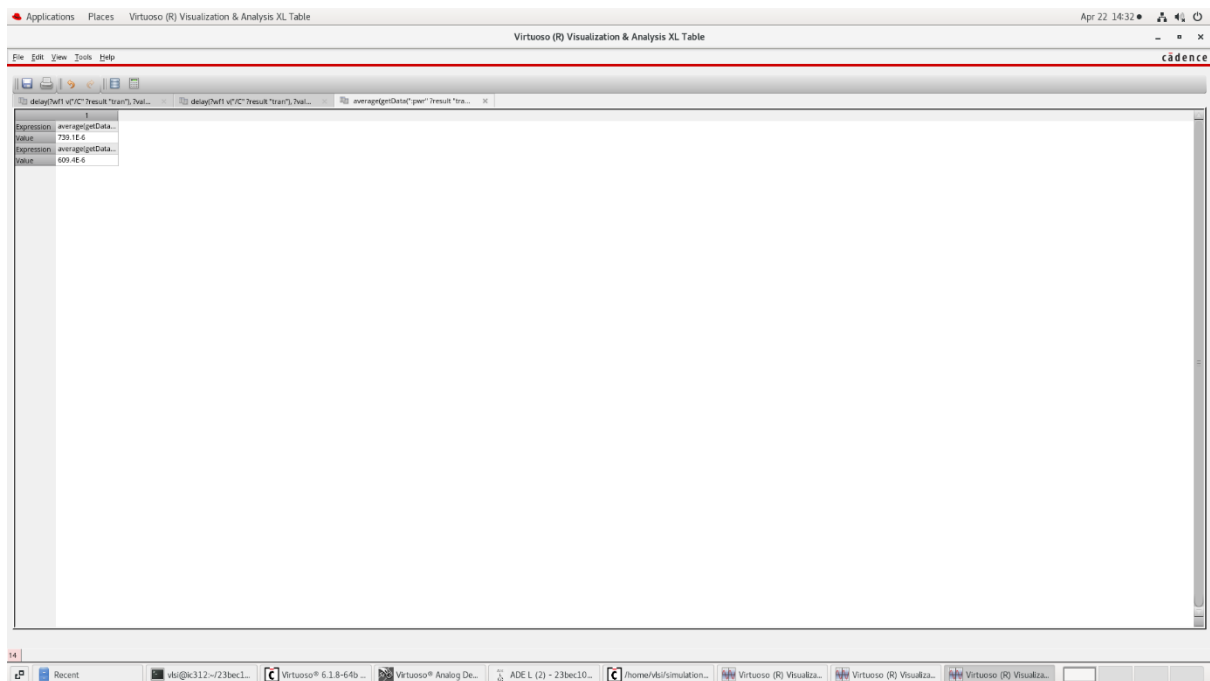
Carry



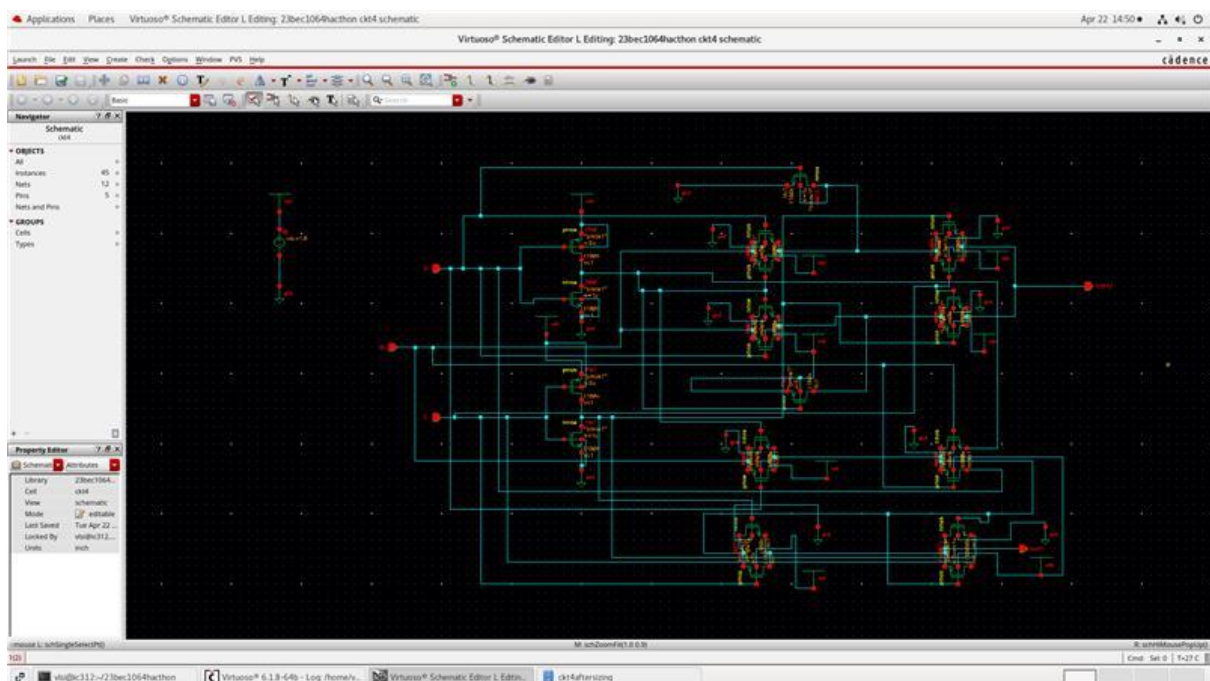
The screenshot shows the Cadence Virtuoso interface with a table titled "Virtuoso (R) Visualization & Analysis XL Table". The table contains the following data:

Expression	Value
delay(wt1 v1C) result train1, 7val...	95.318-12
delay(wt1 v1C) result train1, 7val...	179.28-12
delay(wt1 v1C) result train1, 7val...	112.98-12

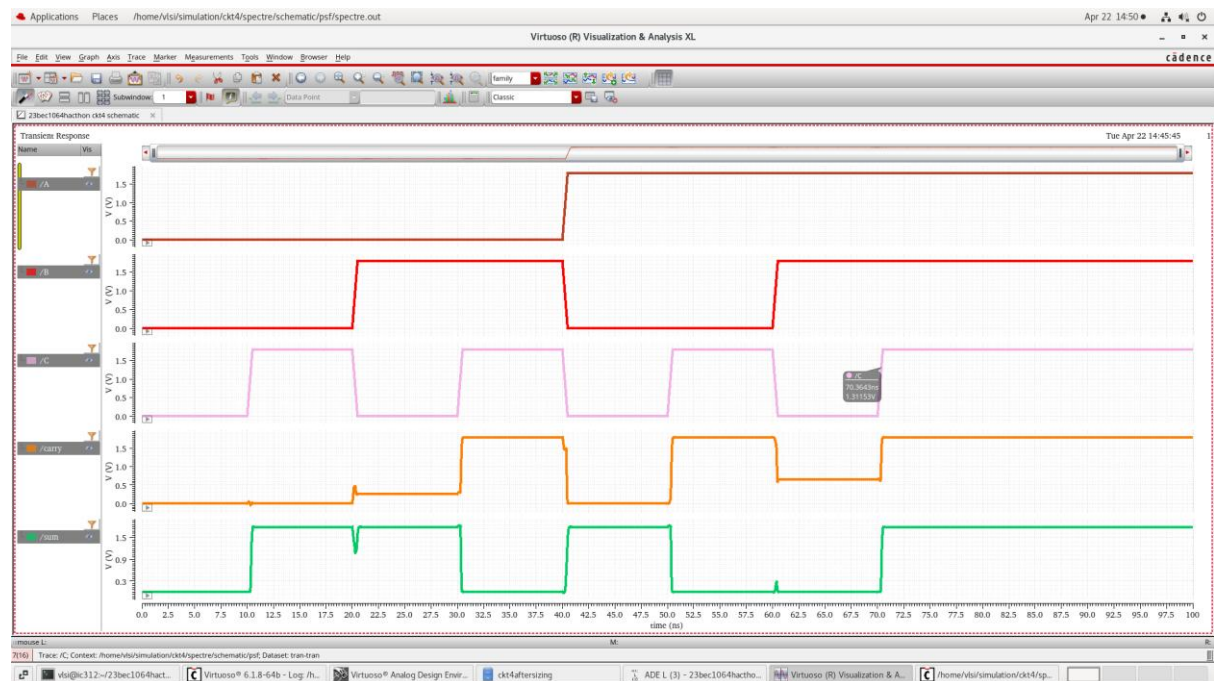
Power calculation



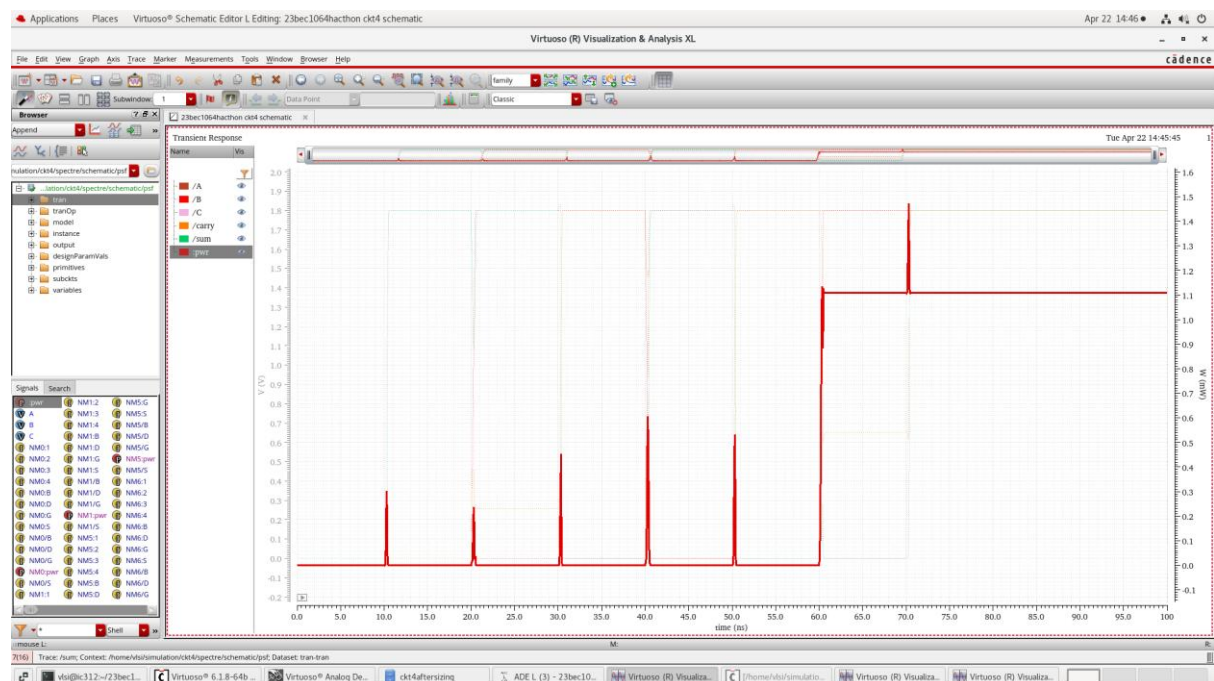
after sizing



Timing diagram

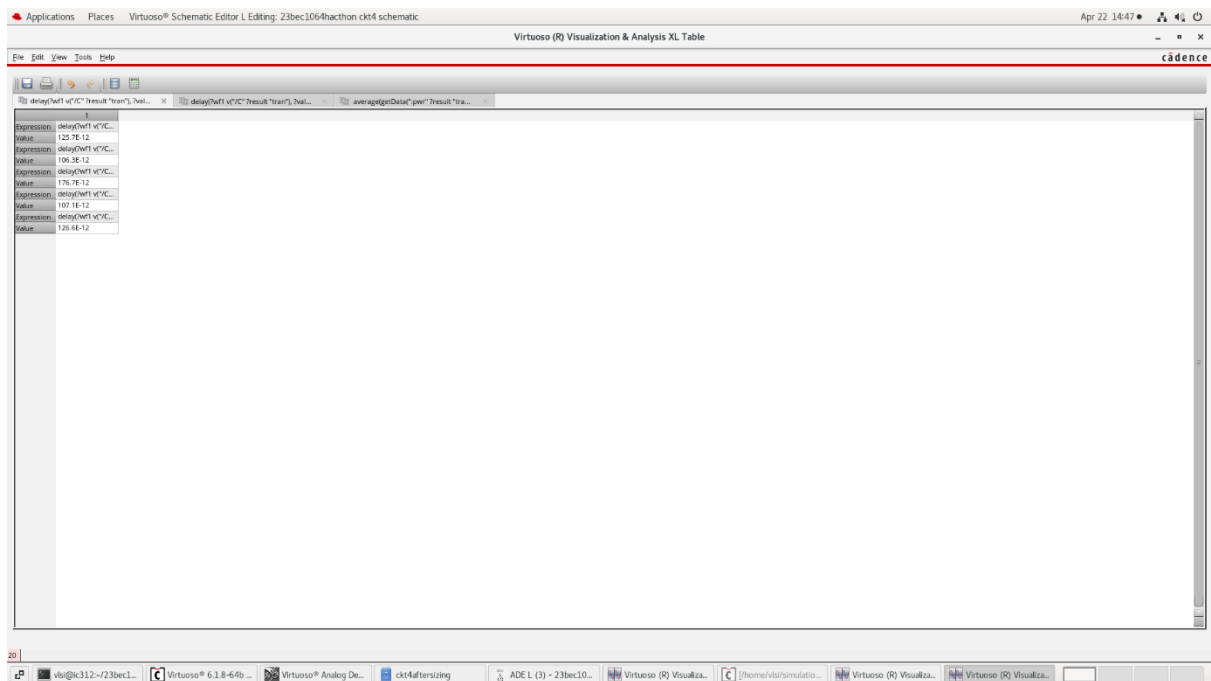


Power

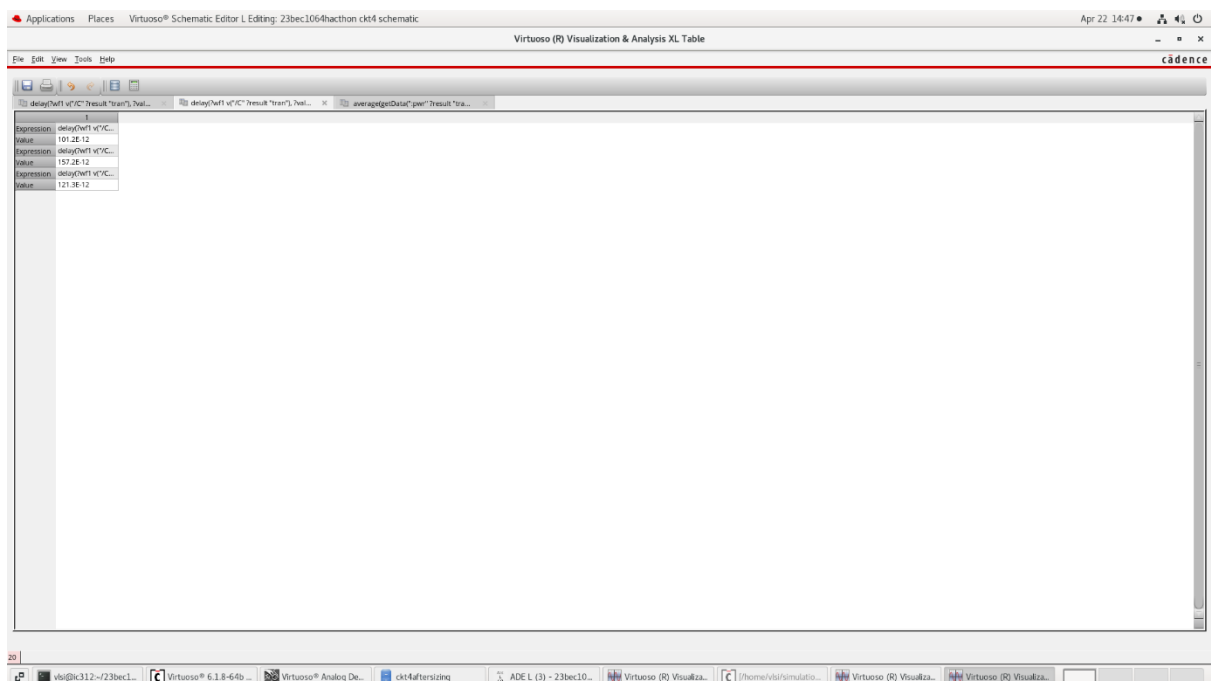


Delay value

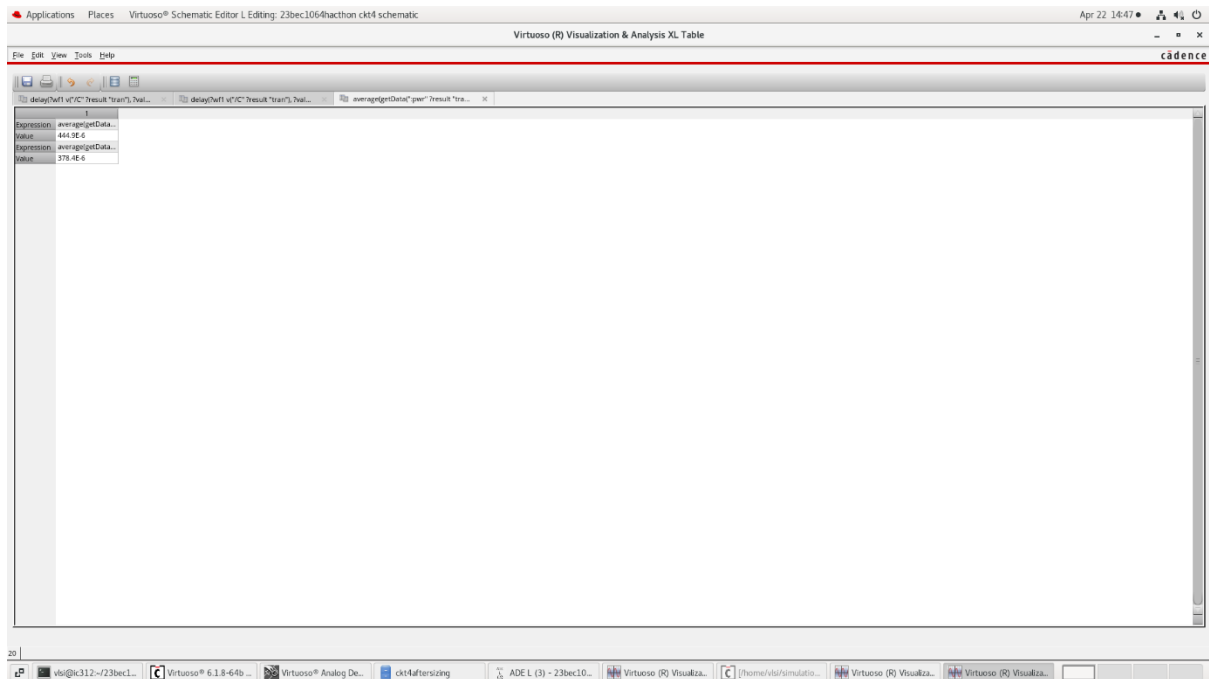
Sum



Carry



Power calculation



Appendix 4:

Sum

Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
001B	137.6 E-12	125.7 E-12
011B	75.39 E-12	106.3 E-12
100B	184.2 E-12	176.7 E-12
101B	76.52 E-12	107.1 E-12
111B	137.6 E-12	126.6 E-12

Carry

Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
011B	93.99 E-12	101.2 E-12
100B	179.2 E-12	157.2 E-12
101B	112.9 E-12	121.3 E-12

Power (Before Sizing) = 739.1 E-6 W

Power (After Sizing) = 444.9 E-6 W