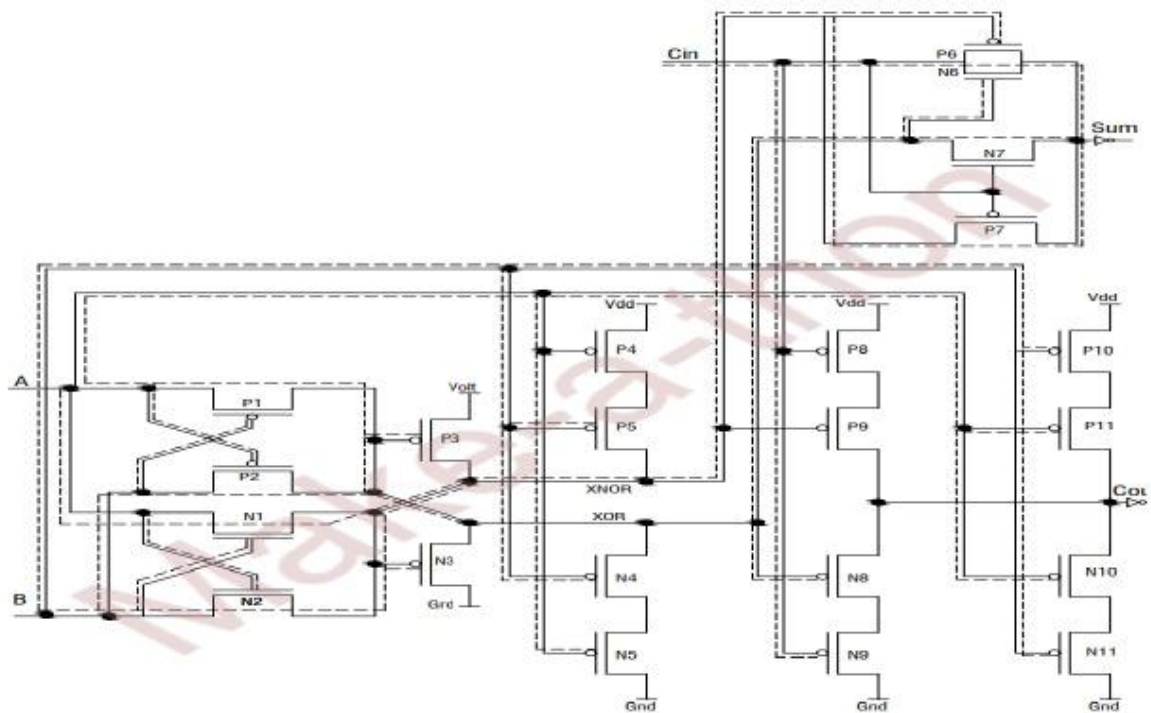


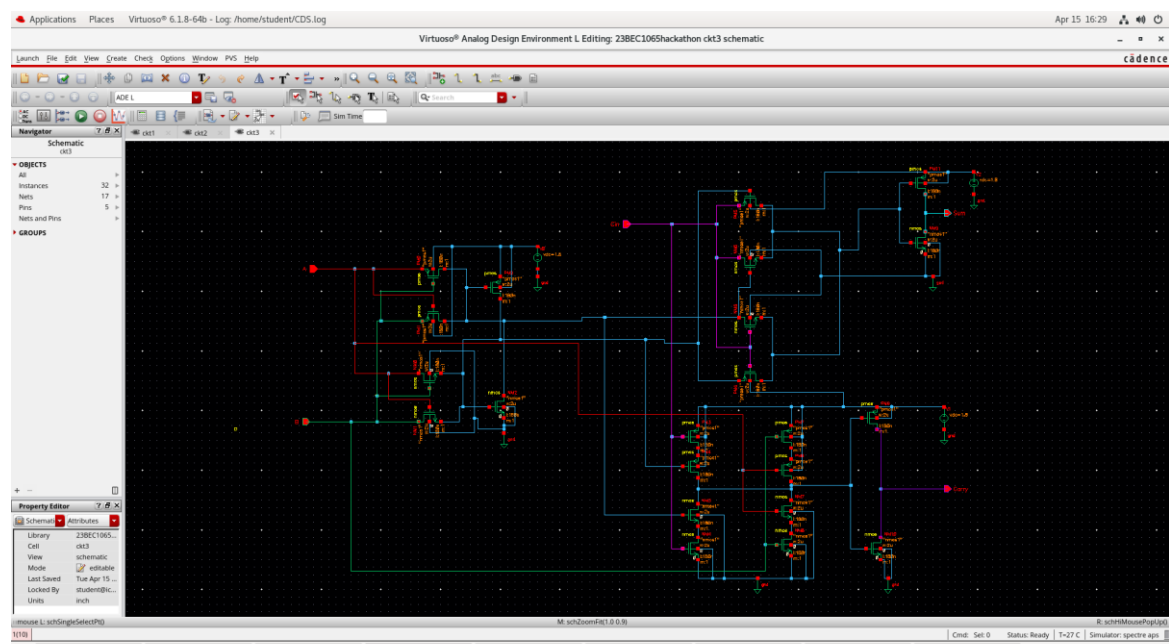
Adder 3

Circuit to be implemented

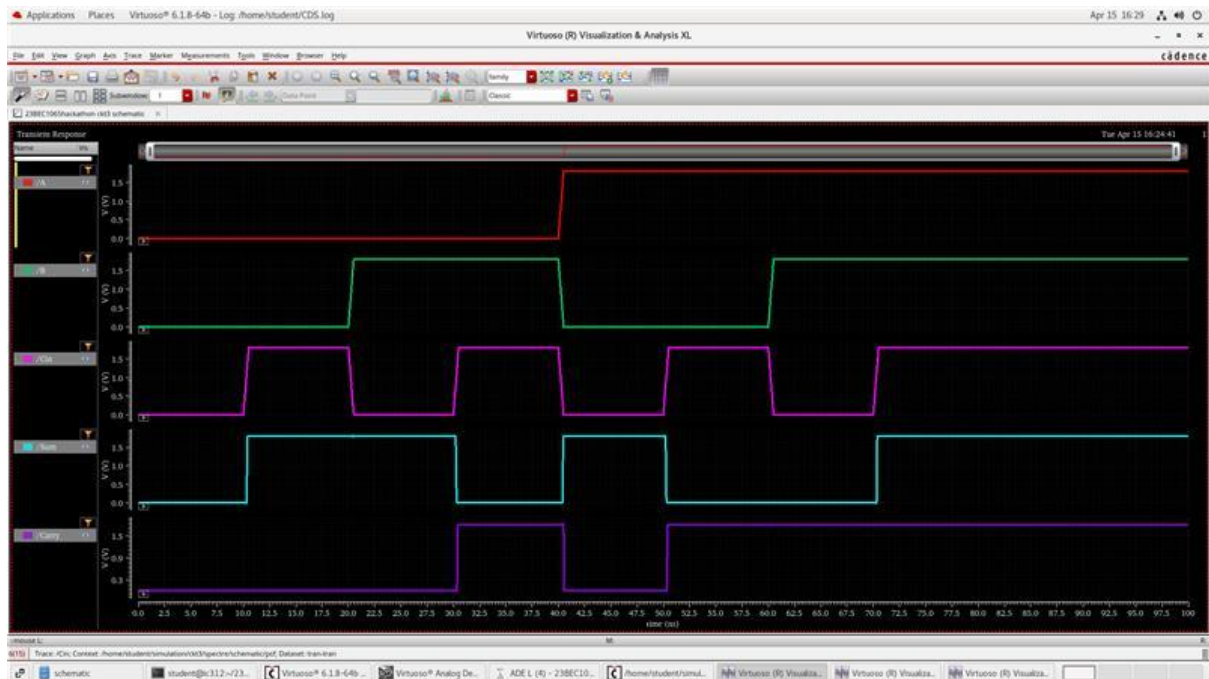


Implementation in cadence

Before sizing



Timing diagram

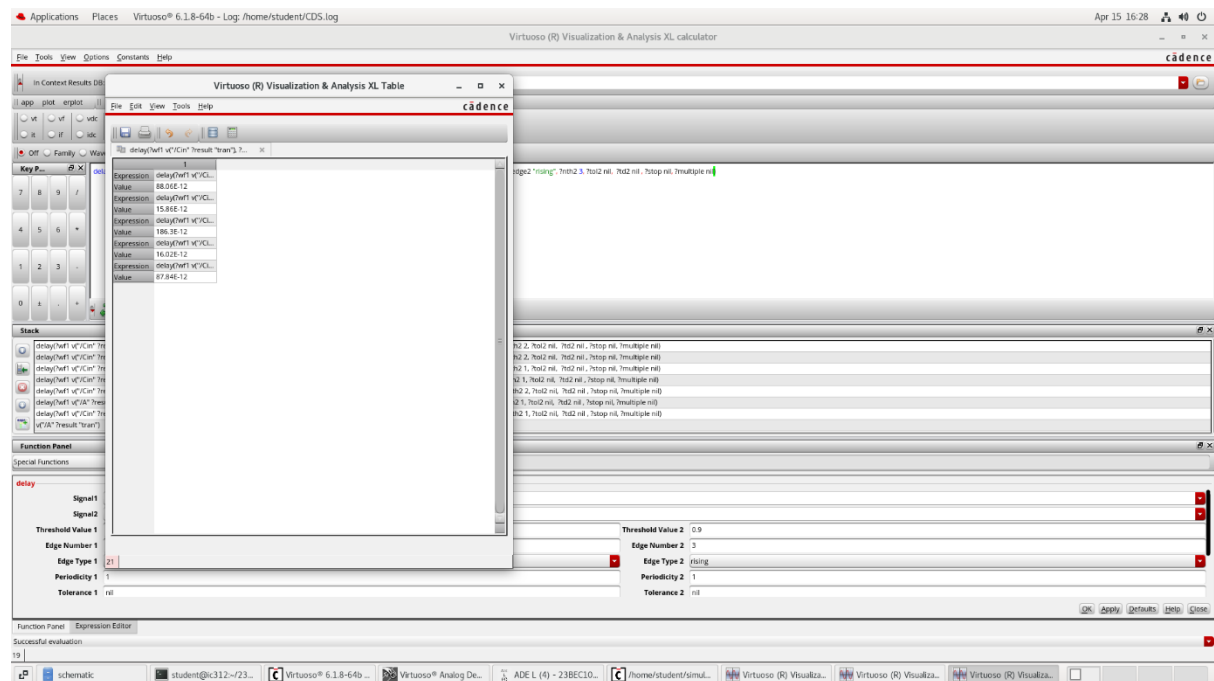


Power

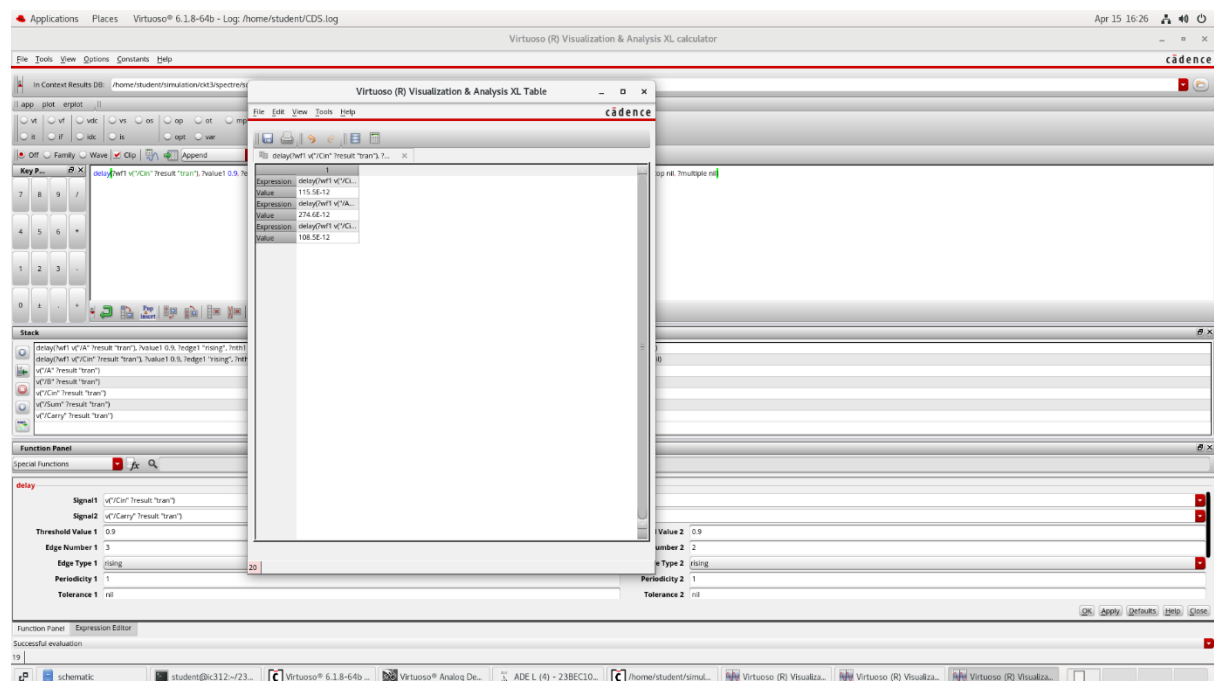


Delay value

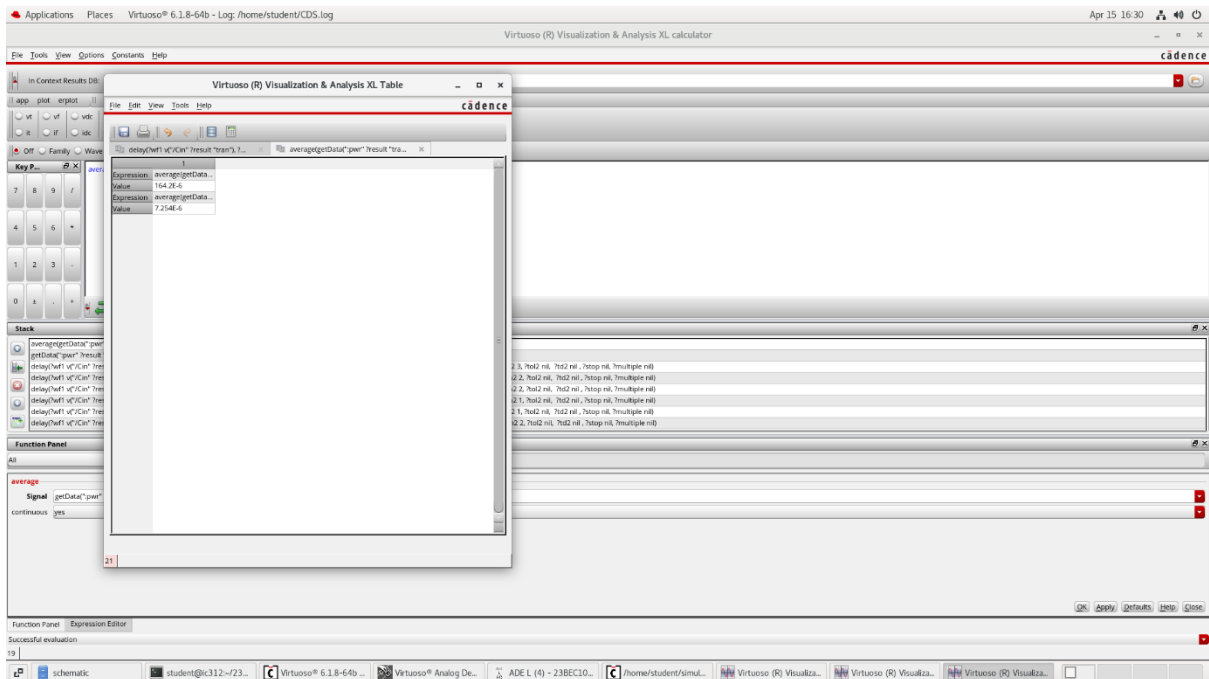
Sum



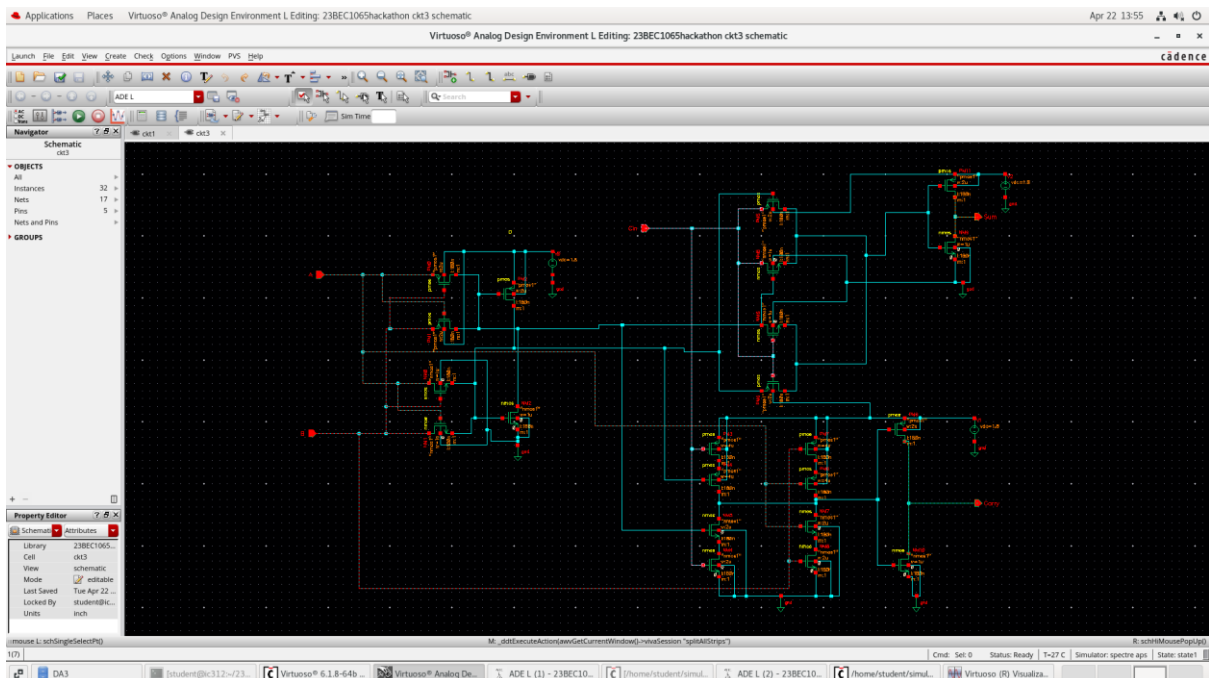
Carry



Power calculation



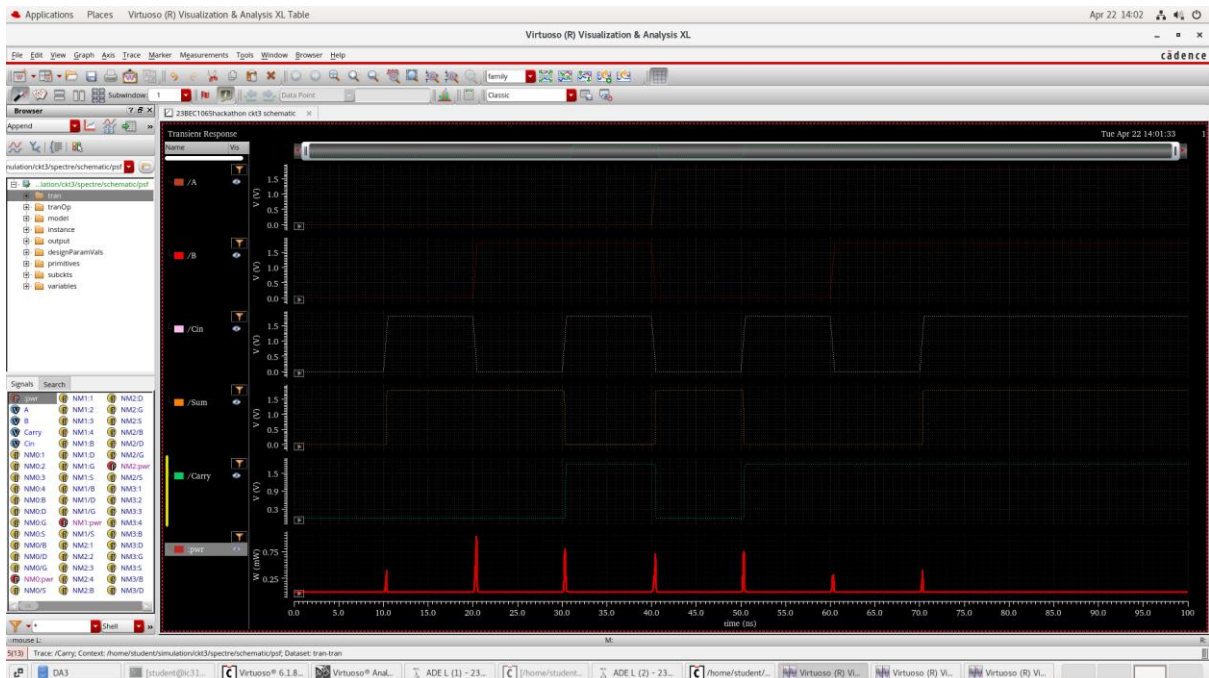
after sizing



Timing diagram

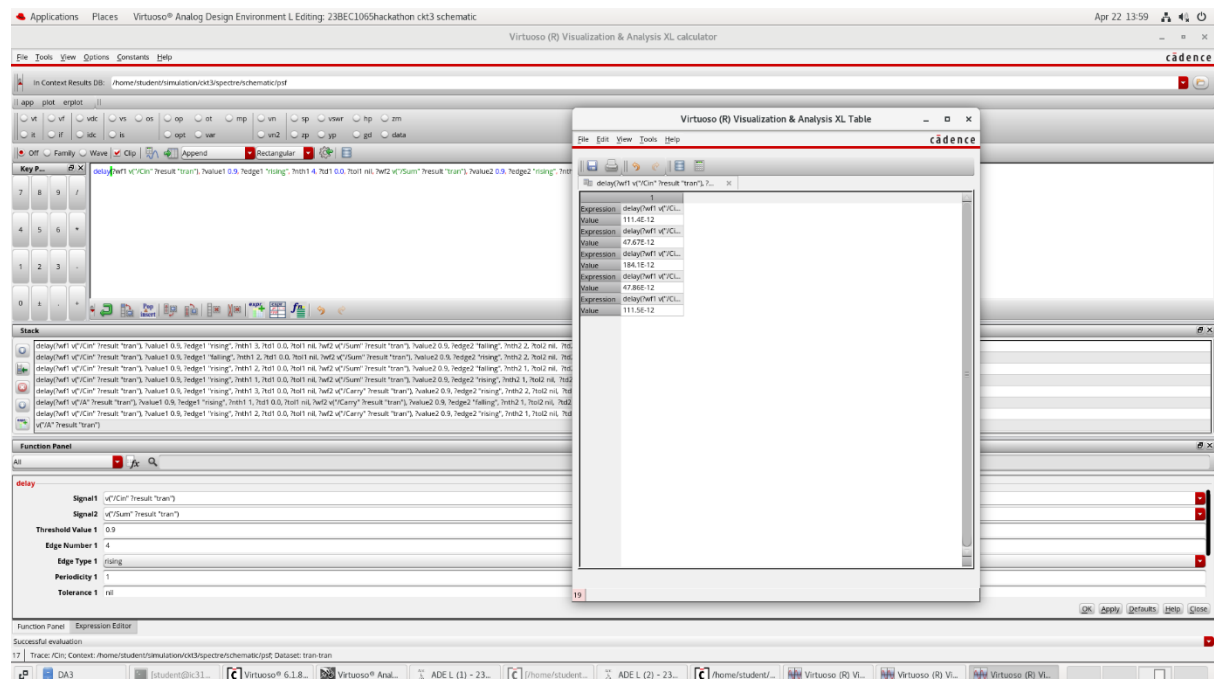


Power

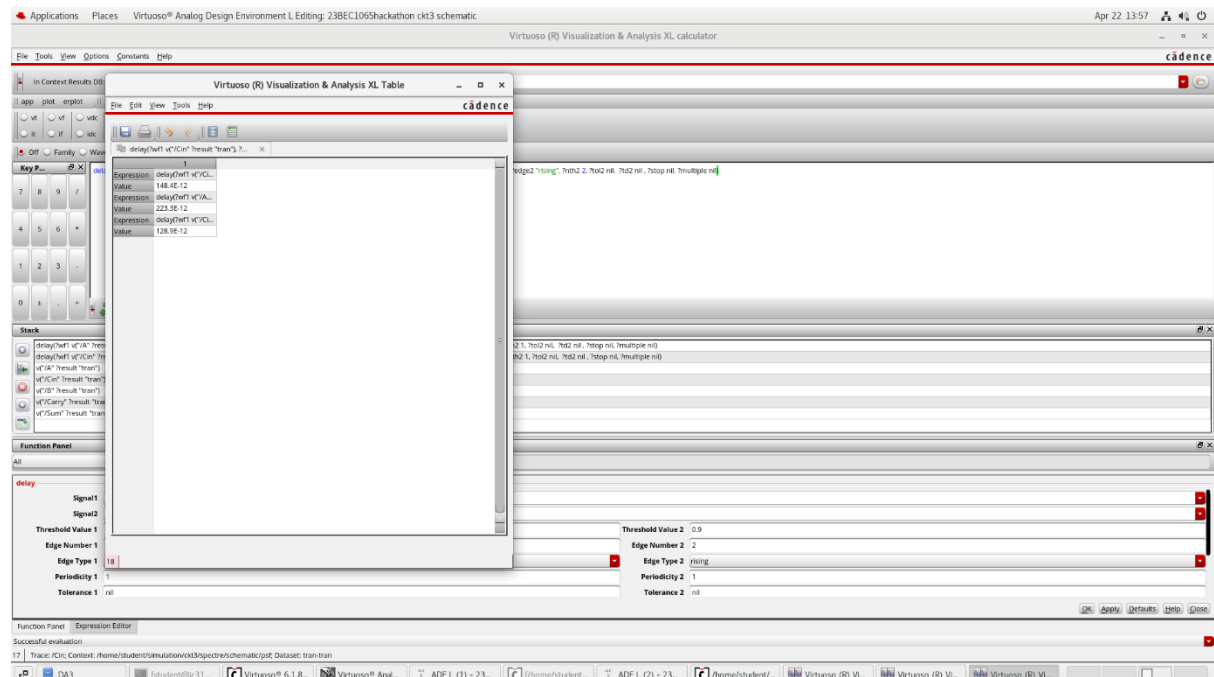


Delay value

Sum



Carry



Power calculation

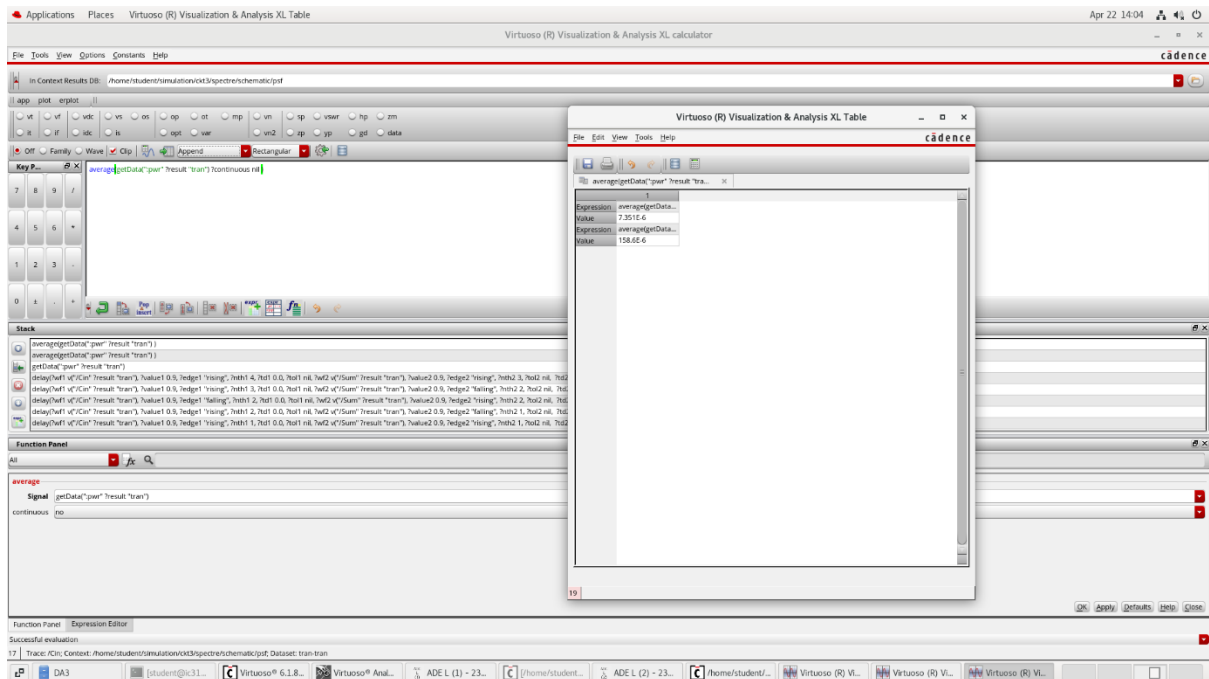


Table 3:

Sum

Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
001B	88.06 E-12	111.4 E-12
011B	15.86 E-12	47.67 E-12
100B	186.3 E-12	184.1 E-12
101B	16.02 E-12	47.86 E-12
111B	87.84 E-12	111.5 E-12

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Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
011B	15.5 E-12	148.4 E-12
100B	274.6 E-12	223.3 E-12
101B	108.3 E-12	128.9 E-12

Power (Before Sizing) = 7.254 E-6 W

Power (After Sizing) = 7.351 E-6 W