Braun Multiplier

Circuit to be implemented

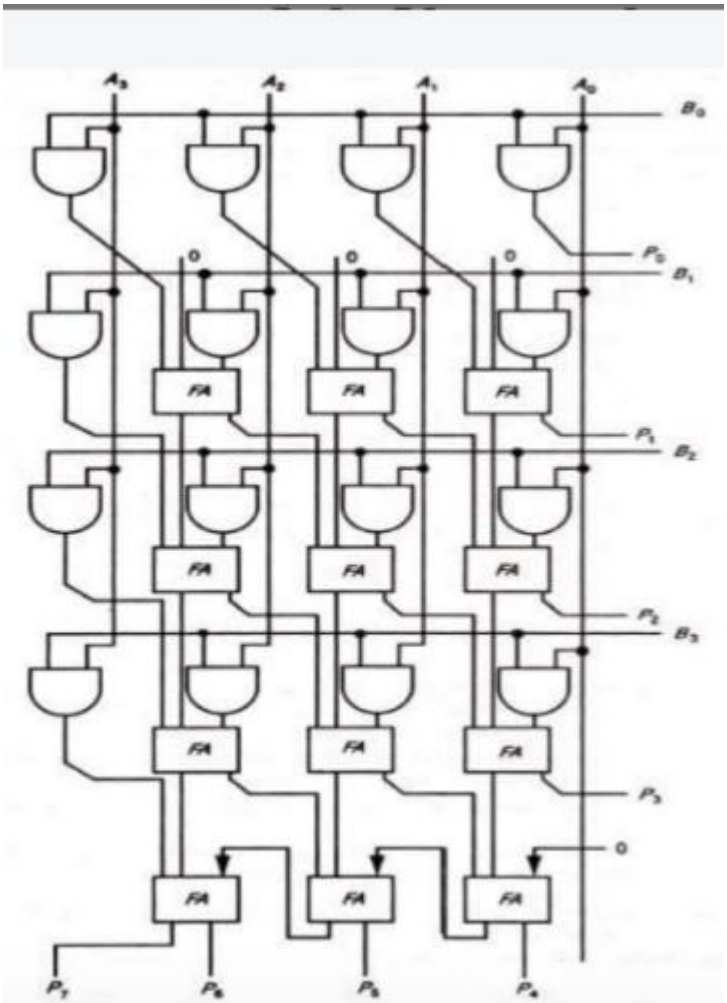
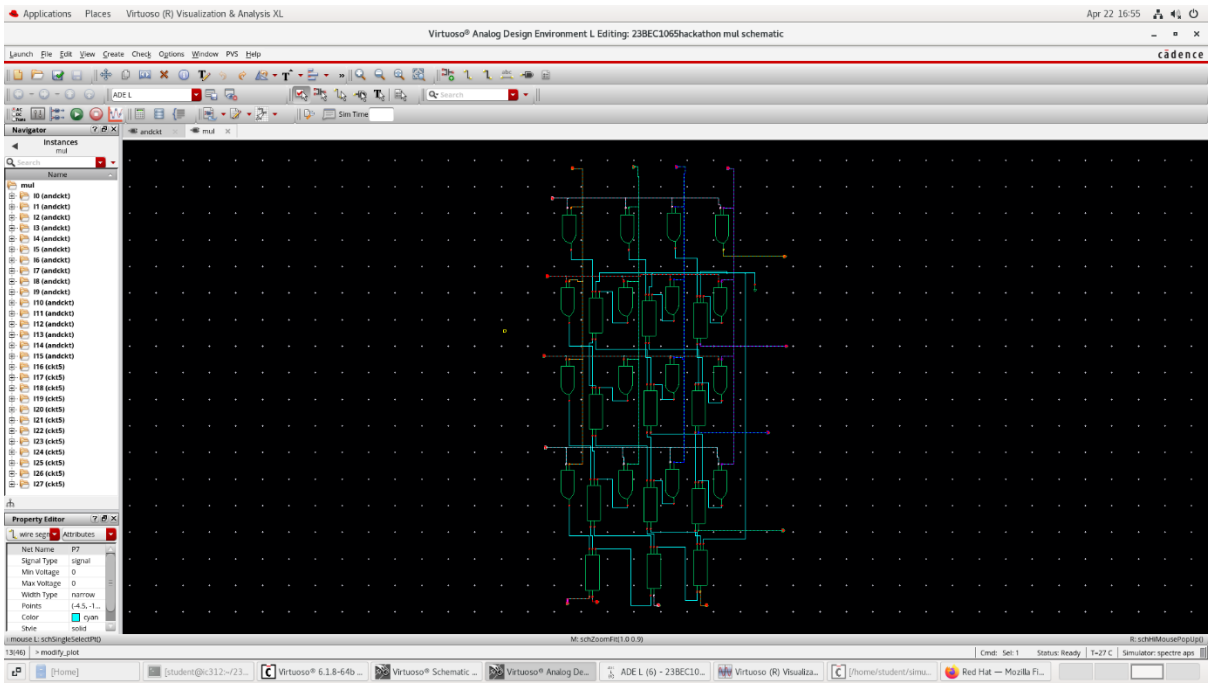
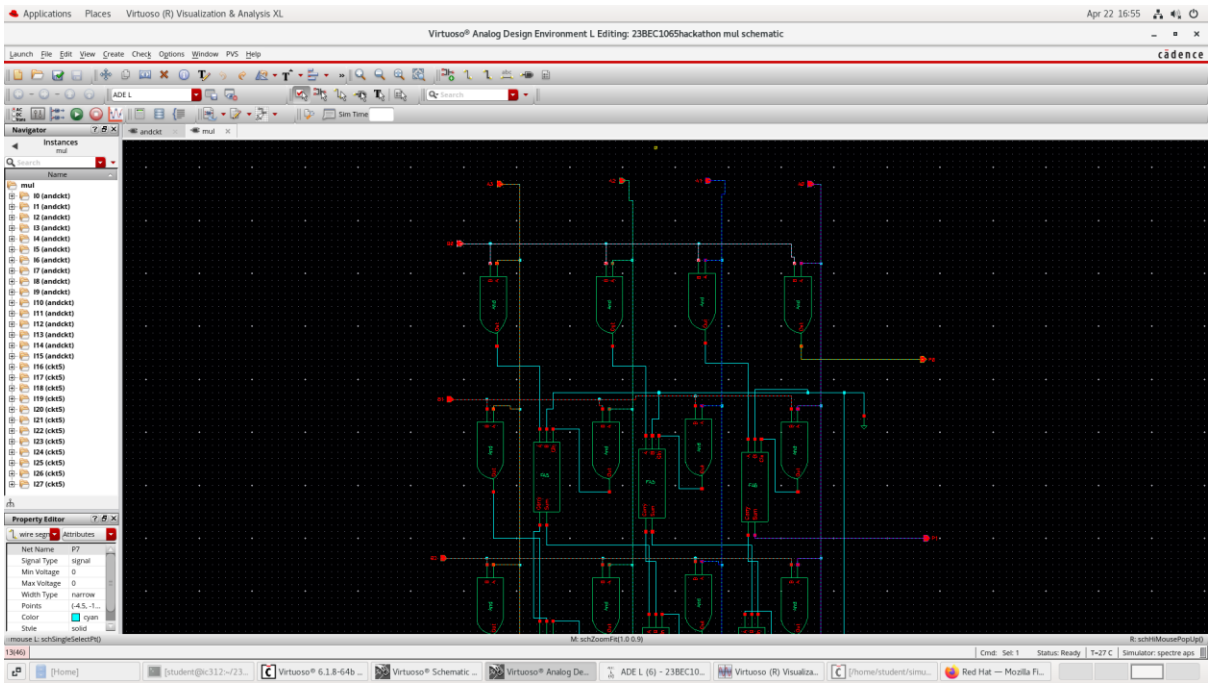


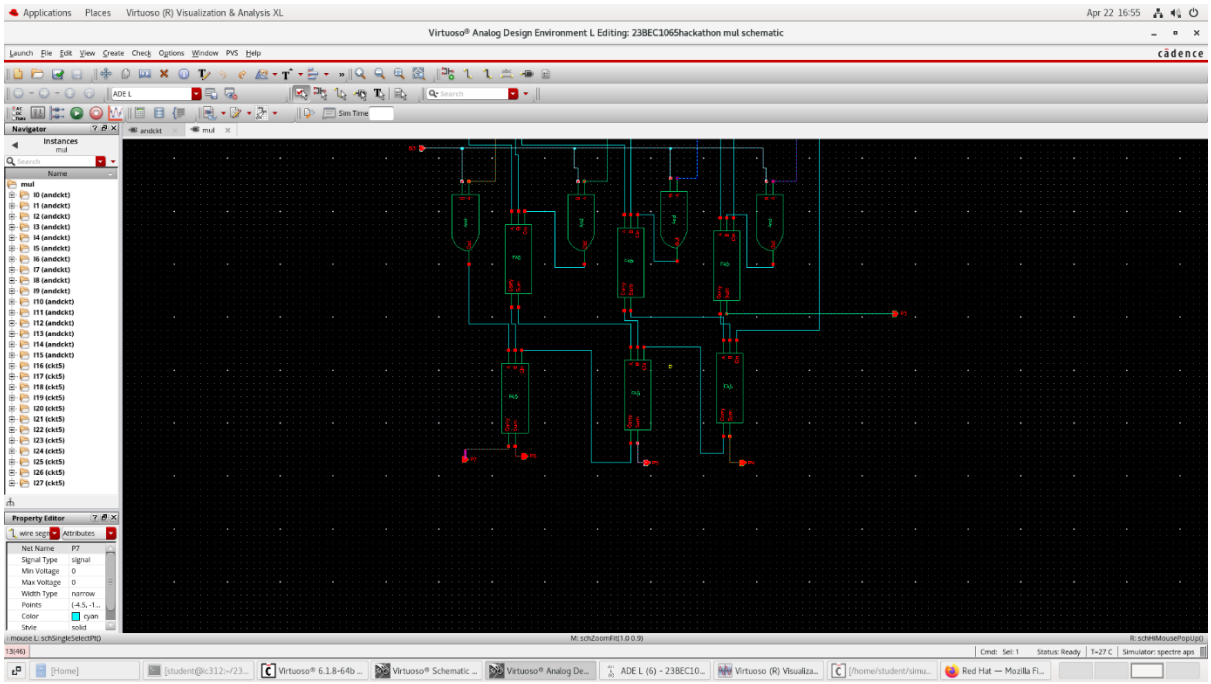
Fig 8: 4 bit Braun multiplier

Circuit implemented in cadence



In depth view





Output verified for bit pattern

Input A3 A2 A1 A0	Input B3 B2 B1 B0	Output P7 P6 P5 P4 P3 P2 P1 P0
0000	0001	00000001
1001	1110	01111110
1110	1100	10101000
1001	0001	00001001
1111	1111	11100001

Output

It is taken as three pictures.

Zoom it for clarity


Virtuoso (R) Visualization & Analysis XL
Transient Response
/P7
/P6
/P5
/P4
/P3
/P2
/P1
/P0
/B3
/B2
/B1
time (ns)


Virtuoso (R) Visualization & Analysis XL
Transient Response
/P2
/P1
/P0
/B3
/B2
/B1
/B0
/A3
/A2
/A1
/A0
time (ns)