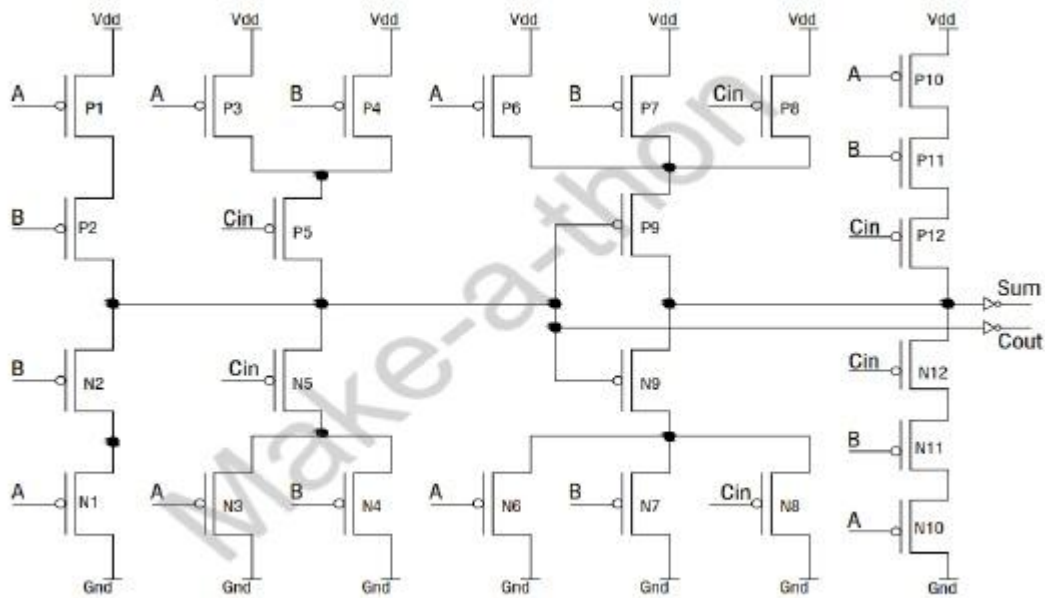


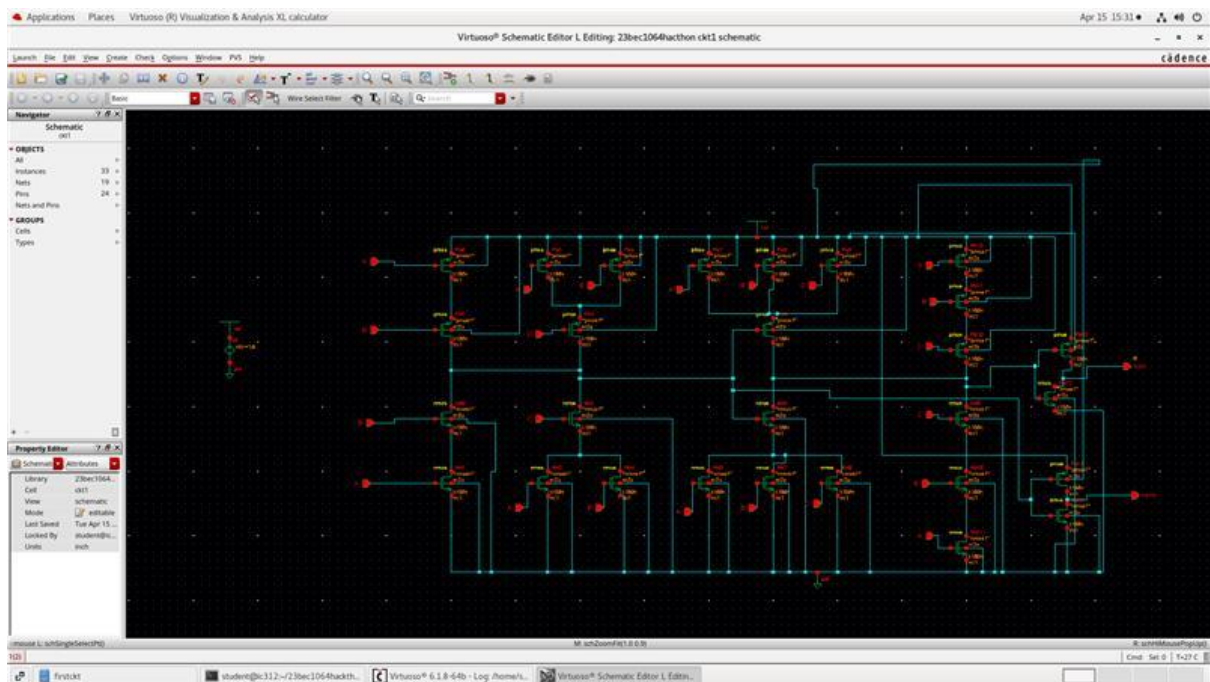
Adder 1

Circuit to be implemented

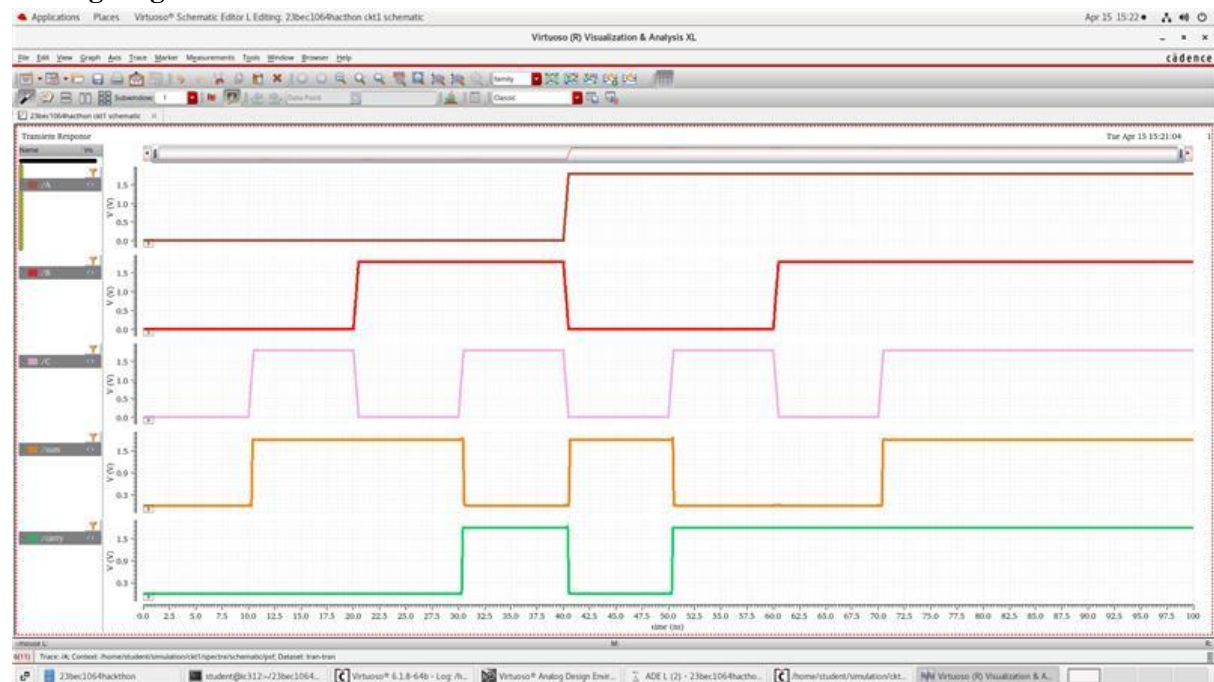


implementation in cadence

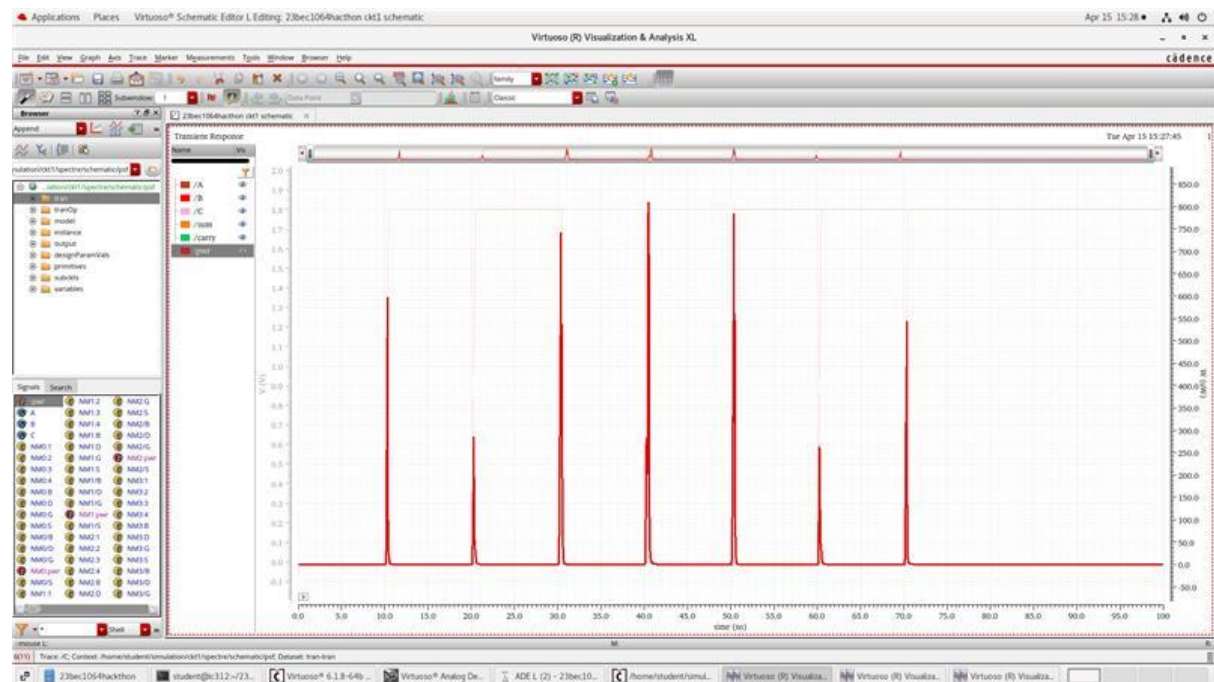
Before sizing



Timing diagram

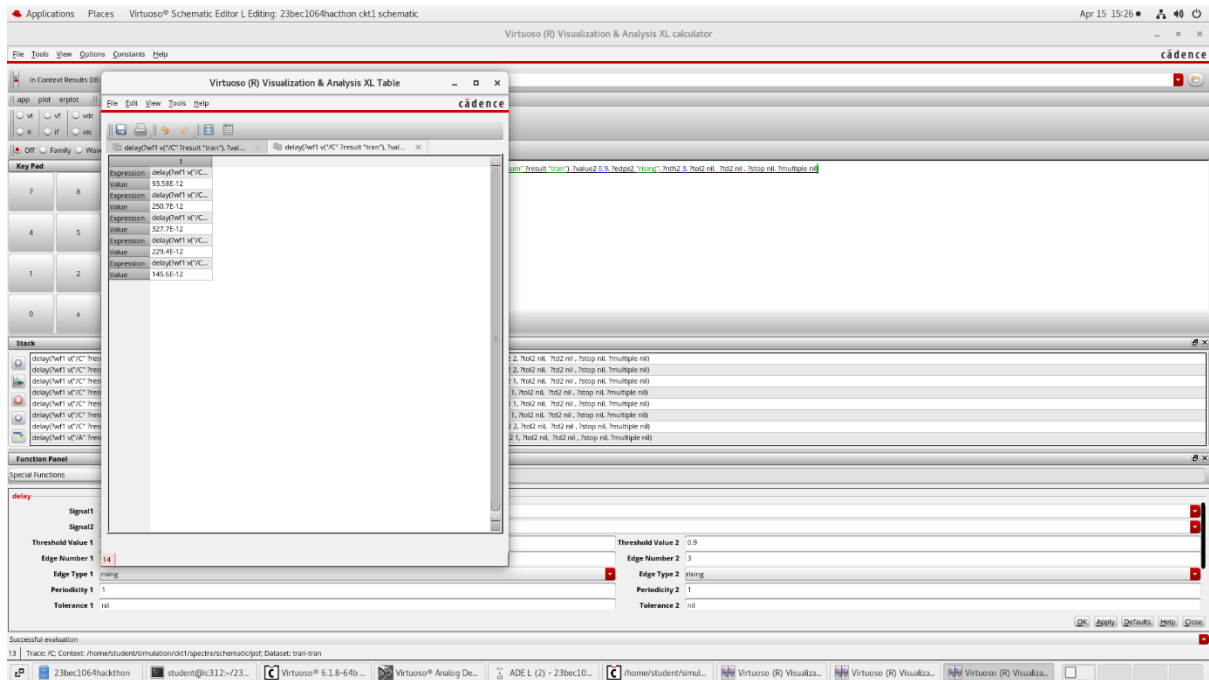


Power wave

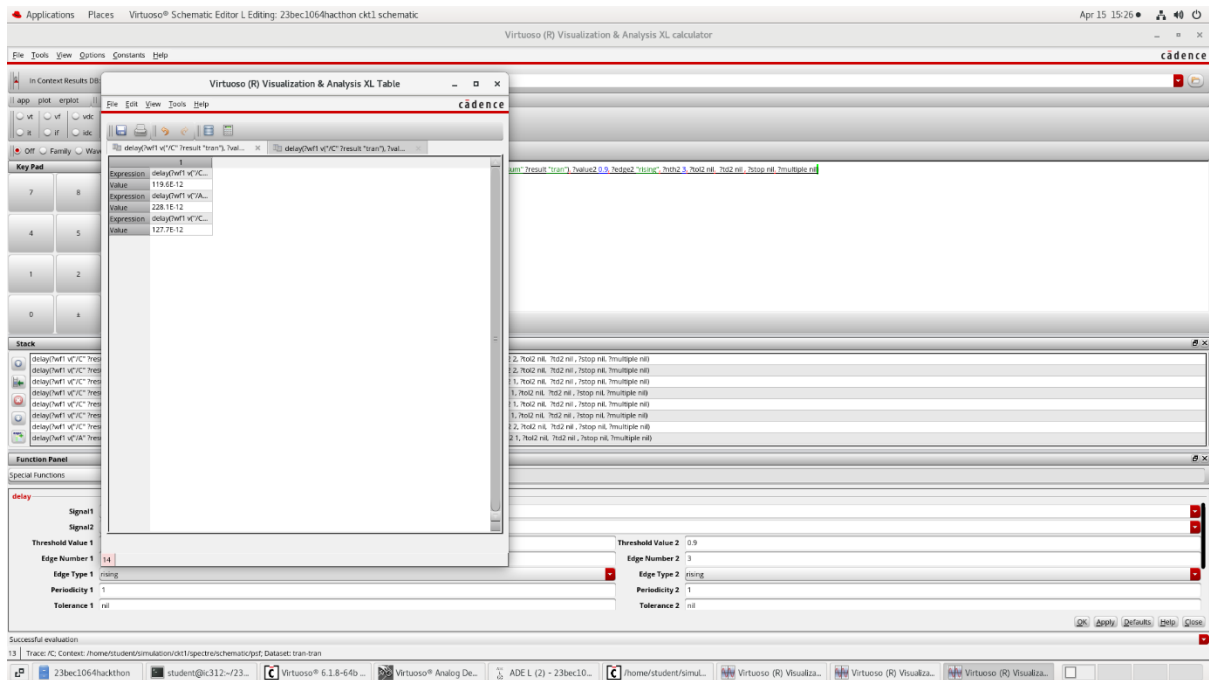


Delay values

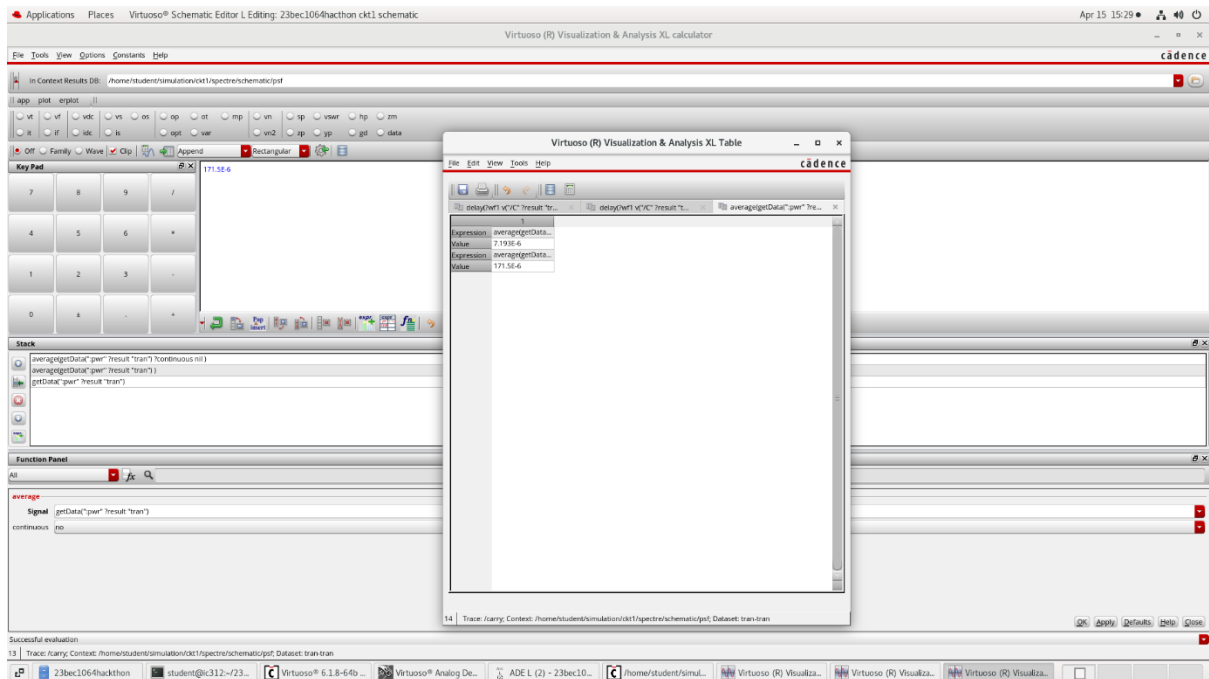
sum



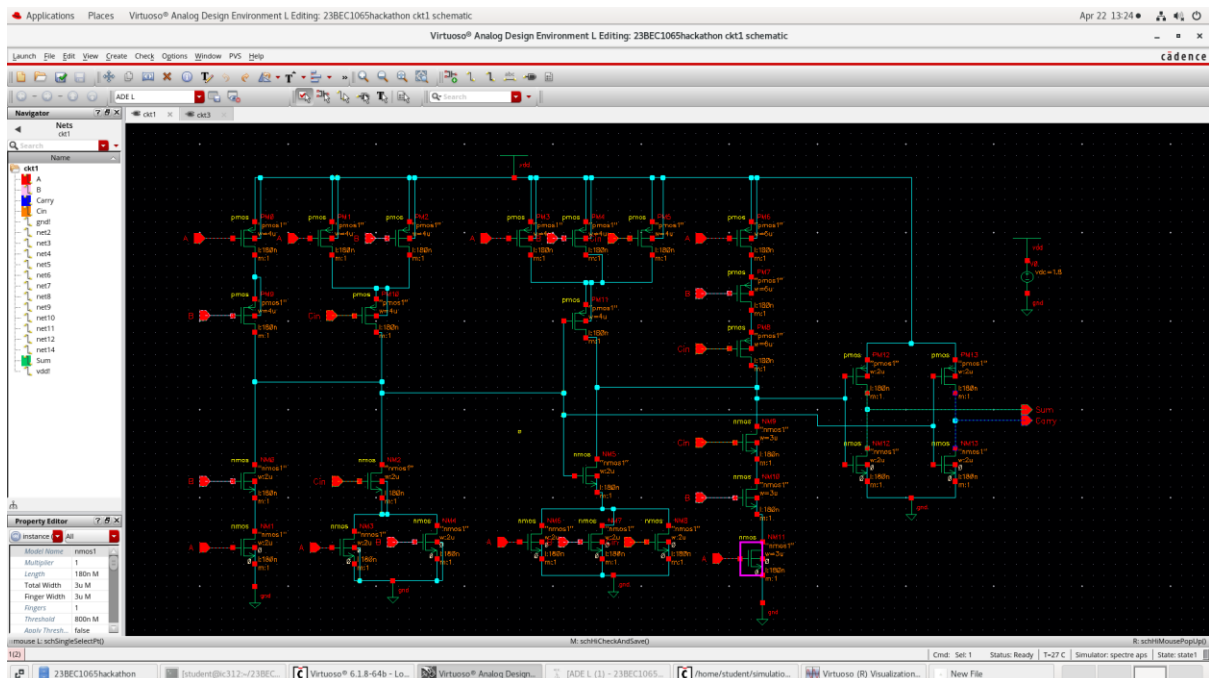
Carry



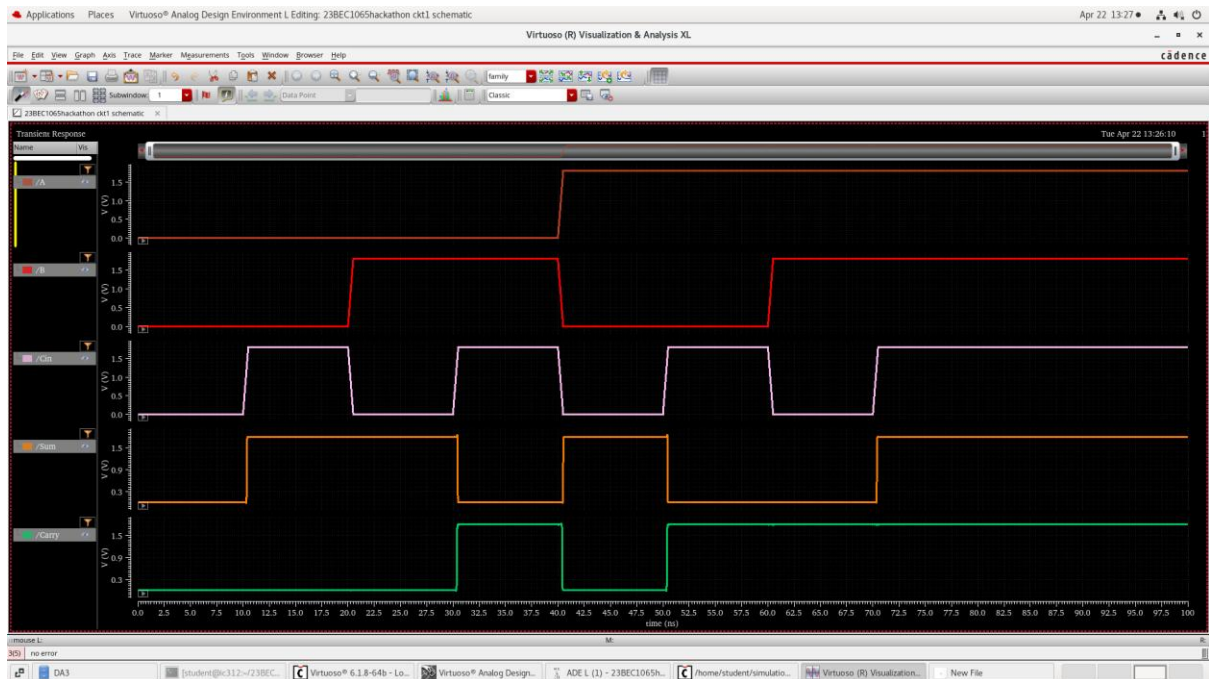
Power calculation



After sizing



Timing diagram

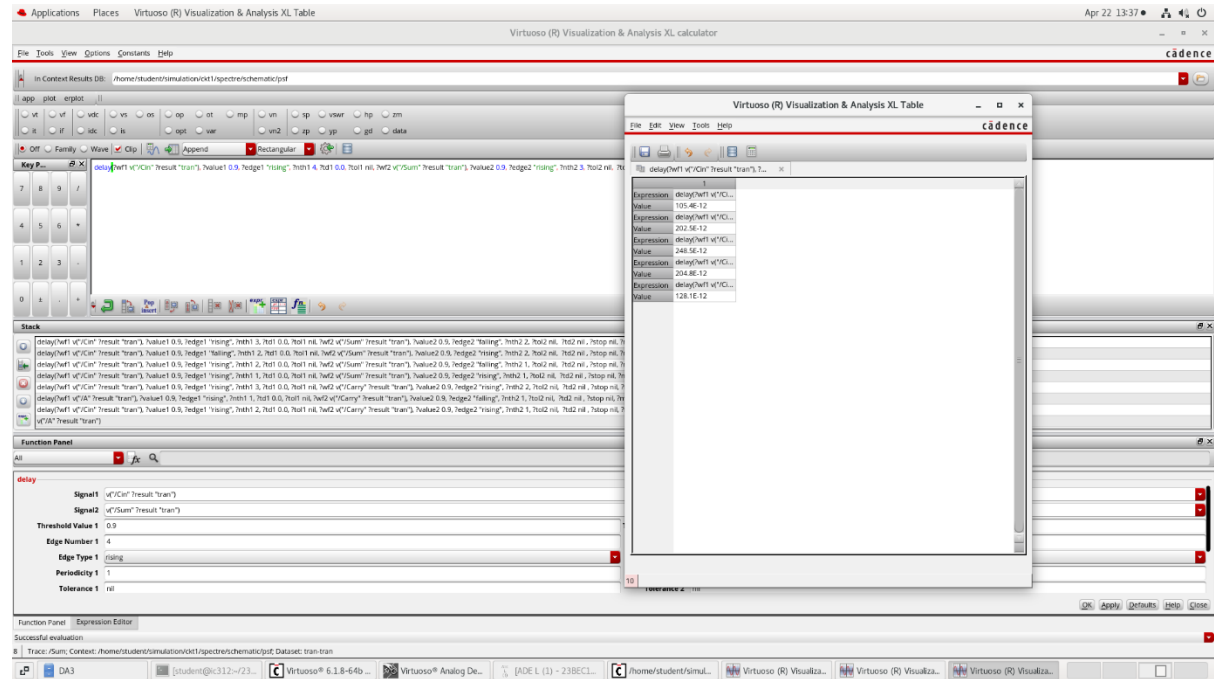


Power wave

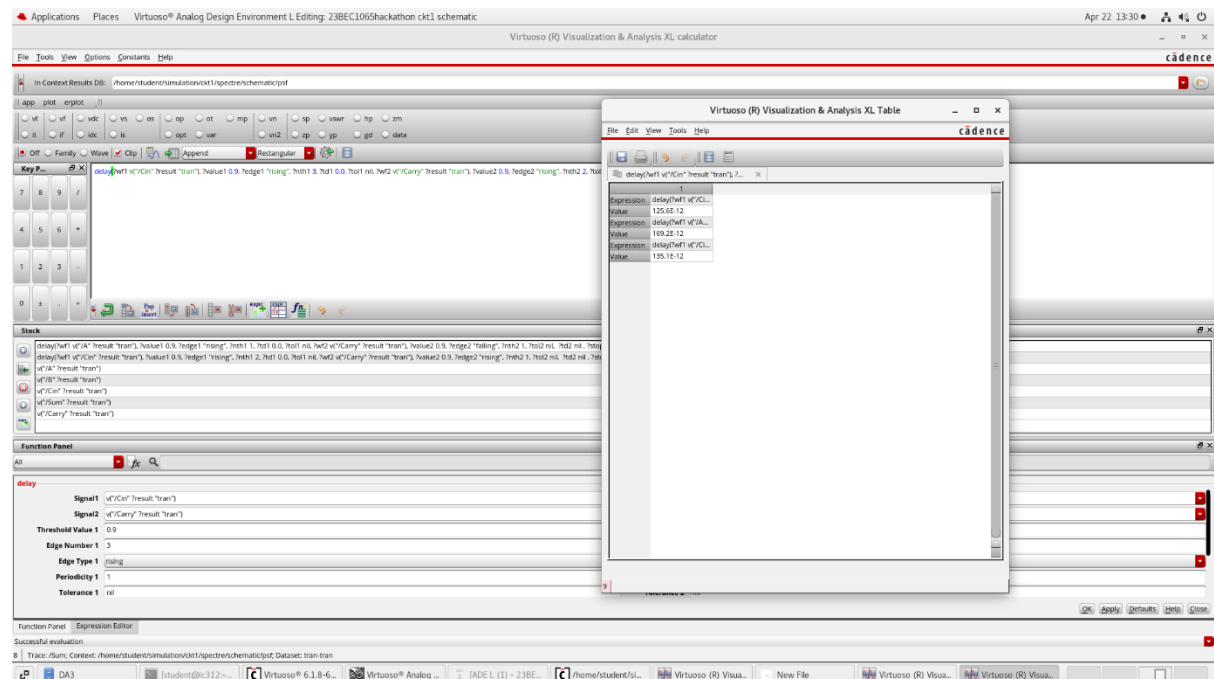


Delay value

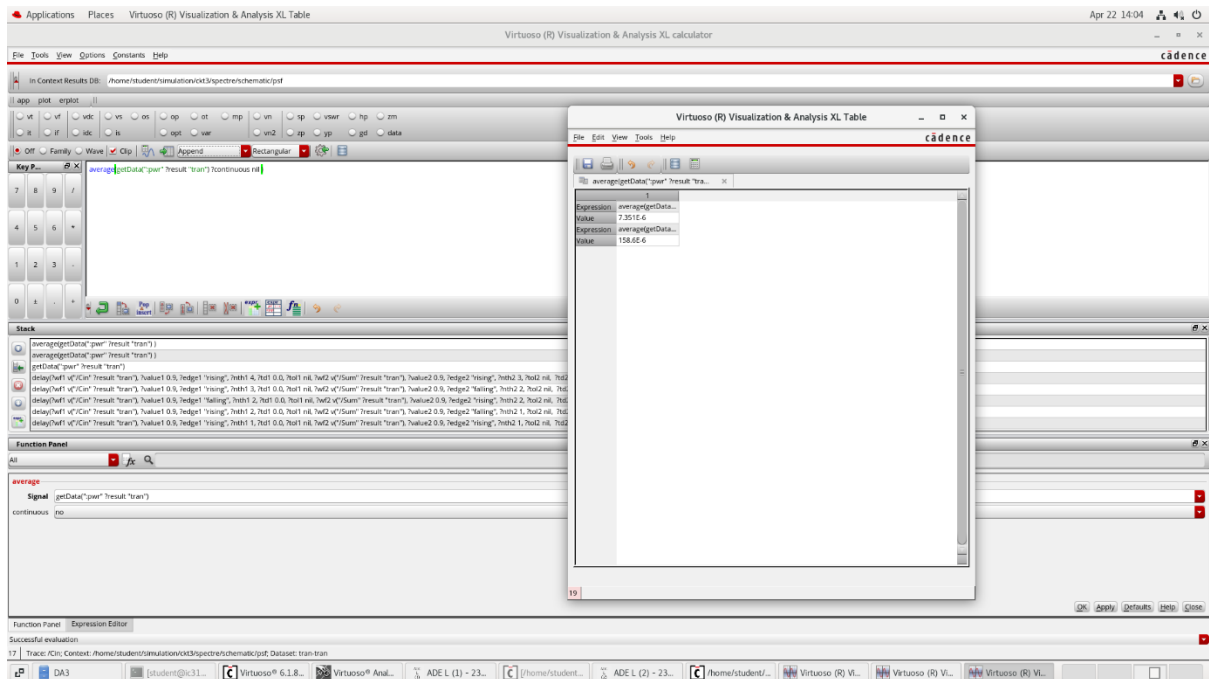
sum



Carry



Power calculation



Answer:

Sum	Bit pattern	Delay (Before sizing) (In seconds)	Delay (After sizing) (In seconds)
001 B		93.58 E-12	105.46 E-12
011 B		200.7 E-12	202.5 E-12
100 B		327.7 E-12	248.56 E-12
101 B		229.4 E-12	204.8 E-12
111 B		145.6 E-12	128.1 E-12

Delay	Bit pattern	Delay (Before sizing) (In seconds)	Delay (After sizing) (In seconds)
011 B		119.6 E-12	125.6 E-12
100 B		228.1 E-12	169.2 E-12
101 B		127.7 E-12	135.1 E-12

Power (Before sizing) = 7.193 E-6 W

Power (After sizing) = 7.351 E-6 W