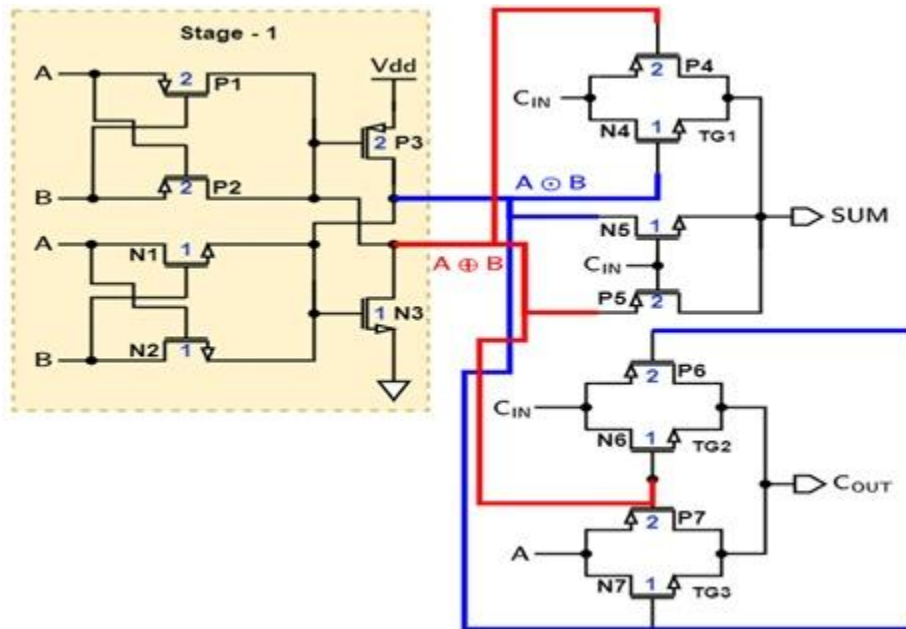


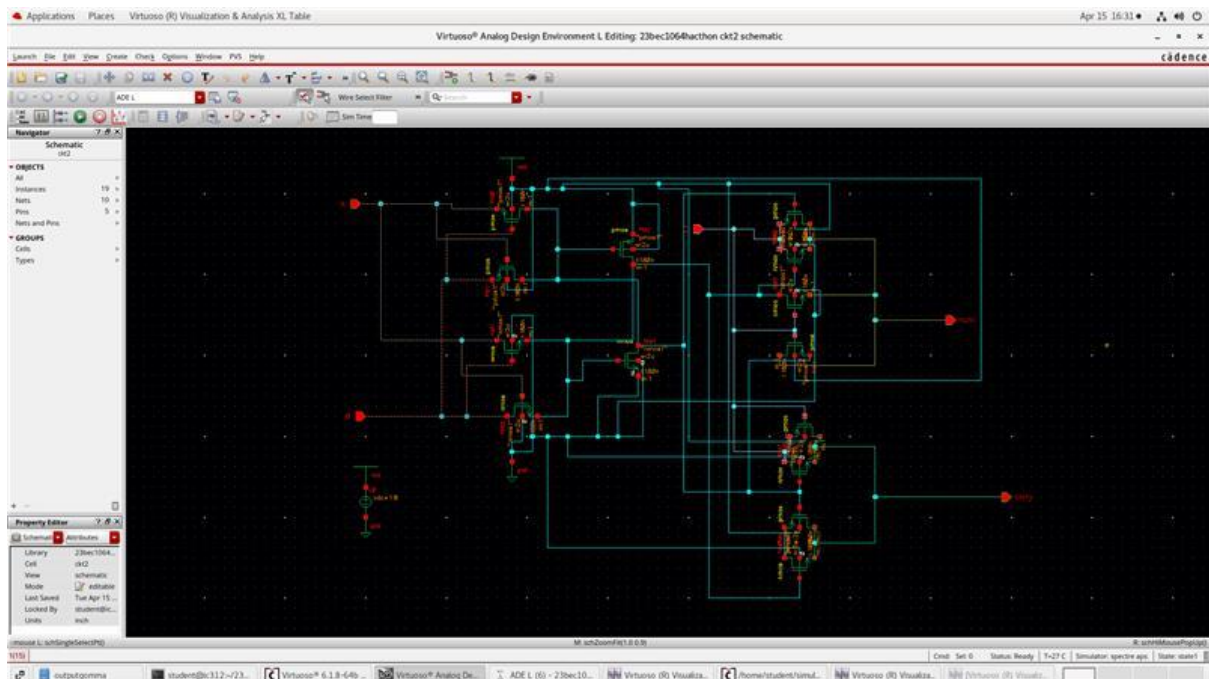
Adder 2

Circuit to be implemented



Implementation in cadence

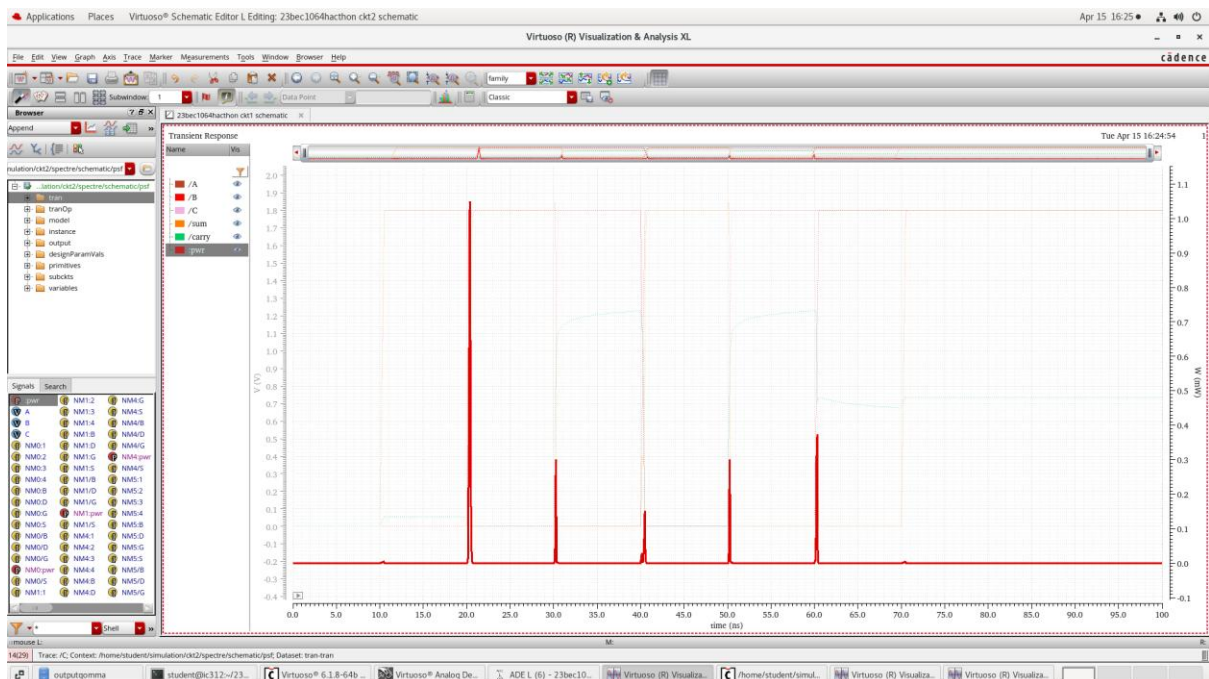
Before sizing



Timing diagram

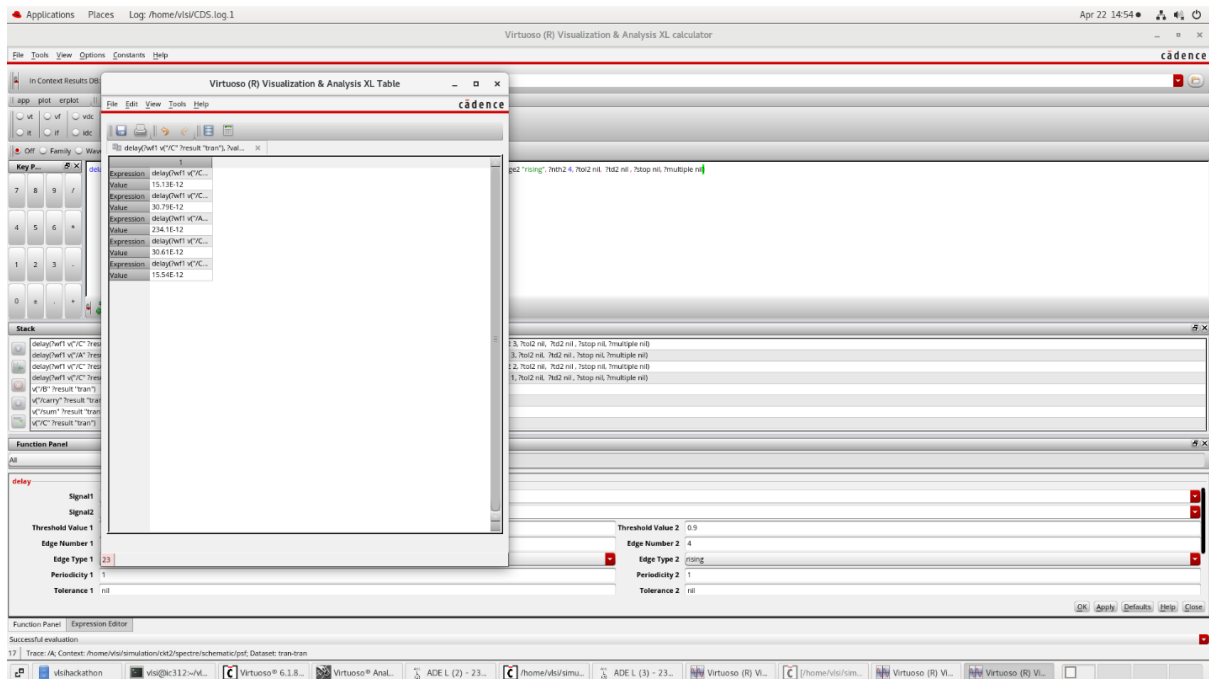


Power

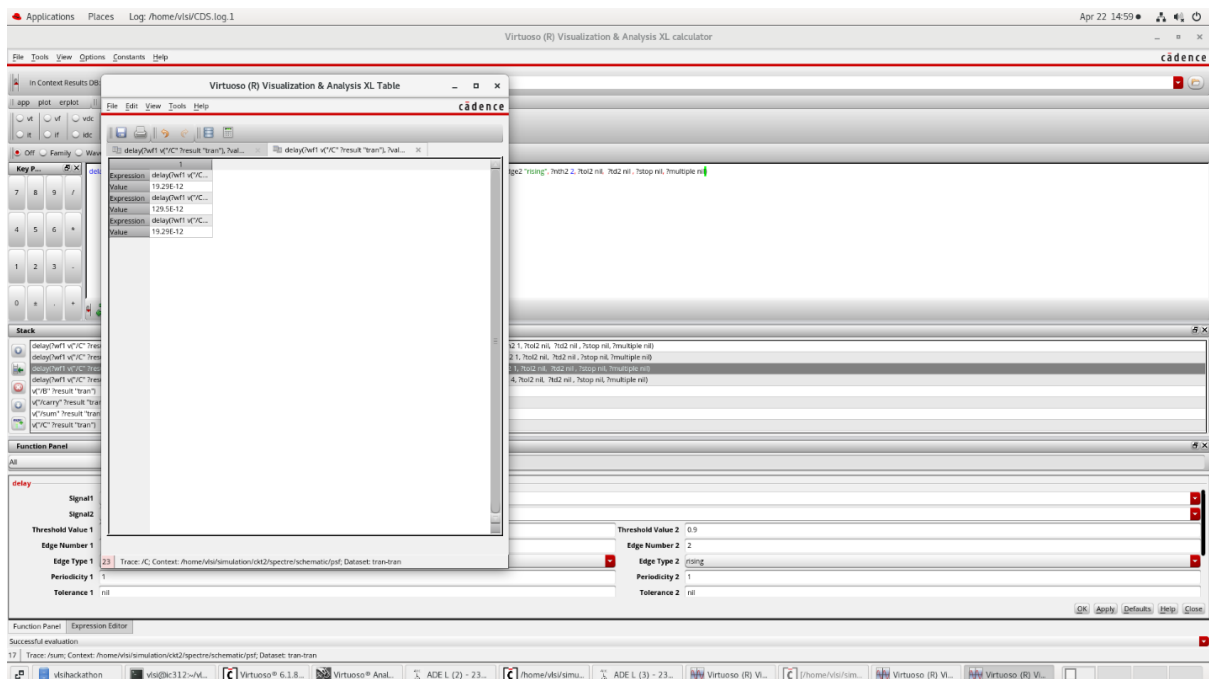


Delay value

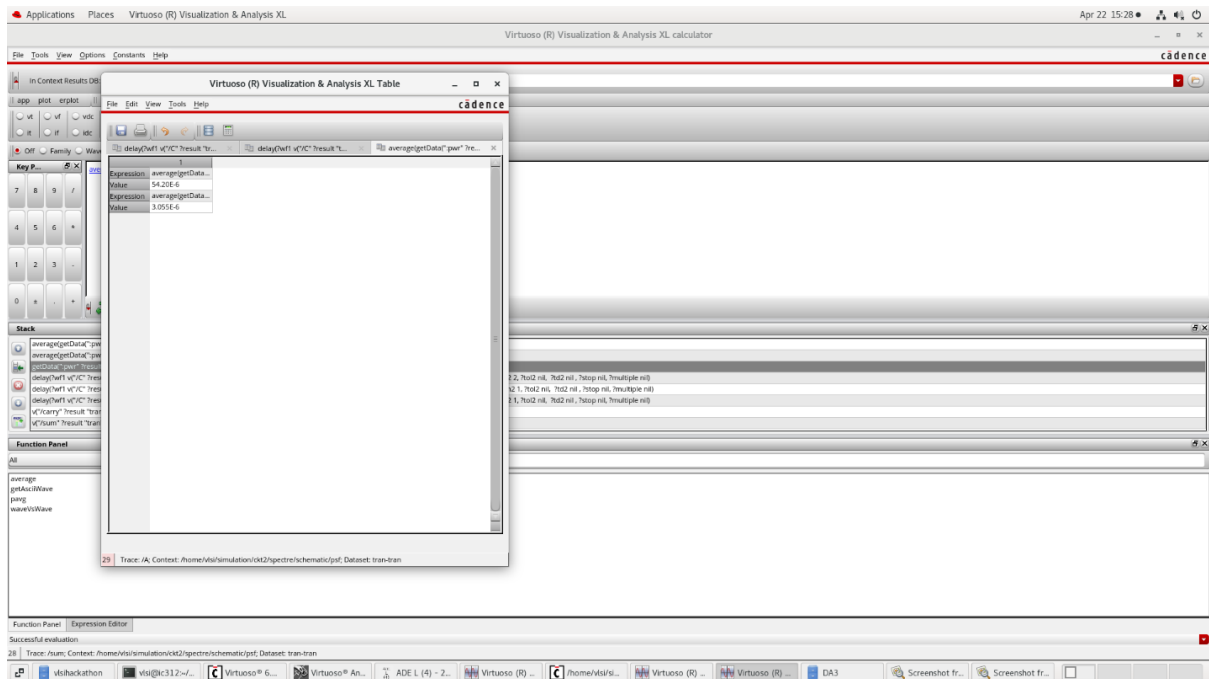
Sum



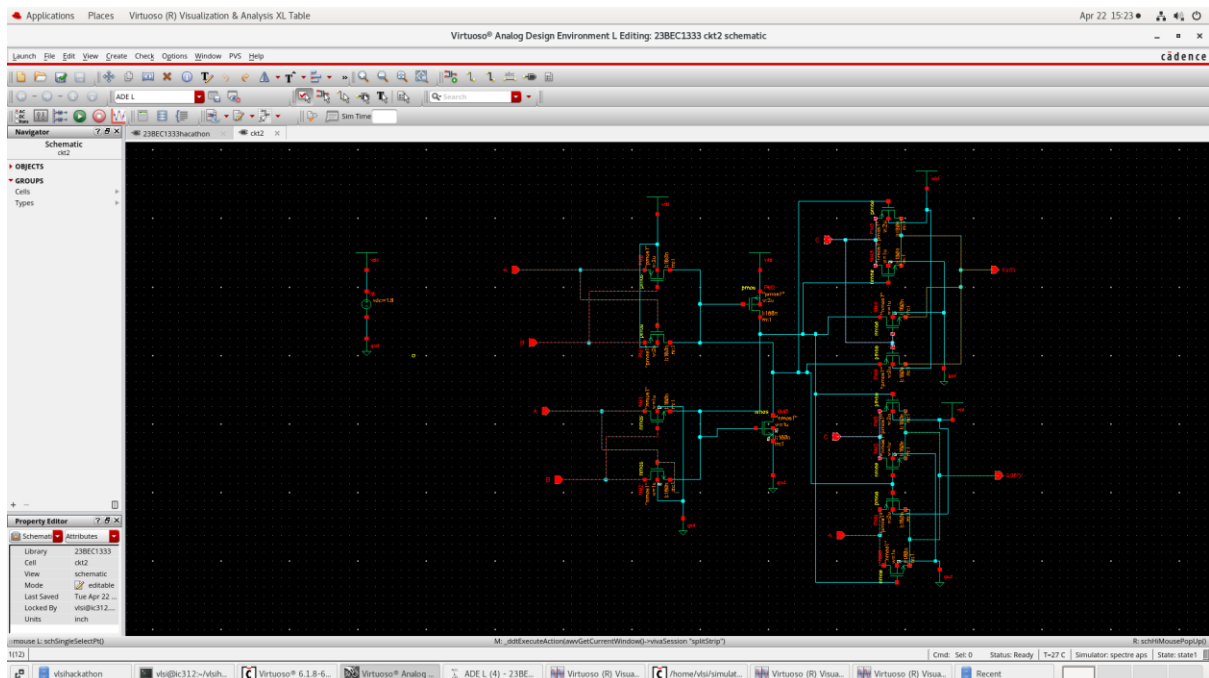
Carry



Power calculation



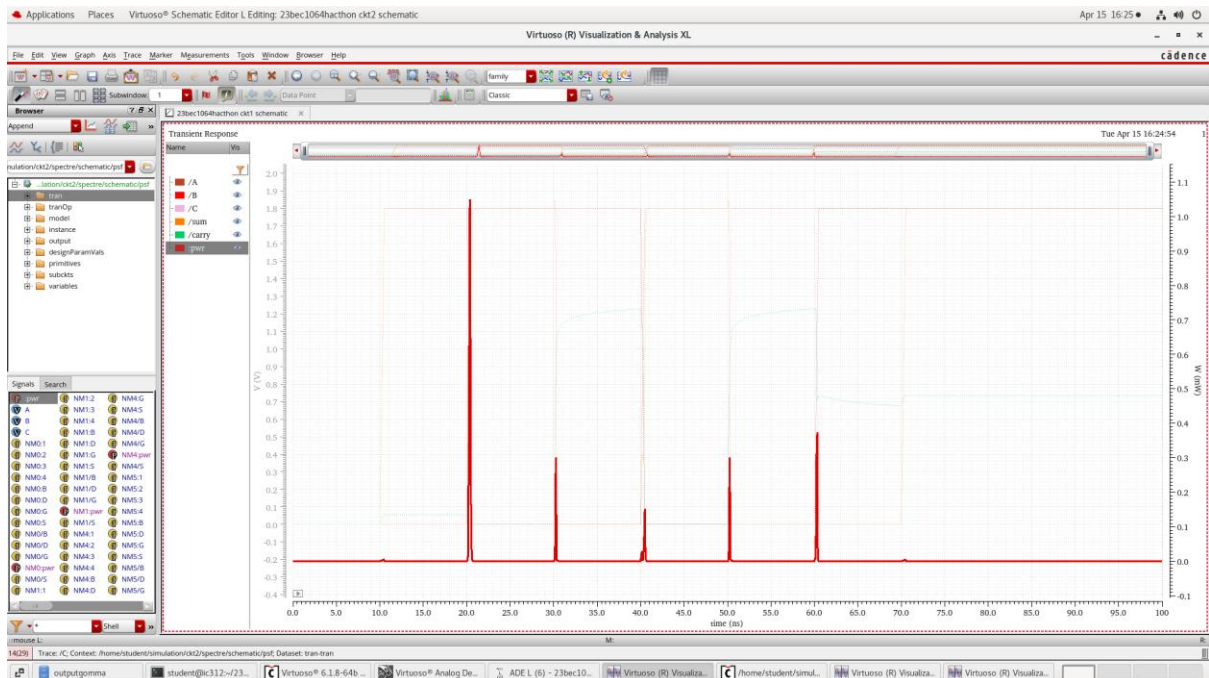
after sizing



Timing diagram

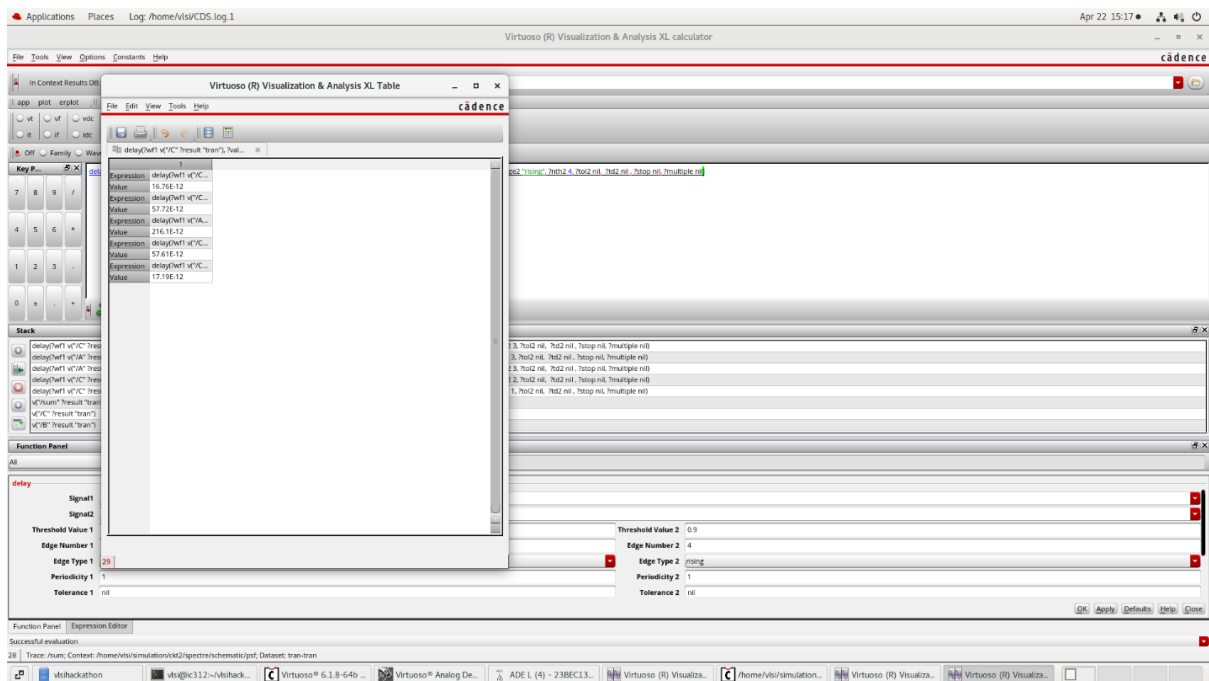


Power

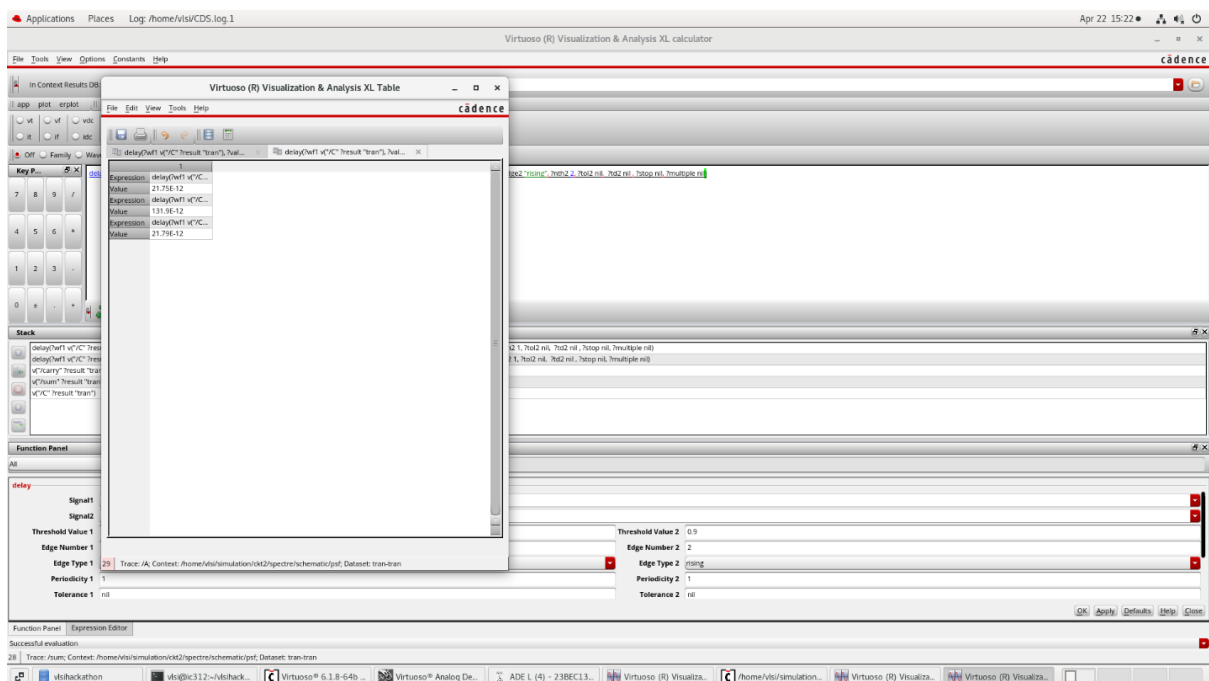


Delay value

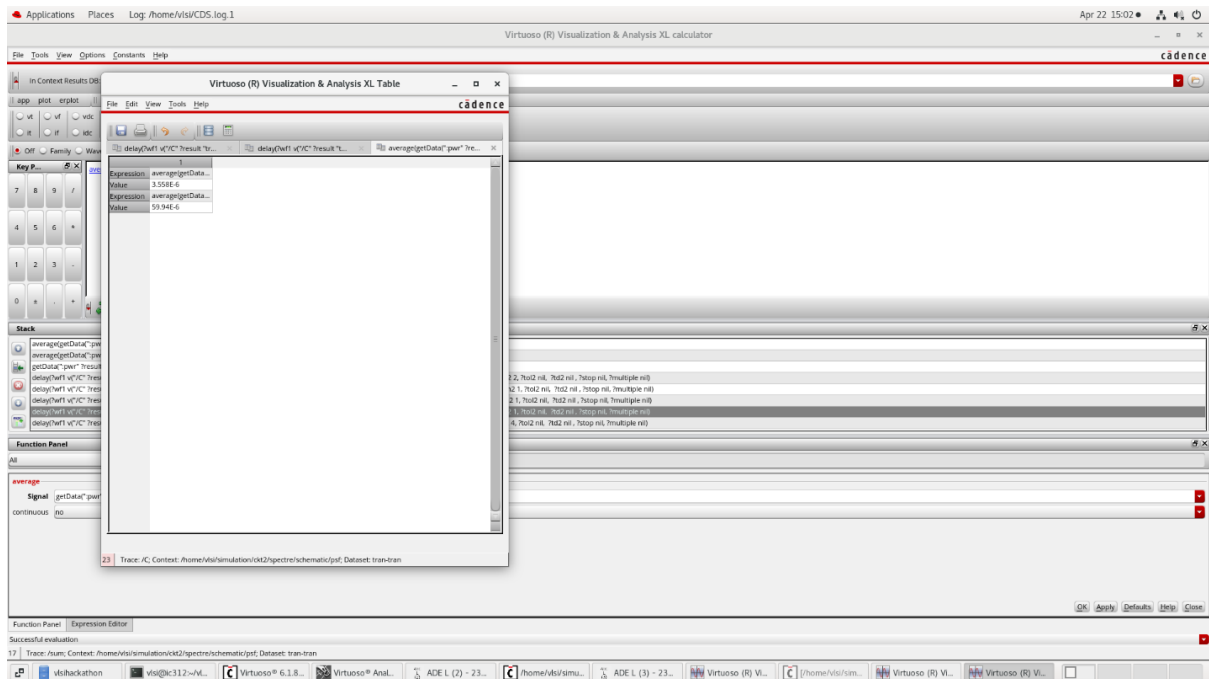
Sum



Carry



Power calculation



Address 2:

Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
001B	15.13 E-12	16.76 E-12
011B	30.79 E-12	57.72 E-12
100B	234.3 E-12	216.1 E-12
101B	30.61 E-12	57.6 E-12
111B	15.54 E-12	17.19 E-12

Casey

Bit pattern	Delay (Before Sizing) (In seconds)	Delay (After Sizing) (In seconds)
011B	19.29 E-12	21.75 E-12
100B	129.25 E-12	131.9 E-12
101B	19.29 E-12	21.79 E-12

Power (Before Sizing) = 54.2 E-6 W

Power (After Sizing) = 3.55 E-6 W