**HARISH KASHA**

**Design Engineer I @ VAALUKA SOLUTIONS**

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 **Hyderabad, Telangana – 500060**

Seeking a challenging career in an organization with a performance-oriented environment for the achievement of personal advancement.

**EXPERIENCE**

**VAALUKA SOLUTIONS [AUG 2023 - PRESENT]**

* **Verified the 1x3 packet router using UVM methodology.**
* **Designed and verified Memory Subsystem containing dual port RAMs with variable read and write latencies with a class-based system Verilog testbench.**
* **Gained knowledge on AXI4 protocol.**
* **Developed a verification plan for asynchronous FIFO and verified it with class-based testbench.**

**INTEL Internship [JULY 2022 - JULY 2023]**

* **Comprehensive understanding of SOC level power intent, with hands-on experience in UPF generation, integration, and proficiently performing static verification of UPF using Synopsys VCLP.**
* **Developed an algorithm to automatically sense the requirement and place the “set\_correlated” command (UPF 3.0) into the output UPF files which significantly reduced manual effort and improved the selection of correct rule (LH or HL or Both) for the level shifters.**
* **Additionally, the proposed algorithm can automatically select the correct rule for level shifters in dynamic voltage scaling (DVFS) scenarios also, improving the correctness of UPF generation.**
* **Upgraded “set\_isolation” command generation algorithm by leveraging the -source and -sink arguments introduced in UPF 2.0, effectively introducing higher levels of abstraction.**
* **Achieved backward compatibility and reusability for all automation solutions developed, enabling seamless deployment across multiple projects.**

**EDUCATION**

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| --- | --- | --- |
| **Degree** | **Institution** | **Score** |
| **Master of Technology in Electronics Design and Technology [M.Tech]** | **National Institute of Technology Calicut** | **9.13/10 CGPA**  **[2023]** |
| **Bachelor of Engineering in Electronics and Communication Engineering [B.E]** | **Matrusri Engineering College** | **8.48/10 CGPA [2021]** |
| **Intermediate**  **[Class XII]** | **Narayana Junior College** | **94.6%**  **[2017]** |
| **SSC [Class X]** | **Raghunatha Model High School** | **90% [2015]** |

**PROJECTS**

**Verification of Memory Subsystem [VAALUKA]**

**Designed and verified a Memory Subsystem utilizing a class-based test bench with a total code coverage of 100%. The memory subsystem features dual port RAMs with configurable read and write latencies, as well as robust support for 1-bit error detection and correction.**

**Verification of 1x3 router [VAALUKA]**

**Developed UVC files for the router input interface using UVM. Developed various test sequences to verify the features of the packet router. Executed design verification, achieving a 100% total functional coverage.**

**Client project and Server project [INTEL]**

**Worked on UPF generation and static verification of UPF using Synopsys VCLP. Automated and implemented “set\_correlated” and “set\_isolation -source -sink” enhancements on these projects.**

**CERTIFICATIONS**

* **UPF Power Aware Design & Verification. [Udemy]**
* **System Verilog Assertions. [Udemy]**