HALF ADDER

- Now in this document let's implement the half adder by the rules stated in the introduction document
- Identify the number of input and output pins
    - The half adder would add two bits so it would require two input pins (say A and B) and the result of addition would be Sum and Carry
- The basic diagram

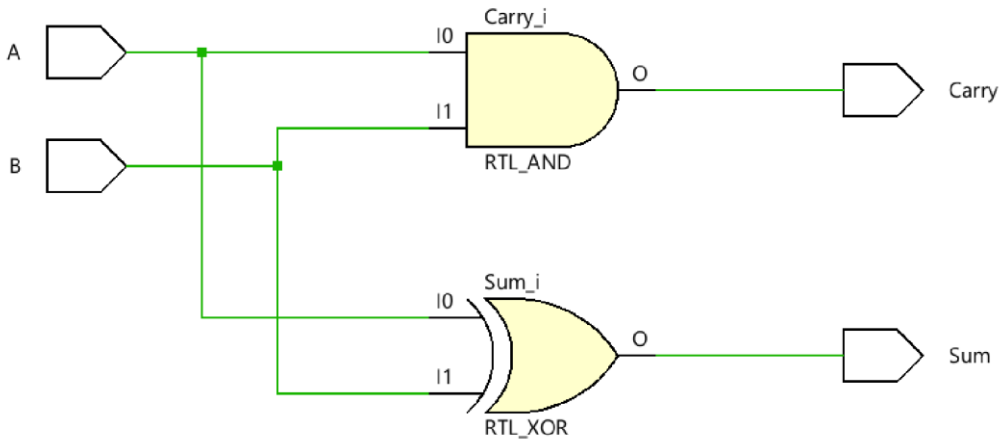
- The truth table
    -

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- The boolean expression
    - Sum: The minterm in the Sum column are to be considered
      The sum will be 1 for the combination A'B+AB' which is nothing but (A $\oplus$ B)
    - The carry will be 1 for the combination A.B

- Software used: Vivado
- **Now implementing the logic in verilog here the Gate level modelling is being used**
    - The code [Digital_Circuits/Half_adder at main · HarishGokul15/Digital_Circuits · GitHub]

- The Circuit Diagram



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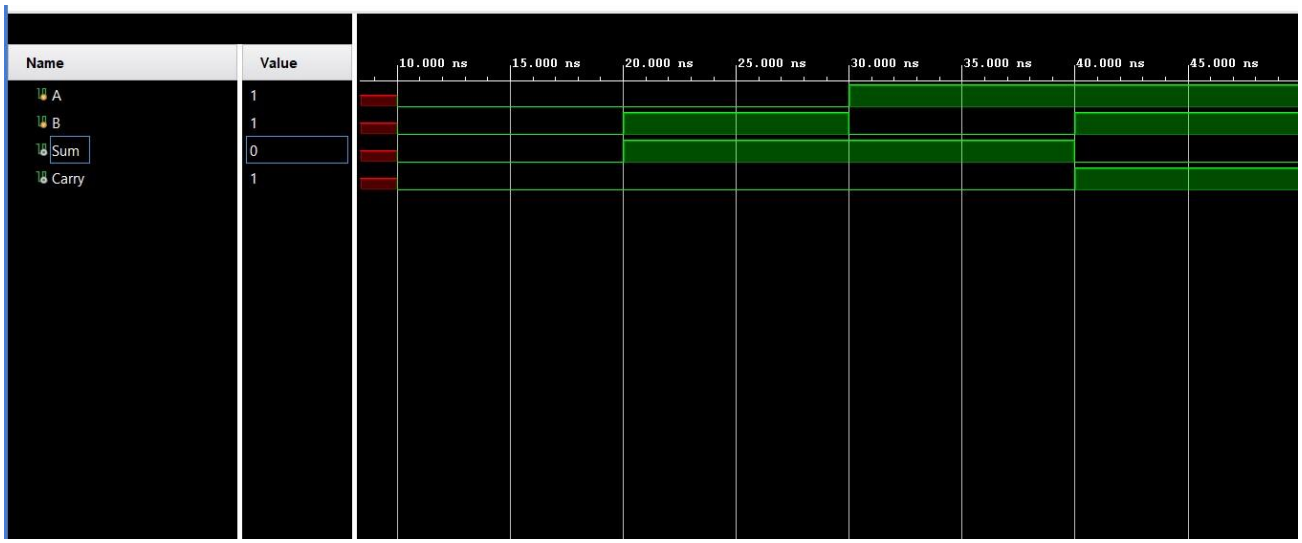
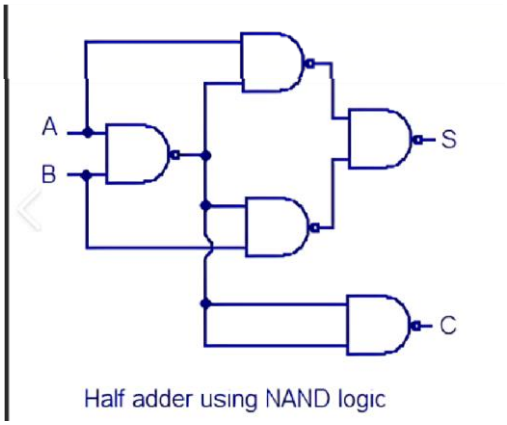
- The Output

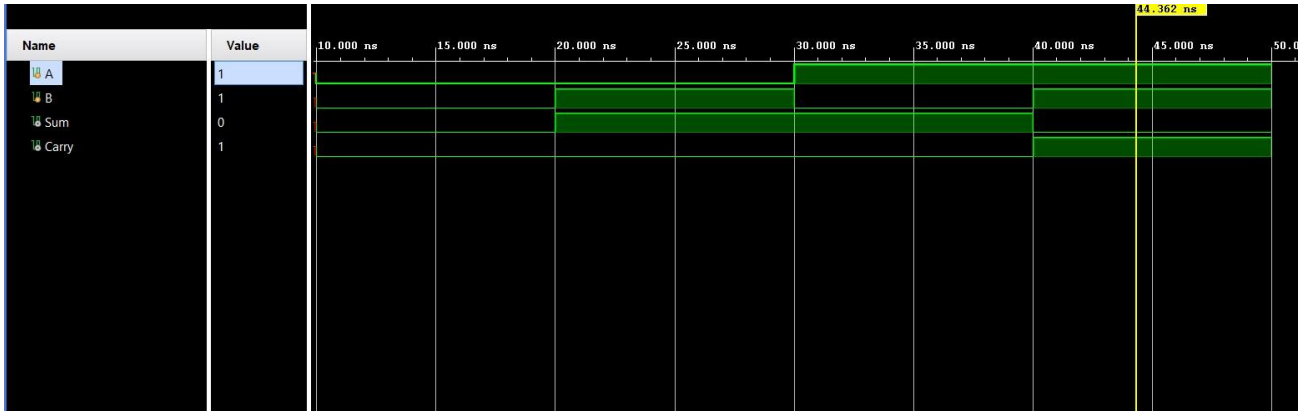


- The IC fabrication of these circuits involve the design of circuit using the NAND, NOR gates (The universal gates) for Simplification and Optimization
- **Now let us consider the implementation of Half adder using nand gate**

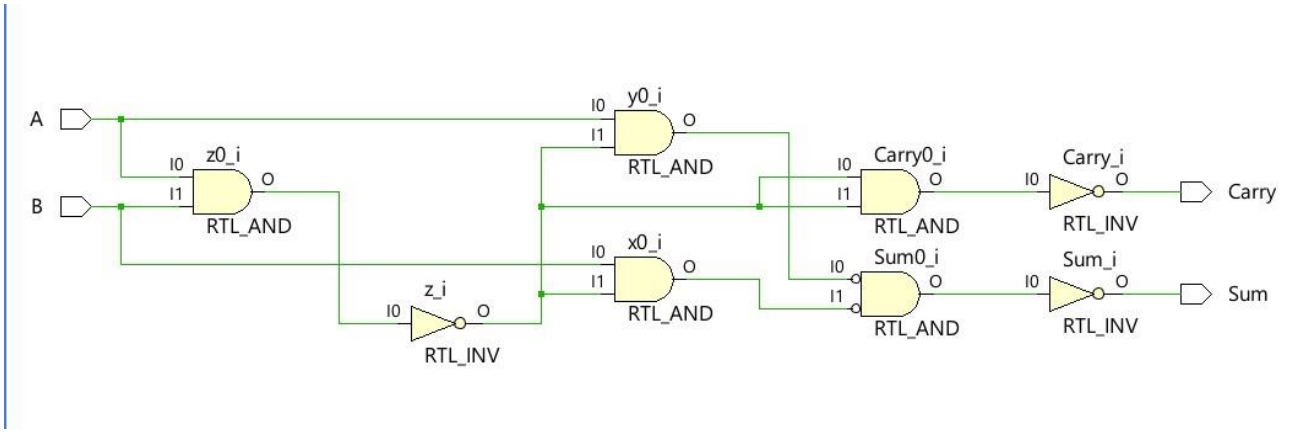


Half adder using NAND logic

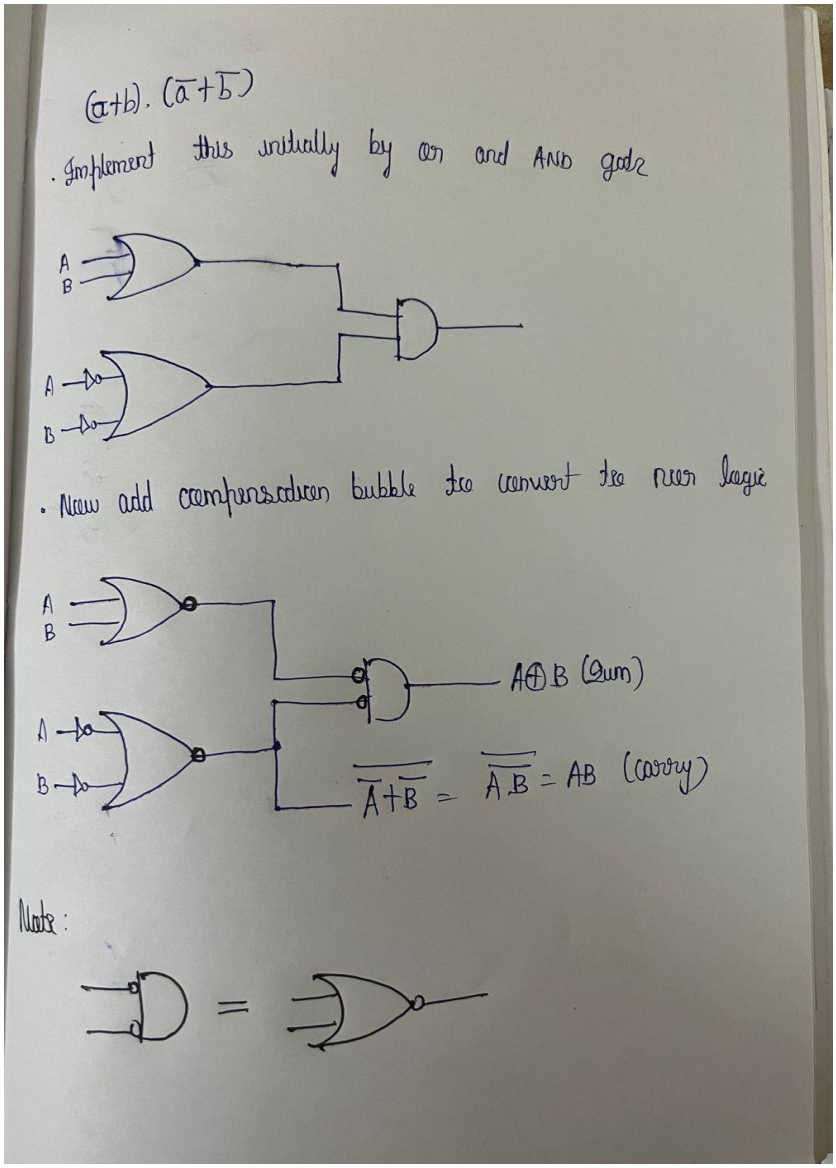
- The 4 nand gate in the top is the implementation of xor logic using nand gate and in order to reduce the number of gate required the carry is being taken as output of the first nand gate
- The Output



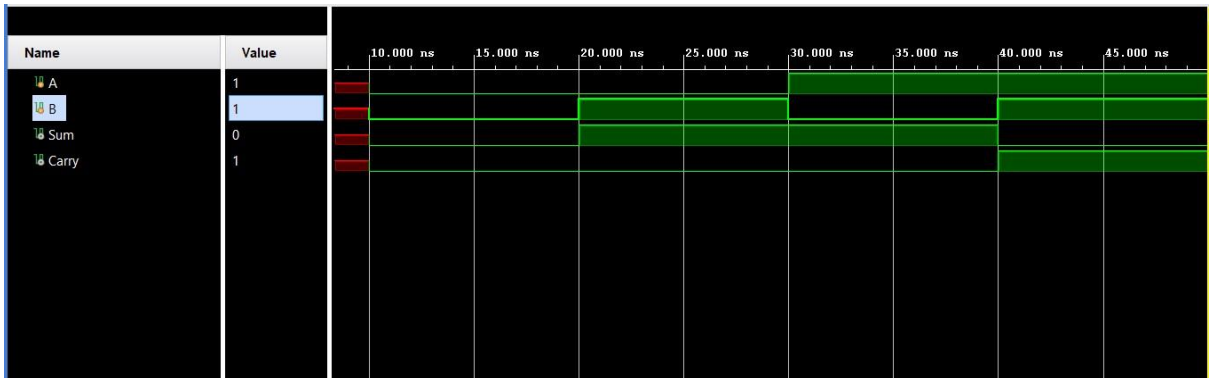
The Schematic



- **The same logic could be implemented by nor gates**
  - The logic require a slight modification in which the equation
  - A ⊕ B = A'B+AB' = (A+B).(A'+B')
- The equation could be implemented by



The output



The schematic