
VLSI PRACTICE DESIGN ACTIVITY-1

Output Screenshots:

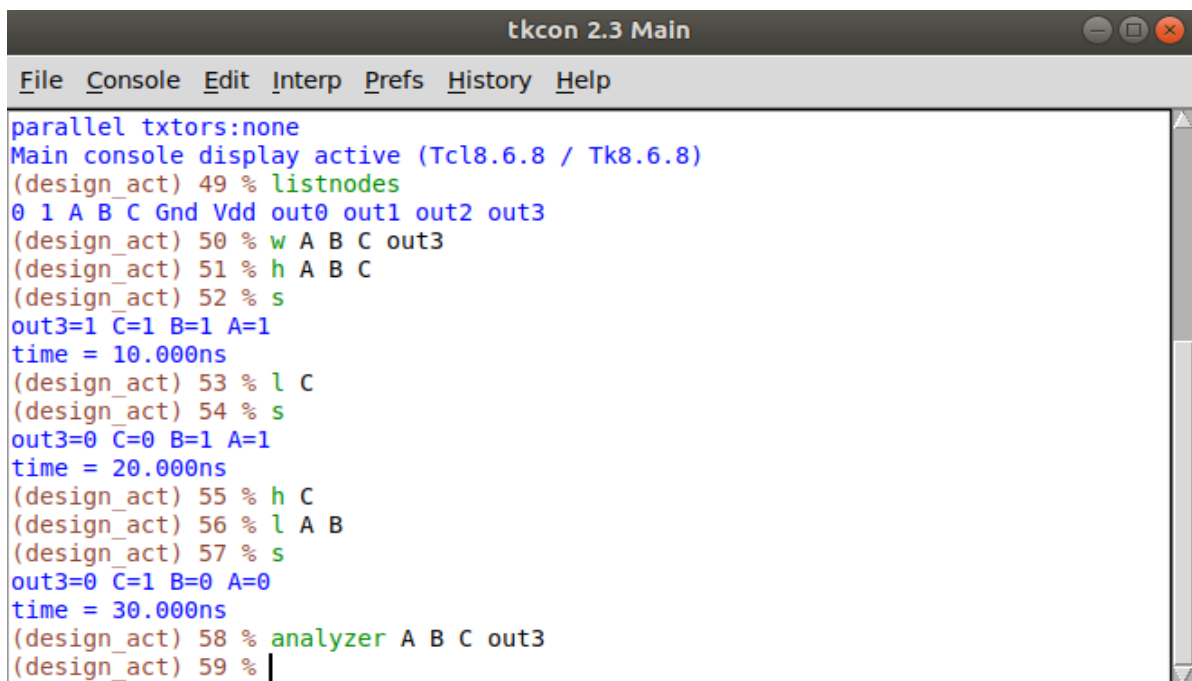
Sample 1:

Expression: $((A+B).C)$

Corresponding sim file is s.sim

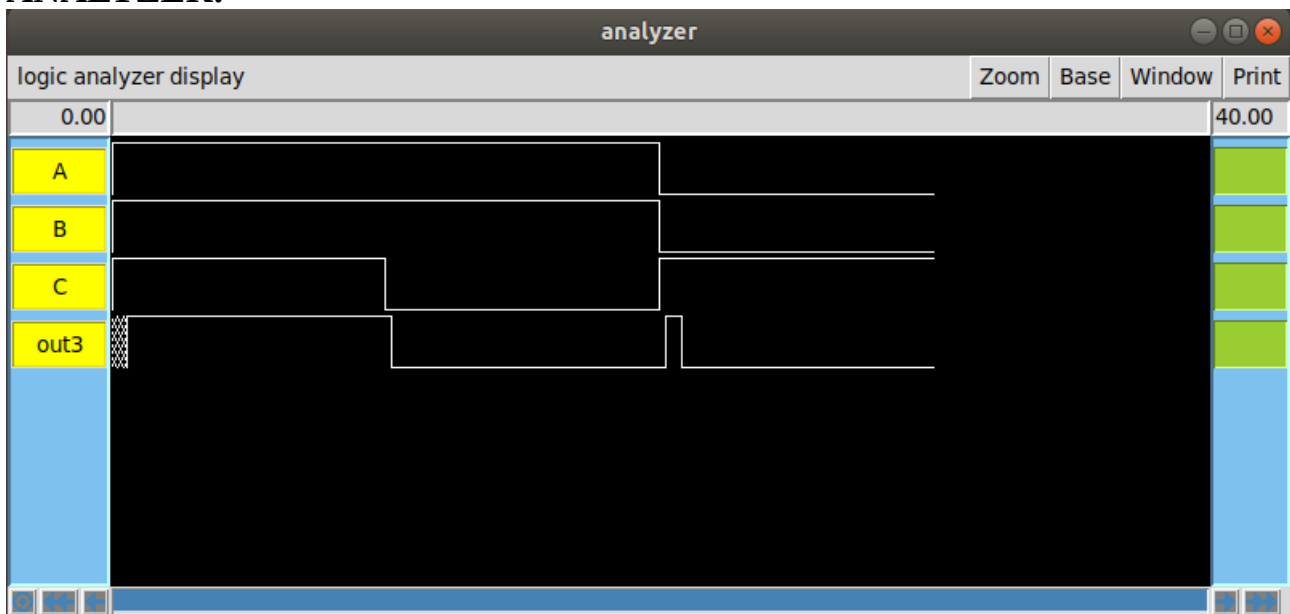
```
harish@harish-ubuntu:~/Desktop/vlsi/design_act$ python3 main.py
Enter expression : ((A+B).C)
Enter filename : s.sim
postfix expression is
['A', 'B', '+', 'C', '.']
your output is out3
sim file created successfully!
harish@harish-ubuntu:~/Desktop/vlsi/design_act$
```

IRSIM:



```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
parallel txtors:none
Main console display active (Tcl8.6.8 / Tk8.6.8)
(design_act) 49 % listnodes
0 1 A B C Gnd Vdd out0 out1 out2 out3
(design_act) 50 % w A B C out3
(design_act) 51 % h A B C
(design_act) 52 % s
out3=1 C=1 B=1 A=1
time = 10.000ns
(design_act) 53 % l C
(design_act) 54 % s
out3=0 C=0 B=1 A=1
time = 20.000ns
(design_act) 55 % h C
(design_act) 56 % l A B
(design_act) 57 % s
out3=0 C=1 B=0 A=0
time = 30.000ns
(design_act) 58 % analyzer A B C out3
(design_act) 59 %
```

ANALYZER:



Sample 2:

Expression: $!(A+B)$

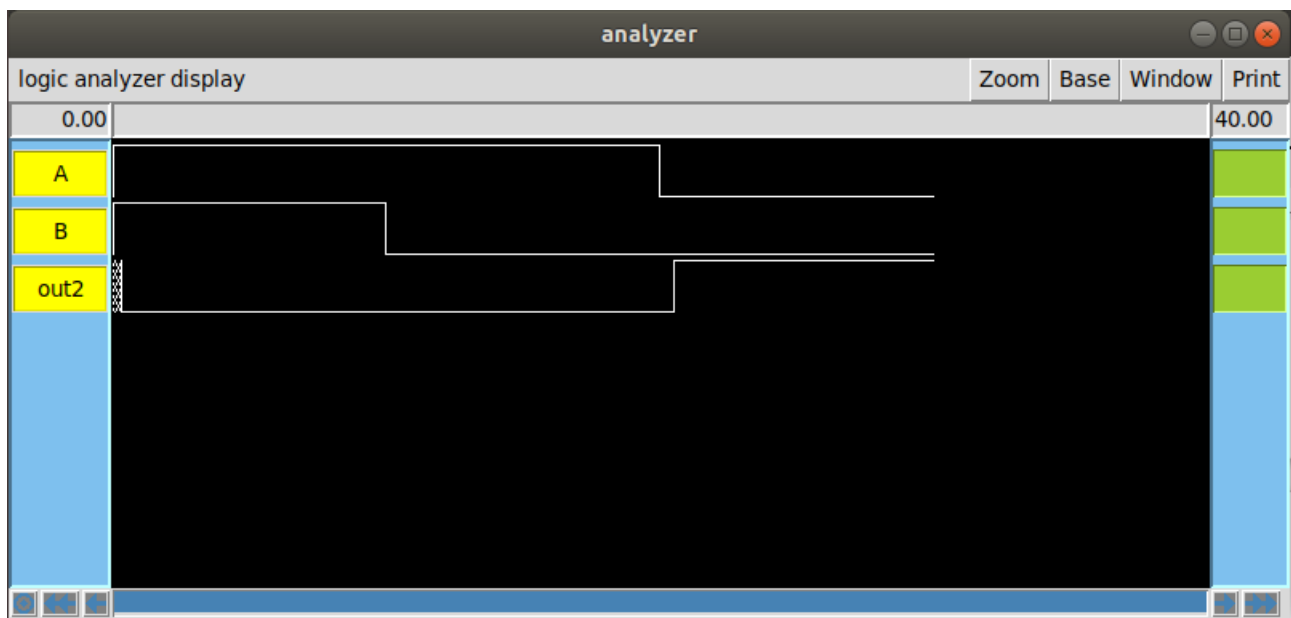
Corresponding sim file is s2.sim

```
harish@harish-ubuntu:~/Desktop/vlsi/design_act$ python3 main.py
Enter expression :  $!(A+B)$ 
Enter filename : s2.sim
postfix expression is
['A', 'B', '+', '!']
your output is out2
sim file created successfully!
```

IRSIM:

```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
8 nodes; transistors: n-channel=4 p-channel=4
parallel txtors:none
Main console display active (Tcl8.6.8 / Tk8.6.8)
(design_act) 49 % listnodes
0 A B Gnd Vdd out0 out1 out2
(design_act) 50 % h A B
(design_act) 51 % w A B out2
(design_act) 52 % s
out2=0 B=1 A=1
time = 10.000ns
(design_act) 53 % l B
(design_act) 54 % s
out2=0 B=0 A=1
time = 20.000ns
(design_act) 55 % l A
(design_act) 56 % s
out2=1 B=0 A=0
time = 30.000ns
(design_act) 57 % analyzer A B out2
(design_act) 58 %
```

ANALYZER:



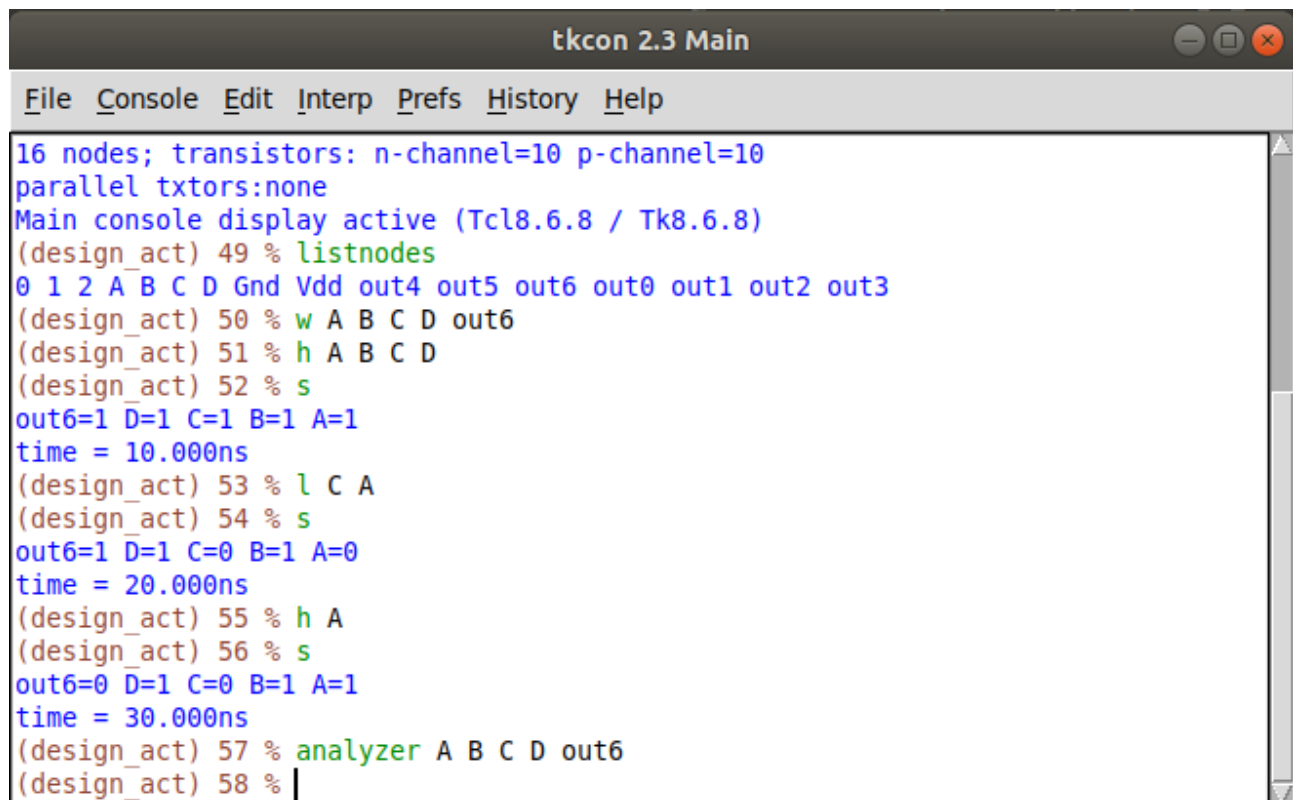
Sample 3:

Expression: $((!(A.B))+(C.D))$

Corresponding sim file is s3.sim

```
harish@harish-ubuntu:~/Desktop/vlsi/design_act$ python3 main.py
Enter expression : ((!(A.B))+(C.D))
Enter filename : s3.sim
postfix expression is
['A', 'B', '.', '!', 'C', 'D', '.', '+']
your output is out6
sim file created successfully!
```

IRSIM:

The screenshot shows a window titled "tkcon 2.3 Main" with a menu bar (File, Console, Edit, Interp, Prefs, History, Help). The console displays the following text:

```
16 nodes; transistors: n-channel=10 p-channel=10
parallel txtors:none
Main console display active (Tcl8.6.8 / Tk8.6.8)
(design_act) 49 % listnodes
0 1 2 A B C D Gnd Vdd out4 out5 out6 out0 out1 out2 out3
(design_act) 50 % w A B C D out6
(design_act) 51 % h A B C D
(design_act) 52 % s
out6=1 D=1 C=1 B=1 A=1
time = 10.000ns
(design_act) 53 % l C A
(design_act) 54 % s
out6=1 D=1 C=0 B=1 A=0
time = 20.000ns
(design_act) 55 % h A
(design_act) 56 % s
out6=0 D=1 C=0 B=1 A=1
time = 30.000ns
(design_act) 57 % analyzer A B C D out6
(design_act) 58 % |
```

ANALYZER:

