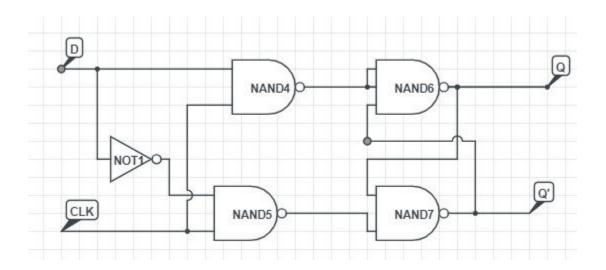
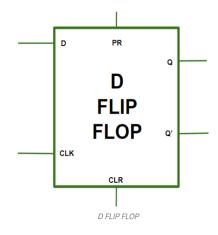
TASK 15: SIMULATE AND VERIFY A D-FLIP-FLOP



Schematic design of D-Flip-flop



Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Truth Table