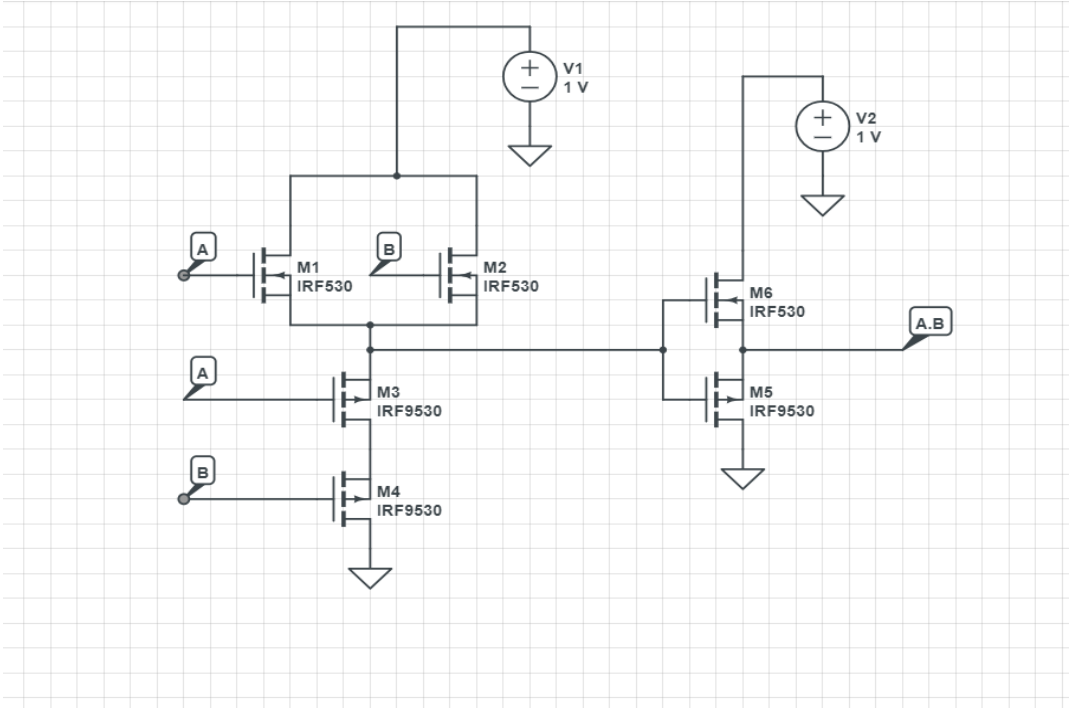
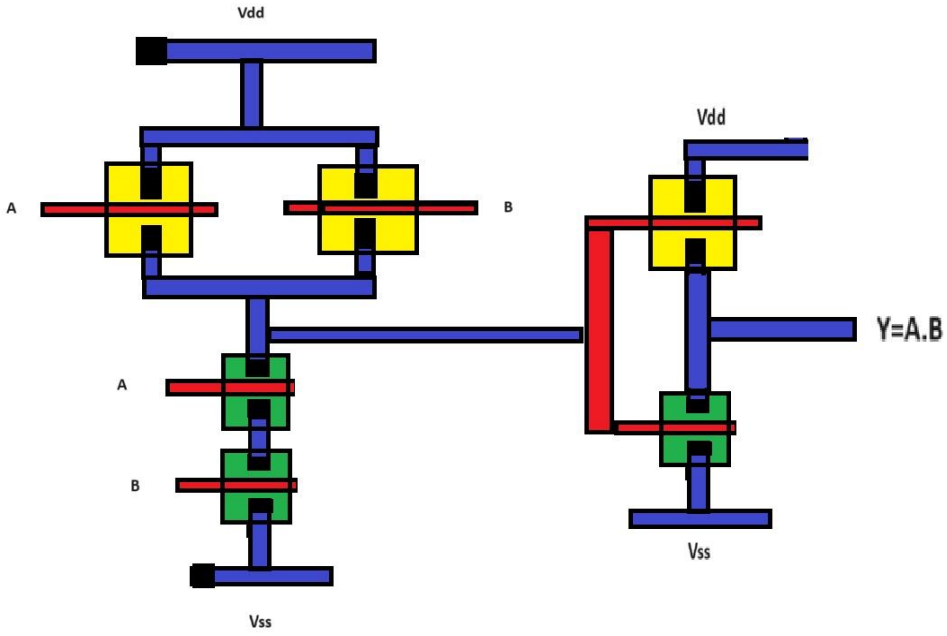
Team 5

Task_1: AND gate using CMOS circuit





Layout design