A Comparative Study on the Various Monolithic Low Noise Amplifier Circuit Topologies for RF and Microwave Applications

Beom Kyu Ko and Kwyro Lee

Abstract— **This paper critically compares the various monolithic low noise amplifier (LNA) circuit topologies using BiCMOS or MESFET technologies for RF and microwave applications. In addition to the conventional techniques, five newly proposed schemes for the simultaneous noise and input power matching are extensively compared with each other at microwave frequencies. At L-band, the best scheme is found to be the proposed cascode inductive series feedback (CCSF) or common-source inductive series feedback (CSSL) + common-gate inductive parallel feedback (CGPF) when 0.5 μm GaAs MESFET is used, while it is cascode resistive parallel feedback (CCPF) when npn BJT is used. At C- and X-bands, the proposed CGPF exhibits the best performance. Other than CGPF, the CSSL + CGPF seems to be the best at 6 GHz, and both CCPF + CGPF and CSSL + CGPF are recommended at 12 GHz. Finally, to verify the feasibility of this approach, a CCPF has been fabricated with 0.5 μm GaAs MMIC technology, of which measured results agree well with the simulated ones.**

I. Introduction

LOW noise amplifier (LNA) is one of the most important building blocks in the front end of the telecommunication system. It determines the noise figure and input voltage standing wave ratio (VSWR) of the overall system because the first block that a signal fed from antenna meets is LNA. So, in order to improve the noise figure and input VSWR of overall receiver system, an LNA is required to have the low noise figure, the high gain, and the low input VSWR, simultaneously.

When designing LNA's with common-source (CS) single-gate (SG) FET, it is well known that the noise matching for achieving the $NF_{\min}$ (minimum noise figure) has resulted in high input VSWR, and vice versa. This is because the $\Gamma_{\rm opt}$ (optimum noise match source reflection coefficient) is usually very different from the $G_{\max}$ (maximum available power gain match source reflection coefficient). So, some tradeoffs between the noise figure, the gain, and the input VSWR are needed.

If, however, we can make $\Gamma_{\rm opt}$ and $G_{\max}$ coincident, $NF_{\min}$ and maximum power gain and low VSWR can be achieved simultaneously. To achieve the aim, this paper proposes five new simultaneous noise and input power matching schemes. Then, based on the following viewpoints such as i) noise figure and/or noise measure, ii) gain, iii) stability, and iv) easiness of input/output power matching, five newly proposed schemes as well as the conventional techniques [1]–[3] are critically compared with each other using BiCMOS or MESFET technologies for RF and microwave applications. Our special emphasis is placed on the possibility of the simultaneous matching of optimum noise match and input power match points.

In Section II, five new LNA circuit topologies for the simultaneous noise and input power matching are introduced and explained. In Section III, they are compared with each others as well as the conventional ones. A test result is presented in Section IV, and concluding remarks are given in Section V.

Manuscript received October 10, 1995; revised February 12, 1996.

The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Yuseong-Gu, Taejeon, 305-701, Korea.

Publisher Item Identifier S 0018-9200(96)05688-0.

II. Concept of the Proposed LNA Circuits

A. CCPF

The first one is the cascode resistive parallel feedback (CCPF), whose schematic is shown in Fig. 1(a). This schematic utilizes the inherent advantages of the cascode such as higher gain, wider bandwidth, and gain-controllability, and of resistive parallel feedback, which allows us better linearity, better stability, and insensitivity against parameter variation. Besides that, most importantly, we can get the simultaneous noise and input power matching by judiciously choosing the feedback resistance and device dimension (W/L). This is illustrated in Fig. 2, which shows that $\Gamma_{\rm opt}$ and $G_{\max}$ points coincide with 1.5 kΩ feedback resistance and device dimension of 300 μm/0.5 μm. This is quite a unique characteristic that the cascode feedback has. The resistively parallel feedback topology with CS does not have this property. So, using the CCPF scheme, we can design LNA's which have high gain, very low input/output VSWR, and good stability.

However, the $NF_{\min}$ of CCPF is slightly increased compared with simple circuit topology such as CS with stabilization resistance at the drain node (see CSRL in Tables I–III). This is due to the noise added from both the feedback resistance and common-gate (CG) stage at high frequency (C- and X-bands), and mainly from the feedback resistance at low frequency (L-band). So, in order to reduce the $NF_{\min}$ of CCPF, we have to make the feedback resistance needed for matching much larger and/or the noise contribution from CG stage smaller by considering the interstage noise matching between CS and CG stages [4]. These result in the second and third schemes as will be illustrated below.

As for LNA's using npn bipolar junction transistors (BJT), in addition to the simultaneous noise and input power matching, we can make both $\Gamma_{\rm opt}$ and $G_{\max}$ points nearer to the 50 Ω point with the proper choice of emitter dimension, which is shown in Fig. 3. The $NF_{\min}$ of CCPF is almost same as that of common-emitter (CE) topology (see Table IV). This is due

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED MATCHING TECHNIQUES WITH OTHER CONVENTIONAL ONES USING 0.5 μm × 300 μm GaAs MESFET AT 2 GHz

Topologies	K	MAG (dB)	NFmin (dB)	Rn	Mmin	Input VSWR*
CS	0.133	17.343	0.570	0.850	0.144	--
CSRL (10Ω)	1.048	15.998	1.313	2.855	0.420	23.20
CSSL (4nH)	1.004	12.625	0.543	0.686	0.144	3.35
CSSF (4.2nH & 600Ω)	1.273	9.699	0.668	0.810	0.187	1.54
CG	0.963	9.370	0.526	0.675	--	--
CGPF (75nH)	1.005	9.106	0.516	0.673	0.144	1.36
cascode	0.099	26.711	0.626	0.868	--	--
CCSF (2.4nH & 1.2kΩ)	2.361	17.662	0.661	0.792	**0.166**	1.84
CCPF (2kΩ)	1.077	15.808	1.478	0.912	0.417	1.31
CCPF+CGPF (2kΩ & 75nH)	1.082	15.655	1.477	0.911	0.417	1.33
CSSL+CGPF (2nH & 10nH)	1.599	17.472	0.610	0.770	**0.154**	1.45

* Input VSWR with the input noise-matched and the output gain-matched.

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED MATCHING TECHNIQUES WITH OTHER CONVENTIONAL ONES USING 0.5 μm × 300 μm GaAs MESFET AT 6 GHz

Topologies	K	MAG (dB)	NFmin (dB)	Rn	Mmin	Input VSWR*
CS	0.274	12.604	0.870	0.870	0.244	--
CSRL (20Ω)	1.032	11.511	1.652	1.845	0.613	11.80
CSSL (0.6nH)	1.018	10.712	0.836	0.600	0.244	3.80
CSSF (0.6nH & 100Ω)	2.500	4.725	1.538	0.837	0.649	1.36
CG	0.741	8.251	0.921	0.716	--	--
CGPF (7.5nH)	1.013	8.797	0.831	0.702	**0.244**	1.36
cascode	0.070	20.856	1.284	0.966	--	--
CCSF (0.6nH & 400Ω)	3.895	10.938	1.651	0.738	0.504	1.36
CCPF (1.7kΩ)	1.074	15.313	2.047	1.019	0.621	1.45
CCPF+CGPF (1.8kΩ & 7.5nH)	1.185	13.903	1.986	1.010	0.605	1.42
CSSL+CGPF (0.6nH & 6nH)	2.287	14.527	1.375	0.658	**0.387**	1.84

* Input VSWR with the input noise-matched and the output gain-matched.

to the large G_m (transconductance) of BJT and much larger feedback resistance needed for the simultaneous matching. Therefore, CCPF is very suitable for LNA design using BJT at L-band.

B. CGPF

The second one we propose is the common-gate inductive parallel feedback (CGPF), whose schematic is shown in Fig. 1(b). It is usually known that CG has larger $NF_{\min}$ and smaller gain and worse stability than CS. However, we found that the inductive parallel feedback makes the $NF_{\min}$ smaller and the gain larger with unconditional stability. The role of the inductive parallel feedback is to cancel the $C_{\rm ds}$ (drain-to-source capacitance). In addition, we can make $G_{\max}$ much closer to $\Gamma_{\rm opt}$ as shown in Fig. 4. The needed inductance value is approximately given by

$$L_{fb} \cong 1/(\omega^2 C_{\rm ds}) \tag{1}$$

where ω is the angular frequency. Therefore, this technique is more practicable as the frequency increases and as the device width increases, in order for the needed inductance to be realizable with current monolithic technology. The $R_{\rm n}$ (normalized noise resistance) of CGPF is smaller than CS,

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED MATCHING TECHNIQUES WITH OTHER CONVENTIONAL ONES USING 0.5 μm × 300 μm GaAs MESFET AT 12 GHz

Topologies	K	MAG (dB)	NFmin (dB)	Rn	Mmin	Input VSWR*
CS	0.496	9.780	1.320	0.730	0.437	--
CSRL (50Ω)	1.083	8.023	1.974	1.077	0.878	6.80
CSSL (0.25nH)	1.031	8.420	1.313	0.394	0.437	3.10
CSSF (0.25nH & 150Ω)	1.962	3.869	1.967	0.497	0.979	1.24
CG	0.438	6.401	1.722	0.686	--	--
CGPF (1.85nH)	1.020	8.721	1.386	0.634	**0.437**	1.45
cascode	-0.287	16.180	2.643	1.051	--	--
CCSF (0.25nH & 300Ω)	2.688	8.744	3.592	0.669	1.490	1.36
CCPF (R_{fb}=700Ω & R_L=600Ω)	1.324	9.576	3.812	1.213	1.580	1.00
CCPF+CGPF (1.8kΩ & 1.85nH)	1.576	11.236	2.928	1.053	**1.043**	1.36
CSSL+CGPF (0.2nH & 1.4nH)	5.078	9.092	2.862	0.560	**1.071**	1.54

* Input VSWR with the input noise-matched and the output gain-matched.

TABLE IV
PERFORMANCE COMPARISON OF THE PROPOSED MATCHING TECHNIQUES WITH OTHER CONVENTIONAL ONES USING SILICON npn BJT WITH EMITTER AREA 20 μm × 6 μm FROM 0.8 μm BiCMOS PROCESS AT 1 GHz

Topologies	K	MAG (dB)	NFmin (dB)	Rn	Mmin	Input VSWR*
CE	0.408	18.908	2.550	0.500	0.817	--
CERL (60Ω)	1.001	18.722	2.609	0.512	0.864	11.80
CESL (1.3nH)	1.003	15.700	2.509	0.445	0.817	4.10
CESF (1.6nH & 200Ω)	1.439	11.500	2.564	0.451	0.868	1.45
CB	0.215	16.977	2.614	0.501	--	--
cascode	-1.351	35.885	2.628	0.505	--	--
CCSF (1nH & 600Ω)	6.045	22.991	2.648	0.470	0.844	1.54
CCPF (R_{fb}=4kΩ & R_L=1.7kΩ)	1.107	27.227	2.722	0.506	**0.873**	1.24
CESL+CBPL (0.8nH & 5nH)	2.795	18.795	2.609	0.472	0.835	1.24

* Input VSWR with the input noise-matched and the output gain-matched.

which means that the radii of constant noise figure circles of CGPF are broader. This CGPF gives us the best noise measure performance with the simultaneous noise and input power matching and unconditional stability at all microwave frequencies (see Tables I–III). However, the manufacturability is a concern for this topology due to the relatively large C_{ds} fluctuation, and the output power matching is rather difficult due to the large output impedance.

C. CCPF + CGPF

Combining the advantages provided from CGPF and CCPF, we obtain the third one, i.e., the cascode resistive parallel feedback with common-gate inductive parallel feedback (CCPF + CGPF). Compared with CCPF, this technique becomes very useful at a higher frequency (X-band) because CGPF can reduce drastically the noise contribution from the CG stage which becomes larger as the frequency increases. In addition to the reduction of $NF_{\min}$ of the CG stage, the local inductive parallel feedback makes it possible to use much larger feedback resistance for simultaneous matching as shown in Table III. Note that the $M_{\min}$ of CCPF + CGPF is much lower than that of CCPF alone at 12 GHz. Another advantage is that the performances of CCPF + CGPF are not sensitive to the variation of the parallel inductance, while that of CGPF is.

D. CCSF

The fourth one is the cascode inductive series feedback (CCSF). It is reported that the simultaneous matching of Γ_{opt}

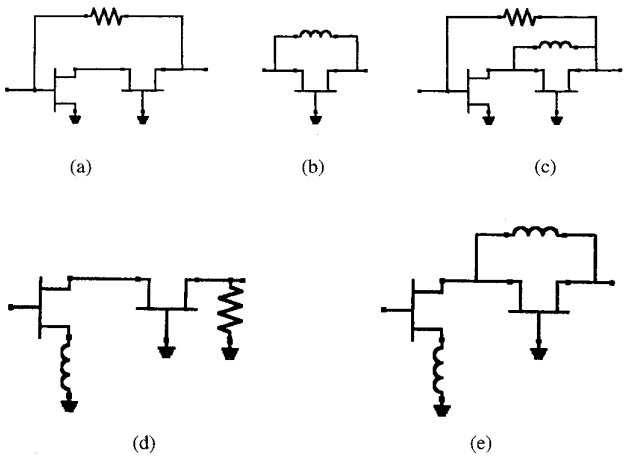

Fig. 1. The ac schematics of the newly proposed simultaneous noise and input power matching techniques for monolithic LNA's. (a) Cascode resistive parallel feedback (CCPF). (b) Common-gate inductive parallel feedback (CGPF). (c) Cascode resistive parallel feedback with common-gate inductive parallel feedback (CCPF + CGPF). (d) Cascode inductive series feedback (CCSF). (e) Common-source inductive series feedback and common-gate inductive parallel feedback (CSSL + CGPF).

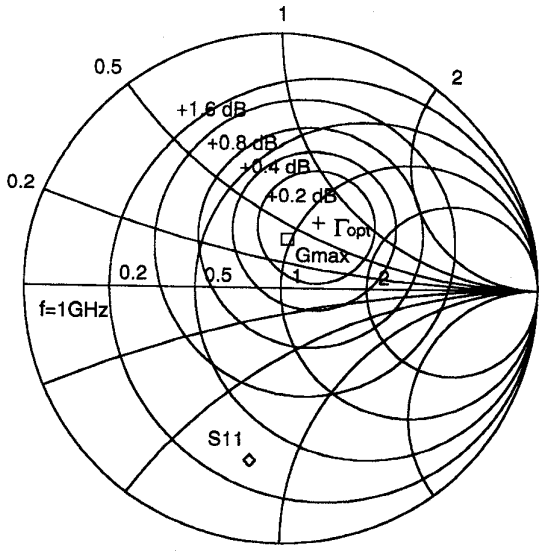

Fig. 3. Constant noise figure circles and $G_{\max}$ of cascode resistive parallel feedback (CCPF) for 4 kΩ feedback resistor and 1.7 kΩ load resistor at 1 GHz. The device is npn BJT with emitter area 20 μm × 6 μm from 0.8 μm BiCMOS process.

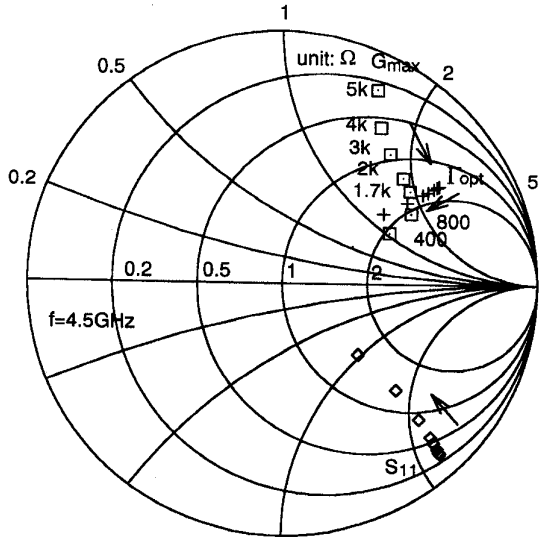

Fig. 2. Impedance mapping of $\Gamma_{\rm opt}, G_{\max}$, and S_{11} of CCPF versus the feedback resistance at 4.5 GHz (solid line: impedance chart, dashed line: admittance chart). The device is 0.5 μm × 300 μm GaAs MESFET. Note that the simultaneous noise and input power matching is obtained with 1.5 kΩ feedback resistance.

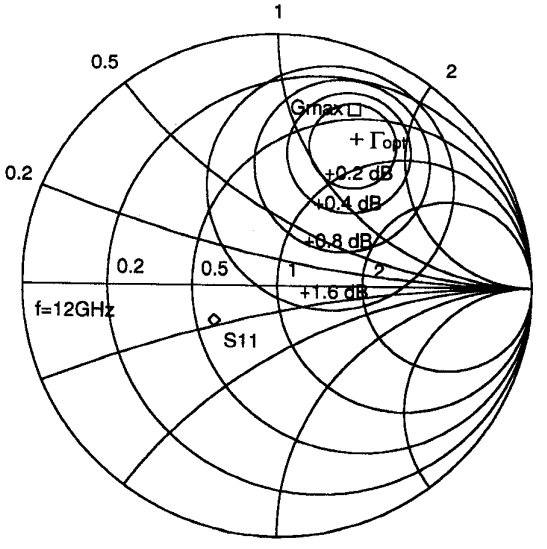

Fig. 4. Impedance mapping of $\Gamma_{\rm opt}, G_{\max}$, and S_{11} of common-gate inductive parallel feedback (CGPF) versus the feedback inductance at 6 GHz. The device is 0.5 μm × 300 μm GaAs MESFET.

and S_{11}^* instead of $G_{\max}$ can be obtained with the inductive series feedback and proper loading using CS topology [3]. However, the gain becomes considerably low due to the series feedback and small loading impedance, and bad output VSWR is inevitable. Furthermore, as the frequency increases, $G_{\max}$ point becomes much different from S_{11}^* due to S_{12}. The cascode solves these problems because the gain of cascode is much larger than that of CS, and the output loading does not affect the input matching due to much smaller S_{12} of cascode. Note that the $M_{\min}$ of CCSF is lower than that of CSSF (CS with inductive series feedback and load resistance) at 2 and 6 GHz, and it is not at 12 GHz (see CSSF in Table I–III). This is because the noise added from the CG stage becomes larger as the frequency increases. To reduce it, the fifth one is introduced as will be explained below. The moving of $\Gamma_{\rm opt}$ and $G_{\max}$ with the series feedback inductance is shown in Fig. 5. The simultaneous noise and input power matching is obtained with 0.8 nH series feedback inductance and 400 Ω load resistance.

E. CSSL + CGPF

The fifth one is the combination of CS inductive series feedback and CG inductive parallel feedback (CSSL + CGPF).

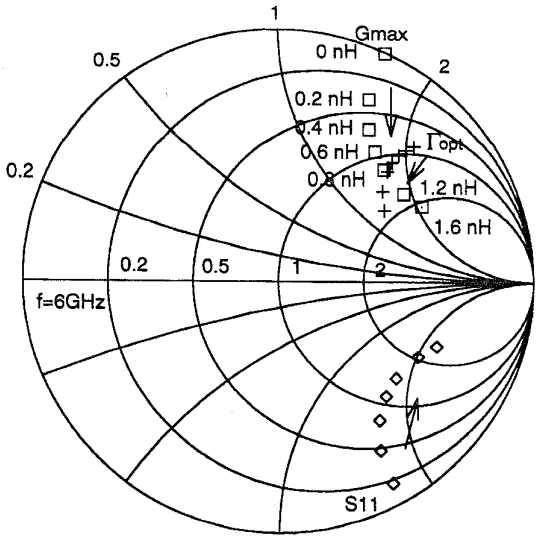

Fig. 5. Impedance mapping of $\Gamma_{\rm opt}$, $G_{\rm max}$, and S_{11} of cascode inductive series feedback (CCSF) versus the feedback inductance at 6 GHz. The load resistance is 400 Ω. The device is 0.5 μm × 300 μm GaAs MESFET. Note that the simultaneous noise and input power matching is obtained with 0.8 nH series feedback.

This scheme utilizes the merits of both inductive series feedback and CG inductive parallel feedback. In other words, the simultaneous noise and input power matching is obtained by inductive series feedback, and both the minimization of noise added from the CG stage and good stability are obtained by inductive parallel feedback. The $M_{\rm min}$ performance of this scheme is very good at all microwave ranges as shown in Tables I–IV. Another advantage is that the performances of CSSL + CGPF are not sensitive to the variation of the parallel inductance, while that of CGPF is. The disadvantage of this scheme, however, is that it requires two inductors, which increases the chip size appreciably.

III. Performance Comparison

We compare the five design schemes as well as the conventional ones using EEsof's Libra™ to find what kind of topology is most suitable for given frequency band, i.e., L- (2 GHz), C- (6 GHz), and X- (1 2GHz) bands. The used active devices are silicon npn BJT with emitter area 20 μm × 6 μm from 0.8 μm BiCMOS process and 0.5 μm × 300 μm GaAs MESFET from SMS foundry [5]. The collect current of BJT is 6 mA and that of MESFET is 18 mA (20% I_{dss}). The cutoff frequency f_T is approximately 10 GHz for BJT and 24 GHz for MESFET. The simulation results for the K (stability factor), the MAG (maximum available power gain), the $NF_{\rm min}$ (minimum noise figure), the $R_{\rm n}$ (normalized noise resistance), the $M_{\rm min}$ (minimum noise measure) [3], and the input VSWR with the input noise-matched and the output gain-matched are given in Tables I–IV, respectively.

The unconditional stability of an amplifier is guaranteed by the condition of $K > 1$ and $B_1 > 0$ [6]. As the B_1 values of all the topologies which have $K > 1$ are larger than zero, we have omitted it in Tables I–IV for simplicity. The $M_{\rm min}$ is given by

$$M_{\rm min} = \frac{F_{\rm min} - 1}{1 - 1/G_A} \tag{2}$$

where $F_{\rm min}$ is the minimum noise factor and G_A is the magnitude of maximum available power gain with input noise-matched [3]. It has been known that the $M_{\rm min}$ is invariant to the addition of lossless feedback [3].

A. L-Band Application

Among those of which VSWR's are less than two (return loss of 9.5 dB) in Table I, the topology that has the lowest $M_{\rm min}$ is CGPF. But, the required inductance is 75 nH, which is too large to be realized with monolithic form. The next best candidates are CSSL + CGPF and CCSF, which also show similar $M_{\rm min}$ performance. Considering the bandwidth, stability, and insensitivity against parameter variation, however, CCPF and CCPF + CGPF are also good techniques even though they have a little larger $NF_{\rm min}$. Overall, CSSL + CGPF and CCSF seem to be the best choice at 2 GHz when 0.5 μm MESFET is used. As for LNA's using npn BJT, the $M_{\rm min}$ of CCPF is almost the same as others because the increase of $NF_{\rm min}$ is very negligible due to much larger gain of CE stage and larger feedback resistance (see Table IV). In addition, the $\Gamma_{\rm opt}$ and $G_{\rm max}$ points are close to 50 Ω, which was shown in Fig. 3. Therefore, the CCPF seems to be the best one for L-band application using silicon npn BJT.

B. C and X-Band Applications

Among those of which VSWR's are less than two in Tables II and III, the topology that has the lowest $M_{\rm min}$ is also CGPF. The needed inductance values are 7.5 nH and 1.85 nH for 6 and 12 GHz, respectively, which are quite realizable with monolithic form. The CSSL + CGPF, CCSF, CCPF, and CCPF + CGPF exhibit reasonably good noise measure performance with unconditional stability and manufacturability. Particularly, at X-band, among those which use cascode scheme, CCPF + CGPF and CSSL + CGPF shows much better noise measure performance than CCSF and CCPF. This means that the common-gate inductive parallel feedback plays an important role in enhancing the noise measure performance at higher frequencies.

Conclusively, if the proper uniformity in the values of $C_{\rm ds}$ and feedback inductance is maintained, the topology which has the best $M_{\rm min}$ performance with the simultaneous noise and input power matching and unconditional stability at 6 and 12 GHz is CGPF. Other than CGPF, the CSSL + CGPF seems to be the best at 6 GHz, and both CCPF + CGPF and CSSL + CGPF are recommended at 12 GHz. This is because the noise performance is not sensitive to the variation of feedback inductance in both CCPF + CGPF and CSSL + CGPF, while it is sensitive in CGPF.

IV. Test Result

In order to show the usefulness of our approach, a CCPF LNA has been fabricated using 0.5 μm GaAs MESFET

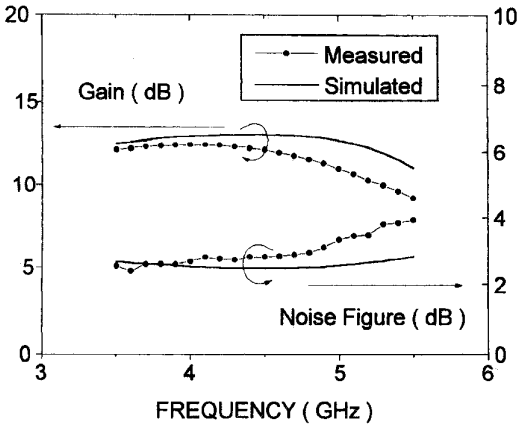

Fig. 6. Plot of measured versus simulated performance of the noise figure and the gain of the fabricated CCPF LNA.

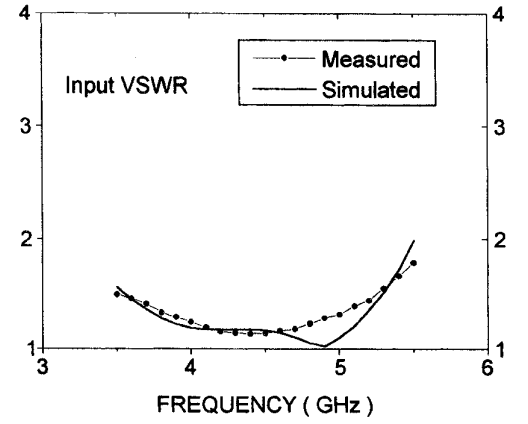

Fig. 7. Plot of measured versus simulated performance of the input VSWR of the fabricated CCPF LNA.

technology. The experimental results are compared with the simulation ones in Figs. 6–8, which experimentally verifies that the simultaneous noise and input/output power matching is feasible.

V. Conclusion

We critically compared the various monolithic LNA circuit topologies using BiCMOS or MESFET technologies for RF and microwave applications, based on the following viewpoints: i) noise figure and/or noise measure, ii) gain, iii) stability, and iv) ease of input/output power matching. In addition to the conventional techniques, five newly proposed schemes for the simultaneous noise and input power matching have been extensively compared with each other at microwave frequencies. Our special emphasis has been placed on the possibility of the simultaneous matching of optimum noise match and input power match points. Finally, to verify the feasibility of this approach, a CCPF has been fabricated with 0.5 μm GaAs MMIC technology, of which measured results agree well with the simulated ones.

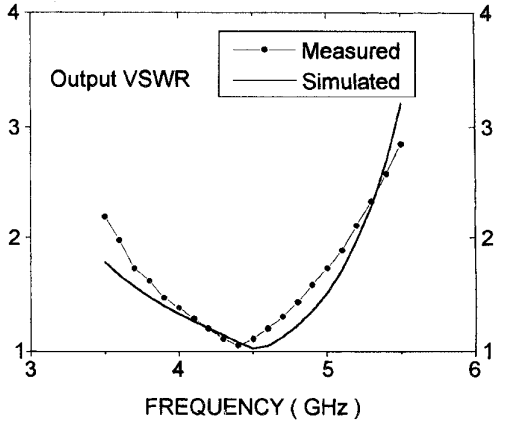

Fig. 8. Plot of measured versus simulated performance of the output VSWR of the fabricated CCPF LNA.

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