2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications

A 75dB-gain Low-power, Low-noise Amplifier for Low-frequency Bio-signal Recording

Dalila Salhi
Division microélectronique & nanotechnologie (DMN)
Centre de développement des technologies avancées CDTA
Algiers, Algeria
dsalhi@cdta.dz

Balwant Godara
Systems for Telecom & Radiocom research team (STAR)
Institut Supérieur d'Electronique de Paris
Paris, France
balwant.godara@isep.fr

Abstract— **This paper presents a low voltage, low noise and very low frequency amplifier suitable for bio-signal recording. The amplifier requires only ± 0.6V supply and consumes 1.24µW, with a 75.5 dB gain over a bandwidth covering a range of frequencies from some hundreds of mHz to 19kHz. A UMC 0.13µm CMOS process is used in design and simulation. The new solution is suitable for a variety of biomedical applications.**

Keywords- analog design, bio-amplifier, biomedical application, bio-signals, , low frequency, low-noise, low-power, OTA.

I. INTRODUCTION

The electronics circuitry of general biomedical implantable devices like pacemakers, cochlear implants, neural prostheses …etc, consists of battery for energy delivery, signal acquisition and signal processing blocks, analog-to-digital conversion block, and also communication subsystems block (figure 1). Each of these blocks must be designed to meet strict constraints that make them more and more sophisticated and efficient. These constraints generally concern reliability, robustness, precision and low power consumption [1].

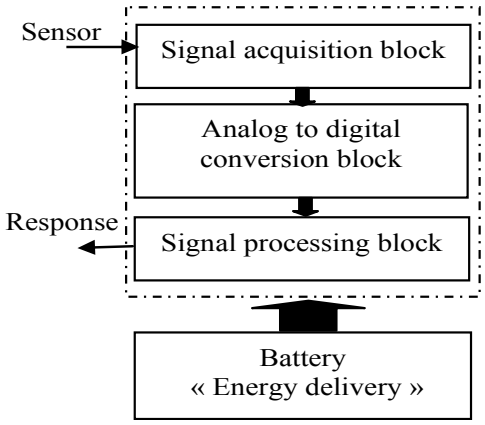

Figure 1. Electronics circuitry of general biomedical implantable devices

Implantable devices are battery-operated systems used to monitor human body all the day (case of pacemakers for example). These batteries are in general lithium-iodine based batteries and deliver 2.8V [2]. Thus, patients using this kind of device need a surgical procedure to replace the batteries of their implant every four or five years [3]. This procedure can be very dangerous, especially for old patients. So, the need for minimizing power consumption is arising in order to extend the device life time. This crucial requirement is taken into account in the design of each one of the blocks that constitute the device.

Signal acquisition represents the most important block in such devices, because of its critical position in the hierarchical order. It provides the interface between the sensor and the signal processing block. Here, the front-end element and the important signal conditioning one is the operational transconductance amplifier (OTA). Its main role is to enhance the level of very low bio-potentials coming from sophisticated sensors based on MEMS technology [4]. The OTA must provide a high quality of function responding to each biomedical application. These requirements depend on the kind of bio-signals to be processed. However, today, a great interest is given to designing universal amplifiers able to cover all kinds of bio-signals.

The signals to condition in the amplification stage are very particular signals like EEG, ECG, EMG, etc, because of their weak amplitude [~ µV to ~ mV] and their very low range of frequency [~ mHz to ~ hundred of Hz] [3][5]. Consequently, amplifiers used in this case are required to present high gain, acceptable bandwidth, good stability with low power consumption and low noise. This kind of application, which is in the heart of this work, presents an interesting subject of several works where many challenges are raised, especially in low-power and low-noise design of very low frequency amplifiers like in [6] and in [7].

This paper reports on the design and simulation of a fully integrated amplifier suitable for bio-signal recording from some hundred of millihertz to some tens of kilohertz and presents a 75dB gain with low power consumption. The article is composed of the description of the architecture of the proposed amplifier, and the simulation results. In the last section, we present a comparison of this new solution with existing ones. We end with a summary of the results and the conclusion.

978-0-7695-3978-2/10 $26.00 © 2010 IEEE
DOI 10.1109/DELTA.2010.20

II. THE NEW BIO-AMPLIFIER DESIGN

The amplifier proposed in this work is inspired from [8]. The original architecture is modified in order to obtain an amplifier able to process a broad range of bio signals included in a wide frequency band with an acceptable gain and as low noise as possible. The schematic is provided in figure 2.

This amplifier is composed of: the pMOS differential input stage (M1-M2), the pMOS amplification circuit (M7-M8), the nMOS supply stage (M9-M10), and the nMOS current mirror (M3-M6) as the first amplification stage. It must amplify a typical signal of the order of 0.1mV. The main idea in our work is to dimension each one of these transistors in order to obtain the required performance for the amplification of bio signals, and to decrease the noise, especially the Flicker noise (also known as the 1/f noise) which dominates at low frequencies. Sizing these transistors is not an easy task because it is critical to achieve a low noise at a low current level with maintaining the high gain.

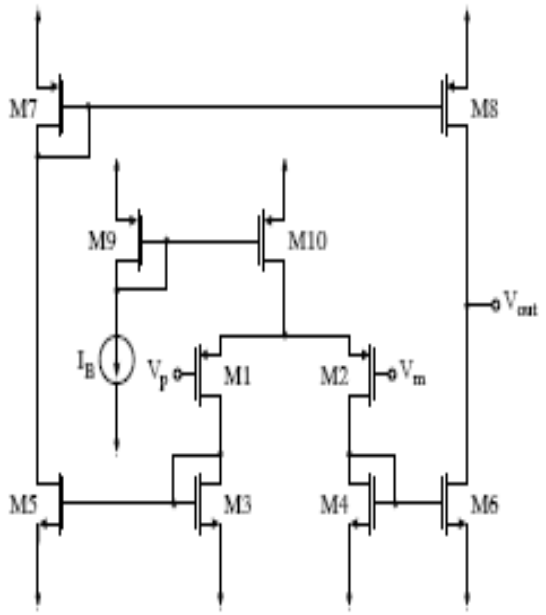

Figure 2. Schematic of the new amplifier.

It is important to note that the origin of Flicker noise is not well identified until now and lot of techniques are studied, proposed and used to minimize the effect of this noise. Generally, a practical technique is used, consisting of the use of pMOS transistors as input stage with large gate areas [8][9]. We adjust the width-to-length (W/L) ratios of both M1and M2 to obtain an optimum gate area allowing the minimization of the 1/f noise.

This design respects the low-consumption requirement because here, only 1.2V power supply is used and only 1.24µW is consumed. Also, the current used to polarise the transistors in this architecture is 2µA.

III. SIMULATIONS & RESULTS

The amplifier was designed using the transistor parameters of a UMC 0.13µm CMOS technology. The simulations were done in the Cadence Analogue design environment.

The new bio-amplifier achieves a 75.47dB gain with very good phase stability. Its -3dB bandwidth goes from 100mHz to 18.8kHz. The gain profile is shown in figure 3. We use a load of 10pF to limit the bandwidth of this design.

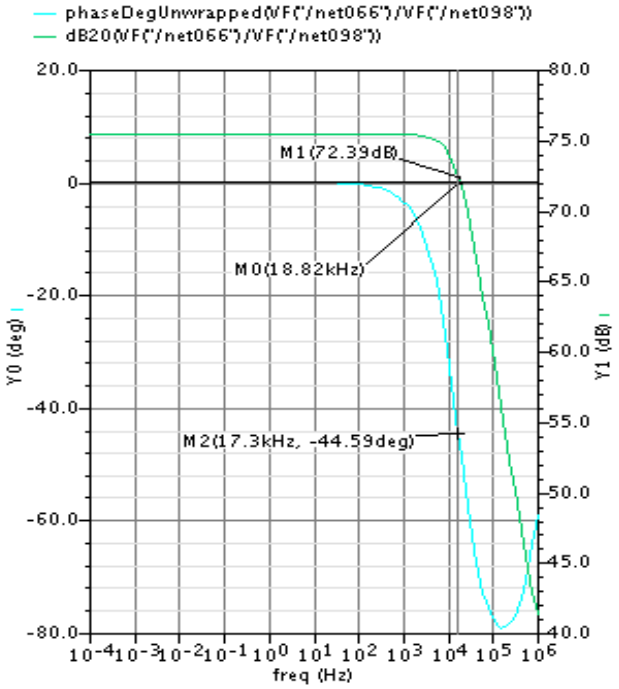

Figure 3. Gain and phase profile of the new amplifier

Table 1 presents the W/L ratios of all the transistors of the proposed amplifier, where M1 and M2 are drawn with optimum gate area, while M3 to M6 are drawn extremely narrow and long in order to achieve the previous trade-off between the low noise and the best gain.

TABLE I. TRANSISTOR DIMENSIONS

Transistor number	W/L (µm)
M1,M2	520 / 2.6
M3, M4, M5, M6	0.39 / 26
M7, M8	2.6 / 39
M9, M10	10 / 10

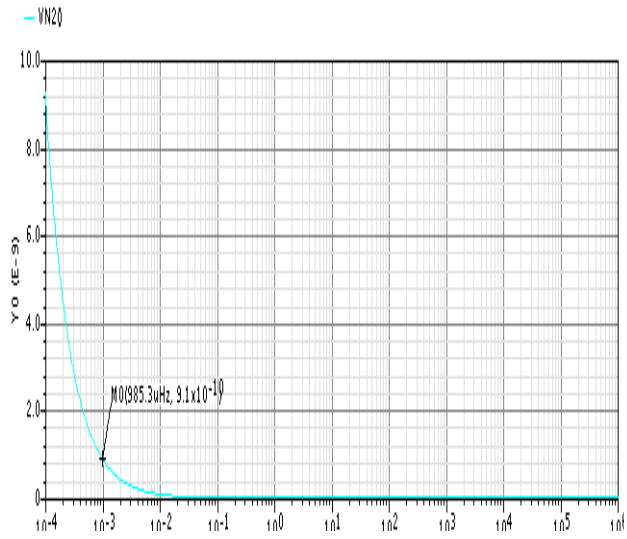

Figure 4. Output-reffered noise response

TABLE II. SIMULATION RESULTS OF THE NEW AMPLIFIER AND COMPARISON WITH STATE OF THE ART

	This work	**[7]**	**[8]**
Supply voltage	± 0.6V	±2.5V	±2.5V
Supply current	2µA	18µA	16µA
Gain	75.47 dB	70 dB	40 dB
Bandwidth	18.8 kHz	2kHz	9 kHz
Output Noise	<0.91nV^2/Hz (1mHz)	123.6µVrms	2.1µVrms
Power consumption	1.24µW	180µW	80 µW
Technology	0.13µm CMOS	0.5µm CMOS	1.5µm CMOS

As far as noise is concerned, the Cadence simulations showed that the output noise presents a very low value over the entire bandwidth. The noise profile of the amplifier is shown in figure 4. On this profile, at 1mHz frequency, the output referred noise is of 0.91nV2/Hz, and it is even lower over the bandwidth from 1mHz to 18.8kHz.

Table II summarizes the simulation results of the proposed amplifier. It also gives a comparison of these results with other recent solutions for biomedical applications. For example applications referenced in [7] and [8], where the bio signal aimed to be processed is the neural activity signals, in these applications different architectures are proposed and different technologies are used to design, simulate and also fabricate the amplifier. The results given are good. However, our work Clearly presents superior results in terms of the best gain 75dB, the supply voltage (± 0.6V vs ±2.5V), the biasing current (2µA vs 18µA and 16µA), the power consumption (1.24µW vs 80µW and 180µW), the bandwidth (18.8kHz vs 9kHz and 2kHz) and the output referred noise.

IV. CONCLUSION

In this paper, we proposed a new architecture for a bio-amplifier, and its simulated performance. The novel amplifier presents a very high gain (75.5dB) at an extremely low consumption (1.24µW, over a ±0.6V supply). The wide bandwidth (up to 18.8kHz) makes this amplifier suitable for several low-power biomedical applications.

REFERENCES

[1] A.P. Chandrakasan, N. Verma and D.C. Daly; "Ultralow-Power Electronics for Biomedical Applications**";** Annual Review of Biomedical Engineering"; Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, Vol. 10; pp. 247-274**.** August 2008.

[2] V. S. Mallela, V. Ilankumaran, and N. S. Rao; "Trends in Cardiac Pacemaker Batteries"; Indian Pacing Electrophysiol. J.; 4(4); pp. : 201–212. Oct. – Dec. 2004.

[3] A. Arnaud and C. Galup-Montoro; "Fully integrated signal conditioning of an accelerometer for implantable pacemakers"; Analog Integrated Circuits and Signal Processing journal; Kluwer Publications; Vol. 49; pp. 313–321.

[4] A. C. Richards Grayson, R. S. Shawgo, A. M. Johnson, N. T. Flynn, Y. Li, M. J. Cima, and R. Langer; "A BioMEMS Review: MEMS Technology for Physiologically Integrated Devices"; Proceedings of the IEEE, Vol. 92, No. 1; Jan. 2004.

[5] R. S. Ananth; " Design of an ultra low-frequency, dc-blocked, implantable electromyogram and cortical sensing amplifier"; 10th Annual Conference of the International FES Society; Montreal, Canada; July 2005.

[6] E. Bottino and M. Valle; **"**Integrated low noise preamplifier for biologic-electronics interfaces"; Proceedings of the 2005 European Conference on Circuit Theory and Design; P:I/103 - I/106 vol. 1, 28 Aug. - 2 Sept. 2005.

[7] Chih Liu; "A 70dB Gain Low-Power Band-Pass Amplifier for Bio-Signals Sensing Applications"; Proceedings of the IEEE International Symposium on Circuits and Systems ISCAS 2007; pp. 577 - 580; May 2007.

[8] R.R. Harrison and C. Charles; "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications"; IEEE Journal of Solid-State Circuits, vol. 38, Issue. 6; pp. 958 – 965, June 2003.

[9] Y. Nemirovsky, I. Brouk, and C.G. Jakobson; "1/f noise in CMOS transistors for analog applications"; IEEE Transactions on Electron Devices, Vol. 48, Issue 5, P:921 – 927,May 2001.