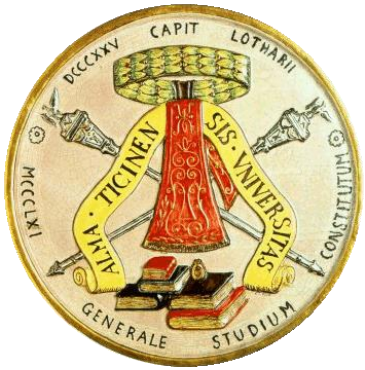

Inductively Degenerated LNA

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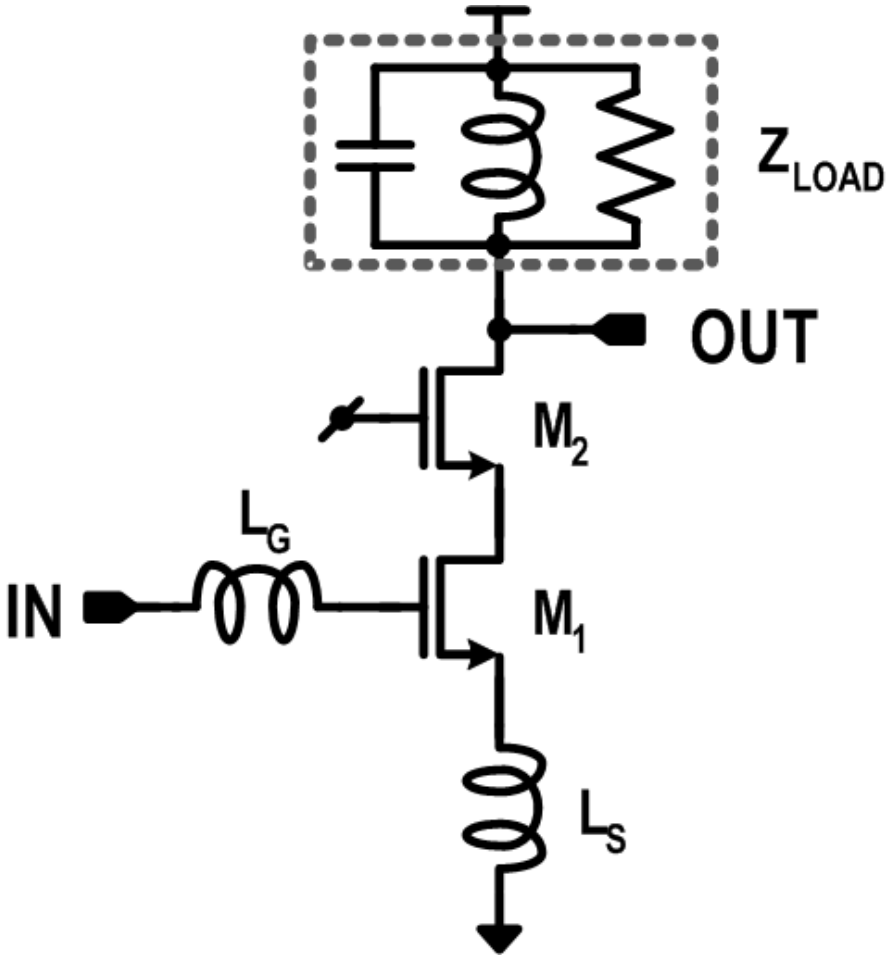
http://www.unipv.it/aic/

Inductively degenerated LNA



$$Z_{IN} = j\omega(L_S + L_G) + \frac{1}{j\omega C_{gs}} + \left(\frac{g_m}{C_{gs}}\right) L_S$$

$$\omega_0 = \frac{1}{\sqrt{(L_G + L_S) \cdot C_{gs}}}$$

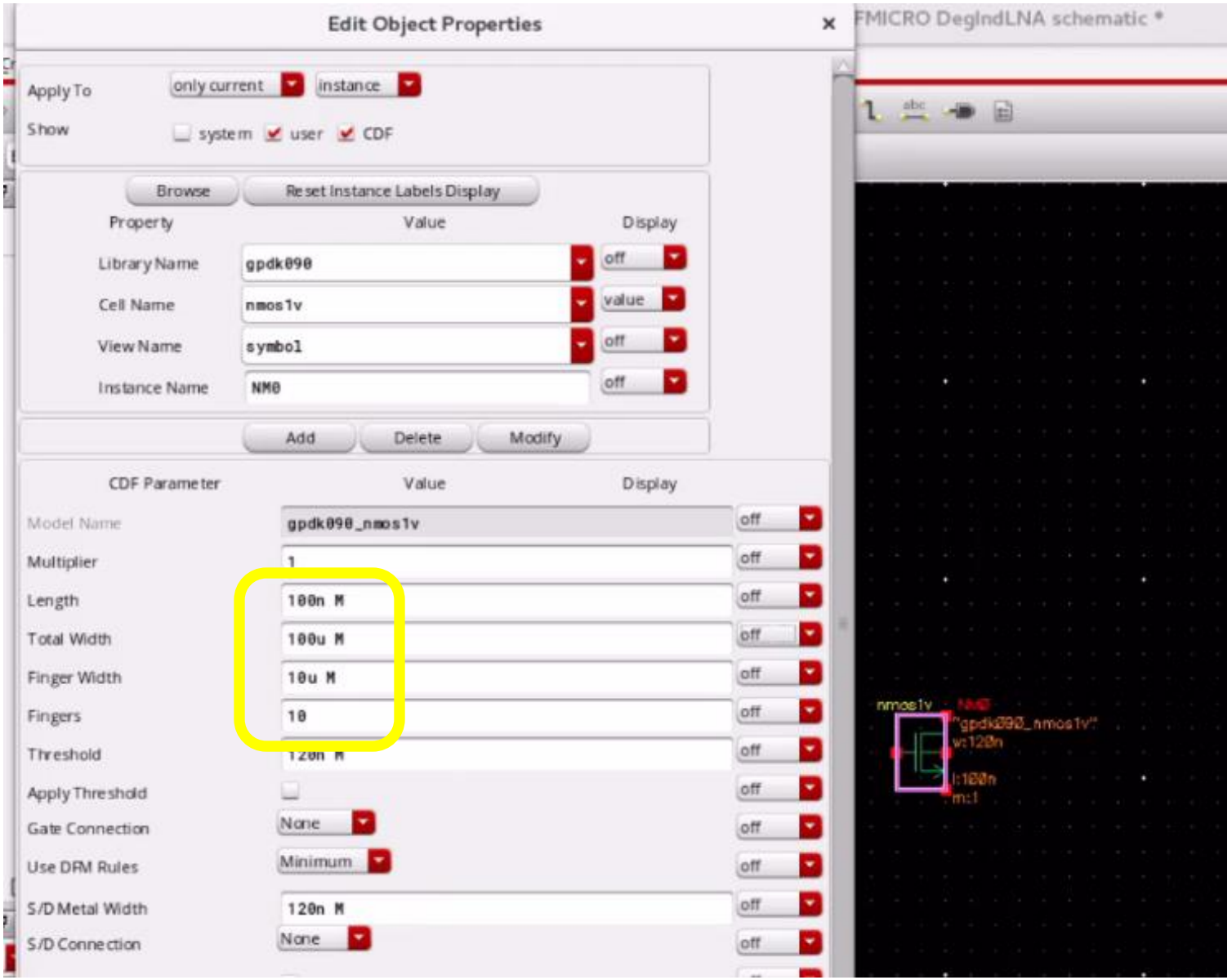
$$Z_{IN} = \left(\frac{g_m}{C_{gs}}\right) L_S = \omega_T L_S = R_S$$

Gain:

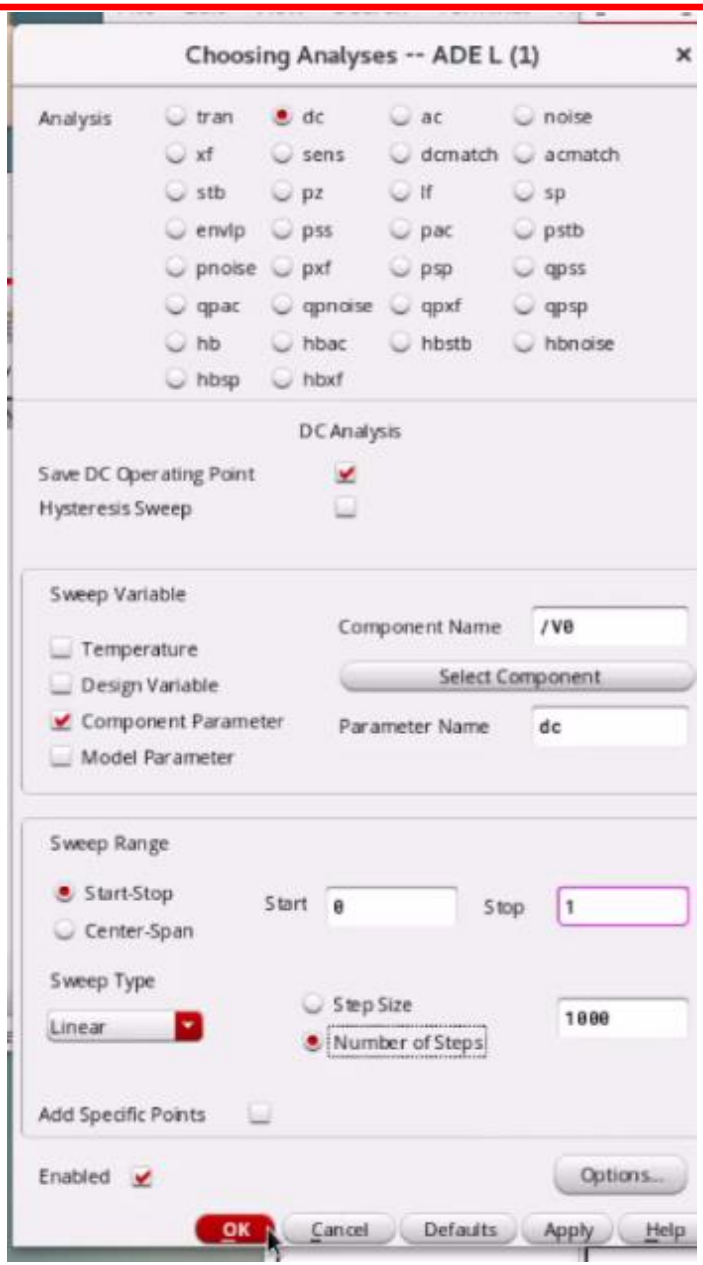
$$\frac{V_{OUT}}{V_{IN}} = G_m Z_L = Q_{IN} g_m Z_L$$

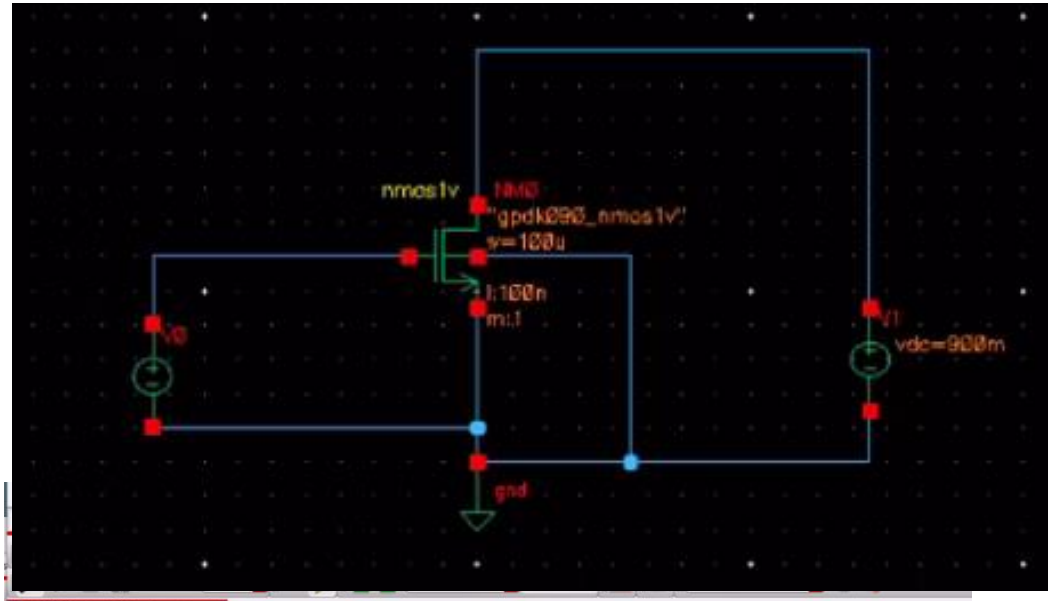
$$Q_{IN} = \frac{1}{2R_S \omega_0 C_{gs}}$$

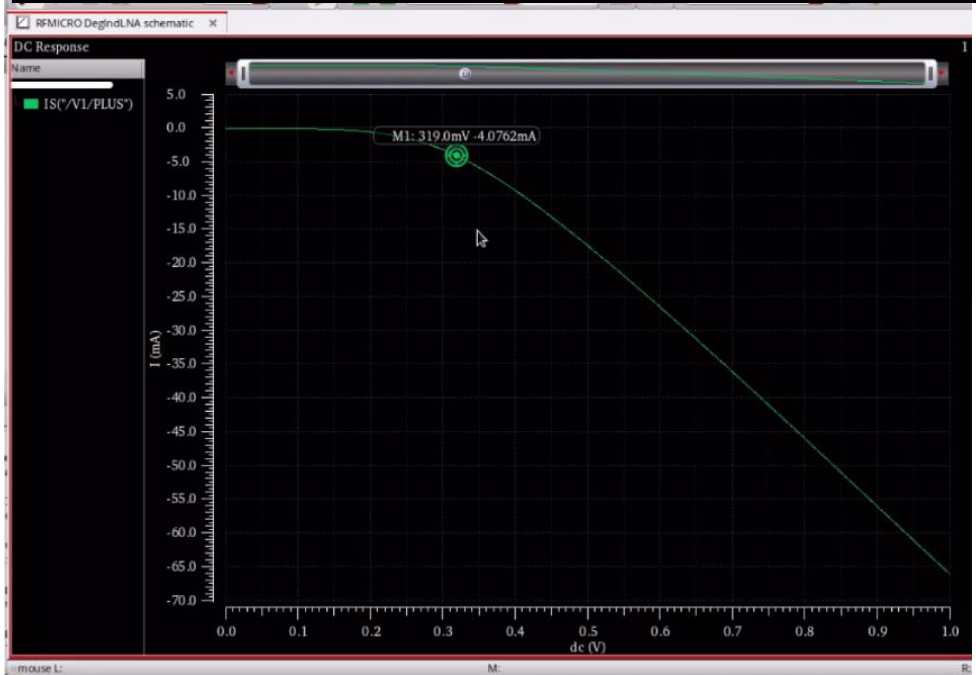
Input transistor: W/L=100/0.1



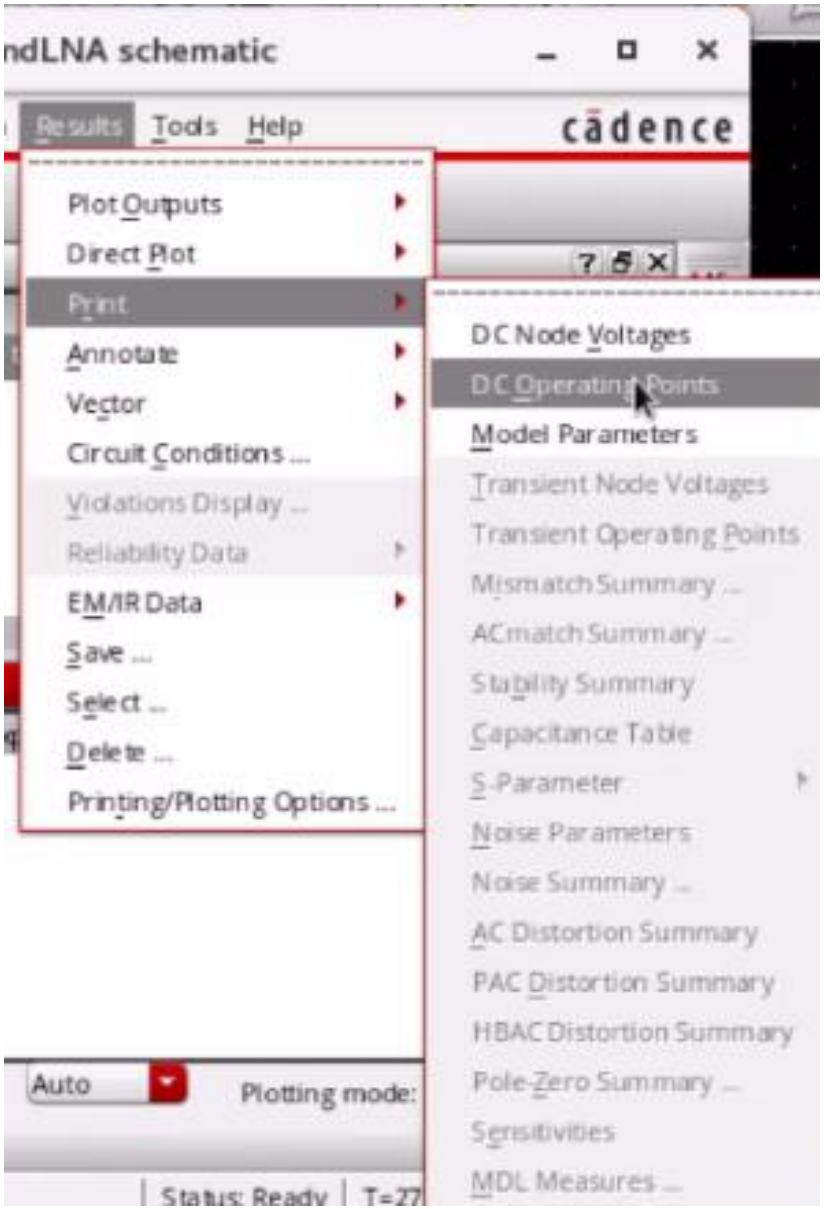
DC sweep to find Ibias=4mA

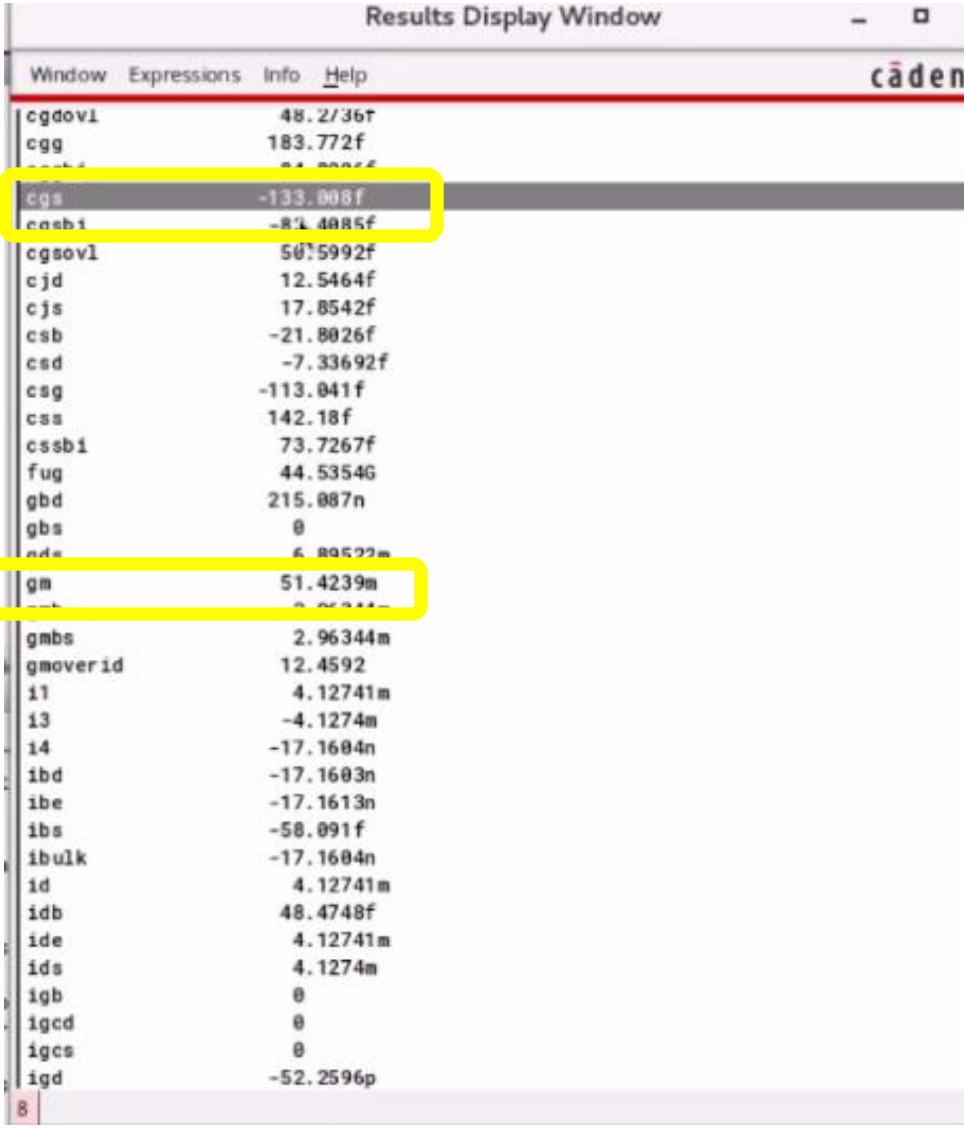




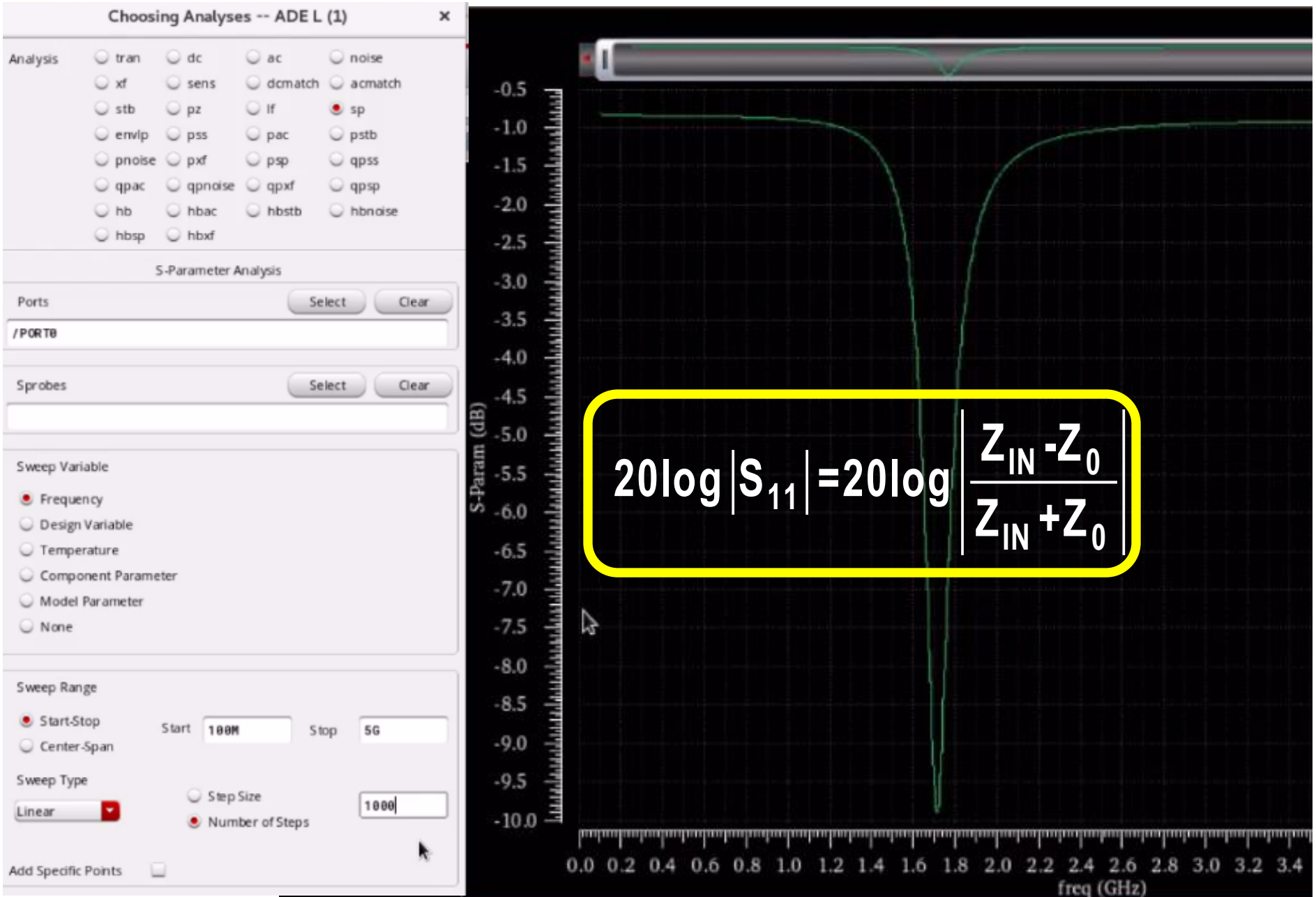


How to Choose Ls and Lg

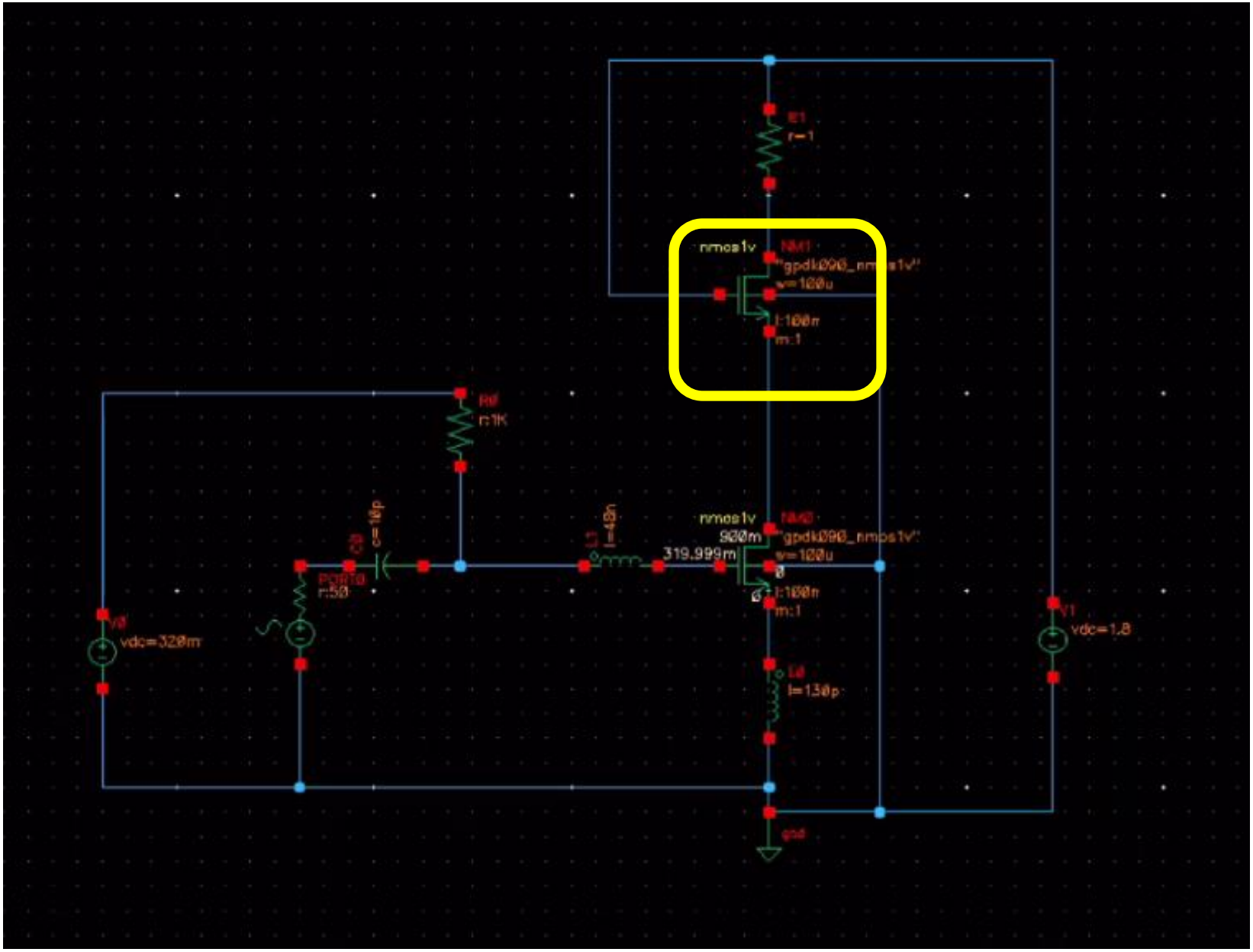




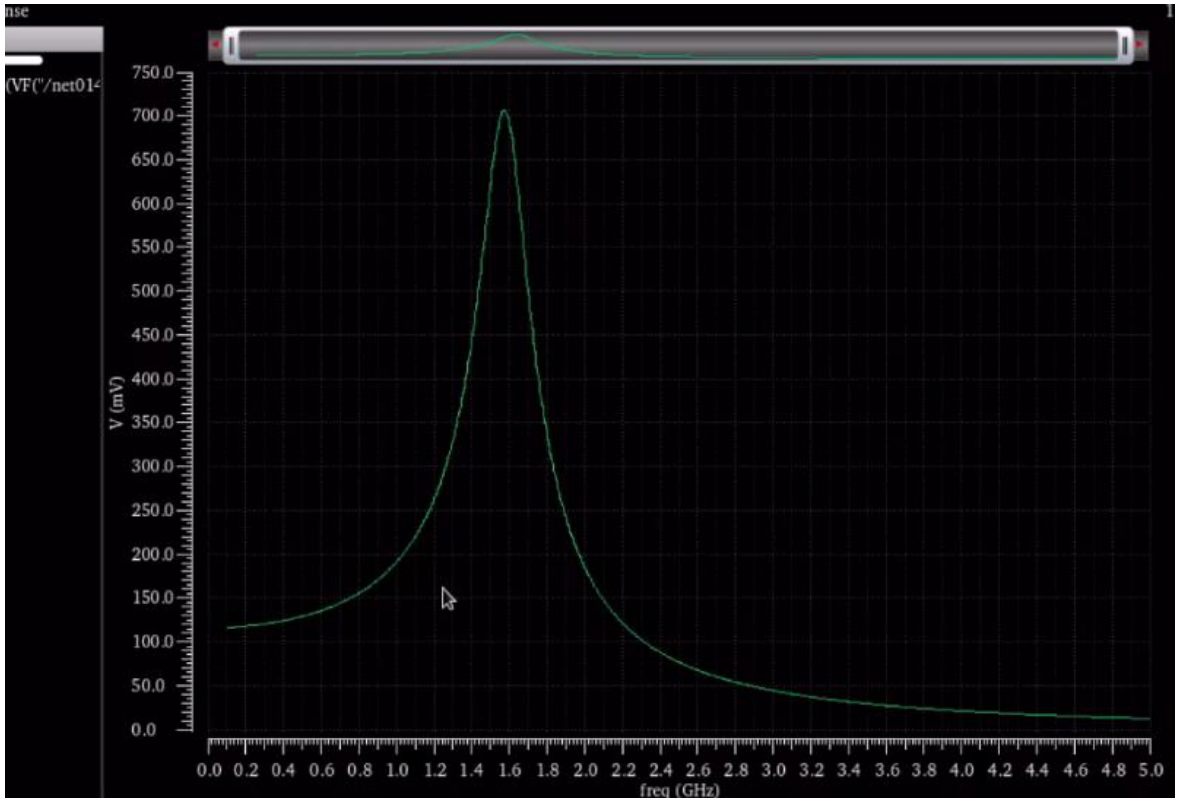
s-parameters simulation



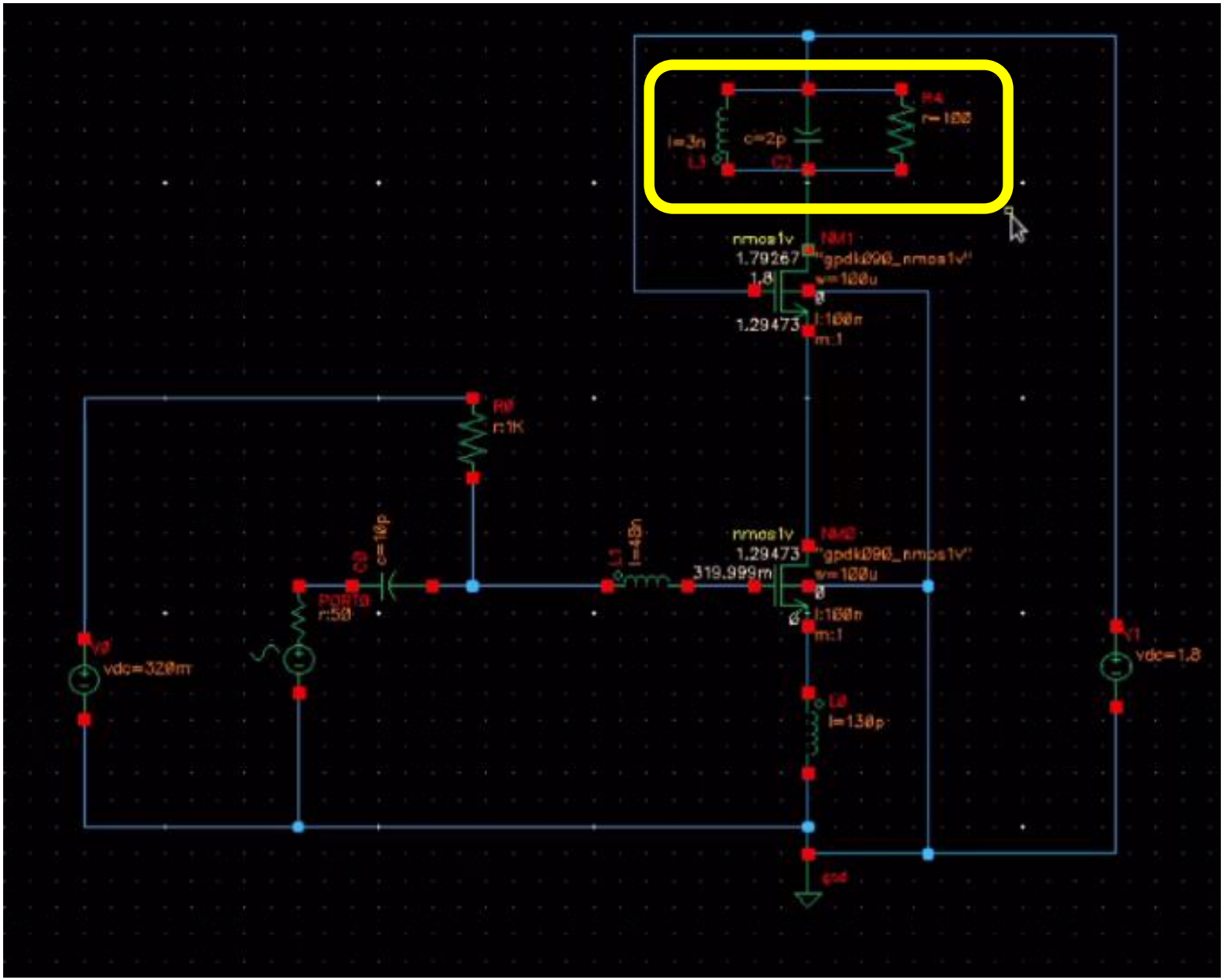
Adding the cascode



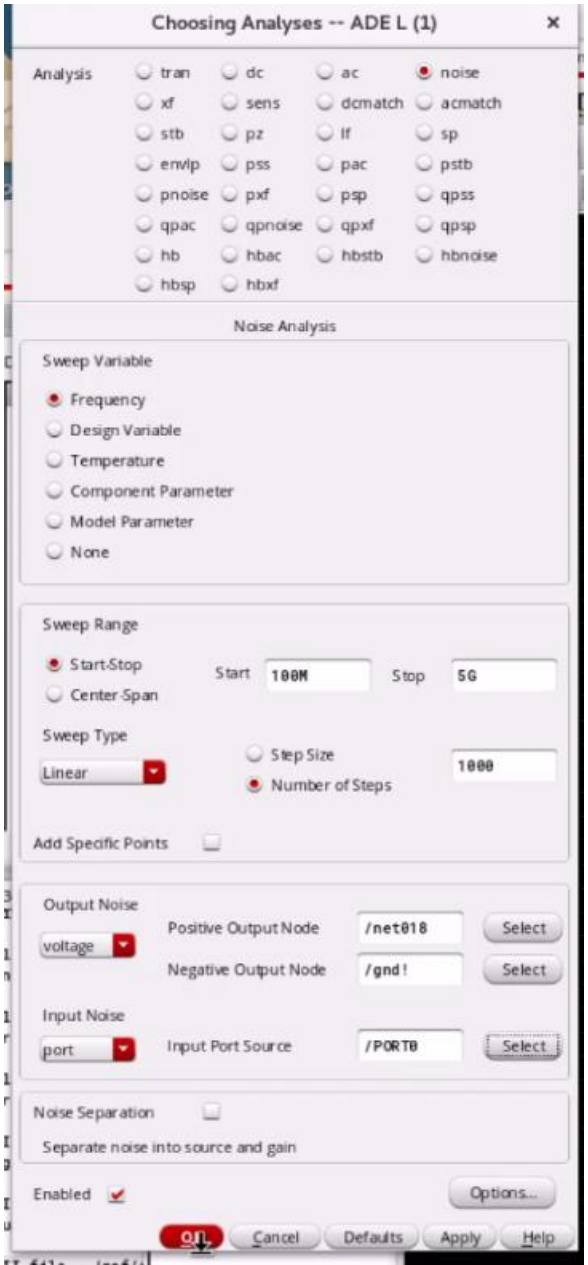
Transconductance Gain Simulation $G_m=Q_{in}g_m$



RLC Load and Voltage Gain of the stage



Noise Figure Simulation



Question #1

What is the way to get the values of Ls and Lg inductances?

1. Finding the Ls :

A) Analysis 1: From the input impedence of the of the circuit Zin, we can find the real compenent Lsg_m/Cgs = Rin , we know the Rin by the design it is the standard 50ohm => from this analysis Ls can be obtained because we know the Cgs and Gm from the transistor bias conditions.

B) Analysis 2: at the unity gain frequency Wt is inversly proportional to the Qality fator of the input matching circuit Wt=1/Qt which gives the room for analysis of the amplifier parameters and the matching circuit. Wt=Gm/Cgs => Rin/Ls

2. Finding of the Lg:

Lg is added to the circuit to give the extra freedom to the matching circuit to design Lg can be directly found from the input resonance freequeny Wo=1/ sqrt ((Ls+Lg)*Cgs)

Question #2

Are 10pF and 1Kohms enought for our 2 GHz design? Why?

1. Adding the R1 : Resistor R1 is added to bais the circuit which is to protect the circuit from the dc bais circuit , gate current of the MoSFET is interms of nA so it is enough that 1kohm bais resistor

2. Adding the C1: C1 is used for to isolate the DC circuit from the RF , 10Pf farade pretty manageble to block the dc from the bais circtuit.

3. R1 and C1 Analysis : The time constant of the R1C1 is 10nS and the input RF frquency is 50nS so the , RF can pass through circuit and blocked to affect the DC bais circuit.

Question #3

How can I tweak the design to improve my matching performance?

Sharp Input Matching can be obtined in three techniques:
(Reflection coefficent at the input depends)

1. Input Q fator(tune the input matching circuit)
2. Increase the gain (essential increasing the gm -> increase the vgs)
3. Tune the Zl(increase)

Question #3

How can I tweak the design to improve my matching performance?

1. Input Q fator(tune the input matching circuit)

At the high frequency Transistor parasitic parameters plays a great role without in usual design the Cgd is neclected, by considering the Cgd at the high frquency S11 improved from –11db to –13db (without considering the load match)

Problems address from this method:

1. Improved the input reflections (S11)
2. Addressed resonance Frequency drift (shifting matching frequency) 1.7GHz to 1.99GHZ

Question #3

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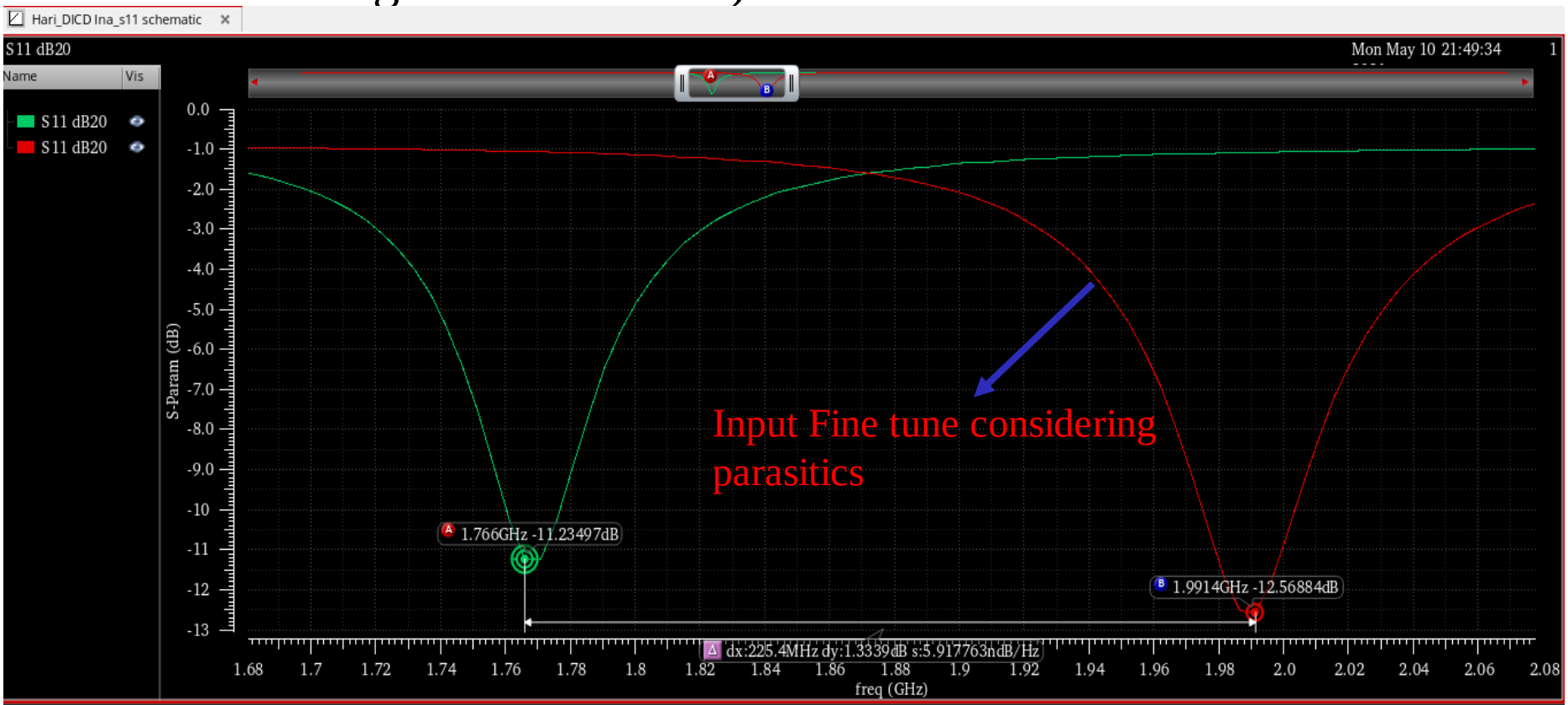
How can I tweak the design to improve my matching performance?

1. Input Q fator(tune the input matching circuit without considering the load match)



Question #3

How can I tweak the design to improve my matching performance?

2. Improving the Intrensic Gain

Improving the intrensic gain will aviod the nonlinearities in the systems and essential it is matched best higer the gain can be obtained by the higher the gm

Gm improved:
1. Operate the Transistor in the weak inversion and keep the maximum diementions (Vdsat less than 100mv)

2. Increase the more Vgs

3. Push Higher external current through external current reuse amplifiers

Question #3

How can I tweak the design to improve my matching performance?

2. Improving the Intrensic Gain

Improving the intrensic gain dosenot impact much untill unless load and input matched perfectly

Improving the Vgs from the bais point 450m v to vdd improved the S11 –4db but the problem from this method is a lot parasitc components impact on the circuit at the higher gain level and the resonance matching frequency drifts

Question #3

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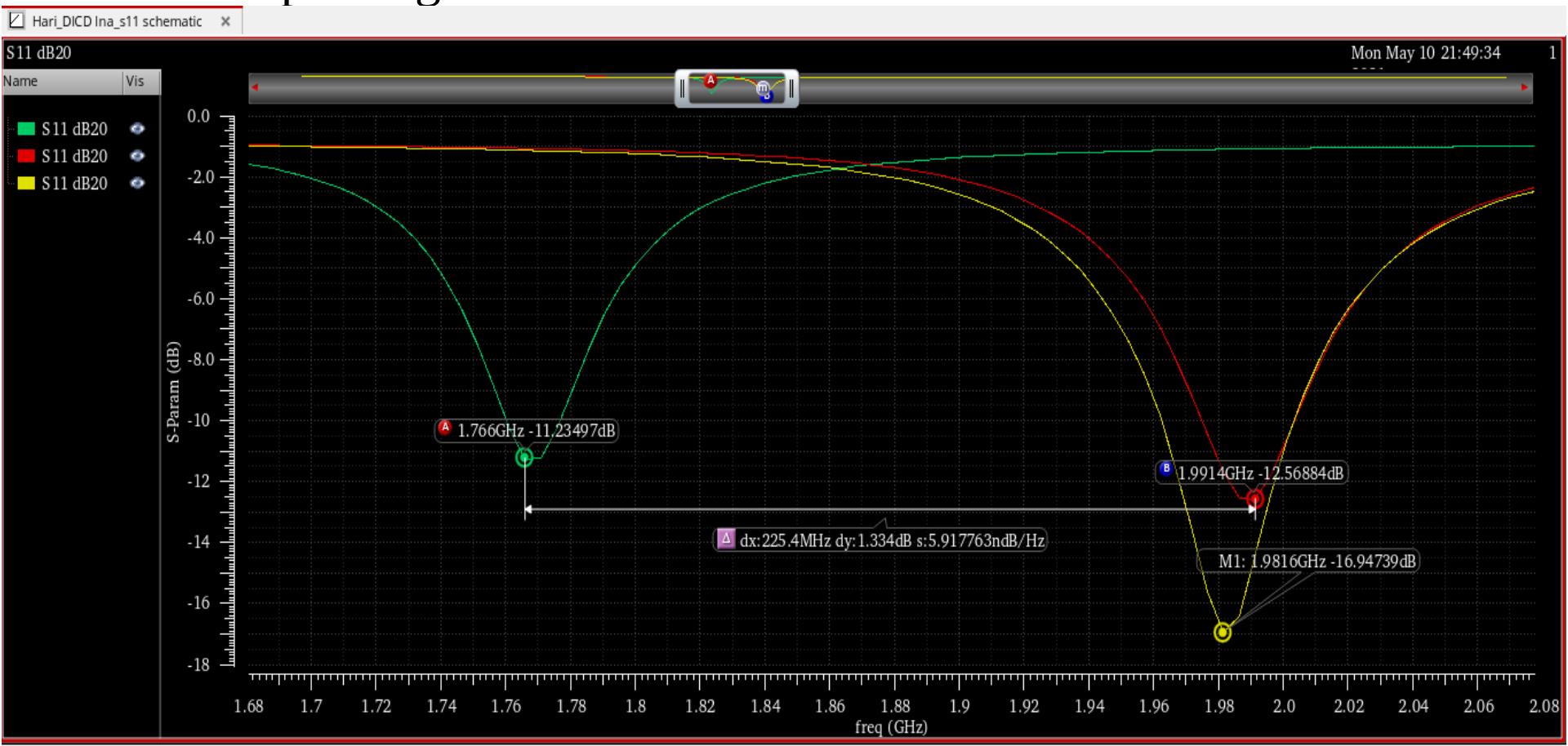
How can I tweak the design to improve my matching performance?

2. Improving the Intrensic Gain



Question #3

How can I tweak the design to improve my matching performance?

2. Tuning the Load

Impact of the load on the Input matching is very important in input matching the method is implemented it 50ohm load is coupled to the output tank 50ohm, resonance frequency matching by the load tank Capacitance and the Inductance Cd and Ld respectively

Improving the ratio between the Ld load tank inductance to input degenerative inducntance Ls improvs the input matching and out matching in terms of tens of dbs but the tuning frequency at the out put changes and the S22 drifts a lot from the input matching frequency

Question #3

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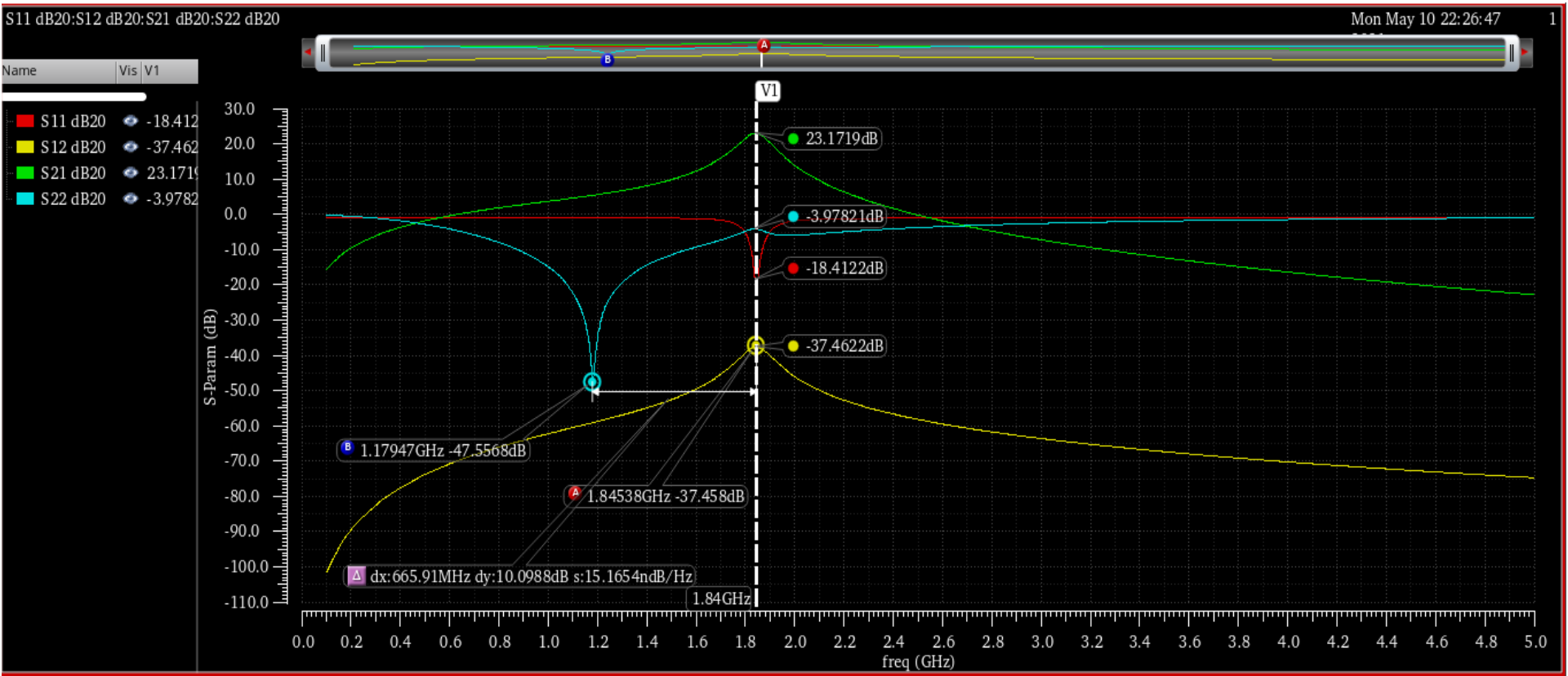
How can I tweak the design to improve my matching performance?

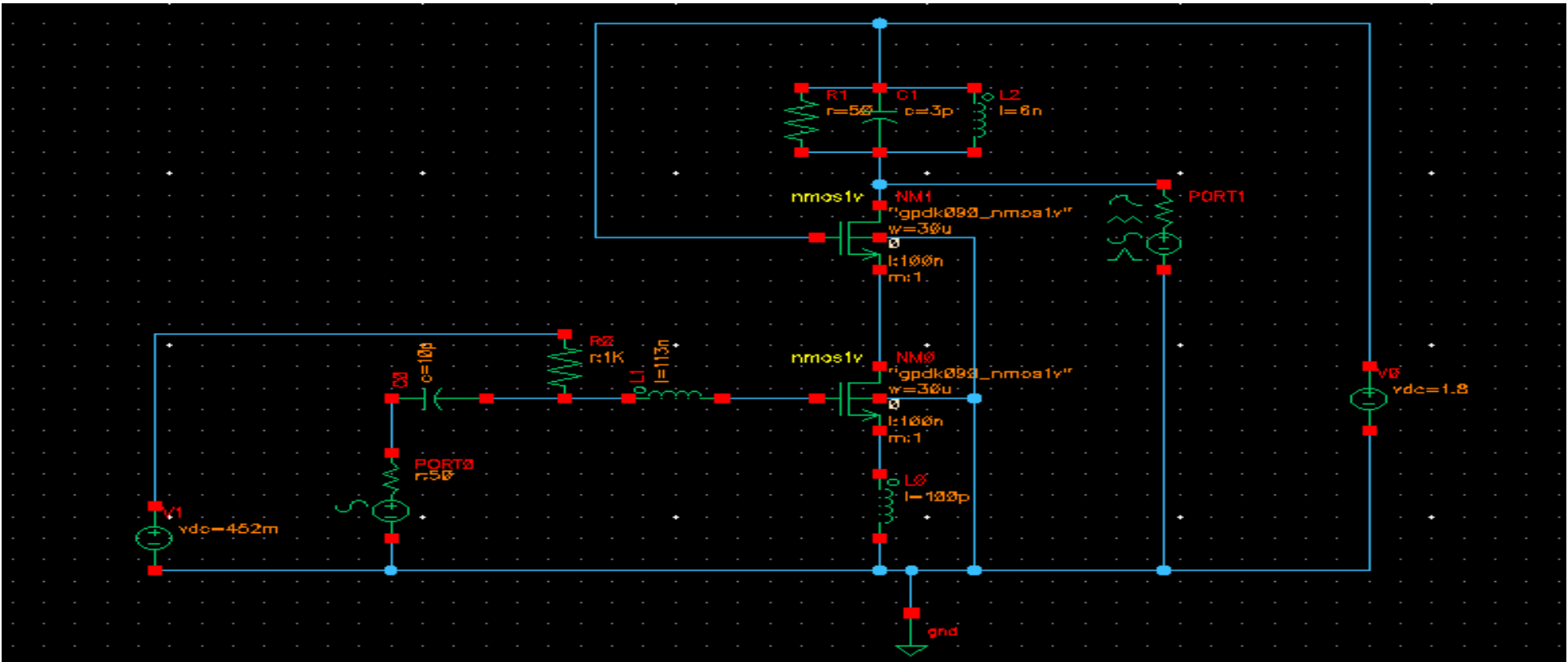
2. Tuning the Load Improving the Ld/Ls ratio and the out put coupled Resistance to 50ohm



Question #4

Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Complete Simulated Circuit



Question #4

Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

1. the input is matched by input quality factor improve and considering the input parasitic capacitances

2. at 4mA desired drain current the achived bais voltage Vgs is 450mv considering the W/Lmin ratio is 300

Design values avoiding the parasitics Ls=92PF , Lg=143nH, Cgs = 42fF, gm=24ms this design values give good matching 1.77GHz instead of 2GHz so there is frequency drift is happend

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Question #4

Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

3. Considering the Cgd 14fF , which is changed the drift frequency significantly from 1.77GHZ to 1.9981GHZ, input is matched well and improved the –4db in S11, new values are Ls=100PF, gm=24ms, ls = 113nH

4. improvement in the input matching circuit obtained by changing the gm which improved the input matching significantly roughly from –12db to –17db Improving the gain improved the noise figure very significantly.

5. noise figure and input matching tremendously improved by the out put tank matching coupling LNA to the 50ohm load from the load tank prallel resistance 50 improves the noise figure

Question #4

Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

6. by changing the Ld/Ls load tank inductance to the input degenerative inductance improves a gain lot and the imput matching which eventually makes Noise figure best but changing a Ld a lot makes drift in resonance frequency and the matching at the desired frequency 2Hz, S22 gose worst

8. So it is the tradeoff between the gain and matching and the resonance frequency

7. All the Achived results are listed below

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