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A Novel Optimization Framework for the Design of Gilbert Cell Mixers

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***Abstract*— This paper presents a new framework for the design optimization of a CMOS down-conversion mixer based on a conventional double balanced Gilbert cell. The framework exploits the g_m/I_D methodology to find the transistors' dimensions that optimize the tradeoff between conversion gain, noise figure, third-order intercept and power DC consumption of the mixer. The mixer has been designed using a 0.13 µm process from IHP Microelectronics, and it exhibits a conversion gain of 13.1 dB at 0 dBm local oscillator's power. The average noise figure is 11.9 dB, the input third-order intercept is -2.8 dBm and the output third-order intercept is 9.7 dBm. Finally, the chip-core without bonding pads measures only 0.028 mm by 0.031 mm and it dissipates 1.5 mW with a 1.5 V supply.**

Keywords—double balanced mixer; down-conversion mixer, Gilbert cell, g_m over I_D

I. INTRODUCTION

In modern telecommunication systems, different receiver topologies are possible. Due to its reduced cost and low power characteristics, the direct-conversion receiver topology is often the preferred option. The design of the direct-conversion mixer is very critical because it affects directly the performance of the entire receiver. The most commonly used mixer in direct-conversion receivers is the conventional double balanced Gilbert cell. The main benefits are good port-to-port isolation and low even-order harmonic distortion [1]. The architecture of the conventional Gilbert cell mixer is shown in Fig. 1. The cell is composed of a stack of three MOS transistor pairs, so it requires large voltage headroom to keep the transistors biased in saturation, and it results in a large DC-power consumption.

In literature [2]-[4], different techniques and ad hoc architectures have been proposed to improve the various performance metrics of the Gilbert cell. For example, MacEachern et al. [2] successfully improve conversion gain and system linearity by using the charge injection method. Unfortunately, this method requires a significant increment of the DC-current and therefore has the drawback of further increasing DC-power consumption. Wei et al. [3] utilize a folded structure in order to reduce the number of stacked transistors. As a result, the mixer can work with a lower DC-power supply, however the current mirror topology in the folded structures reduces the conversion gain and introduces large parasitic capacitances that deteriorate bandwidth. Seo et al. [4] exploit a switched biasing technique for the tail current source I_{BIAS}. This technique allows reducing the noise figure of

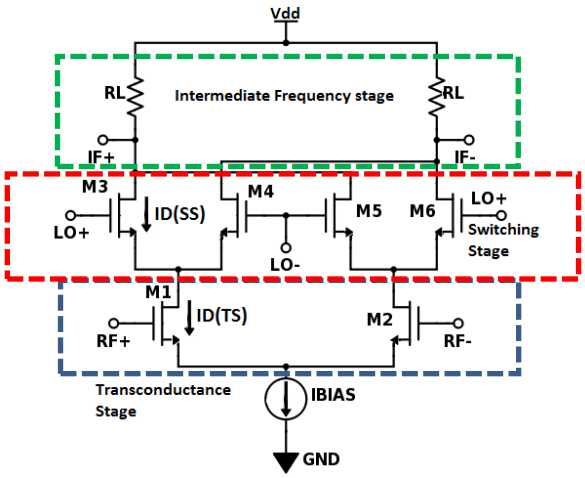

Fig. 1 Architecture of a conventional double balanced Gilbert cell mixer.

the entire system but requires a number of stacked transistors greater than the conventional cell and, therefore it requires significantly larger power consumption than the conventional cell. Each of these methods focuses on improving only a specific aspect of the Gilbert mixer and relies on a fixed size (i.e. a fixed W/L ratio) for all the transistors. Typically, the size of the MOSFETs is fixed by the value of g_m required to achieve the target conversion gain.

The aim of this paper is to show that it is possible to achieve an optimal tradeoff between the various performance metrics of a Gilbert cell mixer without using any ad-hoc architecture but, rather, relying on a systematic approach for calculating the W/L transistor's ratios required for achieving the design specifications. The systematic approach exploits the g_m/I_D methodology [6] and it is based on a unified treatment of all the regions of operation of the MOS transistor. This method and its associated figures of merit are strongly related to the performance of the analog circuit and provide an indication of how to best bias the devices. CMOS fabrication processes with channel lengths in the nanoscale range are plagued by several second-order undesired effects, that alter the device's behavior [6]-[7] and strongly limits the accuracy and effectiveness of the square-law equations traditionally used to determine the MOSFET operating point. The absence of a simple set of closed-form equations pushes many designers toward a "trial and error" approach that is tedious, time consuming, and typically converge toward a sub-optimal result. In all cases for

which the transistor behavior cannot be expressed through a set of closed-form equations, the g_m/I_D methodology provides a systematic tool for calculating the transistors dimensions, and converging to an optimal solution in a very small number of iterations.

The Gilbert cell mixer we present was designed using a 130 nm SiGe process provided by IHP Microelectronics. The rest of the paper is organized as follows. Section II illustrates the design framework used to design the proposed Gilbert cell. Section III shows the results of the post-layout simulations in terms of conversion gain, noise figure, DC-power consumption and system linearity expressed through the third-order intercept (IIP3). Finally, section IV provides conclusions.

II. Design Framework

The conventional architecture of a double balanced Gilbert cell mixer shown in fig. 1 is composed of three distinct stages. A differential *transconductance stage* (TS) composed by the transistors pair M1 and M2 converts the RF voltages at the input ports in current signals for the *switching stage* (SS) composed by the transistors M3-M6. Finally, the switching stage is driven by the Local Oscillator (LO) to reverse the polarity of the RF inputs at the LO frequency rate. Ideally the balanced structure should cancel any RF and LO frequency component appearing at the output. Since the *Intermediate Frequency* (IF) *stage* output is a differential signal the LO appear at the output as a common mode.

Given the desired value of the load resistance R_L, the mixer conversion gain (A_v) is determined by the transconductance value (g_m) of the transistors M1 and M2 [1]:

$$A_v \cong \left(\frac{2}{\pi}\right) g_m R_L \qquad (1)$$

The traditional design approach starts from (1), and consists of first selecting the value of g_m required to achieve the target gain and then choosing a value for the width W and the channel length L of the MOS transistor relying on the square law equation of the drain current I_D:

$$g_m = \sqrt{\frac{2K_n W I_D}{L}} \qquad (2)$$

where K_n is the product of the oxide capacitance of the MOSFET (C_{ox}) and the electron mobility (μ_n). The drain current of the transistors is set based on the tail current of the transconductance stage (TS):

$$I_{BIAS} = 2 \times I_{D(TS)} \qquad I_{D(SS)} = 2 \times I_{D(TS)} \qquad (3)$$

As previously mentioned, for the nano-metric channel lengths of the MOSFETs employed in today's integrated circuits, the square-law equation (2) has become grossly inaccurate. Hence, in the proposed framework, the W/L ratio of the transistors in the mixer's schematic are selected exploiting a systematic approach based on the g_m/I_D methodology. Starting from the DC-analysis of the single transistor, the algorithm implemented by the framework extracts the transit frequency (f_T), the intrinsic gain (g_m/g_{ds}) and the current density I_D/W versus the transconductance efficiency g_m/I_D. These figures of merit are width-independent and are intimately linked to the CMOS fabrication process utilized in the design. Hence, they need to be generated only once and can then be used for designing different circuit topologies [6]. In the proposed framework, the figures of merit are arranged in lookup tables that can be indexed through the g_m/I_D ratio (that is the inversion level of the transistor). S*trong inversion* occurs for values of g_m/I_D in the 5-8 S/A range, while for values, in the 20-25 S/A range, the transistor operates in *weak inversion*. The choice of the inversion level is essentially determined by a tradeoff between speed (f_T), intrinsic gain and power efficiency and it depends on the target application. In strong inversion, the transistor exhibits higher speed than in weak inversion, but the intrinsic gain is lower. However, in strong inversion the drain current is higher, therefore the transistor dissipates more power than in weak inversion. Increasing the g_m/I_D ratio increases the intrinsic gain but the width of the transistor and its associated capacitances are also increased, so the f_T is reduced. On the other hand, for large values of g_m/I_D, the drain current decreases thus the DC power consumption is also reduced. The region separating strong and weak inversion regions is defined as *moderate inversion* and usually provides a good tradeoff between all parameters [6]-[8]. Once the *technology lookup tables* are generated they can be exploited to find out the transistor's W/L ratio associated with a given bias point. The algorithm implemented in the proposed framework considers the transistors in the switching stage and the transconductance stage separately. By varying independently, the g_m/I_D of the two stages the algorithm allows to search the solution space for the optimal bias point that meets design specifications. The optimal solution is reached through the following steps:

1. Given the target gain and the load resistance specifications, use (1) to derive the value of g_m;
2. Once the value of g_m has been set, sweep g_m/I_D (that is the inversion level of the transistors) in the range 5-25, and let the framework computes the corresponding current levels $I_{D(SS)}$ and $I_{D(TS)}$;
3. Exploiting the lookup table of the current density (I_D/W), computes the values of $W_{(SS)}$ and $W_{(TS)}$ for all inversion levels explored. Set the channel length L to the minimum value of 130nm to maximize speed [6];
4. Perform systematic DC analysis of the mixer by independently varying the g_m/I_D ratio for the TS and SS. For each bias point computes the DC-power consumption of the mixer.
5. For each solution checks that the circuit is correctly biased (that is all transistors operates in saturation) and compares the DC-power consumption with the design specification. Discard any unfeasible solution.
6. For each solution left from the previous step, compute the conversion gain of the mixer. Discard any further solution that exhibit a conversion gain lower than the design specifications.
7. Repeat the previous step for the noise figure and the third-order intercept of the system.
8. Explores the pruned solutions space and extracts the optimal bias point, that is the bias point that allows to achieve the best tradeoff among the performance metrics of the mixer.

To achieve the best balance between the different performance metrics, the following figure of merit (FOM) is defined:

$$FOM = \frac{CG_{[dB]} \cdot IIP3_{[mW]}}{NF_{[dB]} P_{DC[mW]}} \quad (4)$$

where CG is the conversion gain expressed in dB, IIP3 is the third-order intercept in mW, NF is the average noise of the mixer in dB and P_{DC} is the DC-power consumption in mW.

III. Optimization Results

The proposed framework has been validated on the design of a Gilbert cell mixer biased with a DC-power supply of 1.5V. The design requirements were: 1) a conversion gain greater than 10 dB, 2) a DC-power consumption lower than 3 mW, 3) a resistive load of 500 Ohms, and 4) a target third-order intercept (IIP3) better than -5 dB. These design specifications were chosen to compare our mixer with similar papers present in literature and reported in Table I. The circuit metrics used to validate our design have been computed considering a LO sine wave with a frequency of 5.7 GHz and a maximum power of 0 dBm.

Fig. 2(a) sketches the solution space extracted by the proposed design framework. Observing Fig. 2(a) we can infer that the transistors of the transconductance stage (TS) should be biased in a g_m/I_D range between 5-13 S/A while the transistors of the switching stage (SS) can be basically biased anywhere in the inversion region. Fig. 2(b) shows the behavior of the IIP3. When the MOSFETs, in SS, are biased in the g_m/I_D range between 5-10 S/A, the IIP3 linearly decays as the biasing point of the TS passes from strong to weak inversion. When biasing the transistors of the SS in weak inversion, the IIP3 curve changes its behavior and it becomes a parabolic curve with a local maximum for $g_m/I_{D(SS)}$ of 20 S/A. The values of IIP3 were computed considering an RF sine source composed of two tones, one at 5.8 GHz and the other one at 5.85 GHz. The behavior of the average noise figure (Fig. 2(c)) over the Ultra-Wide Bandwidth (UWB) frequencies range (3.1÷10.6 GHz) is very similar to that of the IIP3. When the SS is biased in strong inversion, the noise figure exponentially decays as the MOSFETs in the TS pass from strong to moderate inversion. However, once the MOSFETs in the SS reach the moderate inversion, the noise figure slowly decreases and finally reaches a value lower than 12 dB. Fig. 2(d) sketches the conversion gain of the mixer with respect to the g_m/I_D of the two stages. Observing the figure, we see that the conversion gain has a parabolic trend in both g_m/I_D directions, reaching an absolute maximum value of 13.5 dB when the transistors in both stages are biased in moderate inversion. The DC-power consumption of the mixer is sketched in Fig. 2(e). It is essentially determined by the g_m/I_D ratio of the MOSFETs in the TS. In fact, it exponentially decays when the bias point of this stage passes from strong to weak inversion. On the contrary, when the bias point of the SS moves from strong to weak inversion, the DC-power consumption is approximately constant. This type of behavior is strictly related to the working principles of the Gilbert cell. As previously described in section II, the transconductance stage must converts the input voltage signal into a current signal, while ideally, the switching stage transistors must only reverse the polarity of the RF inputs at the

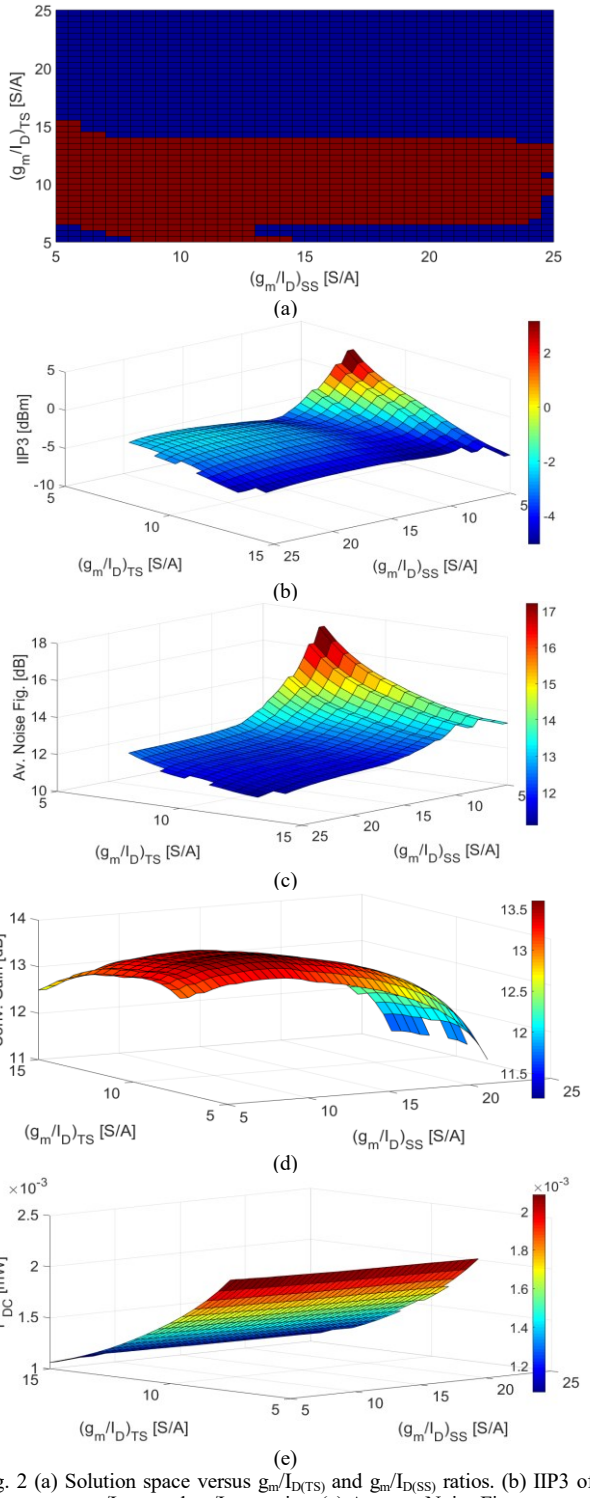

Fig. 2 (a) Solution space versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios. (b) IIP3 of the mixer versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios. (c) Average Noise Figure versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios. (d) Conversion gain of the mixer versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios. (e) DC-power consumption of the system versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios.

LO frequency rate. Finally, Fig. 3 sketches the FOM as a function of $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios. Due to the behavior of the IIP3 and the average noise figure of the system, the graph of the FOM exhibits an irregular trend. However, it reaches a local maximum when the TS is biased in moderate inversion and the SS is biased between moderate and weak inversion.

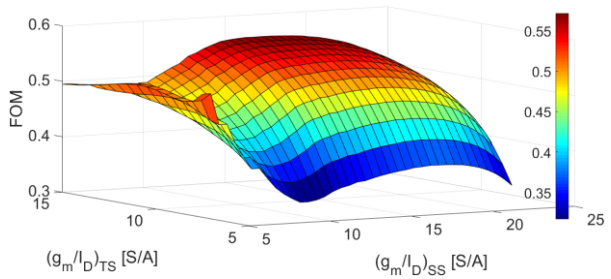

Fig. 3 FOM versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios.

The optimization algorithm returns as optimal solution $g_m/I_{D(SS)}$ = 18 S/A and $g_m/I_{D(TS)}$ = 10.5 S/A. To find out how to optimally bias the transistors, the algorithm searches for the maximum value of FOM. The maximum value of FOM provides the best tradeoff among conversion gain, noise figure, IIP3 and DC-power consumption. Although, the design optimization procedure illustrated is applied to the design of a Gilbert cell, the proposed framework is completely general and represent an extremely scalable and flexible tool. It does not constrain the user to a fixed design flow; the designer can choose to maximize performances with respect to any suitable figure of merit. Table I compares the quality of the design solution obtained against several comparable CMOS Gilbert mixer designs present in literature. As indicated by the FOM values summarized in the table, the main advantage of our design is a better tradeoff between the main performance metrics. In addition, the mixer designed with our proposed framework, exhibits the lowest DC-power consumption. The g_m/I_D-based approach we followed allows to optimize the mixer transistor sizes and to achieve the desired specifications without making use of complex architectures or ad hoc circuit solutions. In general, the g_m/I_D approach exploited can also be extended to the design of more complex architectures presented in literature. Finally, Fig. 4 shows the layout of the core of the designed mixer. In final layout, the ideal bias current generator was realized with a CMOS current mirror. The chip-core without bonding pads and baluns measures 0.028 mm by 0.031 mm (that is an area of 868 μm^2).

IV. CONCLUSIONS

This paper presented a new framework for optimizing the design of a Gilbert down-conversion mixer. The framework is based on the g_m/I_D methodology and allows to meet specifications by optimizing the sizing of the transistors rather

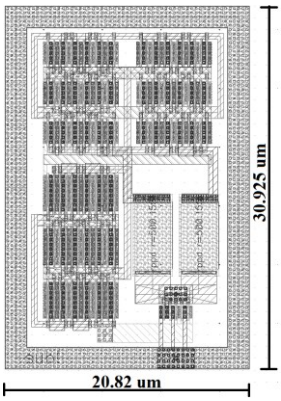

Fig. 4 Final Layout of the Double-Balanced Gilbert Cell Mixer

TABLE I. REPORTED PERFORMANCE OF CMOS GILBERT MIXERS

Ref.	*CMOS Tech.*	*Gain [dB]*	*IIP3 [dBm]*	*NF Av. [dB]*	*P_{DC} [mW]*	*FOM*
[4]	0.13 um	8	-3	11.2	5.57	0.12
[9]	0.18 um	10	4	10	10	0.16
[10]	0.13 um	8.95	-2.2	11.4	3.7	0.16
[11]	0.13 um	21	-1.8	15.7	18.3	0.06
[12]	0.18 um	13.5	-3.25	21.22	7.2	0.06
This Work	0.13 um	13.1	-2.8	11.9	1.5	0.53

The performance metrics indicated refers to the core of the mixer

than having to rely on the use of more complex architectures or ad hoc circuit solutions. To the best of our knowledge, the final mixer exhibits the best-known FOM w.r.t. conversion gain, noise figure, IIP3 and DC-power consumption. The framework, proposed is entirely scalable so a designer can also apply it to the optimization of any of the other circuit solutions presented in literature for improving one or more of the specific performance metrics of the Gilbert mixer.

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