Transactions Briefs

A Study of Oscillator Jitter Due to Supply and Substrate Noise

Frank Herzel and Behzad Razavi

***Abstract*—This paper investigates the timing jitter of single-ended and differential CMOS ring oscillators due to supply and substrate noise. We calculate the jitter resulting from supply and substrate noise, show that the concept of frequency modulation can be applied, and derive relationships that express different types of jitter in terms of the sensitivity of the oscillation frequency to the supply or substrate voltage. Using examples based on measured results, we show that thermal jitter is typically negligible compared to supply- and substrate-induced jitter in high-speed digital systems. We also discuss the dependence of the jitter of differential CMOS ring oscillators on transistor gate width, power consumption, and the number of stages.**

***Index Terms*—Jitter, oscillator, phase-locked loops, supply noise.**

I. Introduction

High-speed digital circuits such as microprocessors and memories employ phase locking at the board-chip interface to suppress timing skews between the on-chip clock and the system clock [1]–[3]. Fabricated on the same substrate as the rest of the circuit, the phase-locked loop (PLL) must typically operate from the global supply and ground busses, thus experiencing both substrate and supply noise. The noise manifests itself as jitter at the output of the PLL, primarily through various mechanisms in the voltage-controlled oscillator (VCO). As exemplified by measured results reported in the literature, we show that the contribution of device electronic noise to jitter is typically much less than that due to supply and substrate noise.

This paper describes the effect of supply and substrate noise on the performance of single-ended and differential ring oscillators, providing insights that prove useful in the design of other types of oscillators as well. Section II summarizes the oscillators studied in this work and Section III defines various types of jitter. Sections IV and V quantify the jitter due to thermal noise in the oscillation loop and frequency-modulating noise, respectively. Sections VI and VII apply the developed results to the analysis of supply and substrate noise, and Section VIII presents the dependence of jitter upon parameters such as device size, the number of stages, and power dissipation.

II. Ring Oscillators under Investigation

In this paper, we investigate both single-ended ring oscillators (SERO's) and differential ring oscillators (DRO's). The latter are much more important in digital circuit applications, since DRO's are less affected by supply and substrate noise. The circuit topologies are shown in Fig. 1 for the SERO and in Fig. 2 for the DRO.

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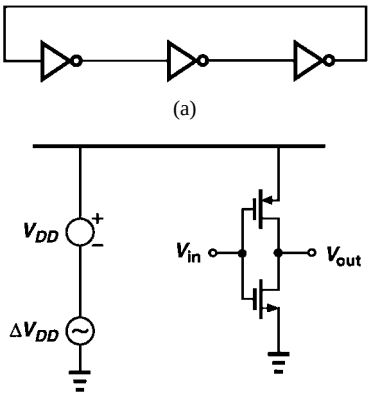


Fig. 1. Single-ended ring oscillator: (a) block diagram and (b) implementation of one stage.

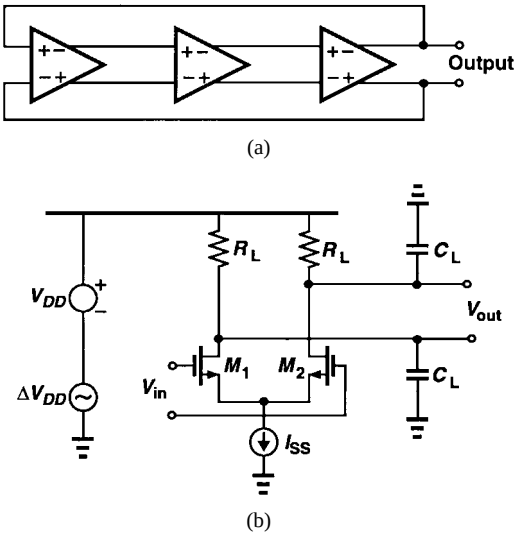


Fig. 2. Differential ring oscillator: (a) block diagram and (b) implementation of one stage.

The simulations were performed with the SPICE parameters of a 0.6-μm CMOS technology. We employed the minimum gate length throughout the paper. Furthermore, unless indicated otherwise, we use the following parameters for the differential stage: $W = 80$ μm, $R_L = 1$ kΩ, $I_{SS} = 1$ mA, $C_L = 0$, $V_{DD} = 3$ V. The rms value of ΔV_{DD} was chosen to be 71 mV, corresponding to a peak amplitude of 100 mV for a sinusoidal perturbation.

III. Definitions of Jitter

We consider the output voltage $V_{out}(t)$ of an oscillator in the steady state. The time point of the nth minus-to-plus zero crossing of $V_{out}(t)$ is referred to as t_n. The nth period is then defined as $T_n = t_{n+1} - t_n$. For an ideal oscillator, this time difference is independent of n, but in reality it varies with n as a result of noise in the circuit. This results in a deviation $\Delta T_n = T_n - \bar{T}$ from the mean period $\bar{T}$. The quantity ΔT_n is an indication of jitter.

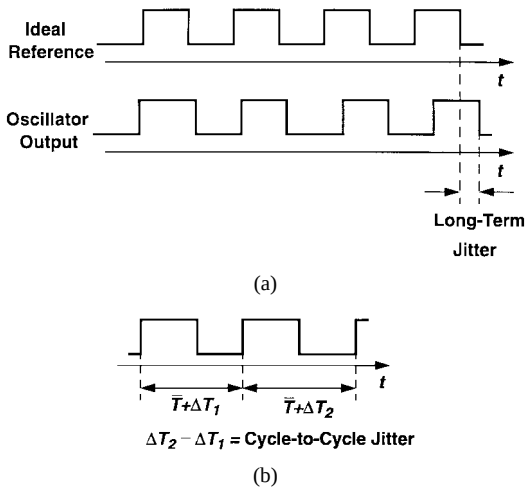


Fig. 3. Illustration of (a) long-term jitter and (b) cycle-to-cycle jitter.

More specifically, absolute jitter or long-term jitter

$$\Delta T_{\rm abs}(N) = \sum_{n=1}^{N} \Delta T_n \tag{1}$$

is often used to quantify the jitter of phase-locked loops. Modeling the total phase error with respect to an ideal oscillator [Fig. 3(a)], absolute jitter is nonetheless illsuited to describing the performance of *oscillators* because, as shown later, the variance of $\Delta T_{\rm abs}$ diverges with time.

A better figure of merit for oscillators is cycle jitter, defined as the rms value of the timing error ΔT_n [1]

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2}. \tag{2}$$

Cycle jitter describes the magnitude of the period fluctuations, but it contains no information about the dynamics.

The third type of jitter considered here is cycle-to-cycle jitter [Fig. 3(b)] given by

$$\Delta T_{\rm cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_{n+1} - T_n)^2} \tag{3}$$

representing the rms difference between two consecutive periods.

Note the difference between the cycle jitter and the cycle-to-cycle jitter: the former compares the oscillation period with the *mean* period and the latter compares the period with the *preceding* period. Hence, in contrast to cycle jitter, cycle-to-cycle jitter describes the short-term dynamics of the period. The long-term dynamics, on the other hand, are not characterized by cycle-to-cycle jitter. For example, if $1/f$ noise modulates the frequency slowly, $\Delta T_{\rm cc}$ does not reflect the result accurately. With respect to the zero crossings, the cycle-to-cycle jitter is a double-differential quantity in that three zero crossings of the output voltage are related to each other. As discussed in Section V, this results in a completely different dependence on the modulation frequency than for the cycle jitter.

We should note that an oscillator embedded in a phase-locked loop periodically receives correction pulses from the phase detector and charge pump, and hence its long-term jitter strongly depends on the PLL dynamics. Thus, for the analysis of a free-running oscillator, cycle jitter and cycle-to-cycle jitter are more meaningful, particularly because the latter type hardly changes when the oscillator is placed in the loop.

A more general quantification of the jitter is possible by means of the steady-state autocorrelation function (ACF) defined as

$$C_{\Delta T}(m) = \lim_{N\to\infty} \frac{1}{N}\sum_{n=1}^{N} (\Delta T_{n+m}\Delta T_n). \tag{4}$$

To obtain an intuitive understanding of this quantity, we insert (4) with $m = 0$ in (2), obtaining

$$\Delta T_c^2 = C_{\Delta T}(0). \tag{5}$$

Equation (5) states that the ACF with zero argument is the squared cycle jitter. For a nonzero argument, the ACF decreases with increasing m, finally approaching zero for $m \to \infty$. This indicates that the timing error ΔT_n has a finite memory. In order to express the cycle-to-cycle jitter by the ACF, we rewrite (3) as

$$\begin{aligned}\Delta T_{\rm cc}^2 &= \lim_{N\to\infty} \frac{1}{N}\sum_{n=1}^{N} (\Delta T_{n+1} - \Delta T_n)^2 \\ &= 2C_{\Delta T}(0) - 2C_{\Delta T}(1).\end{aligned} \tag{6}$$

This expression will be used for an analytical calculation of the cycle-to-cycle jitter in Section V.

IV. Jitter Due to Device Electronic Noise

The electronic noise of the devices in an oscillator loop leads to phase noise and jitter [5], [7], [8]. Our objective is to express jitter in terms of phase noise and vice versa. These relationships are useful as they relate two measurable quantities.

In this paper, we neglect the effect of $1/f$ noise because it introduces only slow phase variations in the oscillator. Such variations are suppressed by the large loop bandwidth of PLL's used in today's digital systems.

As derived in the Appendix, for white noise sources in the oscillator, the single-sideband phase noise S_ϕ (phase noise with respect to the carrier) can be expressed in terms of the cycle-to-cycle jitter according to

$$S_\phi(\omega) = \frac{\left(\omega_0^3/4\pi\right)\Delta T_{\rm cc}^2}{(\omega-\omega_0)^2 + \left(\omega_0^3/8\pi\right)^2 \Delta T_{\rm cc}^4} \approx \frac{\left(\omega_0^3/4\pi\right)\Delta T_{\rm cc}^2}{(\omega-\omega_0)^2} \tag{7}$$

where ω_0 is the oscillation frequency and $\omega - \omega_0$ is the offset frequency. The Appendix also shows that the cycle-to-cycle jitter can be deduced from the phase noise according to

$$\Delta T_{\rm cc}^2 \approx \frac{4\pi}{\omega_0^3} S_\phi(\omega)(\omega-\omega_0)^2. \tag{8}$$

To obtain an estimate of the thermal jitter, we consider the differential CMOS ring oscillator in [5]. For the 2.2-GHz oscillator with a phase noise of -94 dBc/Hz at 1 MHz offset, we obtain from (8) a thermal cycle-to-cycle jitter of 0.3 ps, i.e., less than 0.3°. Similar values are obtained for the 900-MHz CMOS ring oscillators reported in [6]. In most timing applications, such small values are negligible with respect to other sources of random jitter.

The thermal absolute jitter is proportional to the square root of the measurement interval Δt. As derived in the Appendix, the absolute jitter is given by

$$\Delta T_{\rm abs} = \sqrt{\frac{f_0}{2}} \Delta T_{\rm cc} \sqrt{\Delta t}. \tag{9}$$

In [9], the rms value of absolute jitter has been divided by the square root of the measurement time to obtain a time-independent figure of merit. This is not possible for supply and substrate noise, since (7)–(9) are derived for white noise in the feedback loop. Supply and substrate noise, however, are generally not white.

[1] In this paper, we use a time average definition of jitter which is equivalent to the stochastic average if and only if the process ΔT^2 is ergodic.

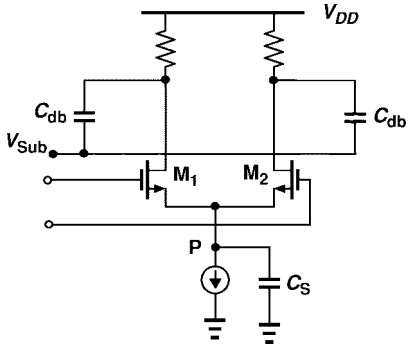


Fig. 4. Illustration of frequency modulation through changes of drain junction capacitances.

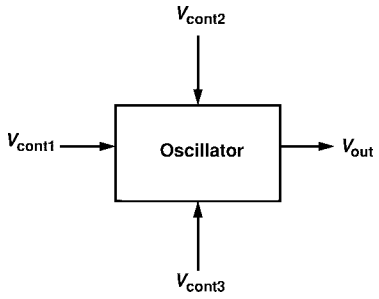


Fig. 5. Illustration of the VCO model of an oscillator.

V. Jitter of a Frequency-Modulated Oscillator

The frequency of an oscillator generally depends on the supply and substrate voltage. The variation of the oscillation frequency with a voltage may be described by a sensitivity function, also called the gain of the VCO and denoted by $K_{\rm VCO}$.

For example, as shown in Fig. 4, the drain junction capacitance of M_1 and M_2 varies with $V_{\rm DD}$ and $V_{\rm Sub}$, thus modulating the frequency of the ring oscillator. In some cases, $K_{\rm VCO}$ itself may be a function of the modulating frequency. In Fig. 4, for example, high-frequency supply noise results in fast changes in V_P and hence substantial displacement current through C_S (the capacitance contributed by M_1, M_2, and the current source). Note that, in general, the frequency of an oscillator depends on various bias and supply voltages, as conceptually illustrated in Fig. 5.

An oscillator subject to supply and substrate noise may be considered as a VCO with different "control" voltages each having a different sensitivity. In this section, we attribute the cycle jitter and the cycle-to-cycle jitter of a frequency-modulated oscillator to the static sensitivity K_0. As shown in Sections VI and VII, these expressions describe supply and substrate noise quite accurately.

Let the modulating control voltage be a small sinusoidal perturbation

$$\Delta V_m(t) = V_m \cos \omega_m t. \tag{10}$$

We assume, as an approximation, that the frequency change follows the control voltage according to

$$\Delta f_0(t) = V_m K_0 \cos \omega_m t \tag{11}$$

where K_0 is the static sensitivity, also called low-frequency VCO gain. This approximation is referred to as quasi-static approximation in the remainder. The deviation of the period from the mean is

$$\Delta T(t) = \frac{1}{f_0 + \Delta f_0(t)} - \frac{1}{f_0} \tag{12}$$

$$\approx -\frac{V_m K_0}{f_0^2} \cos \omega_m t. \tag{13}$$

Multiplying this expression by $\Delta T(t+\tau)$ and averaging the result with respect to t, we obtain the steady-state ACF

$$\overline{\Delta T(t+\tau)\Delta T(t)} = \frac{V_m^2 K_0^2}{2 f_0^4} \cos \omega_m \tau. \tag{14}$$

This quantity represents the ACF of the process $\Delta T(t)$ in a continuous-time description. For the evaluation of the jitter according to (5) and (6), we need the values $C(0)$ and $C(1)$ of the discrete-time ACF. If the ACF does not change significantly during one oscillation period, these values can be determined from the continuous-time ACF at time points $\tau = 0 \times \bar{T}$ and $\tau = 1 \times \bar{T}$. A numerical verification of this approach is given below.

Inserting (14) with $\tau = 0$ in (5), we find the cycle jitter

$$\Delta T_c = \frac{V_m K_0}{\sqrt{2} f_0^2}. \tag{15}$$

For $\tau = 0$ and $\tau = \bar{T} = 1/f_0$, we obtain from (6) and (14) the cycle-to-cycle jitter

$$\Delta T_{\rm cc} = \frac{V_m K_0}{f_0^2} \sqrt{1 - \cos(\omega_m / f_0)}. \tag{16}$$

Equations (15) and (16) express the jitter in terms of the low-frequency sensitivity and the modulation frequency. They will be verified numerically in Sections VI and VII. The main benefit of these equations is that the calculation of the jitter is reduced to the calculation or measurement of the oscillation frequency as a function of the supply or substrate voltage.

From (15), we note that cycle jitter is independent of frequency so long as the quasi-static approximation (11) holds. By contrast, cycle-to-cycle jitter increases with frequency. For $f_m \ll f_0$ we find from (16)

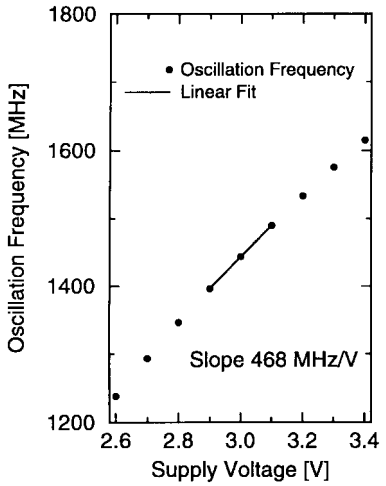
$$\Delta T_{\rm cc} \approx \frac{V_m K_0 \omega_m}{\sqrt{2} f_0^3}. \tag{17}$$

Note that the cycle-to-cycle jitter $\Delta T_{\rm cc}$ is approximately proportional to the modulation frequency f_m. This can be interpreted by noting that $\Delta T_{\rm cc}$ is a double-differential quantity, as is evident from (5) and (6).

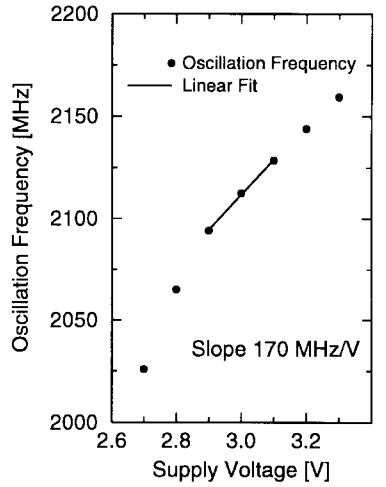
Having reduced the jitter calculation to the static sensitivity K_0, we need to extract this quantity from simulations. For this purpose, we apply a dc voltage perturbation to the supply. Fig. 6 shows the oscillation frequency of the SERO and the DRO as a function of the supply voltage. The frequency varies linearly with the supply voltage over a relatively wide range of $V_{\rm DD}$. The slope of the curves in Fig. 6 represents the low-frequency sensitivity K_0, indicating that the SERO is much more sensitive than the DRO. Using these values in (15) and (16), we can predict the jitter from supply and substrate noise easily.

VI. Jitter Due to Supply Noise

The supply and substrate noise created in a digital system is quite complex. In addition to components at the clock frequency and harmonics and subharmonics thereof, the noise spectrum generally exhibits random signals resulting from the activities of each building block as well. A rigorous treatment requires that the noise spectrum be measured in a realistic environment and subsequently incorporated in the analysis as explained in Section V.

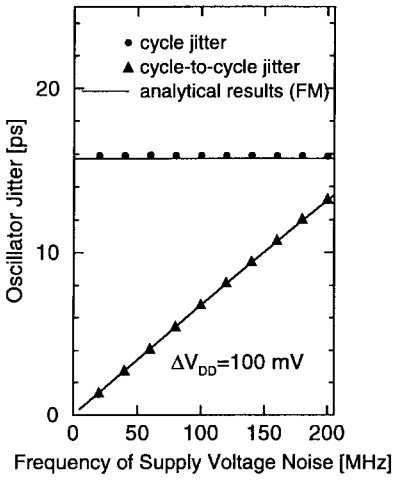


(a)

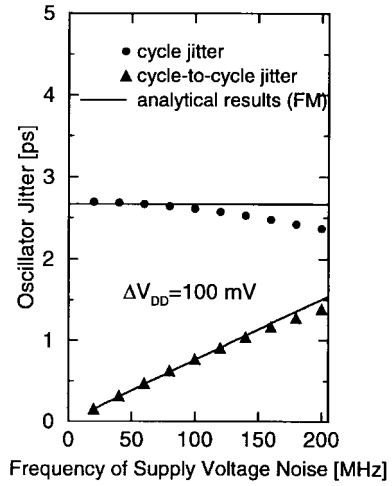


(b)

Fig. 6. Oscillation frequency of (a) the single-ended ring oscillator and (b) the differential ring oscillator as a function of static supply voltage.



(a)



(b)

Fig. 7. Cycle jitter and cycle-to-cycle jitter of (a) the SERO and (b) the DRO as a function of supply voltage noise frequency. The solid lines represent the quasi-static FM expressions.

In the following, we investigate the jitter due to sinusoidal supply voltage perturbations. The calculation of the jitter consists of the following steps: interpolation of the voltage waveform to find the zero crossings; calculation of the periods T_n and subtraction of the mean period $\bar{T}$ to obtain ΔT_n; and calculation of the cycle jitter (2) and the cycle-to-cycle jitter (3) by performing time averaging.

We should also mention that simulations indicate that jitter has a relatively linear dependence on the noise amplitude for supply variations as large as a few hundred millivolts.

Fig. 7 plots the analytical and simulated cycle and cycle-to-cycle jitter of single-ended and differential ring oscillators. As can be seen, the analytical results of Section V predict the jitter with reasonable accuracy.

VII. Jitter Due to Substrate Noise

Substrate noise can be treated in the same fashion as supply noise. For the numerical simulation of substrate noise, the bulk terminal of the transistors is driven by a noise source (Fig. 8). Fig. 9 shows the calculated jitter of the DRO as a function of the noise frequency. Comparison with Fig. 7 indicates that for the DRO, a supply voltage perturbation is almost equivalent to a substrate voltage perturbation of opposite sign. To understand this, note from Fig. 10 that, with an ideal tail current source, a change of ΔV in $V_{\rm DD}$ is equivalent to a change

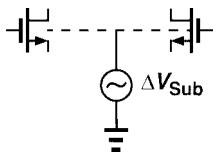


Fig. 8. Substrate noise modeling.

of $-\Delta V$ in $V_{\rm sub}$. Simulations confirm that the static sensitivity K_0 is indeed equal for supply and substrate noise, apart from the sign. Fig. 9 also demonstrates that the quasi-static FM approach is suited to describing the jitter introduced by substrate noise. Furthermore, it suggests that a substantial fraction of the jitter results from the voltage dependence of $C_{\rm db}$ and $C_{\rm sb}$.

VIII. Oscillator Design for Low Jitter

The simulation results presented thus far indicate the superior performance of differential oscillators with respect to single-ended topologies. Nonetheless, even differential configurations have a wide design space; device size, voltage swings, power dissipation, and the number of stages in a ring oscillator influence the overall sensitivity to supply and substrate noise.

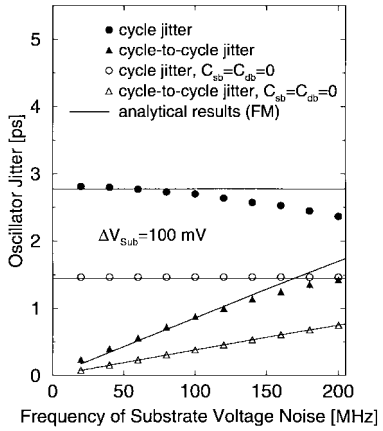


Fig. 9. Cycle jitter and cycle-to-cycle jitter of the DRO versus substrate voltage noise frequency. Solid lines represent the quasi-static FM expressions. The empty symbols show the jitter with the drain-bulk and source-bulk capacitances set to zero.

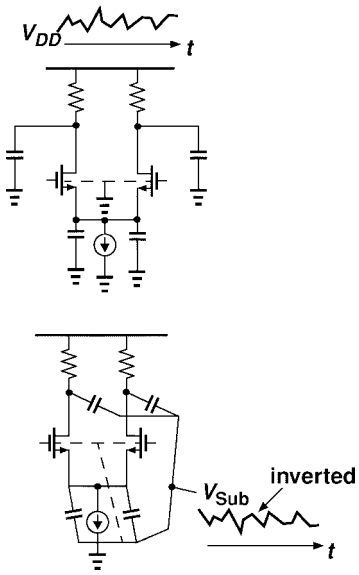


Fig. 10. Illustration of the equivalence of supply and substrate noise for the DRO.

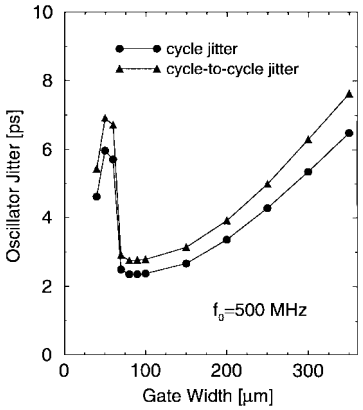


Fig. 11. Jitter of the DRO versus gate width.

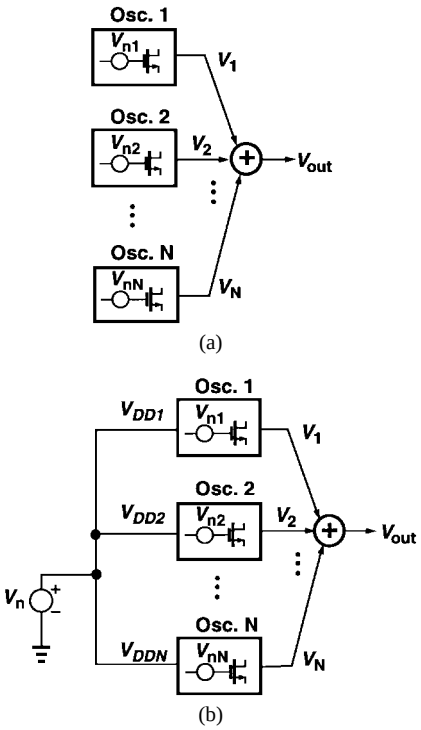


Fig. 12. Illustration of the relationship between power consumption and noise for (a) device electronic noise and (b) supply noise.

In this section, we study jitter as a function of three parameters: transistor gate width, power dissipation, and the number of stages. To make meaningful comparisons, the circuit is modified in each case such that the frequency of oscillation remains constant. These parameters also affect the thermal jitter to some extent, but, considering the vastly different designs reported in [5] and [6], we note that this type of jitter still remains negligible.

A. Effect of Transistor Gate Width

The differential three-stage ring oscillator of Fig. 2 begins to oscillate for $W \geq 30\ \mu$m.

Fig. 11 shows the effect of the gate width on the jitter, where the oscillation frequency is kept constant by adjusting C_L in Fig. 2. The jitter reaches a minimum for $W \approx 80\,\mu$m. For large W, the value of C_L must be reduced so as to maintain the same oscillation frequency, yielding a larger voltage-dependent fraction due to drain and source junctions of each device and hence a higher sensitivity to noise.

B. Effect of Power Consumption

The jitter resulting from device electronic noise generally exhibits an inverse dependence upon the oscillator power dissipation [5], [10]. By contrast, the effect of supply and substrate noise on the jitter of a given oscillator topology is relatively independent of the power drain. This can be understood with the aid of the conceptual illustrations in Fig. 12, where the output voltages of N identical oscillators are added in phase. In Fig. 12(a), only the device electronic noise is considered [5]. Since the noise in each oscillator is uncorrelated, the output noise voltage is $\sqrt{N}$ times that of each oscillator, whereas the output signal voltage is $N \times V_j$. In Fig. 12(b), on the other hand, all oscillators are disturbed by the same noise source, thus exhibiting completely correlated noise. That is, both the noise voltage and the signal voltage are increased by a factor of N.

To confirm the above observation, the gate width and tail current were decreased while the load resistance was increased proportionally. Table I shows that the jitter is quite constant.

C. Effect of Number of Stages

In applications where the required oscillation frequency is considerably lower than the maximum speed of the technology, a ring

TABLE I
IMPACT OF POWER CONSUMPTION

I_{ss} [mA]	R_L	W [μm]	ΔT_c [ps]	ΔT_{cc} [ps]
4	250	320	2.51	1.49
2	500	160	2.51	1.50
1.33	750	106	2.49	1.49
1	1000	80	2.49	1.48
0.8	1250	64	2.49	1.51
0.67	1500	53	2.50	1.49

TABLE II
THREE-STAGE VERSUS SIX-STAGE OSCILLATOR

n	W [μm]	C_L [fF]	R_L [Ω]	ΔT_c [ps]	ΔT_{cc} [ps]
3	40	535	1000	4.62	5.44
3	60	540	1000	5.71	6.72
3	80	535	1000	2.35	2.74
3	100	515	1000	2.38	2.80
3	150	420	1100	2.65	3.12
3	200	320	1200	3.37	3.97
3	250	220	1300	4.43	5.21
3	358	0	1500	7.58	8.76
6	40	265	550	8.09	9.48
6	60	260	530	3.96	4.59
6	80	235	530	3.85	4.52
6	100	200	530	4.25	5.00
6	150	110	530	5.33	6.27
6	207	0	530	6.78	7.98

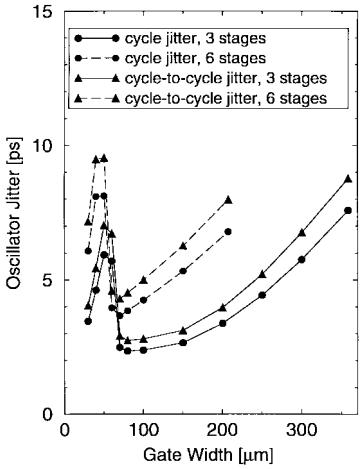


Fig. 13. Jitter of the three-stage and the six-stage DRO versus gate width for an oscillation frequency of 500 MHz.

oscillator may incorporate more than three stages. Thus, the optimum number of stages with respect to the jitter is of interest.

Shown in Table II and plotted in Fig. 13 is the jitter of three-stage and six-stage oscillators designed for a frequency of 500 MHz with constant tail current and voltage swings. We note that the minimum values of cycle jitter and cycle-to-cycle jitter are smaller in a three-stage topology. This is because for the three-stage oscillator, the reduction of the oscillation frequency to the desired value is obtained by means of the fixed capacitances C_L rather than by the voltage-dependent capacitances of the transistors. Hence, a smaller fraction of the total load capacitance is subject to variations with supply and substrate noise.

The addition of a fixed capacitor to each stage nonetheless entails the issue of substrate noise coupling to the bottom plate of the capacitor. In order to minimize this effect, a grounded shield must isolate the capacitor from the substrate, as illustrated in Fig. 14. Here,

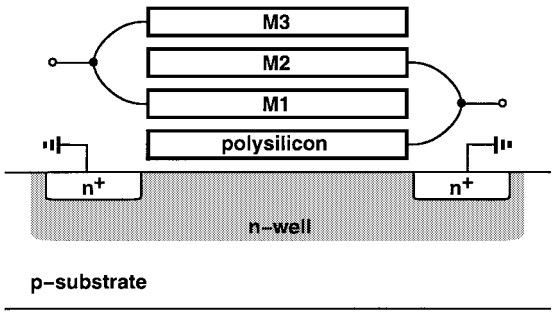


Fig. 14. Grounded shield used under the capacitor to block substrate noise.

an n-well, grounded by a low-resistance n^+ ring, is placed under the capacitor so as to block the noise produced in the substrate.

IX. CONCLUSION

We have investigated the timing jitter in oscillators subject to supply and substrate noise. For digital timing applications, the effect of supply and substrate noise on the jitter is typically much more pronounced than that of thermal noise. For supply and substrate noise, we have derived analytical relationships between the cycle-to-cycle jitter and the low-frequency sensitivity of the oscillation frequency to supply or substrate noise. These relationships have been verified by means of numerical calculations for single-ended and differential CMOS ring oscillators. For differential ring oscillators, we have investigated the dependence of the jitter on the transistor gate width, power consumption, and the number of stages. As a special result, we have found that in applications where the required oscillation frequency is lower than the maximum speed of the technology, a three-stage ring oscillator with additional load capacitances gives the lowest jitter.

APPENDIX
JITTER AND PHASE NOISE DUE TO THERMAL AND SHOT NOISE

The output voltage of an oscillator can be written as

$$V(t) = V_0 \cos[\omega_0 t + \phi(t)] \tag{18}$$

where V_0 is the amplitude, ω_0 is the oscillation frequency, and $\phi(t)$ is the slowly varying excess phase. The excess frequency is

$$\Delta\omega(t) = \frac{d}{dt}\phi(t) \tag{19}$$

and hence

$$\phi(t) = \int_0^t \Delta\omega(u)\, du + \phi(0). \tag{20}$$

Thermal and shot noise may be considered as white noise since their cutoff frequencies are typically much higher than the oscillation frequency. White noise in the feedback loop of the oscillator results in phase diffusion, a phenomenon described by a Wiener process [11]. Extensive investigations of phase noise indicate that white noise sources in all types of oscillators give rise to a phase noise power spectrum proportional to $1/(\Delta\omega)^2$, where $\Delta\omega$ is the offset frequency with respect to the carrier frequency [4], [5]. This trend is valid for offset frequencies as high as several percent of the carrier frequency. Thus, *frequency* noise, $\Delta\omega(t)$, can be assumed white in such a band. The autocorrelation of $\Delta\omega(t)$ is given by

$$\overline{\Delta\omega(t+\tau)\Delta\omega(t)} = 2D_\phi\delta(\tau) \tag{21}$$

where D_ϕ is the diffusivity and $\delta(\tau)$ the Delta function. The probability density of $\phi(t)$ represents a Gaussian distribution centered

at $\phi(0)$ with the variance

$$\sigma_\phi^2 = 2D_\phi t. \tag{22}$$

As evident from (22), the variance diverges with time. The autocorrelation of $V(t)$ is known [12] and reads

$$\langle V(t+\tau)V(t)\rangle = \frac{V_0^2}{2}\exp(-D_\phi|\tau|)\cos(\omega_0\tau). \tag{23}$$

Performing the Fourier transformation, we obtain the one-sided power spectral density

$$S_V(\omega) = V_0^2\frac{D_\phi}{(\omega-\omega_0)^2+D_\phi^2}. \tag{24}$$

This quantity is often normalized to $V_0^2/2$ and referred to as relative phase noise with respect to the carrier [5] or as single-sideband phase noise [8], given by

$$S_\phi(\omega) = \frac{2D_\phi}{(\omega-\omega_0)^2+D_\phi^2}. \tag{25}$$

For $\omega-\omega_0 \gg D_\phi$, we obtain from (25)

$$S_\phi(\omega) \approx \frac{2D_\phi}{(\omega-\omega_0)^2}. \tag{26}$$

Next, we will relate the cycle-to-cycle jitter and the single-sideband phase noise to each other. Note that the stationary Wiener process has no memory and the increments in different time intervals are statistically independent [11]. Therefore, the rms mean increment of the excess phase $\phi(t)$ within one cycle, i.e., the cycle jitter of the phase, equals the increment of $\phi(t)$ between $t=0$ and $t=\bar{T}$. Thus, from (22), we obtain the phase cycle jitter as

$$\Delta\phi_c = \sqrt{2D_\phi\bar{T}}. \tag{27}$$

The excess phase change during the nth cycle is referred to as $\Delta\phi_n$. The nth oscillation period is defined by the relation

$$2\pi f_0 T_n = 2\pi + \Delta\phi_n. \tag{28}$$

For the deviation of the nth period T_n from the mean period $\bar{T} = 1/f_0$, we then find

$$\Delta T_n = \frac{\Delta\phi_n}{2\pi f_0} = \Delta\phi_n\frac{\bar{T}}{2\pi}. \tag{29}$$

Hence, the cycle jitter ΔT_c of the period during one cycle is related to $\Delta\phi_c$ according to

$$\Delta T_c = \Delta\phi_c\frac{\bar{T}}{2\pi}. \tag{30}$$

For white noise sources, two successive periods are uncorrelated. Since cycle-to-cycle jitter represents the difference between two periods, the variance of cycle-to-cycle jitter is twice as large as the variance of one period, yielding

$$\Delta T_{\rm cc} = \sqrt{2}\Delta T_c. \tag{31}$$

Combining (27), (30), and (31), we obtain

$$\Delta T_{\rm cc}^2 = \frac{8\pi}{\omega_0^3}D_\phi \tag{32}$$

with

$$\omega_0 = \frac{2\pi}{\bar{T}}. \tag{33}$$

The cycle-to-cycle jitter can now be expressed in terms of the single-sideband phase noise by inserting (32) in (26) to give

$$\Delta T_{\rm cc}^2 \approx \frac{4\pi}{\omega_0^3}S_\phi(\omega)(\omega-\omega_0)^2. \tag{34}$$

On the other hand, the phase noise can be expressed by the cycle-to-cycle jitter by inserting (32) in (25), yielding

$$S_\phi = \frac{\left(\omega_0^3/4\pi\right)\Delta T_{\rm cc}^2}{(\omega-\omega_0)^2+\left(\omega_0^3/8\pi\right)^2\Delta T_{\rm cc}^4}. \tag{35}$$

A similar expression has been derived for ring oscillators in [10] and reads in our notation

$$S_\phi = \frac{f_0^3\,\Delta T_c^2}{(f-f_0)^2} \tag{36}$$

where $f_0 = \omega_0/2\pi$. Equation (36) turns out to be a special case of (35) for $\omega-\omega_0 \gg D_\phi$.

The absolute jitter increases proportionally to the square root of the measurement interval Δt as evident from (22). Hence, the absolute phase jitter is

$$\Delta\phi_{\rm abs} = \sqrt{2D_\phi\Delta t} = \kappa\sqrt{\Delta t}. \tag{37}$$

Using (32), the proportionality constant κ can be related to the cycle-to-cycle jitter according to

$$\kappa = \sqrt{2D_\phi} = \sqrt{2}\pi f_0^{3/2}\Delta T_{\rm cc}. \tag{38}$$

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