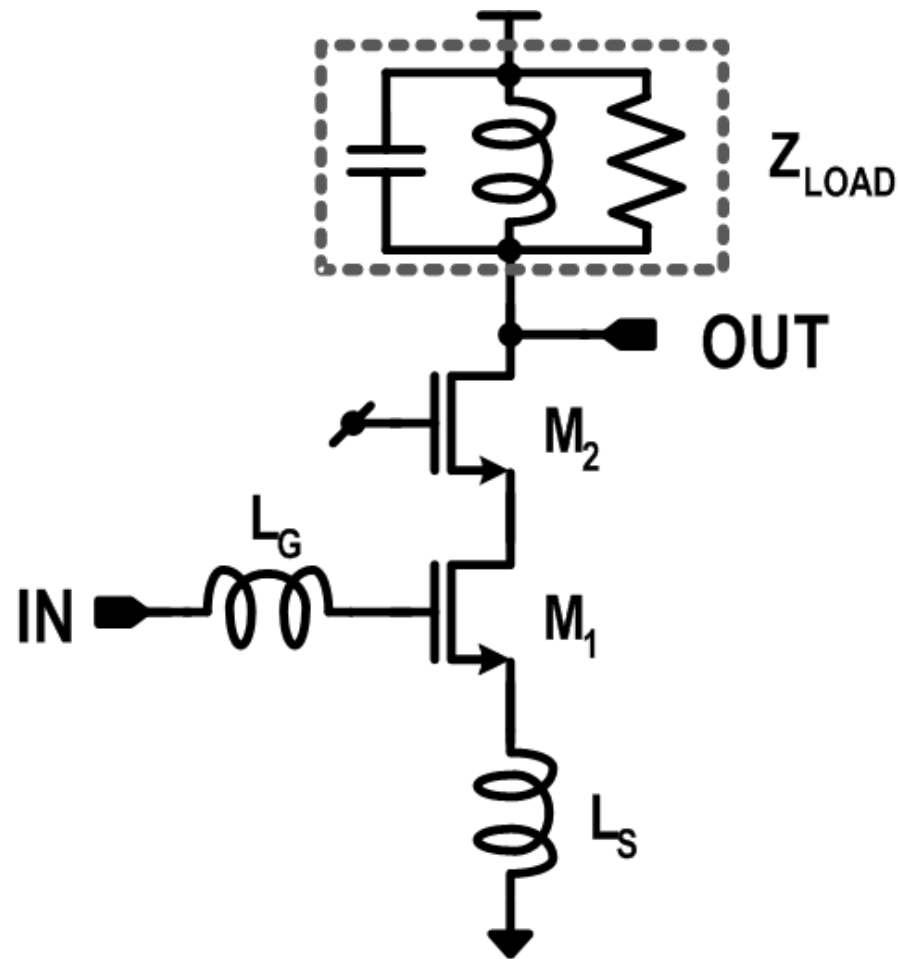


Inductively Degenerated LNA

University of Pavia
<http://www.unipv.it/aic/>

Inductively degenerated LNA



$$Z_{IN} = j\omega(L_S + L_G) + \frac{1}{j\omega C_{gs}} + \left(\frac{g_m}{C_{gs}} \right) L_S$$

$$\omega_0 = \frac{1}{\sqrt{(L_G + L_S) \cdot C_{gs}}}$$

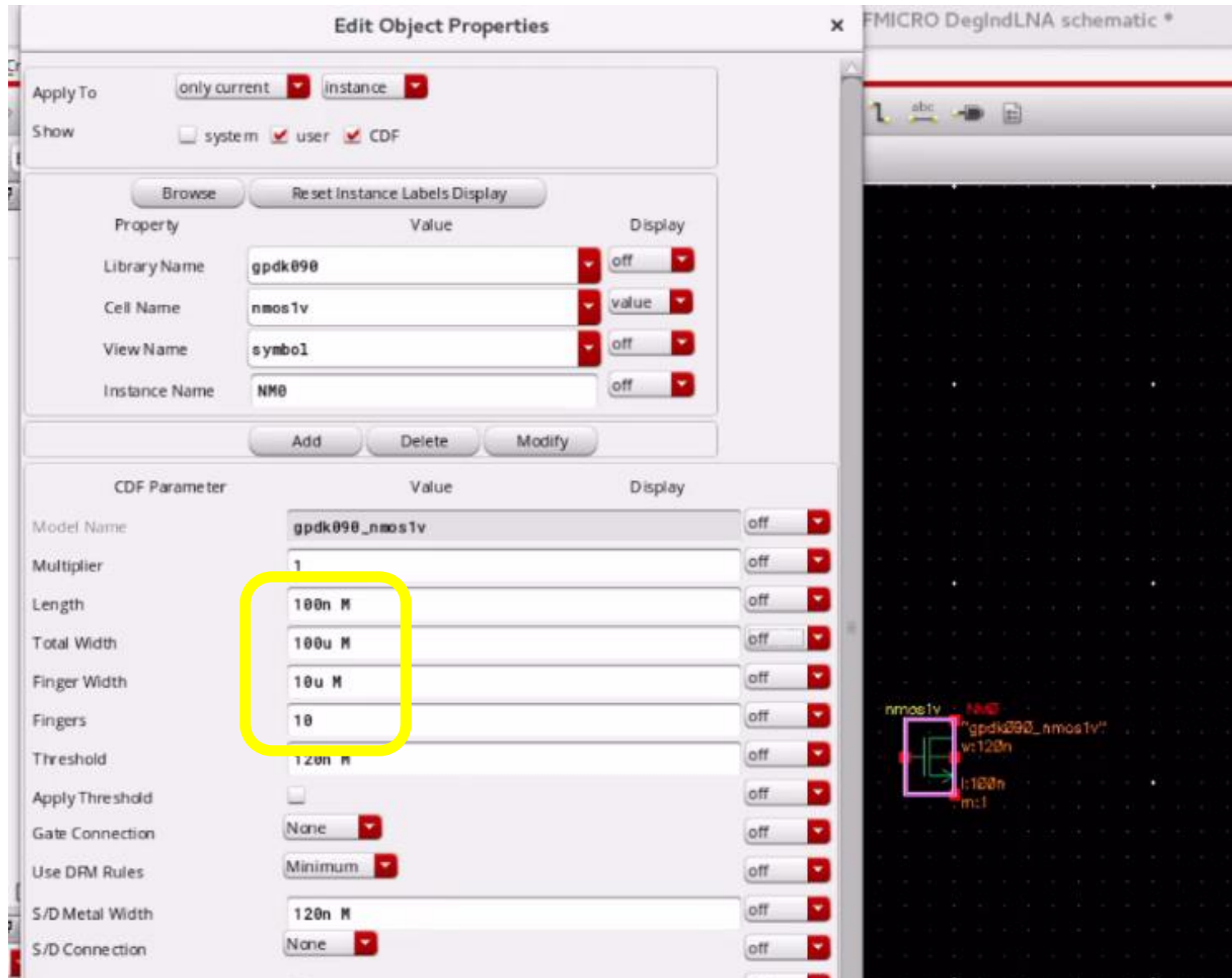
$$Z_{IN} = \left(\frac{g_m}{C_{gs}} \right) L_S = \omega_T L_S = R_S$$

Gain:

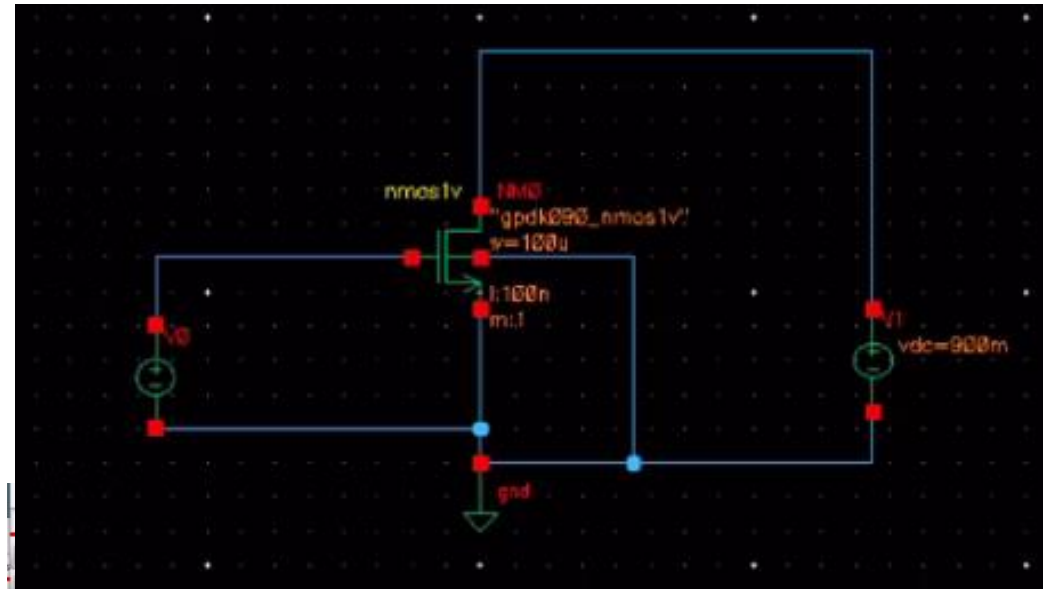
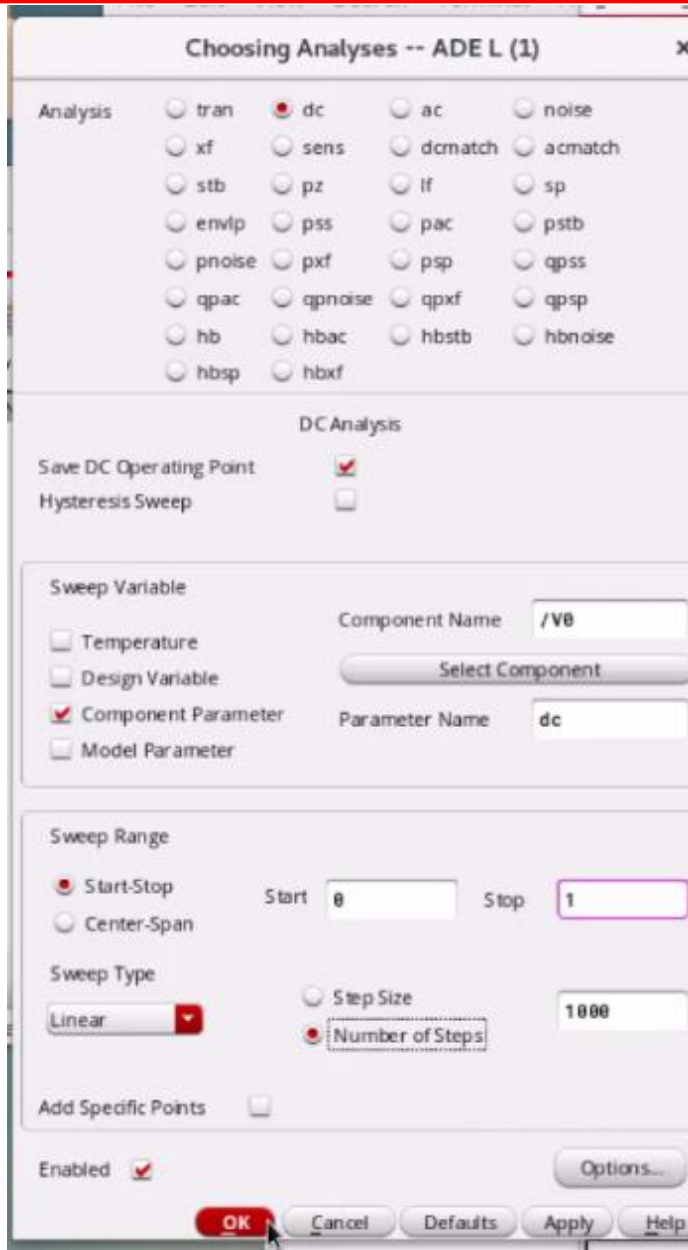
$$\frac{V_{OUT}}{V_{IN}} = G_m Z_L = Q_{IN} g_m Z_L$$

$$Q_{IN} = \frac{1}{2R_S \omega_0 C_{gs}}$$

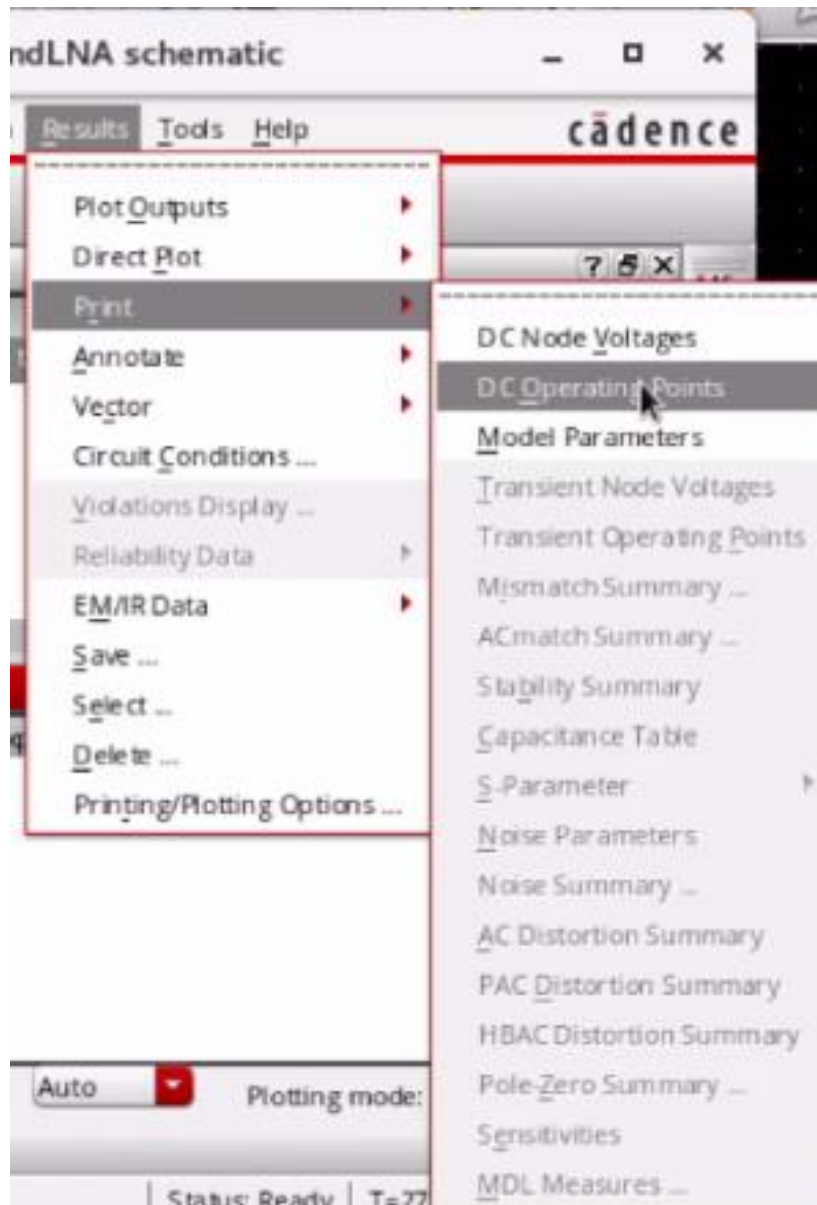
Input transistor: W/L=100/0.1



DC sweep to find $I_{bias}=4mA$



How to Choose Ls and Lg



The screenshot shows the 'Results Display Window' in Cadence. It contains a table of circuit parameters. Two rows are highlighted with yellow boxes: 'cgs' with a value of -133.008f and 'gm' with a value of 51.4239m.

Window	Expressions	Info	Help
cgdov1	48.2736f		
cgg	183.772f		
cgs	-133.008f		
cgsb1	-81.4085f		
cgsov1	50.5992f		
cjd	12.5464f		
cjs	17.8542f		
csb	-21.8026f		
csd	-7.33692f		
csg	-113.041f		
css	142.18f		
cssb1	73.7267f		
fug	44.5354G		
gbd	215.087n		
gbs	0		
gm	51.4239m		
gmbs	2.96344m		
gmoverid	12.4592		
i1	4.12741m		
i3	-4.1274m		
i4	-17.1604n		
ibd	-17.1603n		
ibe	-17.1613n		
ibs	-58.091f		
ibulk	-17.1604n		
id	4.12741m		
idb	48.4748f		
ide	4.12741m		
ids	4.1274m		
igb	0		
igcd	0		
iges	0		
igd	-52.2596p		

s-parameters simulation

Choosing Analyses -- ADE L (1)

Analysis

<input type="radio"/> tran	<input type="radio"/> dc	<input type="radio"/> ac	<input type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input checked="" type="radio"/> sp
<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpssp
<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
<input type="radio"/> hbsp	<input type="radio"/> hbx		

S-Parameter Analysis

Ports

Select Clear

/PORT0

Sprobes

Select Clear

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop

Start 100M Stop 5G

☐ Center-Span

Sweep Type

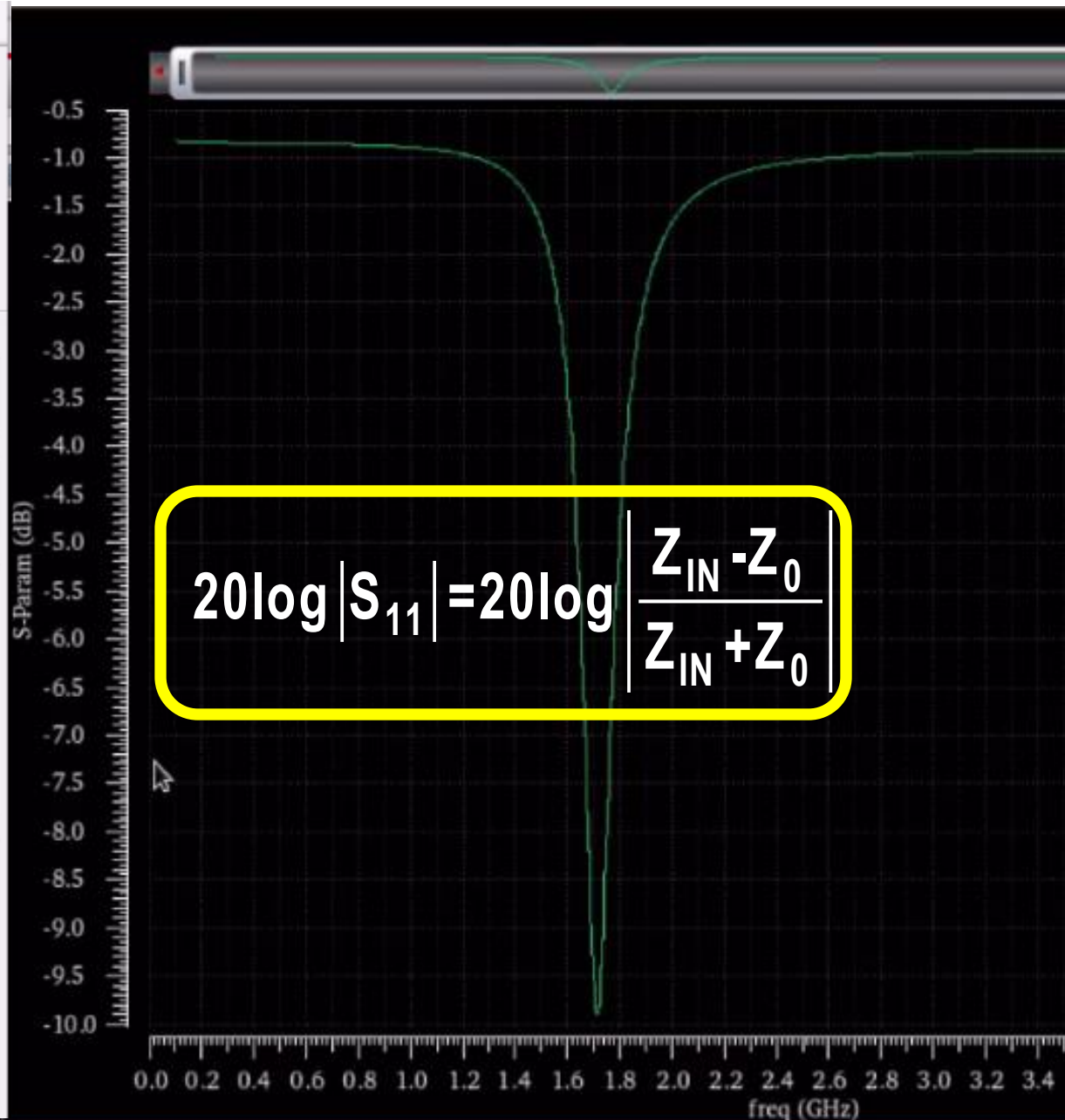
Linear

☐ Step Size

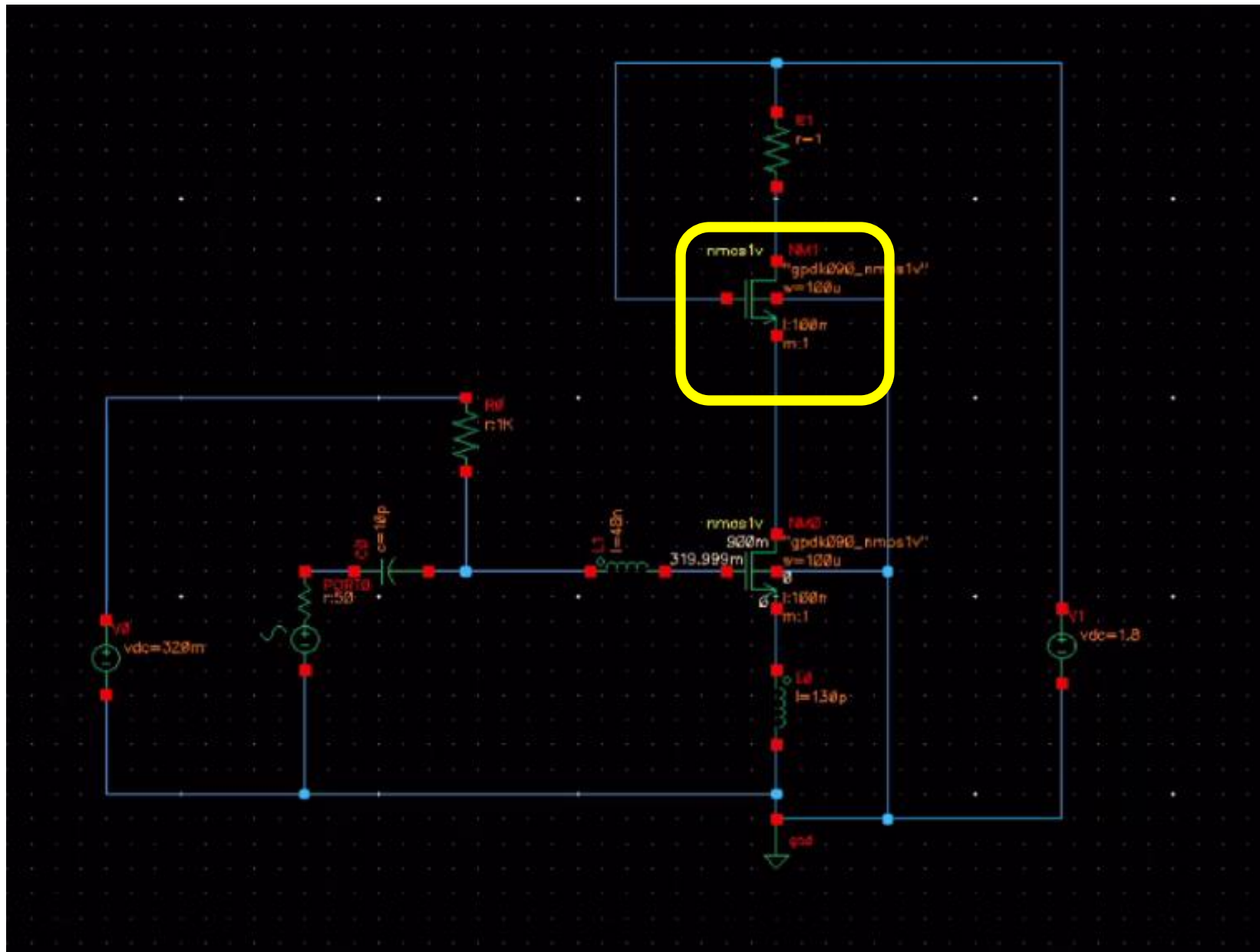
1000

☒ Number of Steps

Add Specific Points



Adding the cascode



Transconductance Gain Simulation $G_m = Q_{in} g_m$

Choosing Analyses -- ADE L (1) x

Analysis

<input type="radio"/> tran	<input type="radio"/> dc	<input checked="" type="radio"/> ac	<input type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input type="radio"/> sp
<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpssp
<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
<input type="radio"/> hbqp	<input type="radio"/> hbxp		

AC Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop

Start: 100M Stop: 5G

☐ Center-Span

Sweep Type

Linear

☐ Step Size

1000

☒ Number of Steps

Add Specific Points

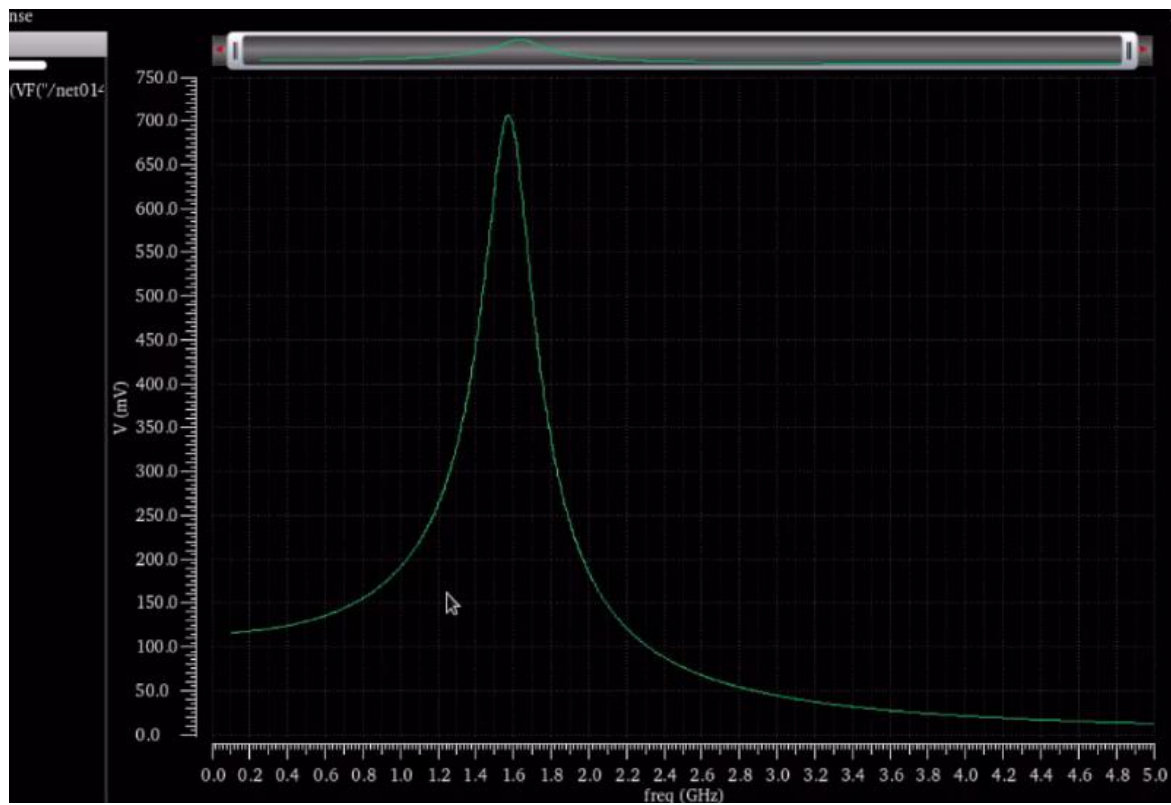
Specialized Analyses

None

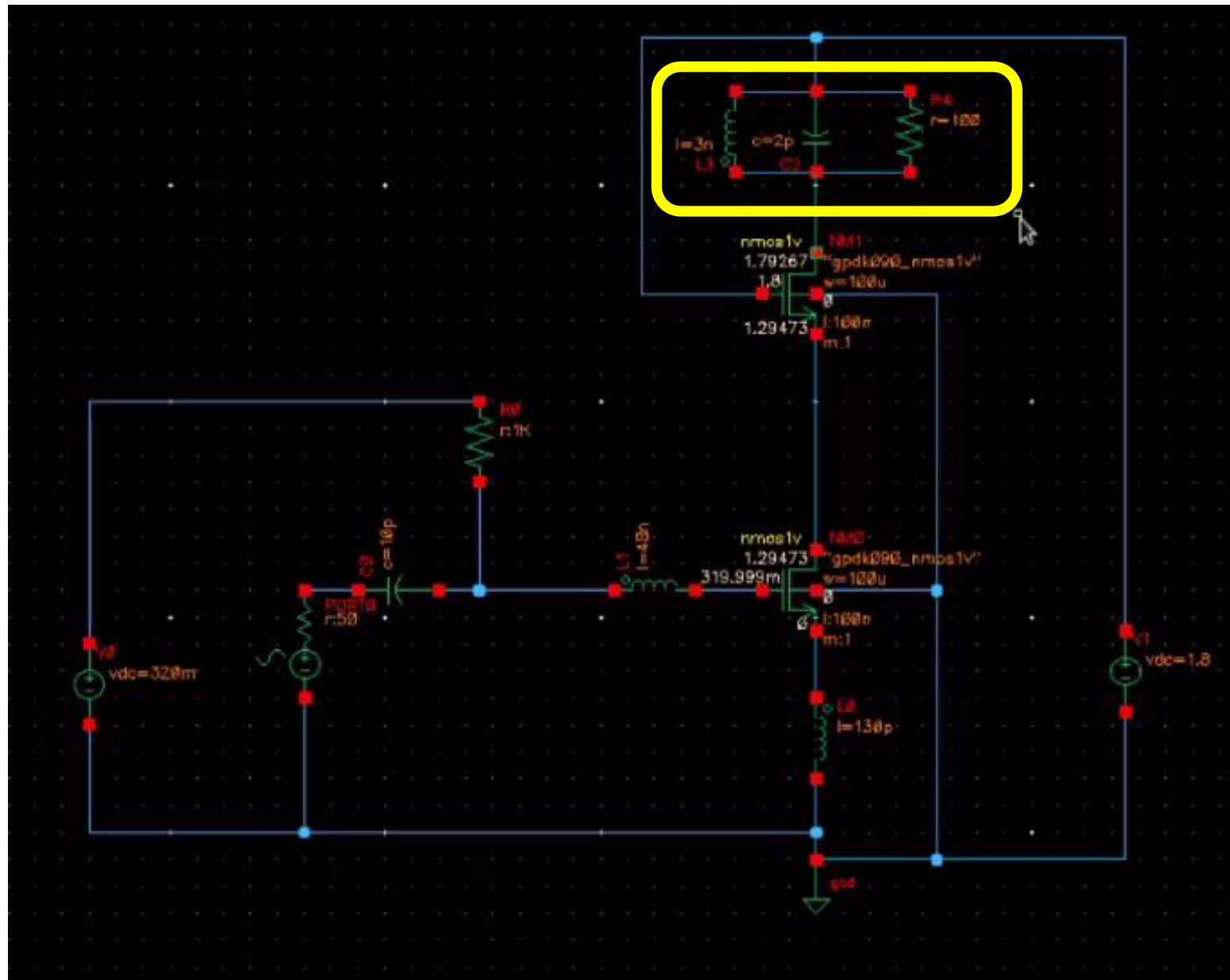
Enabled ☒

Options...

OK Cancel Defaults Apply Help



RLC Load and Voltage Gain of the stage



Noise Figure Simulation

Choosing Analyses -- ADE L (1) x

Analysis

<input type="radio"/> tran	<input type="radio"/> dc	<input type="radio"/> ac	<input checked="" type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input type="radio"/> sp
<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpssp
<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
<input type="radio"/> hbsp	<input type="radio"/> hbxf		

Noise Analysis

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

☐ None

Sweep Range

☒ Start-Stop

Start Stop

☐ Center-Span

Sweep Type

☐ Step Size

☒ Number of Steps

Add Specific Points

Output Noise

Positive Output Node

Negative Output Node

Input Noise

Input Port Source

Noise Separation

Separate noise into source and gain

Enabled ☒



Question #1

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What is the way to get the values of L_s and L_g inductances?

1. Finding the L_s :

A) Analysis 1: From the input impedance of the circuit Z_{in} , we can find the real component $L_s g_m / C_{gs} = R_{in}$, we know the R_{in} by the design it is the standard 50ohm \Rightarrow from this analysis L_s can be obtained because we know the C_{gs} and G_m from the transistor bias conditions.

B) Analysis 2: at the unity gain frequency W_t is inversely proportional to the Quality factor of the input matching circuit $W_t = 1/Q_t$ which gives the room for analysis of the amplifier parameters and the matching circuit.
 $W_t = G_m / C_{gs} \Rightarrow R_{in} / L_s$

2. Finding of the L_g :

L_g is added to the circuit to give the extra freedom to the matching circuit to design L_g can be directly found from the input resonance frequency $W_o = 1 / \sqrt{(L_s + L_g) * C_{gs}}$



Question #2

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Are 10pF and 1Kohms enough for our 2 GHz design? Why?

1. Adding the R1 : Resistor R1 is added to bias the circuit which is to protect the circuit from the dc bias circuit , gate current of the MoSFET is in terms of nA so it is enough that 1kohm bias resistor
2. Adding the C1: C1 is used for to isolate the DC circuit from the RF , 10Pf farade pretty manageable to block the dc from the bias circuit.
3. R1 and C1 Analysis : The time constant of the R1C1 is 10nS and the input RF frequency is 50nS so the , RF can pass through circuit and blocked to affect the DC bias circuit.



Question #3

How can I tweak the design to improve my matching performance?

Sharp Input Matching can be obtained in three techniques:
(Reflection coefficient at the input depends)

1. Input Q factor (tune the input matching circuit)
2. Increase the gain (essential increasing the g_m \rightarrow increase the v_{gs})
3. Tune the Z_I (increase)



Question #3

How can I tweak the design to improve my matching performance?

1. Input Q factor (tune the input matching circuit)

At the high frequency Transistor parasitic parameters play a great role without in usual design the C_{gd} is neglected, by considering the C_{gd} at the high frequency S_{11} improved from -11dB to -13dB (without considering the load match)

Problems addressed from this method:

1. Improved the input reflections (S_{11})
2. Addressed resonance Frequency drift (shifting matching frequency) 1.7GHz to 1.99GHz

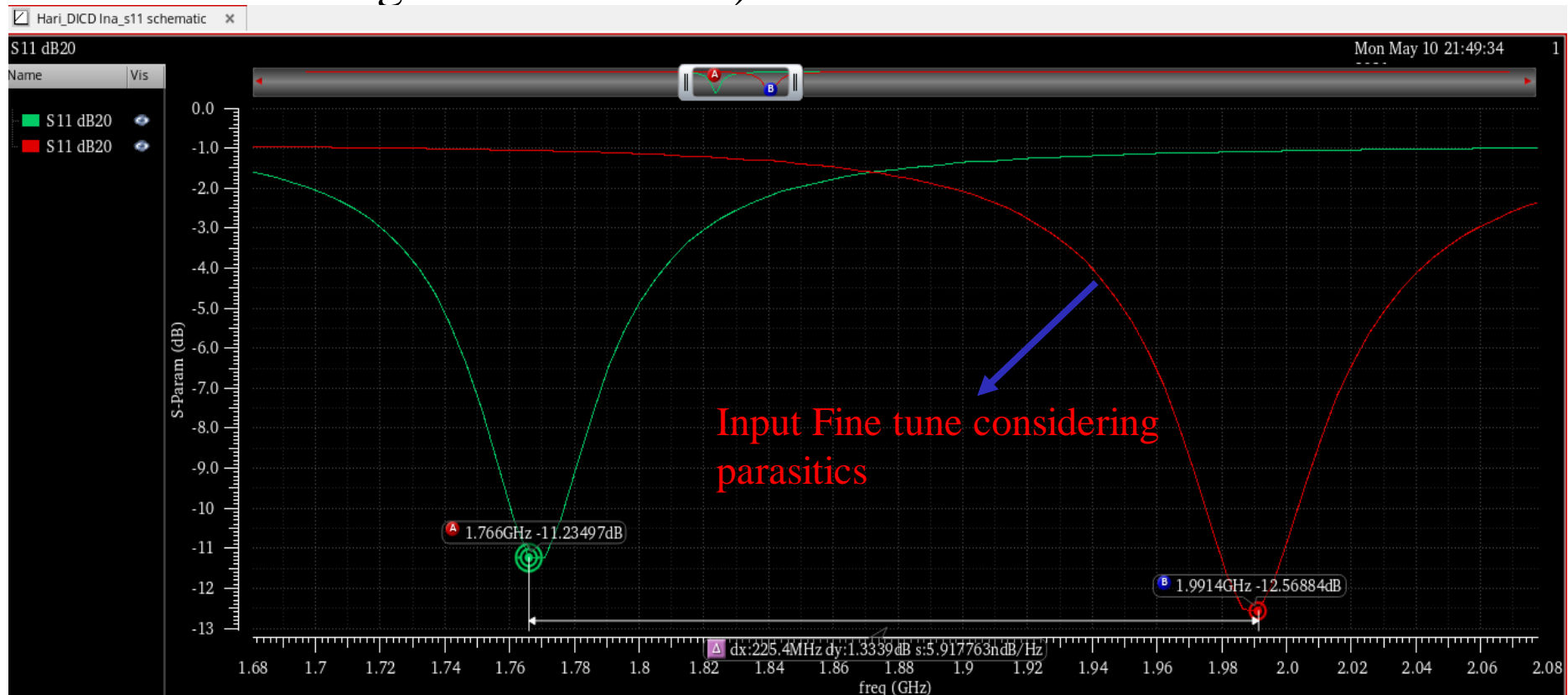


Question #3

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How can I tweak the design to improve my matching performance?

1. Input Q factor (tune the input matching circuit without considering the load match)





Question #3

How can I tweak the design to improve my matching performance?

2. Improving the Intrinsic Gain

Improving the intrinsic gain will avoid the nonlinearities in the systems and essentially it is matched best higher the gain can be obtained by the higher the g_m

G_m improved:

1. Operate the Transistor in the weak inversion and keep the maximum dimensions (V_{dsat} less than 100mV)
2. Increase the more V_{gs}
3. Push Higher external current through external current reuse amplifiers



Question #3

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How can I tweak the design to improve my matching performance?

2. Improving the Intrinsic Gain

Improving the intrinsic gain doesn't impact much until unless load and input matched perfectly

Improving the V_{gs} from the bias point 450mV to VDD improved the S_{11} -4dB but the problem from this method is a lot of parasitic components impact on the circuit at the higher gain level and the resonance matching frequency drifts

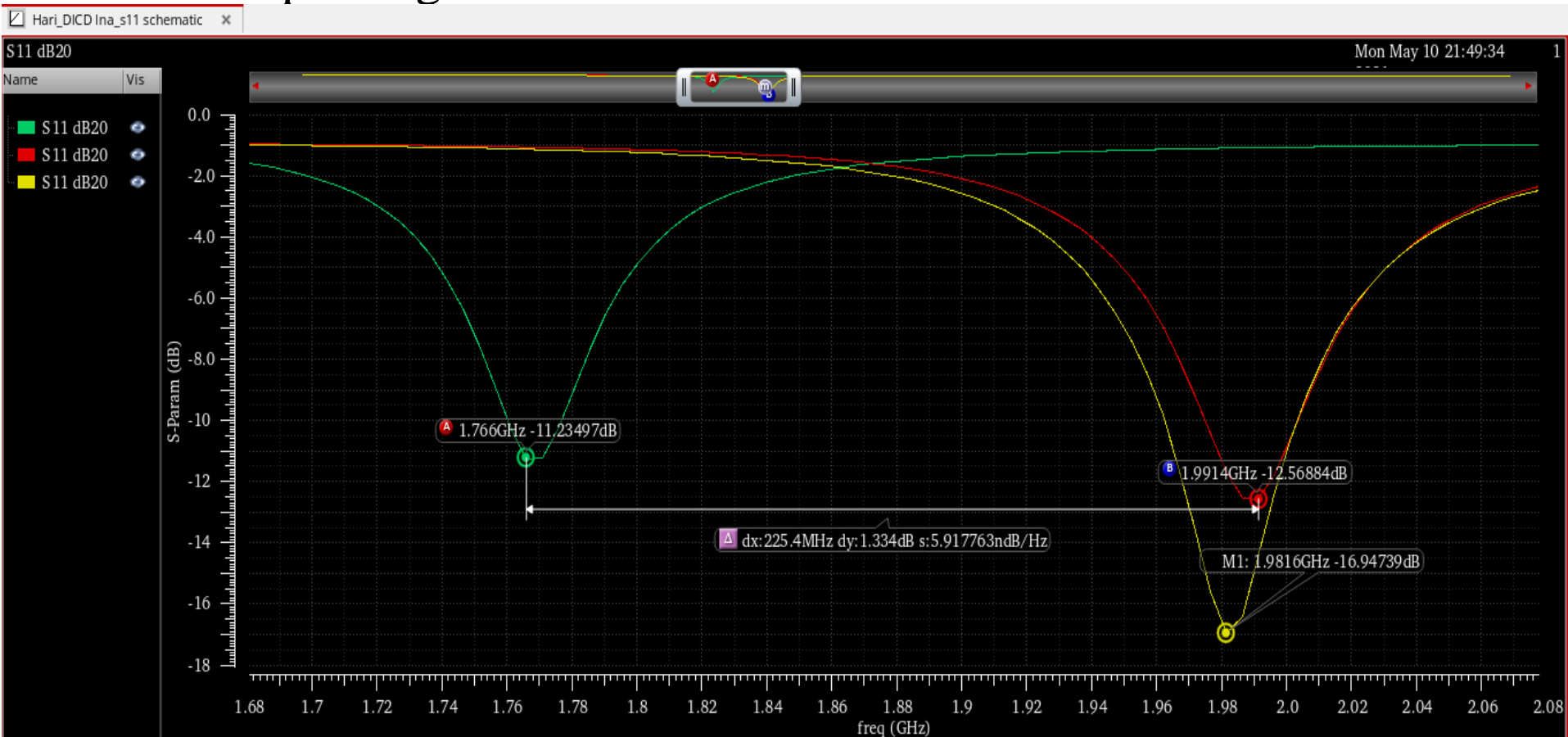


Question #3

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How can I tweak the design to improve my matching performance?

2. Improving the Intrensic Gain





Question #3

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How can I tweak the design to improve my matching performance?

2. Tuning the Load

Impact of the load on the Input matching is very important in input matching the method is implemented it 50ohm load is coupled to the output tank 50ohm, resonance frequency matching by the load tank Capacitance and the Inductance C_d and L_d respectively

Improving the ratio between the L_d load tank inductance to input degenerative inductance L_s improves the input matching and out matching in terms of tens of db but the tuning frequency at the output changes and the S_{22} drifts a lot from the input matching frequency

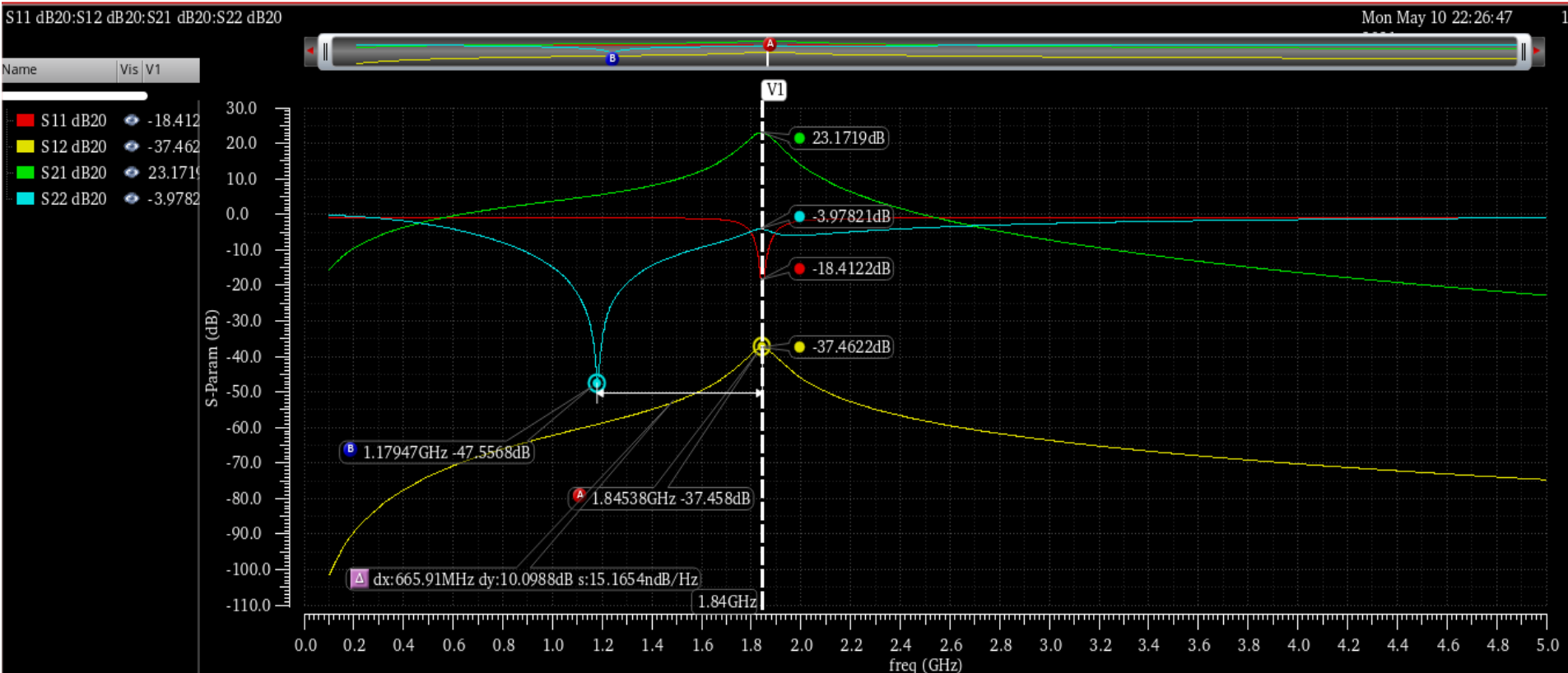


Question #3

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How can I tweak the design to improve my matching performance?

2. Tuning the Load Improving the L_d/L_s ratio and the output coupled Resistance to 50ohm

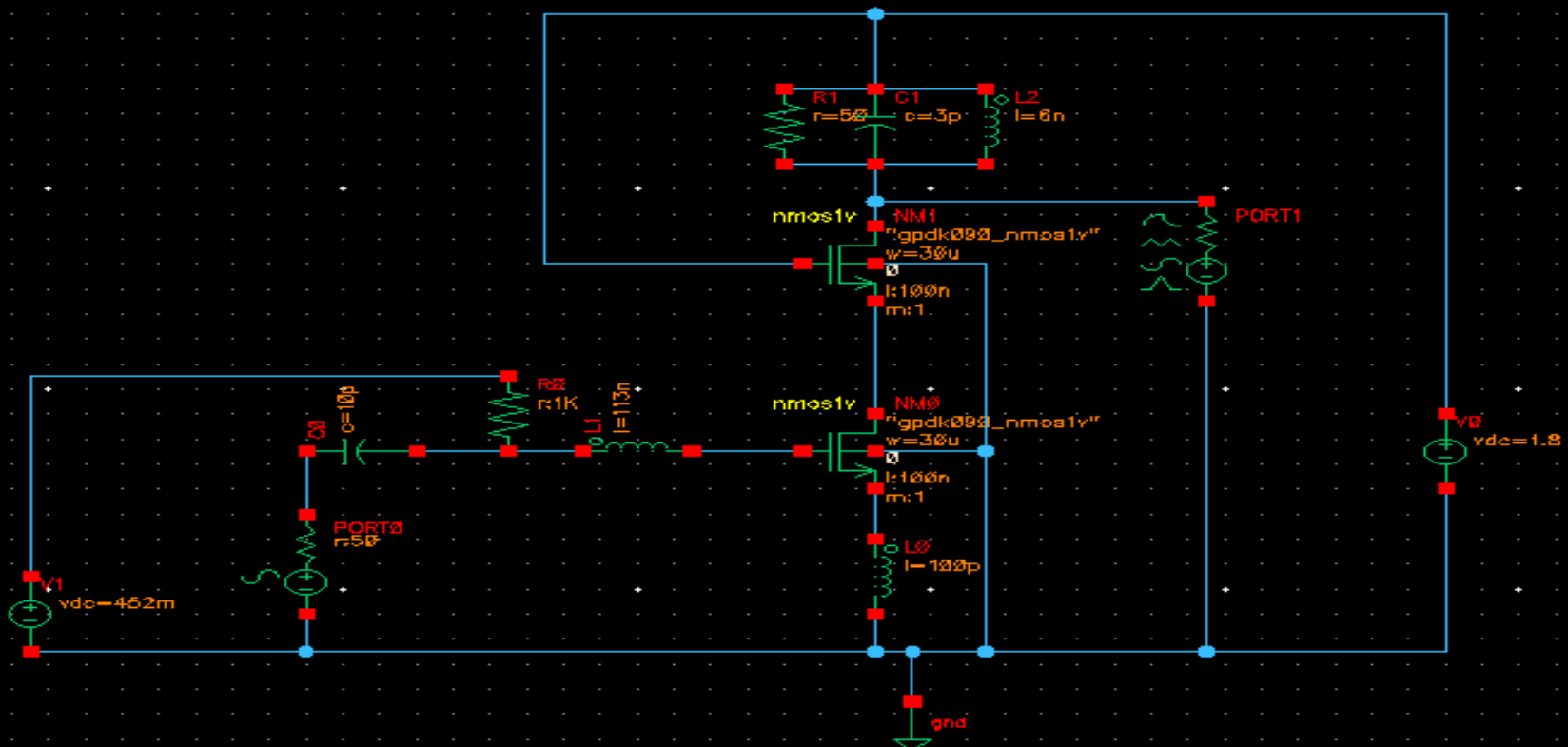




Question #4

Simulate the Complete Design of your LNA.
Check input match, gain and Noise Figure.
Discuss the results

Complete Simulated Circuit





Question #4

Università degli
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Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

1. the input is matched by input quality factor improve and considering the input parasitic capacitances

2. at 4mA desired drain current the achieved bias voltage V_{gs} is 450mV considering the W/L_{min} ratio is 300

Design values avoiding the parasitics $L_s=92\text{pF}$, $L_g=143\text{nH}$, $C_{gs} = 42\text{fF}$, $g_m=24\text{ms}$ this design values give good matching 1.77GHz instead of 2GHz so there is frequency drift is happen



Question #4

Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

3. Considering the C_{gd} 14fF, which is changed the drift frequency significantly from 1.77GHz to 1.9981GHz, input is matched well and improved the -4db in S_{11} , new values are $L_s=100$ PF, $g_m=24$ ms, $I_s = 113$ nH

4. improvement in the input matching circuit obtained by changing the g_m which improved the input matching significantly roughly from -12db to -17db Improving the gain improved the noise figure very significantly.

5. noise figure and input matching tremendously improved by the out put tank matching coupling LNA to the 50ohm load from the load tank prallel resistance 50 improves the noise figure



Question #4

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Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

Results Discussion:

6. by changing the L_d/L_s load tank inductance to the input degenerative inductance improves a gain lot and the input matching which eventually makes Noise figure best but changing a L_d a lot makes drift in resonance frequency and the matching at the desired frequency 2Hz, S_{22} goes worst

8. So it is the tradeoff between the gain and matching and the resonance frequency

7. All the Achieved results are listed below



Question #4

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Simulate the Complete Design of your LNA. Check input match, gain and Noise Figure. Discuss the results

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