130 nm and 90 nm CMOS Technologies for Detector Front-end Applications

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Introduction

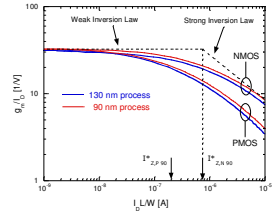
- CMOS commercial technologies of the quarter micron node have been extensively used for the implementation of radiation tolerant, low noise, low power readout circuits with very high channel density for analog and digital processing in pixel and microstrip detectors.
- The IC designers' effort is presently shifting to 130 nm CMOS technologies, or even to the next technology node, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications (SLHC, Linear Collider, Super B-Factory) .
- In this work the results of noise measurements carried out on CMOS devices in 130 nm and 90 nm commercial processes are analysed to provide an evaluation of the impact of technology scaling on the analog performances of a future generation of front-end chips. The behavior of 1/f and channel thermal noise parameters is studied to assess the effects of gate oxide quality and short-channel phenomena in CMOS processes with different gate oxide thickness and minimum channel length.

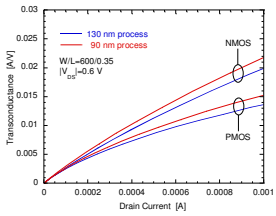
Experimental Details

- MOSFETs studied belong to two standard CMOS processes by STMicroelectronics with 130 nm and 90 nm minimum feature size. The oxide thickness t_{OX} is 2.4 and 2.0 nm, and the gate capacitance per unit area C_{OX} is about 14.8 and 17.7 fF/μm² respectively.
- In the 130 nm process PMOS and NMOS devices with gate lengths L from 0.13 to 1 μm and gate widths W of 200, 600 and 1000 μm were investigated. In the 90 nm process devices of both polarities with gate lengths L from 0.10 to 0.7 μm and gate widths W of 200 and 600 μm were characterized. In both processes, transistors were laid out using a standard open structure configuration.
- The device parameters were characterized at drain currents from several tens of μA to 1 mA, that is, the usual operating currents of input MOSFETs in integrated charge-sensitive amplifiers.

Experimental Results

Transconductance and Device Operating Region





- Transconductance behavior depends on the inversion region where the device is operating. The inversion level of a MOS transistor in saturation can be expressed by means of its transconductance efficiency g_m/I_D as a function of the normalized drain current $I_D L/W$ [1].
- The boundary between weak and strong inversion is expressed by I_Z^*, located at the intersection of weak and strong inversion asymptotes:

$$I_Z^* = 2\mu C_{OX} n V_T^2$$

μ=channel mobility, n=coeffcient proportional to the invers of the subthreshold slope of I_D as a function of V_{GS}, V_T =thermal voltage.

- I_Z^* is larger in devices fabricated in 90 nm ⇒ weak and moderate inversion regions extend to higher normalized drain currents.

I_Z^* [μA]		
Process	130 nm	90 nm
NMOS	0.55	0.75
PMOS	0.15	0.20

- All the investigated devices are operated in weak and moderate inversion region.

Noise Equations

The noise performances of a MOS device can be characterized in terms of the gate referred noise voltage spectrum:

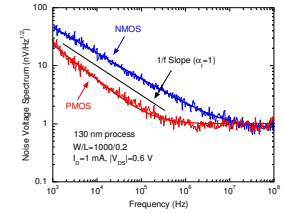
$$S_e^2(f) = S_W^2 + \frac{K_f}{C_{OX} WL} \frac{1}{f^{\alpha_f}}$$

White noise — Channel thermal noise (dominant at low current density) and noise in parasitic resistors [2]

$$S_W^2 = 4k_B T \frac{\Gamma}{g_m} \qquad \Gamma = \alpha_W n \gamma$$

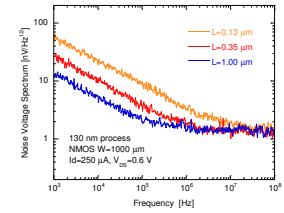
$\alpha_W \geq 1$ excess noise factor, γ ranging from 1/2 in weak inversion to 2/3 in strong inversion

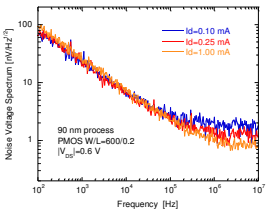
1/f noise — K_f = intrinsic process parameter, $\alpha_f = 1$/f noise slope



Noise Measurement

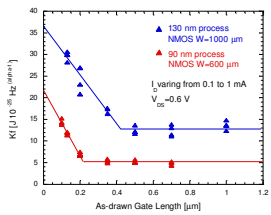
Noise voltage spectra were measured for PMOS and NMOS with different gate widths and lengths and at different drain currents for devices belonging to both the investigated technologies.





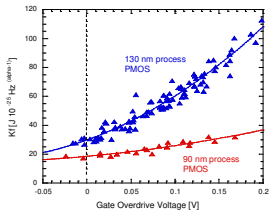
Analysis of Noise Measurement Results

1/f noise coefficient K_f



For N-channel devices K_f is:

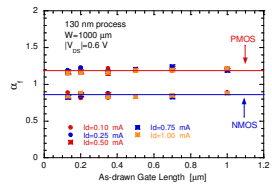
- independent of the drain current.
- larger for deviced with L<0.5 μm in the 130 nm process and with L<0.2 μm in the 90 nm process.
- lower in the 90 nm process by about a factor of 2.



For P-channel devices K_f is:

- dependent of the overdrive voltage V_{GS}-V_{TH}
- larger for deviced with L<0.5 μm in the 130 nm process and with L<0.2 μm in the 90 nm process
- lower in the 90 nm process.

1/f noise slope



α_f is independent of the drain current and of the device geometry.

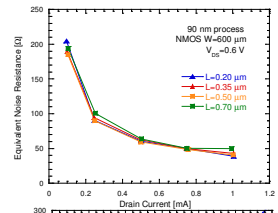
α_f		
Process	130 nm	90 nm
NMOS	0.85	0.85
PMOS	1.19	1.09

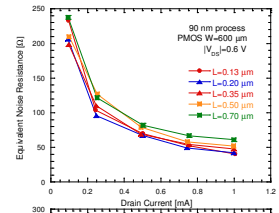
White noise

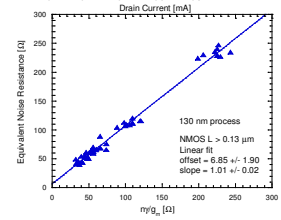
White noise is evaluated in terms of the equivalent noise resistance:

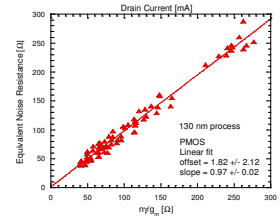
$$R_{eq} = \frac{S_W^2}{4k_B T} = \alpha_W \frac{n\gamma}{g_m}$$

- White noise decreases with the increase of I_D due to the increase of g_m.
- White noise is not sizably affected by L variations since devices are operated in weak and moderate inversion.
- $\alpha_W \approx 1$ is found for all the devices, except for NMOS with L=0.13 μm in the 130 nm process where $\alpha_W \approx 1.2$.









References

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[2] G. De Geronimo , P. O'Connor, "MOSFET optimization in deep submicron technology for charge amplifiers", *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 3223-3232, Dec. 2005.