Design of High Gain and Low Noise CMOS Gilbert Cell Mixer for Receiver Front End Design

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Abstract— **This paper presents the design of a low noise CMOS Gilbert cell mixer in 180 nm technology with the help of cadence tool. The switched biasing technique is used to improve the noise performance by splitting the tail current source into two small transistors. The proposed mixer produces a simulated conversion gain (CG) of 9.95 dB with a noise figure (NF) of about 8.12 dB. The supply voltage required for the circuit is 1.8 V with a power consumption of 3.5 mW. The layout of the present design is also given here. This design results better performance in the conversion gain, noise figure and power consumption than the conventional mixer design available in the literature. Hence, this design is a suitable block for receiver front end design for wireless systems.**

Keywords— CMOS; conversion gain; Gilbert cell; noise figure; switched biasing; tail current source.

I. INTRODUCTION

The radio frequency (RF) integrated circuit has received much more interest due to their linearity, low power, low cost and high level of integration. The RF front end processes the incoming RF signal, before it altered into a lower intermediate signal (IF). As shown in Fig. 1, the conventional receiver front end consists of low-noise amplifier (LNA), mixer, local oscillator (LO), IF amplifier and different filters [1]. RF Mixer is a 3 port active or passive frequency translation device having two inputs and one output port. When RF frequency and LO frequency are inserted into the two input ports, it creates the sum or the difference frequency (RF±LO), which is called the IF frequency. The most accepted double balanced active mixer in RFIC design is the Gilbert cell mixer [2]. Generally, the Gilbert cell mixers are used as the down converter in RF front end receiver design. This is due to the good conversion gain at wide band, high linearity and good isolation. Of course it requires high supply voltage and consumes more power.

From the different advanced technology CMOS mixers found in the literature, it seems that the folded structure mixer works at a low supply voltage [3] due to the small number of stacked transistors. But it requires a higher dc current for the operation. It suffers from large chip area due to the inductor used in the matching network. The bulk driven concept [4] outcomes low supply voltage requirements as number of stacked transistor are less and lower power consumption. However, due to the straight insertion of RF signal through the body terminal, it is noisier. In one hand, the subthreshold technique [5] results low power and high gain by the use of an active load. But in the other hand, it gives more noise to the system due to the high aspect ratio of transistors. By using high output impedance of the PMOS active load transistors, the bulk injection technique [6] achieves low power operation. But it results in low conversion gain and relatively high noise figure. The bulk pumped mixer [7] operates in low supply voltage and consumes low power due to the use of less number of stacked transistors. But, in this case the conversion gain is poor.

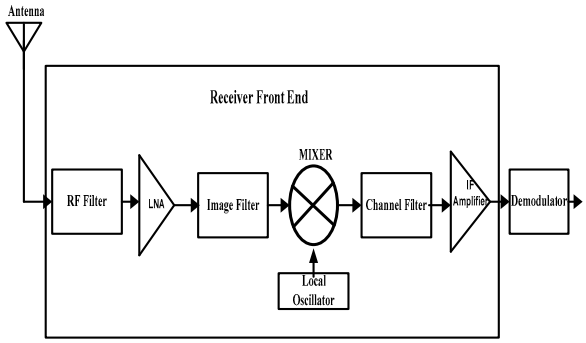

Fig. 1. RF front end schematic

In the present approach, the Gilbert cell mixer is projected to get high gain and low power consumption with improvement in noise performance by the use of switched biasing technique. This technique not only diminishes the white noise, but also the flicker noise [8] by the balanced switching operation of tail current source with an enhancement of noise figure. This paper describes the design of 1.8 V switched biasing technique based Gilbert cell Mixer using 180 nm CMOS process with the layout design. The proposed mixer provides a conversion gain of 9.95 dB and noise figure of 8.12 dB with power consumption of 3.5 mW.

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In Section II, the circuit analysis and design concept of the proposed mixer is described with the operating principles of the switched biasing technique. The simulated results are shown in Section III and the conclusion is given at Section IV.

II. PRINCIPLES AND CIRCUIT DESCRIPTION

A. Gilbert Cell Mixer

The Mixer is one of the most important parts of the receiver front end whose functionality is to change RF to a lower IF for easy signal processing in receivers and also converts IF frequency to a higher IF or RF frequency for efficient transmission in transmitters by keeping amplitude and phase constant. The Fig. 2 shows the three terminal device based mixer.

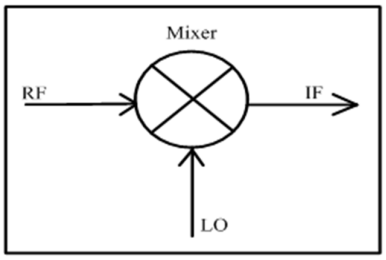

Fig. 2. Symbolic representation of the mixer

Fig. 3 shows the double balanced Gilbert cell mixer, which is the most desirable for high gain and spurious output rejection in the modern receivers [9]. It consists of three stages such as load stage (RL), switching stage (M3-M6) and transconductance stage (M1 and M2).

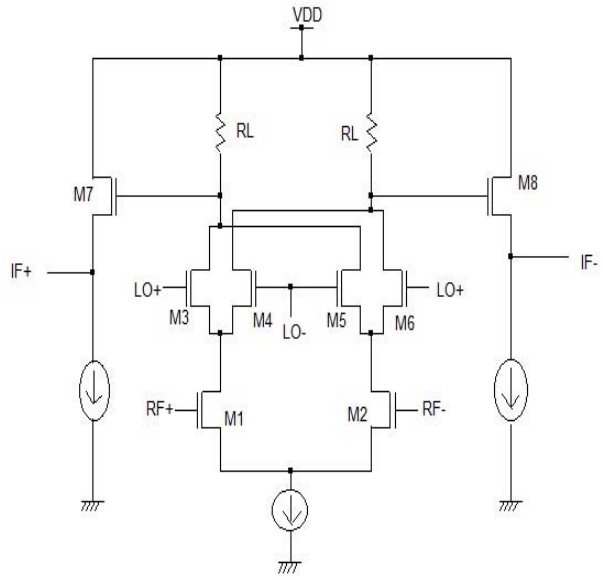

Fig. 3. Schematic of Gilbert cell mixer

The transconductance stage performs a voltage to current conversion to control the gain of circuit. The switching stage multiplies the linear RF signal current with the LO signal to function as a switch. The load stage forms current to voltage transformation through IF output signal.

B. Circuit Analysis of the Proposed Mixer

The circuit diagram of the proposed mixer is shown in Fig. 4. The mixer consists of four major parts including active load stage represented by the transistors (M1 and M2), switching stage represented by the transistors (M3-M6), transconductance stage, which consists of transistors (M7 and M8) and switched biasing stage represented by transistors (M9 and M10) as a current source, whose gate terminals are connected to IF nodes to reduce output noise.

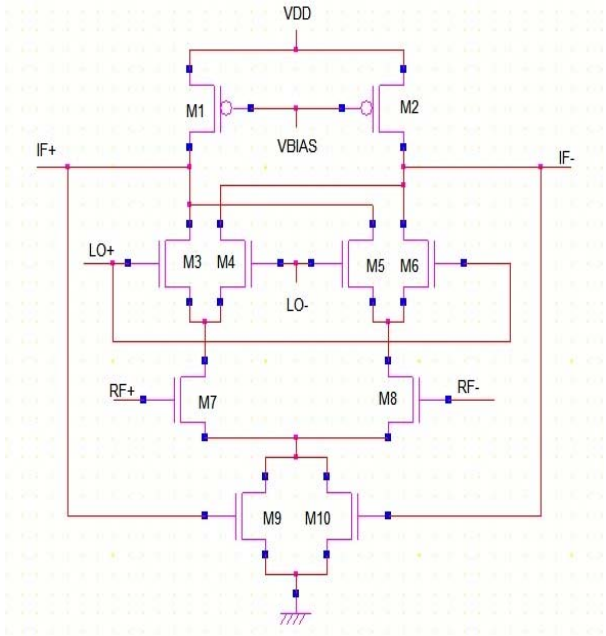

Fig. 4. Schematic of proposed mixer

A square wave signal and a sinusoid signal $V_{RF} \times COS(\omega_{RF}t)$ is applied in LO input side and in the RF input side respectively. The function of square wave is given by

$$F_{sq.wave}(t) = \frac{4}{\pi} COS(\omega_{LO}t) - \frac{4}{3\pi} COS(3\omega_{LO}t) + \frac{4}{5\pi} COS(5\omega_{LO}t) - \frac{4}{7\pi} COS(7\omega_{LO}t) + \cdots\cdots\cdots\cdots \quad (1)$$

The even ordered harmonics are cancelled due to the common mode signals. The IF current is expressed as

$$I_{IF} = I_{RF} \times F_{sq.wave}(t) = [I_{DC} - g_m V_{RF} COS(\omega_{RF}t)] \times F_{sq.wave}(t)$$

$$= \frac{4}{\pi} I_{DC} COS(\omega_{LO}t) - \frac{2}{\pi} g_m V_{RF} [COS(\omega_{RF}t - \omega_{LO}t) + COS(\omega_{RF}t + \omega_{LO}t)] + \cdots\cdots\cdots\cdots \quad (2)$$

So, the mixer transconductance is $G_C = \frac{2}{\pi} g_m$

In Gilbert type mixer

$$V_{IF}^{+} = [\frac{IDC}{2} - g_m V_{RF}^{+} \cos \omega_{RF} t\ ] F_{sq.wave}(t) R_{load}$$
$$= \frac{2}{\pi} I_{DC} R_{load} \cos(\omega_{LO} t) - \frac{2}{\pi} g_m R_{load} V_{RF}^{+} \{ \cos[(\omega_{RF} - \omega_{LO})t] + \cos[(\omega_{RF} + \omega_{LO})t]\} + \cdots \quad (3)$$

$$V_{IF}^{-} = [\frac{IDC}{2} - g_m V_{RF}^{-} \cos \omega_{RF} t] F_{sq.wave}(t) R_{load}$$
$$= \frac{2}{\pi} I_{DC} R_{load} \cos(\omega_{LO} t) - \frac{2}{\pi} g_m R_{load} V_{RF}^{-} \{ \cos[(\omega_{RF} - \omega_{LO})t] + \cos[(\omega_{RF} + \omega_{LO})t]\} + \cdots \quad (4)$$

Putting $V_{RF}^{+} = \frac{VRF}{2}$ and $V_{RF}^{-} = -\frac{VRF}{2}$ (5)

So $V_{IF} = V_{IF}^{+} - V_{IF}^{-}$ (6)

Putting equations (3), (4) and (5) in equation (6), we get

$$V_{IF} = -\frac{2}{\pi} g_m R_{load} V_{RF} \{ \cos[(\omega_{RF} - \omega_{LO})t] + \cos[(\omega_{RF} + \omega_{LO})t]\} + \cdots$$

So voltage conversion gain $C.G = \frac{2}{\pi} g_m R_{load}$ (7)

Here, PMOS transistors (M1 and M2) act as R_{load} in Fig. 4.

The M1 and M2 PMOS transistors work as an active load, which converts current to output voltage through the IF signals. The transistors (M3-M6) are biased at or the near pinch off region as the switching stage. Lo signal is multiplied, when the RF current passes through the switching stage. The transconductance stage (g_m) consists of transistors (M7 and M8), which translates the input RF voltage signal into current signal. To obtain high conversion gain and low noise figure for the mixer, the g_m stage transistors is biased at the saturation region. A current source is replaced by the switched biasing stage represented by transistors (M9 and M10) to control the total bias current of the mixer and improvement in the noise performance.

In this proposed mixer, the tail current source is divided into two half-size transistors (M9 and M10), which works with the IF signals sporadically in between strong inversion and an accumulation region to release trapped charge carriers. It results lower flicker noise [8], as compared to the static biasing current source as shown in Fig. 5. Here, M1 and M2 transistors are periodically switched between two states: (a) an "operational state" in strong inversion, where it results a constant bias current Ib and (b) a "off-state" below threshold stage, predictable to forget about its previous 1/f noise performance [10]. As a result, the operational state achieves a reduced amount of 1/f noise.

So, the reduction in the noise generated by switched biasing transistors concludes a lower noise figure as compared to a fixed biasing current source. The mixer does not need an additional bias, due to the M9 and M10 transistors are operated by the IF output signal, which results extra power consumption.

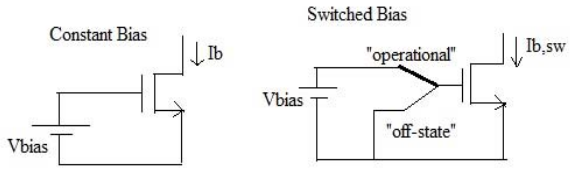

Fig. 5. Principle of switched biasing

III. SIMULATION RESULTS

The proposed mixer is simulated using 180 nm CMOS process technology using cadence design tool. Fig. 6 shows the schematic of the proposed mixer using cadence tool. The transient analysis of the mixer is plotted in the Fig. 7. It shows that, the mixer operates at output frequency (IF) of 100 MHz. The simulated conversion gain versus frequency graph is shown in Fig. 8. From the graph the conversion gain is found to 9.95 dB, which provides a flat response over a wide range of frequency. Fig. 9 demonstrates that the simulated noise figure is 8.12 dB in the frequency range of 1 GHz to 10 GHz. In this graph, the noise figure gradually reduces with the increasing frequency.

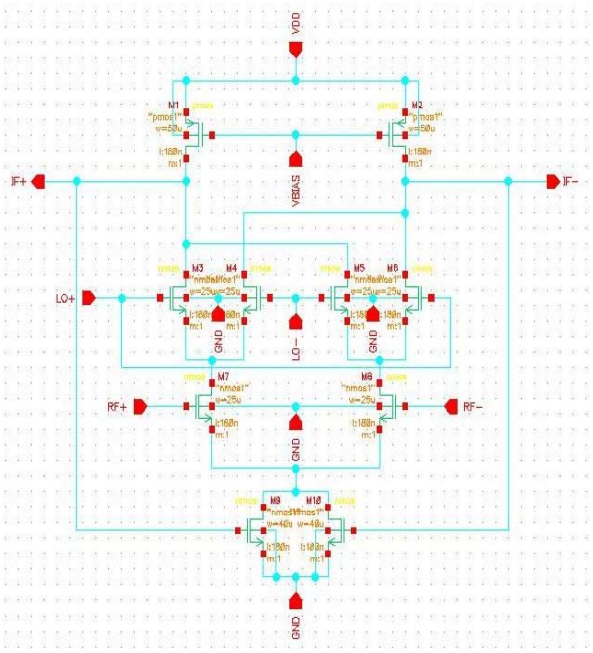

Fig. 6. Schematic of the proposed mixer using cadence tool

Fig. 10 shows the 1-dB compression point of the proposed mixer design. The graph results the 1-dB compression point is about -2.397 dBm. In this proposed mixer, the maximum power consumption is 3.5 mW from the supply voltage of 1.8 V. Fig. 11 shows the layout design of the proposed mixer.

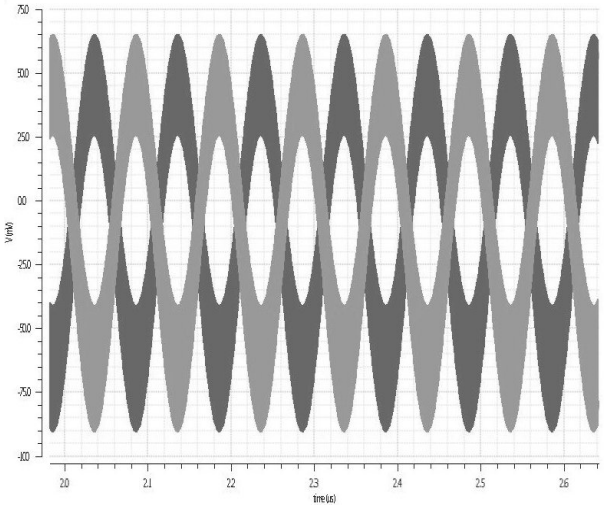

Fig. 7. Transient analysis of the mixer

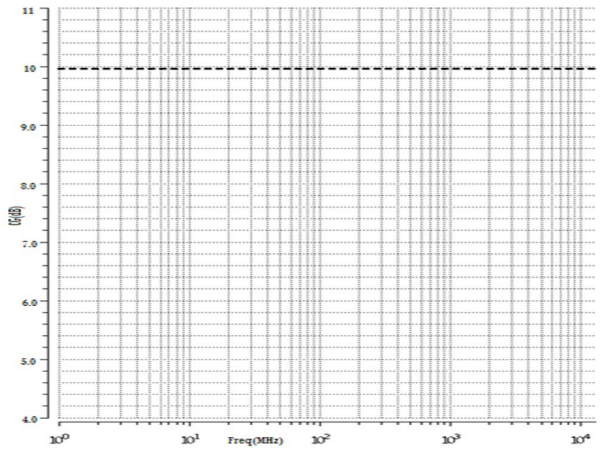

Fig. 8. Simulated conversion gain versus frequency

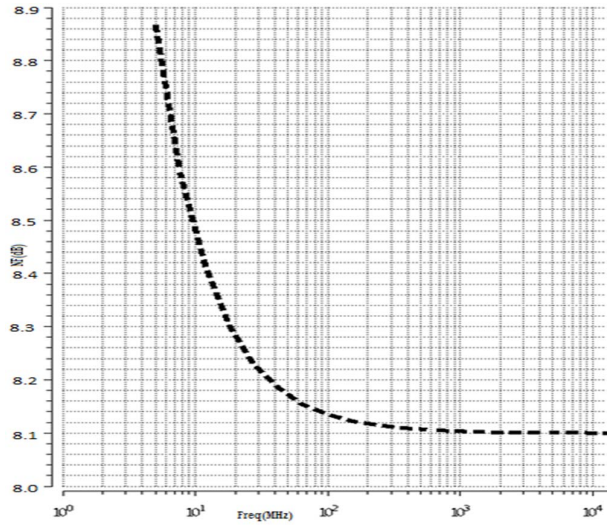

Fig. 9. Simulated noise figure versus frequency

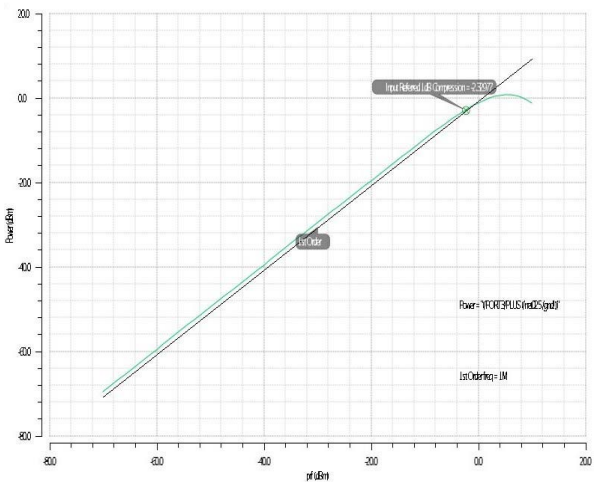

Fig. 10. 1-dB compression point of the mixer

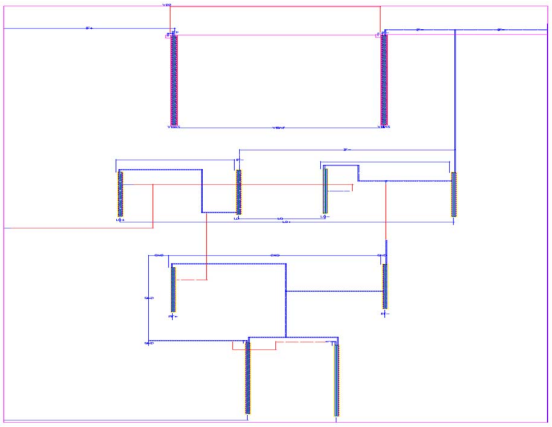

Fig.11. Layout design of the proposed mixer

The comparison of the proposed mixer with other reported works is presented in Table I

TABLE I. PERFORMANCE SUMMERY OF MIXERS

Ref.	CMOS process (nm)	Frequency (GHz)	IF (MHz)	Conversion Gain (dB)	NF (dB)	Supply Voltage (V)	Power (mW)	Technique
3	180	0.2-16	528	5.3	-	1.8	1.5	Folded
4	180	0.9-1	100	1.27	19.8	1	1.6	Bulk Driven
5	130	3.1-10.6	264	9.8	14.5	1.2	1.85	Folded
6	180	0.5-7.5	100	5.7	15	0.5	0.8	Bulk Injection
7	130	10-35	100	1	-	1	6	Bulk Pumped
9	180	2.4	250	13.8	15.5	1.8	10	Conventional
This Work	**180**	**1-10**	**100**	**9.95**	**8.12**	**1.8**	**3.5**	**Switched biasing**

From the table, it seems that the proposed mixer has the advantages of high conversion gain, lower power consumption and low noise figure than the other reported works.

IV. CONCLUSION

The design of a low noise CMOS Gilbert cell mixer using switched biasing technique is explained here. The proposed mixer is implemented in 180 nm technology process with the help of cadence tool. The switched biasing technique is used to improve the noise performance. The proposed mixer results a simulated conversion gain of 9.95 dB and a noise figure is about 8.12 dB. The supply voltage required for the circuit is 1.8 V. The power consumed by the circuit is 3.5 mW. Also the layout design is presented in this paper. This design results improved performance in the noise figure, power consumption and conversion gain than the conventional mixer design. Hence, this design may be implemented in wideband and multi-standard integration applications.

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