

A 1.8V and 2GHz Inductively Degenerated CMOS Low Noise Amplifier

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Abstract— This paper presents the design and simulation of Low Noise Amplifier (LNA) in a 0.18 μ m CMOS technology. The LNA function is to amplify extremely low noise amplifier without adding noise and preserving required signal to noise ratio. Cadence design tool Spectre_RF is used to design and simulation based on resistors, inductors, capacitors and transistors. Power constrained methodology is used for the design of Low Noise Amplifier. The amplifier provides a forward gain (S_{21}) of 18.22dB with noise figure (NF) of 2.49dB while drawing 8.1mW power from a 1.8V voltage supply.

Keywords- Low Noise Amplifier (LNA), CMOS, noise figure, gain, IIP3

I. INTRODUCTION

The growth of wireless services and other telecom applications has pushed the semiconductor industry towards complete system-on-chip solutions. Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range while the back-end section processes analog and digital signals in the baseband low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications. It lies typically from 100 KHz to 100 GHz. However in general, frequencies below 1 GHz are considered baseband frequencies while those greater are described as RF. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver. Generally, the main goal of LNA design is to achieve simultaneous a low noise and high power gain for the given power dissipation and frequency condition [1]. There are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascode inductor source degeneration [2].

The design is based on a cascode configuration including feedback to the common source amplifier for simultaneous noise and input impedance matching. This paper describes the

operation and the simulation of s-parameters, gain and minimum noise figure using 0.18 μ m CMOS technology.

Section II describes LNA and the design steps followed for the design and simulation of single-ended LNA. Section III shows the simulated performance results focused at gain and noise figure. Finally, the last section draws conclusions obtained from the simulation of Single-ended LNA.

II. LNA DESIGN

A. Low Noise Amplifier Topology

Out of the several topologies for narrow band single ended LNA design, an appropriate topology should be selected for low power and low voltage optimized LNA design. For common gate topology, the gain is less than 10.0 dB in very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among gain, small noise figure and better input/output matching in very low power consumption. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascode inductor source degeneration topology, which can get the similar low noise amplifier performance in very low power consumption. Above all, the cascode inductor source degeneration topology is selected for this design.

B. Design Challenges

In the communication system, Low noise amplifier is the second element after antenna. LNA is used to boost up the signal of desire energy from the weak information signal of required energy with noise suppression. So, noise figure (NF) is the key issue to concern in this design. The receiver is the most power hungry block and should be as low as possible. So, noise figure and power consumption are more important issue than gain.

With the small power consumption, the LNA should amplify the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding small amount of noise as possible. Matching of each block of the receiver is also an important. So, LNA matching is also a concern issue which can

affect the performance of the device. The gain should be large enough at the same time noise should be as less as possible. However, the gain of LNA should not be too high otherwise the following stages, mixer is saturated. In my design, the noise figure should be around 3-4 dB and gain should be more than 10 dB. The LNA should present specific impedance at the input, e.g. 50 Ω to interface with the filter or antenna. Finding the delicate balance in all issues or parameters becomes the challenge more often than simply maximizing a single key parameter. The most recognizable trade-off is between LNA gain and noise figure (NF). Linearity is also an important design issue. Third order intercept point, IP3 has emerged as an important parameter in LNA design. The easiest way to improve the IP3 performance for a given frequency is to increase the current density or current drawn of LNA. If current draw is less important than IP3 performance, then it can be increased with the usual slight increase in gain and NF. So, in this case, IP3 improves with the trade-off in current draw and NF. Input and output return losses, S_{11} and S_{22} , are also available for trading off to achieve improved gain and NF performance. Typically, the input and output matches are designed to afford good gain and NF performance. It is a balance of performance parameters. Emitter degeneration presents an entire range of opportunities for trading off performance parameters. Added emitter degeneration can also bring the match required for good return losses closer to the match for better NF. Adding emitter feedback, however, trades off gain with IP3 and P1dB performance. Emitter degeneration also trades off linearity and stability, especially at higher frequencies. At the lower frequencies of the cellular bands, stability improves with emitter degeneration, while at frequencies greater than around 5 GHz, stability decreases as degeneration increases. So the tradeoff between linearity and stability must be examined across a full range of frequencies.

Small changes in inductance added to the emitter of a LNA can have large impacts on gain, NF and stability. As inductance increases, stability increases at the expense of gain. NF can also improve. However, continued increases in inductance can soon lead to degraded gain and NF. In the LNA transistor, device size can be increased to improve linearity at the expense of current draw. Increasing current density in the LNA device can improve gain and NF, but again it is at the expense of current draw.

C. Single-Ended LNA Design

The circuit diagram of the Single-Ended LNA is shown in Fig. 1. It employs inductive source degeneration (inductor L_s connected to the source of transistor M_1) [2]. This method has the advantage that one has a greater control over the value of the real part of the input impedance through the choice of inductance. Cascoding transistor M_2 is used to reduce the interaction of the tuned output with the tuned input.

The RF input is coupled to the gate of the amplifier by the coupling capacitance C_0 . Transistor M_3 is the biasing transistor and forms a current mirror with transistor M_1 . The width of M_3 is kept a small fraction of the width of M_1 to minimize the power overhead of the bias circuit.

Output Inductor, L_d resonates with output load to maximize output power transfer and gain at resonance frequency. The width of the cascoded transistor must be sized to trade-off

common source gain reduction and increase of parasitic source capacitance of M_2 (both are consequence of a wider M_2) [3]. Cascode transistor helps to reduce S_{21} and reduce C_{gd1} Miller effect [4]. R_{bias} is large enough so that its equivalent current noise is small enough to be ignored. L_g is used to set the resonant frequency.

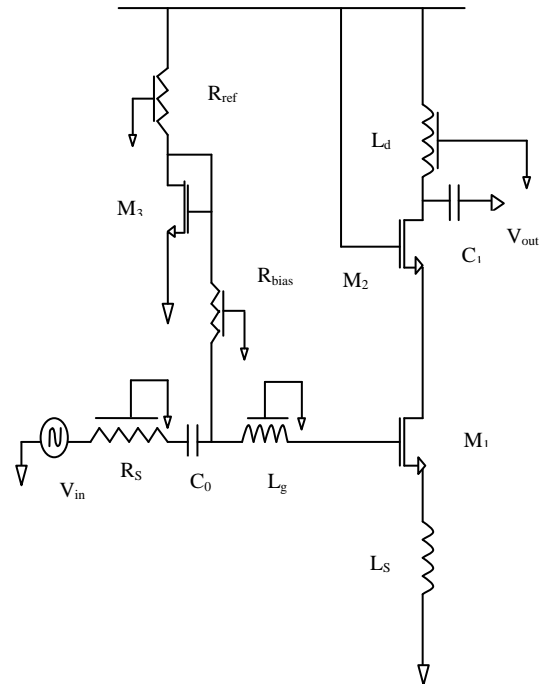


Figure 1. Single-Ended LNA

D. Design Steps

The design procedure followed for the design of single-ended LNA is Power optimization based. The input impedance for the single stage LNA design is [5]:

$$R_{in} = R_g + \frac{L_s \cdot g_m}{C_{gs}} + j(\omega L_s - \frac{1}{\omega C_{gs}}) \quad (1)$$

It can be written as,

$$R_{in} = R_g + R_a + j(X_{LS} - X_{CGS}) \quad (2)$$

Where,

$$R_a = \frac{L_s \cdot g_m}{C_{gs}}$$

Therefore, the impedance of the MOSFET without feedback is:

$$R_{in} = R_g - jX_{CGS} \rightarrow R_{in} = -jX_{CGS} \quad (3)$$

Adding series feedback adds the $R_a + jX_{LS}$ term to the original input impedance. Additionally, another inductor is added in series with the gate L_g that is selected to resonate with the C_{gs} Capacitor. The Input resistance achieved is: $R_{in} = L_s \cdot g_m / C_{gs}$. Where R_{in} may be say 50 ohms. L_g is designed so that at the resonant frequency it cancels out C_{gs} i.e. $j(\omega L_s - 1/\omega C_{gs}) = 0$. In most LNA designs the value of L_s is

picked and the values of g_m and C_{gs} are calculated to give the required R_{in} . The design steps followed by me for the design of single-ended low noise amplifier are given below:

Step1: Find the optimum device width

The optimal value of Q in case of power optimization technique is [6]:

$$Q_{L,opt,P_d} = |C| \sqrt{\frac{5\gamma}{\delta}} \left[1 + \sqrt{1 + \frac{3}{|C|^2} \left(1 + \frac{\delta}{5\gamma} \right)} \right] \approx 3.9 \quad (4)$$

Where, $\gamma = 2$, $\delta = 4$, $\alpha = 0.85$. The equation for the device (M_1) width is:

$$W_{M1,opt,P_d} = \frac{3}{2C_{ox} L Q_{L,opt,P_d} R_S \omega_0} \quad (5)$$

Step2: Find C_{GS} (Gate-Source capacitance)

We know,

$$C_{gs1} = \frac{2}{3} C_{ox} W_{M1} L_{min} \quad (6)$$

Step3: Find device transconductance (g_{M1})

$$g_{M1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L} \right)_{M1} I_{DM1}} \quad (7)$$

Step4: Find the transistor unity gain frequency (ω_T)

$$\omega_T = \frac{g_{M1}}{C_{gs1}} \quad (8)$$

Step5: Expected noise figure F_{min,P_d}

The expected noise figure can be computed by below formula:

$$F_{min,P_d} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left(\frac{\omega_0}{\omega_T} \right) \geq 1 + 1.62 \left(\frac{\omega_0}{\omega_T} \right) \quad (9)$$

When I_D increase then ω_T increase and NF decreases at the

expense of more power.

Step6: Starting value of Degeneration Inductor L_S

The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH.

$$R_S = \frac{g_m L_S}{C_{gs}} = \omega_T L_S \quad (10)$$

Step7: Evaluation of L_g

We know,

$$L_g = \frac{1}{\omega_0^2 C_{gs}} - L_S \quad (11)$$

Step8: Evaluation of L_d

$$L_d = \frac{1}{\omega_0^2 C_L} \quad (12)$$

Step7: Width of transistors

Size of M_3 is chosen to minimize power consumption. Size of $M_1 = M_2$, So that they can have shared drain area. It can reduce the impedance looking into gate and drain of M_1 degrading the input match and noise performance, so both transistors sizes are to made equal. Transistor M_2 is used to reduce the miller effect.

Step8: Value of bias resistor

R_{bias} must be large enough so that it's equivalent current noise can be neglected.

Step7: Calculation of power dissipation (P_d)

$$P_d = V_{dd} I_D \quad (13)$$

III. SIMULATION

The schematic of fully single-ended LNA designed with 0.18 μ m technology is shown in Fig. 2. We have simulated our design using Cadence EDA tools-Virtuoso Schematic Editing and it's Simulator: Spectre.

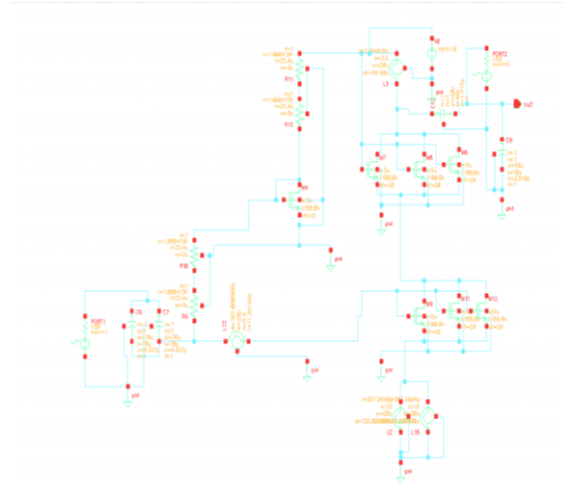


Figure 2. Schematic of Single-Ended LNA.

A. Simulation results

The various simulation iterations are performed on the proposed LNA circuit to meet design requirements. The simulation results of single-ended LNA achieved at the typical process are summarized in the Table 1.

B. Simulation Figures

After the simulation of the single-ended LNA at 2GHz frequency we obtained various results which are shown in the below figures.

As is shown, Fig. 3 gives us the Noise Figure parameter. The noise figure (NF_{min}) in our design is 2.49dB. Fig. 4 and Fig. 5 show the voltage gain and power gain at 2GHz frequency. The voltage gain is 16.7dB and power gain is 18.22dB obtained by simulation.

The input return loss value can be expressed in terms of the measured S parameter S_{11} is shown in Fig. 6. The value of S_{11} obtained after the simulation is -12.21dB. Third-order intercept (IP3) and 1-dB compression point (P_{1dB}) are two measures of linearity. The 1 dB point and IIP3 obtained after the simulation is -19.3297 dBm and -10.3012 dBm.

At last, the power dissipation is calculated. After the simulation, we got the current value of 4.5mA. So the power dissipation is ($1.8V \cdot 4.5mA$) 8.1mW.

TABLE I. SUMMARY OF LNA PERFORMANCE

Performance Parameter	Value	Unit
Noise Figure (NF_{min})	2.49	dB
Voltage Gain	16.7	dB
Power Gain (S_{21})	18.22	dB
S_{22}	-12.21	dB
S_{11}	-8.032	dB
S_{12}	-40.86	dB
I_D	4.5	mA
Power consumption	8.1	mW
K_f	5.391	
B_{if}	1.055	
1-dB Point	-19.3297	dBm
IP3 Point	-10.3012	dBm

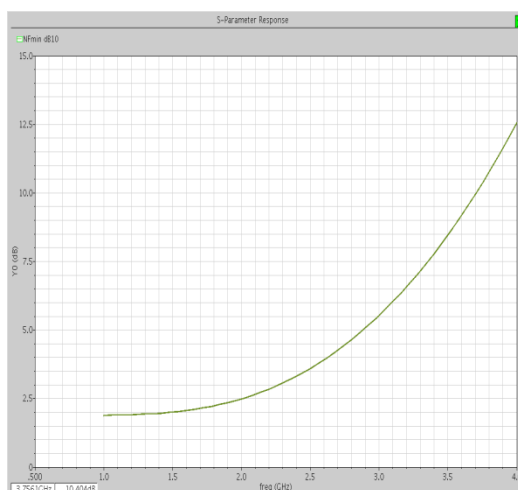


Figure 3. NF of Single-Ended LNA (2GHz).

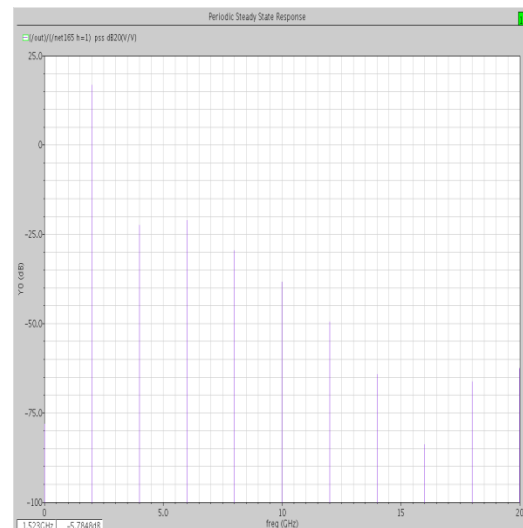


Figure 4. Voltage gain of Single-Ended LNA.

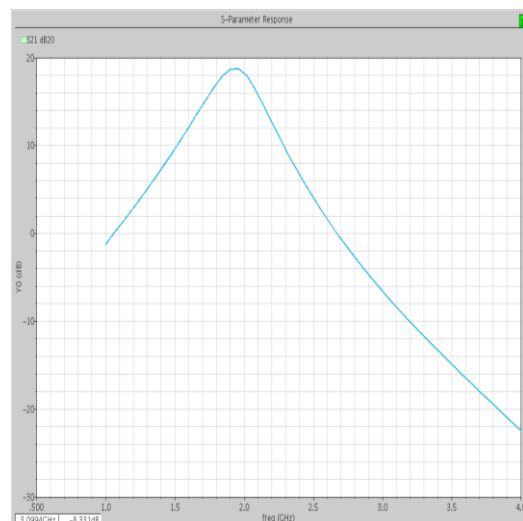


Figure 5. Power gain (S_{21}) of Single-Ended LNA.

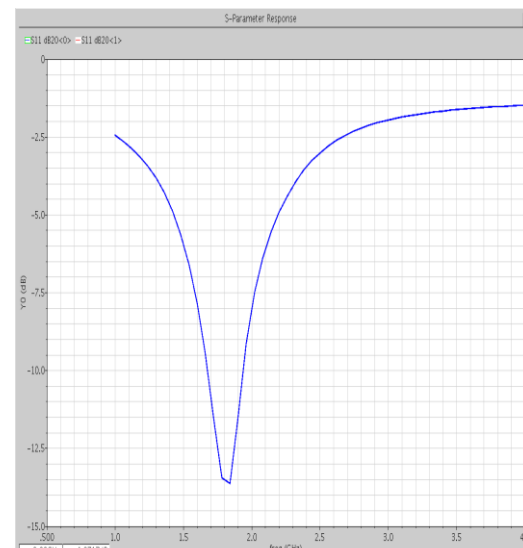


Figure 6. S_{11} plot of Single-Ended LNA

IV. CONCLUSION

From the simulation of the designed Single-Ended LNA, we obtained a noise figure of about 2.49dB and gain (S_{21}) is 18.22dB. In this design the gain can be increased by decreasing the value of L_s . Using the power constrained method the power dissipation of the designed LNA is 8.1mW which is very important parameter in the design of single-ended LNA. The low dissipation LNA exhibits good linearity and Noise Figure and achieves a high Voltage Gain and a good reflection coefficient S_{11} . Noise figure can be varied by changing the geometry of the transistors. The simulation result shows that if the input is match, then the NF would be equal to NF_{min} .

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