# A Time-Variant Analysis of Fundamental $1/f^3$ Phase Noise in CMOS Parallel LC-Tank Quadrature Oscillators

Andrea Mazzanti, Member, IEEE, and Pietro Andreani, Senior Member, IEEE

Abstract—This paper presents a rigorous time-variant analysis of the 1/f MOS device noise upconversion into  $1/f^3$  phase noise for two of the most popular parallel-coupled quadrature CMOS harmonic oscillators. Simple closed-form equations for the fundamental  $1/f^3$  phase-noise spectrum are derived and validated through SpectreRF simulations, proving that the two topologies display remarkably different sensitivities to the low-frequency noise sources. Based on the developed analysis, useful general design insights are also presented.

*Index Terms*—CMOS RFICs, flicker noise, impulse sensitivity function (ISF), phase noise, quadrature oscillator.

### I. INTRODUCTION

UADRATURE local oscillators are often used in many of today's wireless/wireline front-end circuits [1]–[10] as power-efficient alternatives to quadrature-phase generation via frequency division of a double-frequency (differential) signal. Two very popular circuit topologies to generate quadrature oscillations are shown in Fig. 1. In each topology, two harmonic LC-tank oscillators are directly coupled in one direction and are cross coupled in the other direction by means of two additional differential pairs, determining a quadrature sequence among the generated waveforms.

Unfortunately, quadrature coupling also deteriorates phase noise, as compared to a stand-alone oscillator drawing the same total power [11]–[16], and a rigorous time-variant phase-noise analysis has been performed to explain and quantify the amount of phase noise caused by all thermal noise sources in the two quadrature oscillators of Fig. 1[13]. On the other hand, the close-in phase-noise spectrum has not been investigated that well. It is well known that, in stand-alone oscillators, nonlinear MOS parasitic capacitors and tuning varactors result in 1/f noise upconversion, which, of course, occurs in parallel-coupled oscillators as well [17]–[21]. In the latter case, however, 1/f noise is upconverted into close-in phase noise, even in the presence of ideal linear passive components, possibly leading

Manuscript received August 31, 2008; revised November 21, 2008. First published February 13, 2009; current version published September 30, 2009. This work was supported in part by the Italian research program PRIN 2007B5RZLE. This paper was recommended by Associate Editor J. Hellums.

A. Mazzanti is with the Dipartimento di Ingegneria dell'Informazione, Università degli Studi di Modena e Reggio Emilia, 41100 Modena, Italy (e-mail: amazzanti@unimore.it).

P. Andreani is with the Department of Electrical and Information Technology, Lund University, 221 00 Lund, Sweden (e-mail: piero@eit.lth.se).

Digital Object Identifier 10.1109/TCSI.2009.2015214

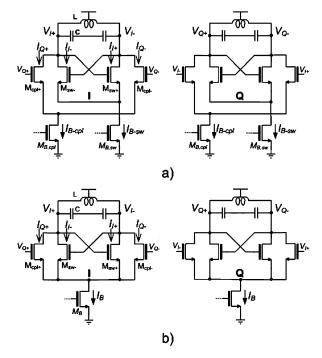


Fig. 1. Schematic of parallel-coupled harmonic oscillators. (a) Disconnected sources (DSs). (b) Connected sources (CSs).

to a much more severe deterioration of the  $1/f^3$  phase-noise level. Very important advances in the comprehension of the mechanisms behind the generation of  $1/f^3$  phase noise in quadrature oscillators have been presented in [14]–[16]; however, the time-invariant approach pursued in these works is not generally suitable for an exact phase-noise analysis, which must necessarily be time variant [22].

In this paper, the time-variant impulse sensitivity function (ISF) method [22]–[24] is employed to analyze the 1/f noise upconversion in the two topologies of Fig. 1, showing that, despite their apparent similarity, their behavior is remarkably different. Furthermore, the ISF analysis yields closed-form  $1/f^3$  phase-noise equations accounting for the contributions of all active devices in the two oscillator topologies, extending the results obtained in [15] and [16], where only the bias transistors in the oscillator of Fig. 1(a) were considered. The analysis provides at times counterintuitive predictions, which are

<sup>1</sup>It may be remarked that more general but much less intuitive theories of phase noise are found in, e.g., [25]–[27]. As a matter of fact, the closed-form expression of the ISF, as given by (4) in Section II, was derived in [13] by resorting to Kärtner's approach [25] since the original formulation of the ISF theory [22] is not very well suited for a (general) symbolic analysis.

subsequently fully confirmed by SpectreRF simulations. These results, together with those derived in [13], extend our understanding of the fundamental phase noise for the two most popular parallel-coupled quadrature harmonic oscillators.

# II. $1/f^3$ Phase-Noise Analysis

The phase noise of a generic oscillator can be expressed as [22]–[24]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\sum_{i} N_{Li}}{A_0^2/2}\right) \tag{1}$$

with  $A_0$  being the oscillation amplitude and  $N_{Li}$  (simply referred to as *effective noise* hereinafter) being the power spectral density (PSD) of the phase-noise-generating noise for each noise source inside the oscillator. For low-frequency noise sources,  $N_{Li}$  is given by

$$N_{Li} = \frac{1}{4C^2\Delta\omega^2} \frac{1}{T} \left[ \int_0^T \Gamma_i(t) \cdot \overline{i_{n,i}(t)} dt \right]^2$$
 (2)

where C is a node capacitance (e.g., a tank capacitance in an LC-tank oscillator),  $\Delta\omega$  is the offset from the angular oscillation frequency  $\omega$ ,  $i_{n,i}$  is the 1/f noise current of the ith current source, and the weighting function  $\Gamma_i$  is the associated ISF, encoding the time-dependent sensitivity of the phase of the oscillation to  $i_{n,i}$ . In LC-tank oscillators, it is possible to relate the various ISFs to the ISF of each tank, where a tank ISF is defined as the ISF of a noise current flowing into that tank [13], [28].

In single-ended and differential harmonic oscillators, the ISF of each tank is very well approximated by a sinusoid in quadrature with the voltage across the same tank, but this assumption is no longer valid when two (or more) oscillators are coupled to each other [13].

For the two circuits in Fig. 1, assuming square-wave like currents through the differential pairs, and a tank quality factor that is at least moderately high to filter off current harmonics, the output voltages are (almost) sinusoidal

$$V_{I+} = -V_{I-} = A_0 \sin(\omega t)$$

$$V_{O+} = -V_{O-} = -A_0 \cos(\omega t).$$
(3)

Under these assumptions, a very simple expression for the ISF of the  $I_+$  and  $I_-$  tanks (i.e., the tanks associated to  $V_{I+}$  and  $V_{I-}$ , respectively) is [13]<sup>2</sup>

$$\Gamma_{I+}(\phi) = -\Gamma_{I-}(\phi) = \frac{1}{4 \cdot \cos(\psi)} \cos(\phi + \psi), \quad \psi = \arctan(m)$$
(4)

where the angle  $\phi$  is used instead of  $\omega t$  for simplicity,  $m=i_Q/i_I$  is the ratio between the fundamental Fourier components of the in-phase and quadrature currents injected into each resonator, and the factor four at the denominator accounts for the total number of resonators.

<sup>2</sup>When studying the phase noise in oscillators built around several resonators, we may focus on a single resonator, which is arbitrarily selected [12]. In the analysis to follow, we choose to consider each I/Q oscillator as consisting of two distinct resonators. The ISFs associated to the four resonators are simply phase-shifted replicas of each other [13]

The difference between the two circuits in Fig. 1 is that the sources of the coupling and crossed-coupled differential pairs are separated in the topology of Fig. 1(a), while they are connected together in the topology of Fig. 1(b). Accordingly, we will refer in the following to the two circuits as disconnected sources quadrature oscillator (DS-QO) and connected sources quadrature oscillator (DS-QO), respectively.

Low-frequency noise in both circuits is produced by the tail bias transistors and by the transistors in all differential pairs. Despite the apparent similarity between DS-QO and CS-QO, we will prove next that, in the DS-QO, the 1/f noise from all differential pairs is ideally rejected, with the main contributors to the close-in phase noise being the tail-current sources, while exactly the opposite is true in the CS-QO.

### III. DISCONNECTED SOURCES QUADRATURE OSCILLATOR

### A. Contributions From Differential-Pair Transistors

We will start analyzing the low-frequency noise generated by the differential pairs in the DS-QO, proving that their 1/f effective noise, and therefore the contribution to phase noise, is ideally nil.

Let us focus on one "switching" differential pair, i.e., the differential pair implementing the negative resistance for the respective LC tanks.<sup>3</sup> Before making use of (2) to calculate the effective noise from the switching-pair transistors, we have to find the amount of 1/f noise that is actually injected into the tank(s) by each device. To this end, we recall that the 1/f MOS noise is modeled by a current generator between the transistor drain and source, having a PSD of  $i_f^2$ . Clearly, the transfer function of  $i_f$  from the device to tanks is calculated in the same way as for the MOS thermal channel noise. Thus, reusing the results derived in [28] in the analysis of phase noise due to the thermal noise in the stand-alone LC-tank oscillator, we obtain

$$i_{n,M_{\text{sw+}}}(\phi) = i_{f,M_{\text{sw+}}} \cdot \left(\frac{2gm_{\text{sw-}}(\phi)}{gm_{\text{sw+}}(\phi) + gm_{\text{sw-}}(\phi)}\right)$$
(5)

where, referring to Fig. 1(a),  $M_{\rm sw+}(M_{\rm sw-})$  is the device driven by  $V_{I+}(V_{I-}), gm_{\rm sw+}(\phi)[gm_{\rm sw-}(\phi)]$  is its time-variant transconductance,  $i_{f,M_{\rm sw+}}$  is the 1/f noise current generated by  $M_{\rm sw+}$ , and  $i_{n,M_{\rm sw+}}$  is the fraction of  $i_{f,M_{\rm sw+}}$  flowing differentially into the  $I_+/I_-$  tanks. It is well known that a simplified expression for the PSD of the 1/f noise current  $\overline{i_{f,M_{\rm sw+}}}$  of the drain current  $I_{D,M_{\rm sw+}}$  is [32]

$$\overline{i_{f,M_{\text{sw}+}}^{2}(\phi)} = \frac{K_{N} \cdot I_{D,M_{\text{sw}+}}(\phi)}{C_{\text{ox}} L_{M_{\text{sw}+}}^{2}} \cdot \frac{1}{\Delta \omega}$$

$$= \frac{K_{N} \cdot g m_{\text{sw}+}^{2}(\phi)}{2\beta_{\text{sw}+} C_{\text{ox}} L_{M_{\text{sw}+}}^{2}} \cdot \frac{1}{\Delta \omega} \tag{6}$$

 $^3$ It should be noted that our analysis does not account for a possible reduction of 1/f noise occurring when MOS transistors are periodically switched on and off [29]–[31]. Therefore, it may be possible that our equations overestimate the amount of  $1/f^3$  phase noise contributed by the differential-pair transistors. Nevertheless, we expect a good matching between theoretical analysis and SpectreRF simulations since the bsim3v.3 MOS device model does not take into account the impact of switching on the generation of 1/f noise.

<sup>4</sup>With respect to phase-noise analysis, this is equivalent to considering the fraction of  $i_{f,M_{\mathrm{sw}+}}$  flowing separately into  $I_{+}$  and  $I_{-}$ , since  $\Gamma_{I+}=-\Gamma_{I-}$ , as shown by (4).

where  $K_N$  is a process constant,  $C_{\rm ox}$  is the unit oxide capacitance,  $L_{M_{\rm sw+}}$  is the gate length of  $M_{\rm sw+}$ ,  $\beta$  is equal to  $\mu_{n,{\rm eff}}C_{\rm ox}W_{M_{\rm sw+}}/L_{M_{\rm sw+}}$  (with  $\mu_{n,{\rm eff}}$  being the effective electron mobility and  $W_{M_{\rm sw+}}$  being the width of  $M_{\rm sw+}$ ), and where we made use of the ideal quadratic dependence of the MOS drain current on the gate-to-source voltage. Substituting (6) in (5), we find

$$i_{n,M_{\text{sw+}}}(\phi) = \sqrt{\frac{2K_N}{C_{\text{ox}}\beta_{\text{sw+}}L_{M_{\text{sw+}}}^2} \cdot \frac{1}{\Delta\omega}} \cdot \left(\frac{gm_{\text{sw+}}(\phi) \cdot gm_{\text{sw-}}(\phi)}{gm_{\text{sw+}}(\phi) + gm_{\text{sw-}}(\phi)}\right). \quad (7)$$

The tank voltages and the currents flowing through the switching pairs of DS-QO are shown in Fig. 2(a) and (b), respectively. The current waveforms [and, therefore, also the corresponding transconductances  $gm_{\text{sw+}}(\phi)$  and  $gm_{\text{sw-}}(\phi)$ ] look like square waves aligned with the corresponding driving voltages, with rise and fall times being set by the device size and oscillation amplitude. The time-variant term in (7), which is dependent on  $gm_{\text{sw+}}(\phi)$  and  $gm_{\text{sw-}}(\phi)$ , is shown in Fig. 2(c) and is made of symmetrical narrow pulses equally spaced by half a period. It is therefore straightforward to realize that the product  $\Gamma_{I_+}(\phi) \cdot i_{n,M_{\mathrm{sw}+}}(\phi)$  has a zero average over the oscillation period and that the effective noise contributed by the differential-pair devices, proportional to the integral in (2), is nil. This is because (7) is symmetrical in  $gm_{sw+}(\phi)$  and  $gm_{\rm sw-}(\phi)$  and therefore sweeps exactly the same values across the two current transitions centered on  $\phi = 0$  and  $\phi = \pi$ , respectively, while, as clearly seen in (4),  $\Gamma_{I_{+}}(\phi)$  sweeps the same absolute values but with opposite signs across the two transitions ( $\Gamma_{I_{\perp}}(\phi)$  is shown in Fig. 2(b), together with the device currents).

Looking at in a slightly different way, the integrand in (2) is the product of two functions, namely,  $\Gamma_{I_+}(\phi)$  and  $i_{n,M_{\mathrm{sw}+}}$ , having both a zero average and with  $i_{n,M_{\mathrm{sw}+}}$  at double frequency compared to  $\Gamma_{I_+}(\phi)$ . The integral in (2) therefore vanishes, and this is true not only for  $M_{\rm sw+}$  but also for all other switch and (in the ideal case) coupling transistors, which means that such transistors do not contribute any 1/f noise upconversion. SpectreRF simulations fully confirm this prediction. However, it should be noticed that this surprising result is strongly dependent on the particular symmetry of (7), which, in turn, relies on the dependence of the noise PSD on  $gm^2$  [see (6)] and on transistors working in the saturation region during commutations. If any transistor enters the triode region, the symmetry is broken, and 1/f noise upconversion from the differential-pair devices does usually ensue as a result. While the switch-pair transistors are easily kept in saturation [28], this is indeed what happens to the coupling-pair transistors if the oscillation amplitude is large enough compared to the MOS threshold voltage  $(V_T)$ . Fig. 3 shows the current waveforms for one pair of coupling transistors, for an oscillation amplitude of 600 mV and a  $V_T$  of 250 mV, with the switching asymmetry generating a modest current peaking. This apparently minor deviation from ideality results, in this simulation example, in an upconversion boost of the coupling-transistor 1/f noise by approximately

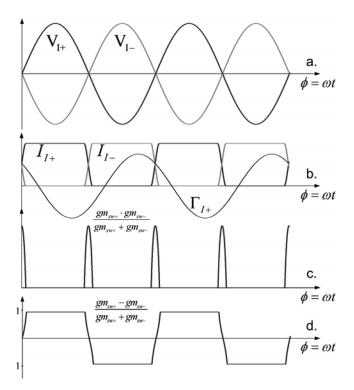


Fig. 2. DS-QO waveforms. (a) Tank voltages. (b) Currents in  $M_{\rm sw+}$  and  $M_{\rm sw-}$ , together with  $\Gamma_{I+}$ . (c) Noise modulating function for  $M_{\rm sw+}$ . (d) Noise modulating function for  $M_{B,\rm sw}$ .

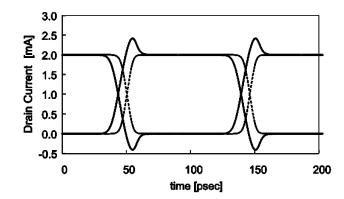


Fig. 3. Current waveforms for the coupling transistors  $M_{\rm cpl+}$  and  $M_{\rm cpl-}$  in Fig. 1(a) when (dotted gray curve) they stay in the saturation region and when (black curve) they partially enter the triode region during commutations.

three orders of magnitude, making their contributions to  $1/f^3$  phase noise no longer negligible compared to the tail transistors, to which we now turn.

## B. Contributions From Bias Transistors

We start by considering the impact of the 1/f noise from the tail current  $I_{B,\mathrm{sw}}$  biasing the switching differential pair. The first step is again to calculate the actual amount of 1/f noise injected into the tanks by  $I_{B,\mathrm{sw}}$ . The 1/f noise transfer function  $i_{n,M_{B,\mathrm{sw}}}$  from  $M_{B,\mathrm{sw}}$  to the differential  $I_+/I_-$  tanks is again calculated as in the case of the thermal MOS channel noise [28], obtaining

$$i_{n,M_{B,\text{sw}}}(\phi) = i_{f,M_{B,\text{sw}}} \cdot \left(\frac{gm_{\text{sw-}}(\phi) - gm_{\text{sw-}}(\phi)}{gm_{\text{sw-}}(\phi) + gm_{\text{sw+}}(\phi)}\right)$$
 (8)

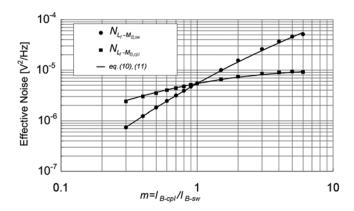


Fig. 4. Comparison between (dots) simulated and (lines) calculated effective noise at 1-kHz offset due to the 1/f noise of the tail-current sources in the DS-QO.

where  $i_{f,M_{B,sw}}$  is the amplitude of the 1/f noise of the tail current, with PSD being given by (6) with the corresponding device parameters. The time-variant term in (8) is represented by the curve in Fig. 2(d). The analysis is greatly simplified by approximating the curve as a square-wave toggling between +1 and -1, aligned with the driving voltage of the differential pair

$$i_{n,M_{B,\text{sw}}}(\phi) \approx i_{f,M_{B,\text{sw}}} \cdot \text{sign}(\sin(\phi))$$
 (9)

where  $\mathrm{sign}(x) = +1$  if x > 0 and  $\mathrm{sign}(x) = -1$  if x < 0. This approximation becomes rigorously valid for fast current commutations in the differential pair, while it will lead to a slight overestimation of the upconverted 1/f noise for slower switching transients.

The effective noise contributed by the current source  $I_{B,\mathrm{sw}}$  is found by multiplying (9) by  $\Gamma_{I_+}(\phi)$  and evaluating the integral in (2). Taking also into account the fact that there are two identical but uncorrelated tail bias sources (one for each oscillator) leads to a total effective noise

$$N_{L_f, M_{B,sw}} = \frac{2i_{f, M_{B,sw}}^2}{4C^2 \Delta \omega^2} \cdot \left[ \frac{1}{2\pi} \int_0^{2\pi} \frac{\cos(\phi + \psi)}{4 \cdot \cos(\psi)} \cdot \text{sign} \left[ \sin(\phi) \right] d\phi \right]^2$$

$$= \frac{2i_{f, M_{B,sw}}^2}{4C^2 \Delta \omega^2} \cdot \frac{\tan^2(\psi)}{4\pi^2} = \frac{1}{8\pi^2 C^2 \Delta \omega^3} \cdot \frac{K_N m^2 I_{B,sw}}{C_{ox} L_{M_{B,sw}}^2}.$$
(10)

The same approach is followed to calculate the effective 1/f noise generated by the current biasing the coupling pair, which yields

$$N_{L_f, M_{B, \text{cpl}}} = \frac{1}{8\pi^2 C^2 \Delta \omega^3} \frac{K_N I_{B, \text{cpl}}}{C_{\text{ox}} L_{M_{B, \text{cpl}}}^2}$$

$$= \frac{1}{8\pi^2 C^2 \Delta \omega^3} \frac{K_N \cdot m I_{B, \text{sw}}}{C_{\text{ox}} L_{M_{B, \text{cpl}}}^2}$$
(11)

where we made use of the fact that, in the DS-QO, m is determined by the ratio between  $I_{B,\rm cpl}$  and  $I_{B,\rm sw}$ . As an example, plots of (10) and (11) versus m, at an offset frequency of 1 kHz, are shown in Fig. 4, together with SpectreRF simulations. Circuit and device parameters are given in Table I; furthermore,

TABLE I
COMPONENT VALUES AND DEVICE PARAMETERS ADOPTED IN SIMULATIONS

Parameter	Value	Units
Inductance, L	1.0	nН
Tank Quality Factor, Q	15	/
Resonance Frequency, fo	5.0	GHz
Size of M <sub>sw</sub> and M <sub>cpl</sub>	150 / 0.35	μm/μm
Size of M <sub>B,sw</sub> and M <sub>B,cpl</sub>	400 / 2	μm/μm
Total Current Consumption	4 x 2	mA
Oxide Capacitance, C <sub>OX</sub>	4.4	fF/μm²
Electron Mobility, μ <sub>n,eff</sub>	320	cm <sup>2</sup> /(V·sec)
1/f noise constant, K <sub>N</sub>	2π x 1.525 10 <sup>-28</sup>	A·F

the total current drawn by each oscillator from the supply, i.e.,  $I_{B,\text{sw}} + I_{B,\text{cpl}}$ , is kept constant at 4 mA while m is swept. To avoid second-order effects due to nonlinear reactive components, the transistor models have been modified to eliminate stray capacitances. As clearly seen in Fig. 4, numerical simulations match admirably the theoretical predictions from (10) and (11). Adopting real MOS models, simulations show on average a 25% higher effective noise compared to that of (10) and (11), resulting in  $\approx$ 1 dB higher  $1/f^3$  phase noise.

By means of (1), the  $1/f^3$  phase noise of the DS-QO is now readily found using (10) and (11) and remembering that the oscillation amplitude is  $A_0 \approx (2/\pi)RI_{B,\mathrm{sw}}$ , obtaining

$$L(\Delta\omega) = 10\log\left(\frac{K_N}{16C_{\text{ox}}} \frac{m}{C^2 R^2 I_{B,\text{sw}}} \cdot \left(\frac{m}{L_{M_{B,\text{sw}}}^2} + \frac{1}{L_{M_{B,\text{cpl}}}^2}\right) \cdot \frac{1}{\Delta\omega^3}\right). \quad (12)$$

It is possible to show that equivalent results have been obtained in [15] and [16] through alternative approaches and with different notations. It is, however, important to remark once more that the 1/f noise from the differential pairs, not discussed in [15] and [16], has a negligible impact only if the differential-pair transistors do not leave the active region. Equation (12) is plotted versus SpectreRF simulations for three different values of m in Fig. 5 (dotted and solid black curves, respectively), again for the component values found in Table I.

Looking back at the effective noise contributed by the tail transistors, a closer examination of the plots in Fig. 4 points out a very noteworthy theoretical prediction, which subsequently suggests a straightforward way of optimizing the design: It is the smallest bias current (i.e., the bias current producing the *lowest* 1/f noise) that generates the *highest* amount of 1/f noise upconversion. The cause of this is that, when the 1/f noise PSD is multiplied by the ISF in (2), the effective noise of the device with the lowest 1/f noise becomes higher than the effective noise of the device with the highest 1/f noise. Therefore, when either small or large m values are selected (i.e., when the difference between  $I_{B,sw}$  and  $I_{B,col}$  is large), it is convenient to increase the gate length of the bias transistor carrying the lowest current as long as its drain-source saturation voltage does not exceed that of the bias transistor carrying the largest current; in this way, we can achieve a substantial phase-noise improvement without any penalty in reduced voltage headroom. It is easy to show that

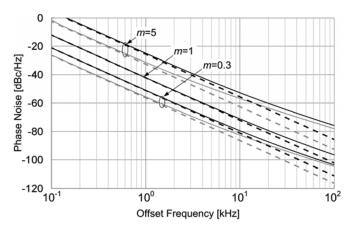


Fig. 5. (Solid lines) Simulated and (dotted lines) calculated phase noise for the DS-QO and three different values of m, with bias transistors having the following: (black curves) 1) a length of 2  $\mu$ m, independent of m, and (gray curves) 2) an optimal length for minimum  $1/f^3$  phase noise.

this choice implies the following relation between the aspect ratios of the biasing devices:

$$\frac{(W/L)_{M_{B,\text{cpl}}}}{(W/L)_{M_{B,\text{sw}}}} = \frac{I_{B,\text{cpl}}}{I_{B,\text{sw}}} = m.$$
 (13)

Two examples of optimization are shown in Fig. 5 (gray curves). The length of the bias transistors carrying the largest current is kept fixed at 2  $\mu$ m, while the length of the other transistors is adjusted according to (13), achieving a minimum of the generated effective noise. The improvements at 1-kHz offset, captured again by (12), are 4.5 and 6.5 dB, respectively, when m=0.3 and m=5.

### IV. CONNECTED SOURCES QUADRATURE OSCILLATOR

Despite the apparent similarity of the circuit topology with the DS-QO, the tank current waveforms in the CS-QO in Fig. 1(b) are considerably different. The voltage and current waveforms are shown in Fig. 6(a) and (b), respectively. Assuming the same size for transistors  $M_{\rm cpl}$  and  $M_{\rm sw}$ , each transistor carries now the whole tail current for one quarter of the oscillation period. Furthermore, the in-phase and quadrature components of the resonator currents are no longer set by two independent current sources, as was the case in the DS-QO, and it is therefore much more difficult to change their ratio m from the value m=1 [13], [33]. Therefore, we will assume m=1 in the CS-QO.

### A. Contributions From Bias Transistors

The mechanisms of 1/f noise upconversion into phase noise are also considerably different than in the DS-QO. Interestingly, the role of the noise sources is perfectly swapped: The  $1/f^3$  phase noise is generated by the transistors in the differential pairs, while the 1/f noise from tail-current generators is totally rejected. We will start focusing on the effective noise produced by the tail transistor  $M_B$  in the left oscillator of Fig. 1(b). When  $M_{\rm cpl+}$  or  $M_{\rm sw-}$  is active, the 1/f noise from  $M_B$  is injected into node  $V_{I+}$ , while when  $M_{\rm cpl-}$  or  $M_{\rm sw+}$  is active,

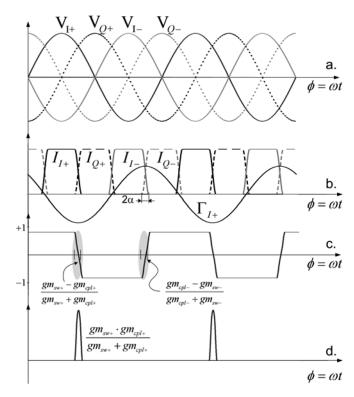


Fig. 6. CS-QO waveforms. (a) Tank voltages. (b) Device currents, together with  $\Gamma_{I+}$ . (c) Noise modulating function for  $M_B$ . (d) Noise modulating function for  $M_{\rm sw+}$ .

it is injected into node  $V_{I-}$ . During current commutations, the noise transfer function is governed by the time-variant transconductances of the devices. Straightforward circuit analysis yields the following expression for the low-frequency noise  $i_{n,M_B}$  injected differentially by  $M_B$  into the  $I_+/I_-$  tanks:

$$i_{n,M_B}(\phi) = i_{f,M_B} \cdot \begin{cases} 1, & \text{for } 0 < \phi < \frac{3}{4}\pi - \alpha \\ \frac{gm_{\text{sw}+}(\phi) - gm_{\text{cpl}+}(\phi)}{gm_{\text{sw}+}(\phi) + gm_{\text{cpl}+}(\phi)}, & \text{for } \frac{3}{4}\pi - \alpha < \phi < \frac{3}{4}\pi + \alpha \\ -1, & \text{for } \frac{3}{4}\pi + \alpha < \phi < \frac{5}{4}\pi - \alpha \\ \frac{gm_{\text{cpl}-}(\phi) - gm_{\text{sw}-}(\phi)}{gm_{\text{cpl}-}(\phi) + gm_{\text{sw}-}(\phi)}, & \text{for } \frac{5}{4}\pi - \alpha < \phi < \frac{5}{4}\pi + \alpha \\ 1, & \text{for } \frac{5}{4}\pi + \alpha < \phi < 2\pi \end{cases}$$

$$(14)$$

where  $i_{f,M_B}$  is the amplitude of the 1/f noise of the tail current, with PSD being expressed again by (6);  $gm_{\rm sw+}(gm_{\rm sw-})$  and  $gm_{\rm cpl+}(gm_{\rm cpl-})$  are the transconductances of  $M_{\rm sw+}(M_{\rm sw-})$  and  $M_{\rm cpl+}(M_{\rm cpl-})$ , and  $\alpha$  is half the angle required for complete current switching, as shown graphically in Fig. 6(b). The time-variant term in (14) is shown in Fig. 6(c). Noticing that (14) defines a waveform that is delayed by a quarter of a period with respect to  $\Gamma_{I_+}(\phi)$  (shown in Fig. 6(b) together with the device currents), and considering the symmetry of the transitions (leading to a fundamental Fourier component of (14) that is  $\pi/2$ -shifted with respect to  $\Gamma_{I_+}(\phi)$ ), the product  $\Gamma_{I_+}(\phi)$  ·  $i_{n,M_B}(\phi)$  has a zero average over the oscillation period. The effective noise contributed by the tail bias devices is therefore nil.

### B. Contributions From Differential-Pair Transistors

We examine now the effective noise contributed by the devices in the differential pairs. First of all, we notice that each transistor generates noise only during *one* current transition, not during both, as was the case in the DS-QO. To understand why, we consider, e.g.,  $M_{\rm sw+}$  in Fig. 7(a), and notice that, during the transition when the tail current switches from  $M_{\rm cpl-}$  to  $M_{\rm sw+}$ , no noise from  $M_{\rm sw+}$  is injected into the tanks, since  $M_{\rm cpl-}$  and  $M_{\rm sw+}$  are in parallel, and the noise from  $M_{\rm sw+}$  is rejected by the cascoding effect of  $M_B$  at the common-source node. On the other hand, as shown in Fig. 7(b), when the tail current switches from  $M_{\rm sw+}$  to  $M_{\rm cpl+}$ , the noise from  $M_{\rm sw+}$  does flow into the tanks in the same fashion as in the DS-QO case; thus, the amount  $i_{n,M_{\rm sw+}}(\phi)$  of 1/f noise injected differentially by  $M_{\rm sw+}$  into the  $I_+/I_-$  tanks during this transition is

$$i_{n,M_{\text{sw}+}}(\phi)$$

$$= i_{f,M_{\text{sw}+}}(\phi) \cdot \left(\frac{2gm_{\text{cpl}+}(\phi)}{gm_{\text{sw}+}(\phi) + gm_{\text{cpl}+}(\phi)}\right)$$

$$= \sqrt{\frac{2K_N}{C_{\text{ox}}\beta_{\text{sw}+}L_{M_{\text{sw}+}}^2} \cdot \frac{1}{\Delta\omega}} \cdot \left(\frac{gm_{\text{sw}+}(\phi) \cdot gm_{\text{cpl}+}(\phi)}{gm_{\text{sw}+}(\phi) + gm_{\text{cpl}+}(\phi)}\right)$$
(15)

where  $i_{f,M_{\rm sw+}}$  is the amplitude of the 1/f noise from  $M_{\rm sw+}$ . The fundamental difference, compared to that in the DS-QO case, is that  $i_{f,M_{\rm sw+}}$  is injected into the tanks only once during each oscillation period, leading to the transfer function shown in Fig. 6(d). The fundamental Fourier component is at the same frequency as  $\Gamma_{I_+}(\phi)$ , leading to a nonzero value for the integral in (2).

Closed-form expressions for device transconductances in the CS-QO can be found in [13]. The effective noise from  $M_{\text{sw}+}$ can be calculated using (15) in (2), and the same approach is, of course, used to determine the effective noise produced by all differential-pair transistors. While the integral in (2) can be solved numerically, simple closed-form results cannot be found in the general case for the CS-QO. We can, however, highly simplify the problem, assuming equal device sizes for  $M_{\rm cpl}$  and  $M_{\rm sw}$ (motivated by the fact that different sizes basically do not impact on the CS-QO behavior) and approximating the time-variant term in (15), as shown in Fig. 6(d), with a triangular shape having a peak value of  $(1/2)gm_{\text{max}}$  (where  $gm_{\text{max}}$  is the maximum value of either transconductance), and a base length of  $2\alpha$ . With these assumptions,  $M_{\rm sw}$  and  $M_{\rm cpl}$  produce the same effective noise, and considering that we have eight identical but uncorrelated sources, a simplified but nevertheless very accurate expression for the total effective noise generated by the differential-pair devices is

$$N_{L_f, M_{\mathrm{sw,cpl}}} \approx 8 \cdot \frac{1}{256C^2R^2} \frac{K_N}{\mu_{n, \mathrm{eff}} C_{\mathrm{ox}}^2 L_{\mathrm{sw,cpl}} W_{\mathrm{sw,cpl}}} \frac{1}{\Delta \omega^3}.$$
(16

We notice in (16) an inverse dependence of the effective noise on the (common) device width  $W_{\rm sw,cpl}$ . This may seem unexpected since (6) shows a 1/f noise PSD that is independent of the device width. This welcome behavior, however, is due to the

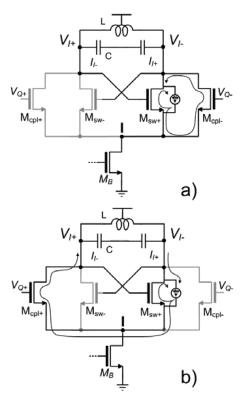


Fig. 7. (a) During current commutation between  $M_{\rm sw+}$  and  $M_{\rm cpl-}$ , the noise from  $M_{\rm sw+}$  does not flow into the tanks. (b) During current commutation between  $M_{\rm sw+}$  and  $M_{\rm cpl+}$ , a fraction of noise from  $M_{\rm sw+}$  flows into the tanks.

fact that larger transistors speed up current commutations [reducing  $\alpha$  in Fig. 6(d)], therefore reducing the limits of integration in (2) and consequently ultimately decreasing the effective noise.

Finally, the  $1/f^3$  phase noise is found by substituting (15) into (1), with oscillation amplitude  $A_0 = (\sqrt{2}/\pi)RI_B$  [33]

$$L(\Delta\omega) = 10\log\left(\frac{\pi^2 K_N}{32 \cdot \mu_{n,\text{eff}} C_{\text{ox}}^2} \frac{1}{C^2 R^4 I_B^2} \cdot \frac{1}{W_{M_{\text{sw.cpl}}} L_{M_{\text{sw.cpl}}}} \cdot \frac{1}{\Delta\omega^3}\right). \quad (17)$$

Equations (16) and (17) are shown in Figs. 8 and 9, respectively, for different values of  $W_{\rm sw,cpl}$  and are compared with the results from SpectreRF simulations (other component values and device parameters are still as reported in Table I). Also, in this case, the agreement between theory and simulations is very good.

### V. DISCUSSION AND CONCLUSION

The phase-noise analysis in the previous sections has shown that the 1/f noise upconversion into  $1/f^3$  phase noise is a first-order effect in both DS-QO and CS-QO, unlike what happens in the stand-alone harmonic oscillator, where, ideally, no 1/f noise upconversion takes place in the absence of second-order effects (such as the nonlinearities introduced by parasitic device capacitances and, in particular, varactors). However, if it is important that the  $1/f^3$  phase noise be kept to a minimum, and the different mechanisms of 1/f noise upconversion in the two topologies indicate that the DS-QO is (probably) the best choice. This is because the majority of 1/f noise upconversion

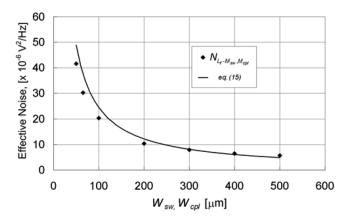


Fig. 8. Comparison between (dots) simulated and (line) calculated effective noise at 1 kHz due to the 1/f noise of the differential-pair devices in the CS-QO.

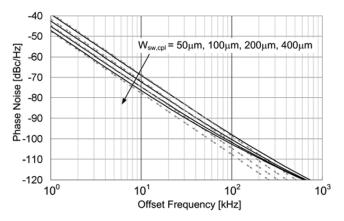


Fig. 9. (Solid lines) Simulated and (dotted lines) calculated CS-QO phase noise for different widths of the differential-pair transistors.

in the DS-QO is caused by the tail bias current MOS transistors, which are not part of the oscillator core and, as such, offer relatively straightforward ways to reduce their 1/f noise, e.g., by replacing them with resistors (at the price of a higher tail voltage drop). It is important to remark once more that the 1/f noise from the differential-pair devices in the DS-QO has a negligible impact only if these transistors do not leave the active (saturation) region of operation. To this end, a simple dc-voltage shift at the transistor gates (see, e.g., [34]) can easily be introduced to maximize the oscillation swing while keeping the transistors out of the triode region.

Our analysis has also derived a simple formula for the optimal size of the bias transistors in the DS-QO to minimize the close-in phase noise. To further reduce the noise level, the simplest measure is, of course, to increase the length of these transistors at the price of an increased width or an increased minimum drain voltage to keep them in saturation; however, alternative solutions, such as a two-transistor tail [35], are also possible. A more advanced approach is introducing a phase shifter before each coupling differential pair so that these pairs inject a coupling current that is in phase with the corresponding tank voltage [11]. In this case, the upconverted 1/f noise ideally vanishes [16].

In the CS-QO, on the other hand, the upconverted 1/f noise is predominantly generated by the core transistors. To improve

the  $1/f^3$  phase-noise performance, both width and length for these transistors may be increased, but devices cannot be made arbitrarily wide/long without adversely affecting the oscillator high-frequency and tuning performances. As an aside, we remark that, when the close-in phase noise is of a lesser concern, the CS-QO displays a better far-out phase noise than the DS-QO, for the same current consumption [13], and a lower sensitivity of the quadrature accuracy to component mismatches [33].

### REFERENCES

- [1] A. Rofougaran, G. Chang, J. J. Rael, J. Y.-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M.-K. Ku, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS—Part I: Architecture and transmitter design," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 515–534, Apr. 1998.
- [2] H. Shin, Z. Xu, and M. F. Chang, "A 1.8-V 6/9-GHz reconfigurable dual-band quadrature LC VCO in SiGe BiCMOS technology," IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 1028–1032, Jun. 2003.
- [3] S. Li, I. Kipnis, and M. Ismail, "A 10-GHz CMOS quadrature LC-VCO for multirate optical applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1626–1634, Oct. 2003.
- [4] F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour, A. Kheirkhahi, M. Nariman, M. Conta, and S. Bhatia, "A fully integrated low-IF CMOS GPS radio with on-chip analog image rejection," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1721–1727, Dec. 2002.
- [5] S. Byun, C.-H. Park, Y. Song, S. Wang, C. S. G. Conroy, and B. Kim, "A low-power CMOS bluetooth RF transceiver with a digital offset canceling DLL-based GFSK demodulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1609–1618, Oct. 2003.
- [6] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with an half rate binary phase/frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13–21, Jan. 2003.
- [7] C.-F. Liao and S.-I. Liu, "40 Gb/s transimpedance-AGC amplifier and CDR circuit for broadband data receivers in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 642–655, Mar. 2008.
- [8] I. R. Chamas and S. Raman, "A comprehensive analysis of quadrature signal synthesis in cross-coupled RF VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 689–704, Apr. 2007.
- [9] H. Zheng and H. C. Luong, "A double-balanced quadrature-input quadrature-output regenerative frequency divider for UWB synthesizer applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2944–2951, Oct. 2008.
- [10] A. Mazzanti and F. Svelto, "A 1.8-GHz injection-locked quadrature CMOS VCO with low phase noise and high phase accuracy," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 554–560, Mar. 2006
- [11] J. van der Tang, P. van der Ven, D. Kasperkovitz, and A. van Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," IEEE J. Solid-State Circuits, vol. 37, no. 5, pp. 657–661, May 2002.
- [12] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multiphase LC CMOS VCOs," IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.
- [13] P. Andreani, "A time-variant analysis of the  $1/f^2$  phase noise in CMOS parallel LC-tank quadrature oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1749–1760, Aug. 2006.
- [14] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS quadrature VCO," *IEEE J. Solid-State Cir*cuits, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.
- [15] L. Romano, S. Levantino, C. Samori, and A. L. Lacaita, "Multiphase LC oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 7, pp. 1579–1588, Jul. 2006.
- [16] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The quadrature *LC* oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.
- [17] B. Soltanian and P. Kinget, "AM-FM conversion by the active devices in MOS LC-VCOs and its effect on the optimal amplitude," presented at the RFIC Symp., San Francisco, CA, Jun. 2006.
- [18] S. Levantino, C. Samori, A. Zanchi, and A. L. Lacaita, "AM-to-PM conversion in varactor-tuned oscillators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 7, pp. 509–513, Jul. 2002.

- [19] S. Levantino, C. Samori, A. Bonfanti, S. L. J. Gierkink, A. L. Lacaita, and V. Boccuzzi, "Frequency dependence on bias current in 5 GHz CMOS VCOs: Impact on tuning range and flicker noise upconversion," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1003–1011, Aug. 2002.
- [20] A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 481–488, Mar. 2006.
- [21] A. Buonuomo, "Nonlinear analysis of voltage-controlled oscillators: A systematic approach," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1659–1670, Jul. 2008.
- [22] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [23] A. Hajimiri and T. H. Lee, "Corrections to "A general theory of phase noise in electrical oscillators"," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, p. 928, Jun. 1998.
- [24] L. Lu, Z. Tang, P. Andreani, A. Mazzanti, and A. Hajimiri, "Comments on "Comments on a general theory of phase noise in electrical oscillators"," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, p. 2170, Sep. 2008.
- [25] F. X. Kärtner, "Determination of the correlation spectrum of oscillators with low phase noise," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 1, pp. 90–101, Jan. 1989.
- [26] F. X. Kärtner, "Analysis of white and  $f^{\alpha}$  noise in oscillators," *Int. J. Circuit Theory Appl.*, vol. 18, no. 5, pp. 485–519, 1990.
- [27] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: A unifying theory and numerical methods for characterization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 655–674, May 2000.
- [28] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [29] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van derWel, G. Hoogzaad, E. van Tuijl, and B. Nauta, "Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 1022–1025, Jul. 1999.
- [30] H. Tian and A. E. Gamal, "Analysis of 1/f noise in switched MOSFET circuits," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 2, pp. 151–157, Feb. 2001.
- [31] R. Brederlow, J. Koh, and R. Thewes, "A physics-based low frequency noise model for MOSFETs under periodic large signal excitation," in *Proc. ESSDERC*, Grenoble, France, 2005, pp. 333–336.
- [32] "BSIM MOSFET Model—User's Manual," Univ. Berkeley, Berkeley, CA. [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/bsim\_ent.html

- [33] A. Mazzanti, F. Svelto, and P. Andreani, "On the amplitude and phase errors of quadrature *LC*-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1305–1313, Jun. 2006.
- [34] A. Mazzanti and P. Andreani, "A 1.4 mW 4.9-to-5.65 GHz class C CMOS VCOs, with an average FoM of 194.5 dBc/Hz," in *Proc. IEEE ISSCC*, Feb. 2008, pp. 474–475.
- [35] P. Andreani and A. Fard, "More on the  $1/f^2$  phase noise performance of CMOS differential-pair LC-tank oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.



Andrea Mazzanti (S'01–M'06) received the Laurea and Ph.D. degrees in electrical engineering from the Università degli Studi di Modena e Reggio Emilia, Modena, Italy, in 2001 and 2005, respectively.

During the summer of 2003, he was an Internship Student with Agere Systems, Allentown, PA, working on the design of a highly integrated CMOS FM transmitter. In 2005, he got a postdoctoral position with the Dipartimento di Elettronica, Università di Pavia, Pavia, Italy. He is currently an Assistant Professor with the Dipartimento di Ingeg-

neria dell'Informazione, Università degli Studi di Modena e Reggio Emilia, teaching a course in advanced analog IC design. His main research interests include device modeling and integrated circuit for RF and millimeter-wave communications.



**Pietro Andreani** (M'03–SM'07) received the M.S.E.E. degree from the University of Pisa, Pisa, Italy, in 1988 and the Ph.D. degree from Lund University, Lund, Sweden, in 1999.

In 1990–1993, he was with the Department of Applied Electronics (currently the Department of Electrical and Information Technology), Lund University, where he was an Associate Professor who was in charge of the analog IC courses in 1995–2001. Between 2001 and 2007, he was a Professor with the Center for Physical Electronics, Technical University

of Denmark, Lyngby, Denmark. Since 2007, he has been with the Department of Electrical and Information Technology, Lund University, with analog/RF IC design as his main research field.