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Design and implementation of Phase Locked Loop on 180nm Technology node

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Abstract— **This paper signifies the transient analysis of the PLL and is implemented in cadence tool using 180nm technology node. Frequency is expected to be in GHz range for present communication systems to increase the speed and therefore PLL is designed to produce the frequency in GHz range. The designed PLL consists of Phase frequency detector/Charge pump (PFD/CP), second order Low pass filter (LPF) and Schmitt trigger based current starved voltage controlled oscillator (CSVCO). PLL is designed to achieve a stable frequency output. The designed PLL produces 1.084 GHz with 2.382mW of average power consumption.**

Keywords—Frequency, Phase locked loop (PLL), Phase frequency detector/Charge pump (PFD/CP), Low pass filter (LPF), Schmitt trigger, Current starved voltage controlled oscillator (CSVCO).

I. INTRODUCTION

In today's world, Phase Locked Loop (PLL) is the major part of all SOC's since it is the only circuit that will generate the system clock. Fundamentally, PLL is a form of servo loop. It is a control system that compares the phase of output signal with input signal and also detects the phase error. Fig. 1 illustrates the basic block diagram of PLL which consists of phase detector (PD), Low pass filter (LPF) and Voltage controlled oscillator (VCO). Phase error is detected by the PD block where one input is the reference signal and the other is the feedback signal from VCO output. A question may arise that when we already have a stable reference oscillator then what is the need for PLL. This can be justified by saying that the reference oscillator has low frequency and hence we need VCO in order to generate high frequency. The reference oscillator with low frequency is stable whereas VCO's high frequency is slightly unstable. To make it stable Schmitt trigger based CSVCO is implemented in the design of PLL. The main objective is to get a stable frequency output. Then the stabilized frequency can be used for synchronization purpose in many applications.

PLL is a useful circuit block that can also be widely used in the fields like wireless applications, general electronic items from mobile phones to broadcast radios, televisions to Wi-Fi routers, FM demodulation, AM demodulation, frequency synthesizers, signal recovery and many more.

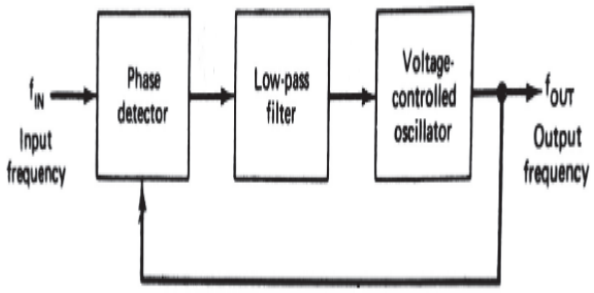

Fig. 1. Basic block diagram of PLL

Earlier, multiplier was used as analog phase detector but it had limited lock range and also when the phase error was greater than 90°, it would result in reduced output voltage. Later, digital phase detector was implemented whose average value was proportional to the phase error. Initially, X-OR phase detector was used which was linear but if the phase error was greater than 180° then it would lose its linearity. Therefore phase frequency detectors are designed to detect both phase and frequency difference which is very useful because it increases the lock speed of PLLs. Hence the PFD blocks can be implemented using D, SR or JK Flip Flops [1].

For the design of LPF, earlier first order low pass filter was designed but it would result in ripple because control voltage experiences large jump when current is injected from charge pump. To solve this problem second order low pass filter can be designed which will suppress the ripple created. Hence using the second order LPF makes PLL of third order [2].

Initially Voltage controlled oscillators were implemented using ring oscillators or LC oscillators. But the drawback of ring oscillators was that it was not stable as it was based on the switching characteristics of logic gates which may fluctuate +/-20% and the drawback of LC oscillators was large die area utilization [3][4]. So current starved VCO are being implemented [5].

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II. METHODOLOGY

As mentioned in introduction, from Fig. 1 PLL has mainly three blocks: phase detector, low pass filter and voltage controlled oscillator. PD gives the phase error output voltage. This voltage is fed to the LPF that produces control voltage which is required for tuning the VCO. Next, the VCO's output is fed back to the PD block in order to get locked.

A. PHASE DETECTOR:

Earlier analog PD was used such as multiplier but digital types PD are majority in use because of their simplicity when compared to analog PD. In digital type PD, Exclusive-OR PD is the simplest type. The output of this circuit is high only when one of the two input signals is high. The next is the edge triggered phase detectors using flip flop. Here phase and frequency errors can be detected by D Flip Flop, JK Flip Flop or SR Flip Flop.

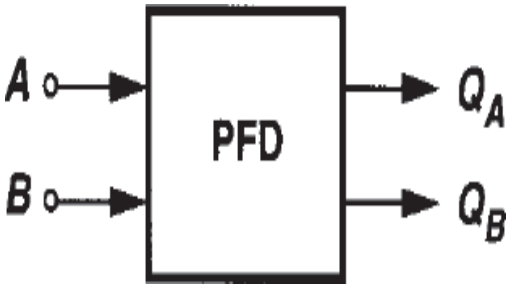

Fig. 2. PFD block

Fig. 2 illustrates the block of PFD block with two inputs and two outputs where reference frequency is given as one input and the other input is given by the feedback from the output of VCO. The two output Fig. 2(a) and Fig. 2(b) show the phase and frequency errors respectively [6].

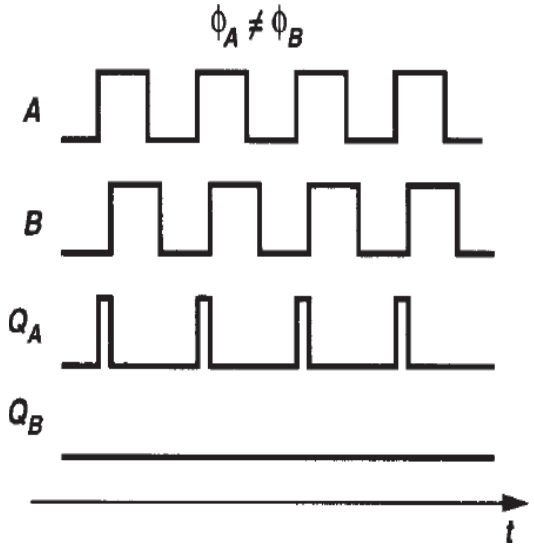

Fig. 2(a). Phase error

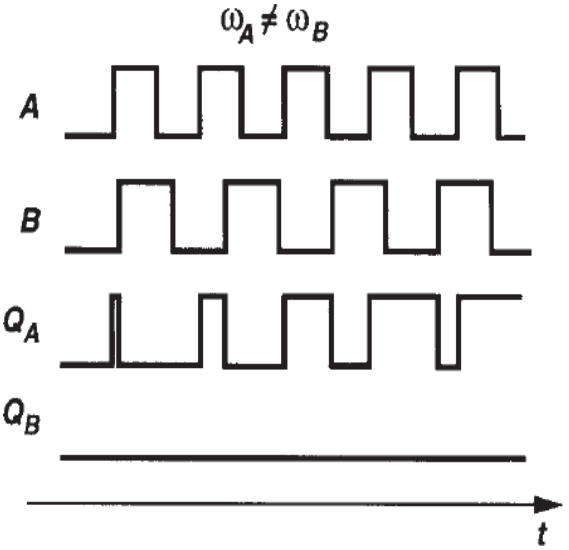

Fig. 2(b). Frequency error

B. LOW PASS FILTER:

It is more commonly used to filter out the high frequency signals and it allows only the required range of frequency. In order to produce a stable and clean control voltage for the VCO, further filtering of the error signal is needed. Active or passive filters can be used. Active filters add noise components that can affect the VCO hence passive filters can be used. Depending on application the order of the LPF can be chosen [2].

C. VOLTAGE CONTROLLED OSCILLATOR:

As the name implies, by controlling the input voltage the output frequency can be varied that is, the frequency can be increased or decreased as illustrated in Fig. 3.

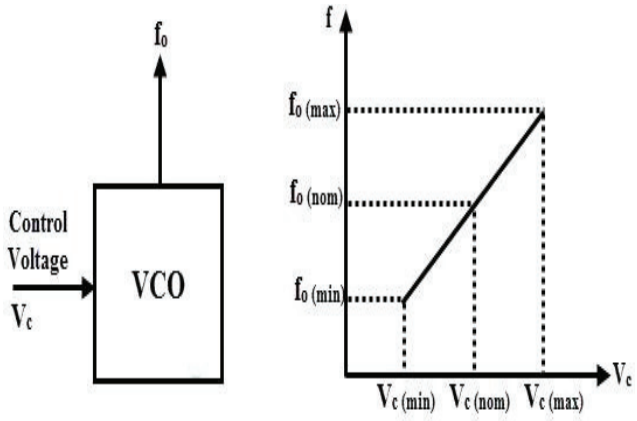

Fig. 3. VCO block

III. DESIGN AND IMPLEMENTATION

The implementation of PLL as mentioned earlier consists of PFD/CP, second order LPF and Schmitt trigger based CSVCO. Fig. 4 shows the block diagram of PLL.

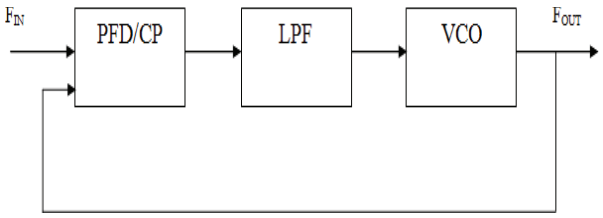

Fig. 4. Block diagram of PLL

A. PHASE FREQUENCY DETECTOR/CHARGE PUMP:

PFD is phase frequency detector which gives the phase and frequency difference between the reference signal and the VCO generated signal and this results in an output voltage that is proportional to the phase error. Fig. 5 illustrates the gate level implementation of PFD/CP block.

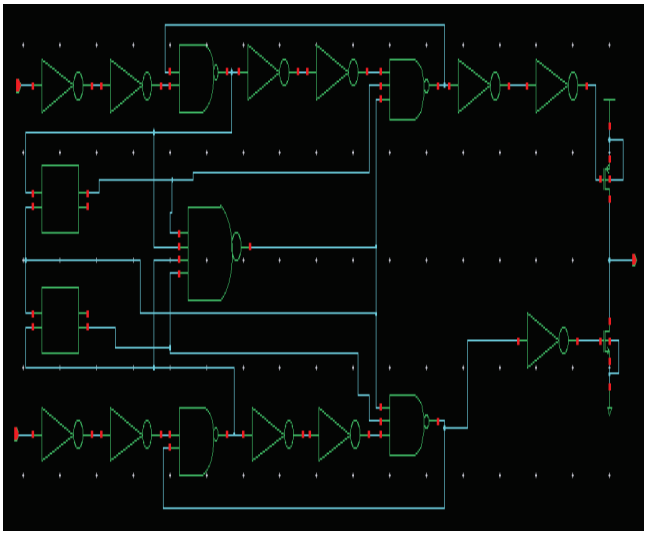

Fig. 5. Gate level implementation of PFD/CP

This block consists of two SR flip flops along with the resetting chain. The reset signal is triggered when both the inputs are high at the same time. The reset pins of both the SR flip-flops are connected together and the two set pins are the inputs with reference signal being one input and VCO's output as another input.

The charge pump is used so that the output from the PFD should be combined into a single output to drive the LPF and it also pumps in and pumps out the charge through the LPF and hence the name charge pump. The digital pulses generated from the PFD are sent to the charge pump and this gives the continuous analog signal. A charge pump in the Fig. 5 comprises of an inverter and a PMOS at the top and an NMOS at the bottom (right side).

B. LOW PASS FILTER:

The low pass filter used in this design is the passive low pass filter, which permits only low frequency signals and doesn't let the high frequency to pass through. Therefore, this filter permits only the DC voltage that is desired which acts as control input voltage to the next block of the design that is VCO.

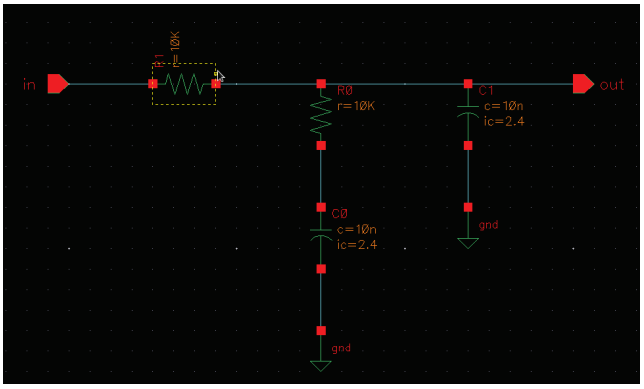

Fig. 6. Schematic of LPF

Fig.6 illustrates that the low pass filter is of the second order. Here C_1 is concurrently placed with respect to the resistor R_0 and capacitor C_0, so that C_1 will filter out the ripple that is generated by resistor which affects the control input voltage required for VCO.

C. SCHMITT TRIGGER BASED CSVCO:

The performance of VCO is of paramount importance as its design is critical for the performance of the system. VCO is an oscillator whose output frequency is controlled by a voltage input.

VCO schematic includes three blocks: current starved inverter, Schmitt trigger and followed by the regular CMOS inverters.

1) CURRENT STARVED INVERTER:

Fig. 7 illustrates the schematic of current starved inverter.

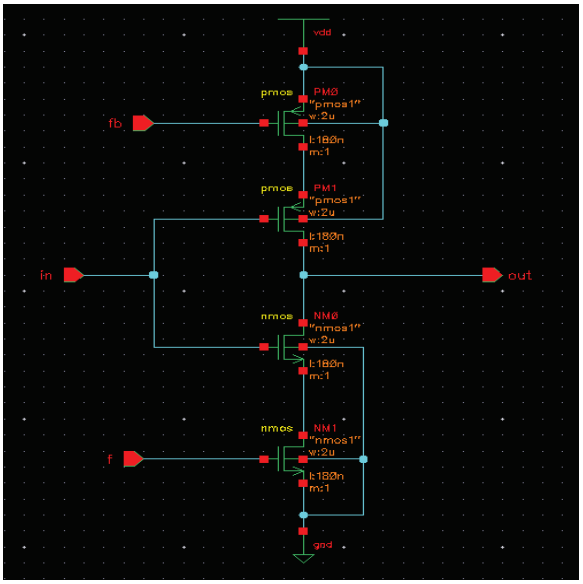

Fig. 7. Schematic of current starved inverter

In order to get stable frequency each inverter stage must be delay controlled because the oscillation frequency depends on the delay of each inverting stage and therefore two extra transistors PM0 and NM1 are added to an inverter circuit in Fig. 7. Hence by controlling the amount of current to charge and discharge the load capacitance of each inverting stage the delay can be controlled. The pins of these two extra transistors PM0 and NM1 are connected to PMOS and NMOS transistors as shown in Fig. 9 (1st and 3rd inverter from the right). Both PMOS and NMOS have same drain currents and is set by the input control voltage. Hence the current in these PMOS and NMOS are mirrored to transistors PM0 and NM1 respectively and also to the next stages when cascaded.

2) SCHMITT TRIGGER CIRCUIT:

When the input is triangular or sine wave Schmitt trigger circuit generates clean square wave pulses and it also removes noise from these input signals. Fig. 8 illustrates the schematic of Schmitt trigger circuit.

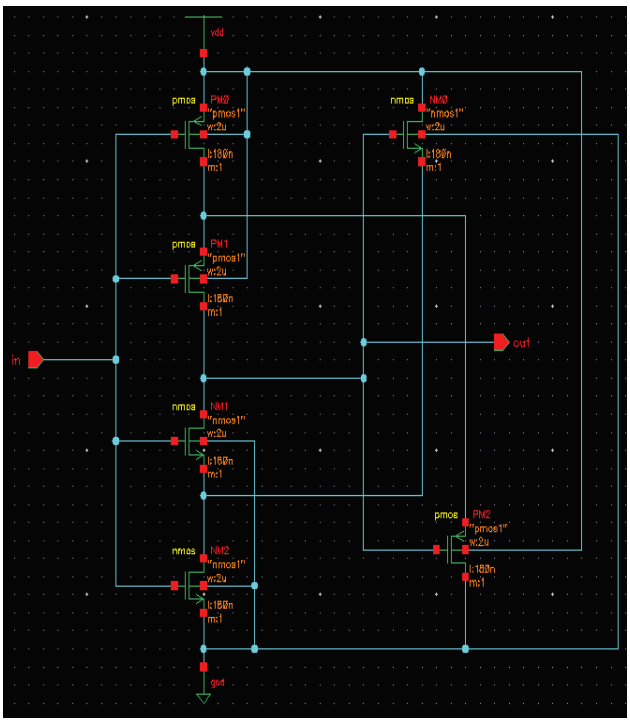

Fig. 8. Schematic of Schmitt trigger circuit

In Fig. 8 MOSFETs PM1 and NM1 have high threshold voltage than PM0 and NM2. The hysteresis width is determined by the MOSFETs PM2 and NM0. If input is low then PM0 and PM1 are turned ON and NM1 and NM2 are OFF and so the output is at VDD level. When input arrives at the threshold voltage of NM2 then it turns ON and NM1 is OFF, hence pass transistor logic NM0 also turns ON when NM2 turns ON. When the input voltage arrives at the threshold voltage of NM1 then it is in ON state. Hence instead of complete supply level NM0 pulls the node to VDD-VT. When NM2 turns ON it pulls the output node between NM1 and NM2 and when NM1 turns ON there will be low logic level at the output node. This high voltage is called V_{IH}. When input is high then PM0 and PM1 turn OFF and NM2 and NM1 are ON. This low voltage is called V_{IL}.

VCO with the combined current starved inverter, Schmitt trigger circuit and regular CMOS inverter is illustrated in Fig. 9. From the right side of the figure, first and third inverters are the current starved inverters, second and fourth are the Schmitt trigger circuits and the rest are normal inverters.

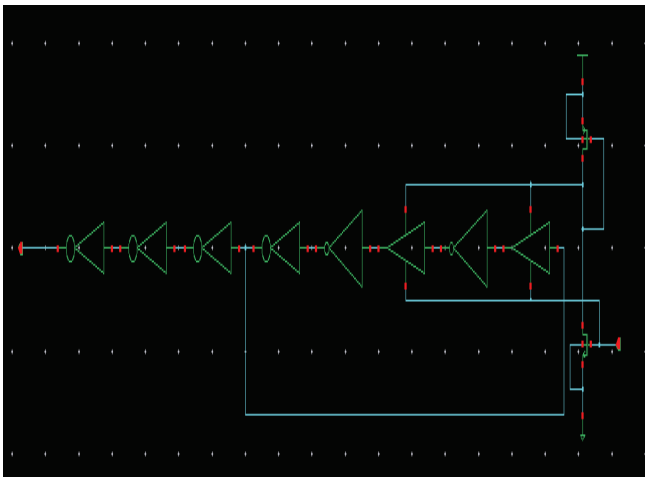

Fig. 9. Schmitt trigger based CSVCO

IV. RESULTS AND OBSERVATIONS

Fig. 10 and Fig. 11 are the outputs of PFD. Fig. 10 illustrates the scenario when the 1st signal is leading the 2nd and so here the error signals are shown in the up signal that is the third signal of waveform. Fig. 11 illustrates the case when 2nd signal is leading the 1st and hence error signals are shown in the down signal that is the fourth signal of the waveform. Fig. 12 illustrates the output of VCO where oscillations can be seen in the form of pulse and it operates with the supply voltage of 1.8V.

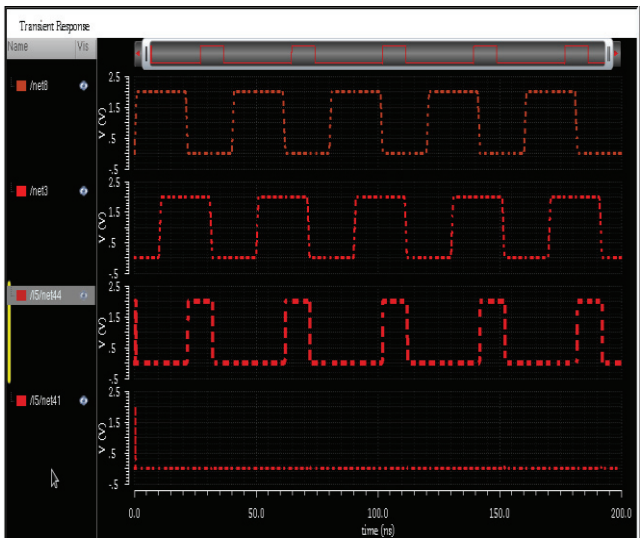

Fig. 10. Error signal when 1st signal is leading

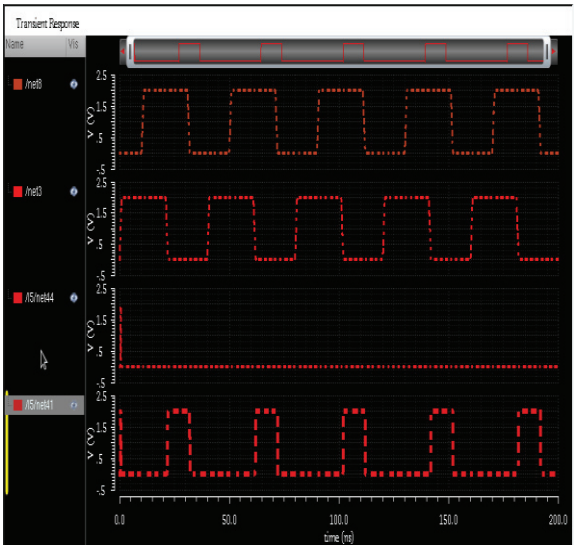

Fig. 11. Error signal when 2nd signal is leading

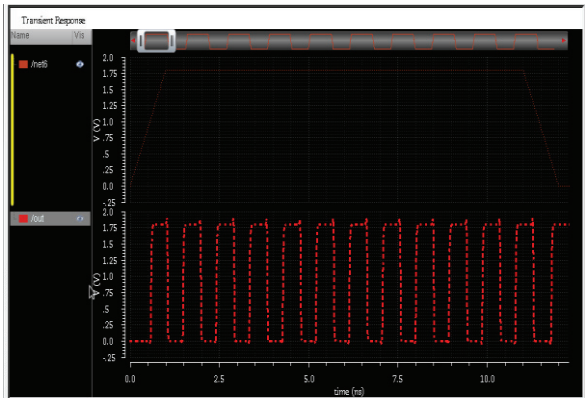

Fig. 12. VCO output

After the connection of all three blocks of PLL in Fig. 13 and then simulating this design the output obtained is illustrated in Fig. 14 where the stable frequency is acquired. Detailed view of PLL output is illustrated in Fig. 15.

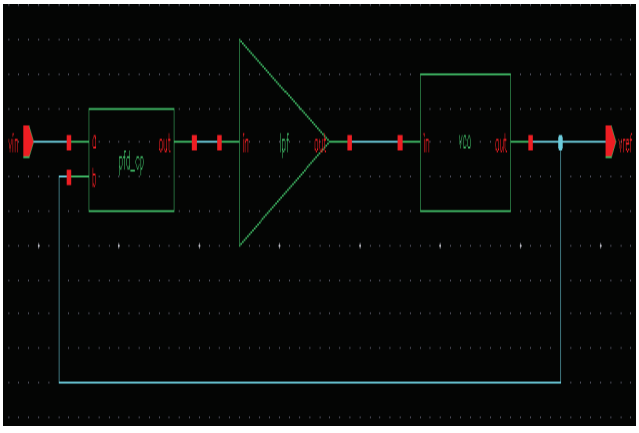

Fig. 13. Connection of all three blocks

The PLL generates frequency of 1.084GHz from the 100MHz input and operates at 1.8V power supply. The PLL consumes 2.382m watt of average power.

Frequency is calculated with the formula frequency(v("/out" ?result "tran")) and average power by average(getData(":pwr" ?result "tran")) in cadence.

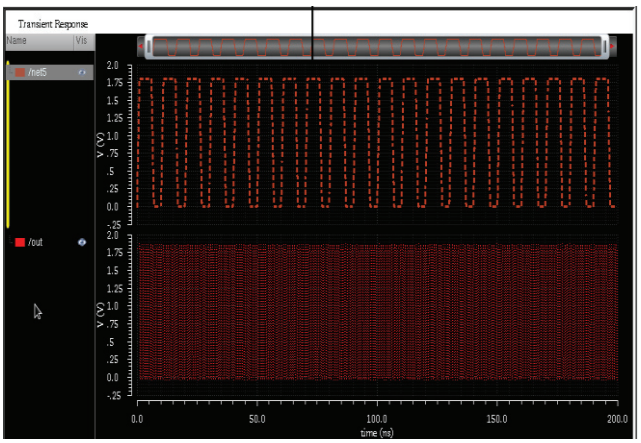

Fig. 14. Output waveform of PLL

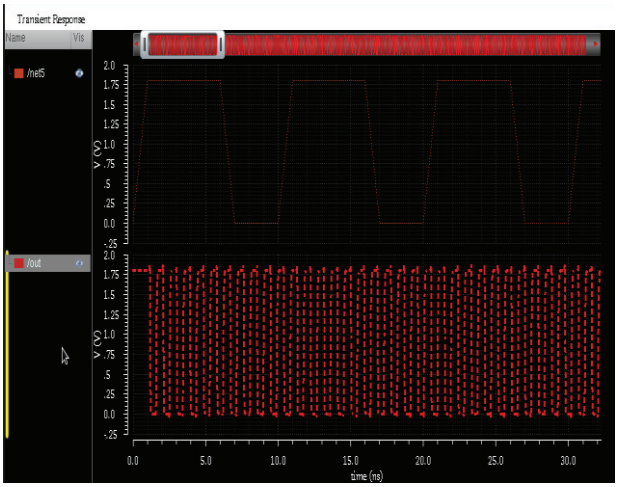

Fig. 15. Detailed view of PLL output

V. CONCLUSION

The PLL in this paper is implemented on 180nm technology using cadence tool. The designed PLL works at 1.8V and produces an output frequency of 1.084GHz which falls under the category of ultra high frequencies ranging from 300MHz to 3GHz and finds its application in the RF wireless communication system, cellular phones, PAN (personal area network), etc. The average power consumed by the PLL is 2.382mw.

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