CMOS Low Noise Amplifier Design Optimization Techniques

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***Abstract*—This paper reviews and analyzes four reported low noise amplifier (LNA) design techniques applied to the cascode topology based on CMOS technology: classical noise matching (CNM), simultaneous noise and input matching (SNIM), power-constrained noise optimization (PCNO), and power-constrained simultaneous noise and input matching (PCSNIM) techniques. Very simple and insightful sets of noise parameter expressions are newly introduced for the SNIM and PCSNIM techniques. Based on the noise parameter equations, this work provides clear understanding of the design principles, the fundamental limitations, and the advantages of the four reported LNA design techniques so that the designers can get the overall LNA design perspective. As a demonstration for the proposed design principle of the PCSNIM technique, a very low power folded-cascode LNA is implemented based on 0.25 μm CMOS technology for 900 MHz Zigbee applications. Measurement results show the noise figure of 1.35 dB, power gain of 12 dB, and IIP3 of –4 dBm while dissipating 1.6 mA from 1.25 V supply (0.7 mA for the input NMOS transistor only). The overall behavior of the implemented LNA shows good agreement with theoretical predictions.**

***Index Terms*— LNA, CMOS, Noise Optimization, RF, Zigbee, Low-Power, Low-Voltage.**

I. INTRODUCTION

THE CMOS has become a competitive technology for radio transceiver implementation of various wireless communication systems due to the technology scaling, higher level of integrability, lower cost, etc. [1], [2]. In a typical radio receiver, the low noise amplifier (LNA) is one of the key components as it tends to dominate the sensitivity. The LNA design involves many trade-offs between noise figure (NF), gain, linearity, impedance matching, and power dissipation [3]. Generally, the main goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. A number of LNA design techniques have been reported to satisfy these goals. To name a few representatives: the classical noise matching (CNM) technique [4], simultaneous noise and input matching (SNIM) technique [5], power-constrained noise optimization (PCNO) technique [6], and power-constrained simultaneous noise and input matching (PCSNIM) technique [7]. However, these previously reported works describe only one of these techniques and the analysis approaches tend to be inconsistent with each other. The goal of this paper is to analyze the four LNA design techniques based on the noise parameter expressions and try to provide consistent and perspective understanding of CMOS based LNA design techniques. Section A summarizes the reported analytic details of the CNM technique based on the noise parameter expressions and point out the limitations. In section B, the noise parameter expressions of the SNIM technique are newly introduced, and the LNA design principles as well as the limitations are discussed. Section C summarizes the key concept and the limitations of the PCNO technique described in [6]. In section D, the noise parameter expressions of the PCSNIM technique are newly introduced, and the LNA design principles, the potential as low power LNA, and the practical limitations are explained. Section III describes the design and measurement details of a very low power LNA following the design guidelines provided in section D based on 0.25 μm CMOS technology. Section IV concludes this work.

II. NOISE OPTIMIZATION TECHNIQUES

A. Classical Noise Matching (CNM) Technique

The classical noise matching (CNM) technique was reported in [4]. In this technique, the LNA is designed for minimum noise figure F_{min} by presenting the optimum noise impedance Z_{opt} to the given amplifier, which is typically implemented by adding a matching circuit between the source and the input of the amplifier. By using this technique, the LNA can be designed to achieve NF equal to F_{min} of transistor, the lowest NF that can be obtained with given technology. However, due to the inherent mismatch between Z_{opt} and Z_{in}^* (where Z_{in}^* is the complex conjugate of the amplifier input impedance), the amplifier can experience a significant gain mismatch at the input. Therefore, the CNM technique typically requires compromise between the gain and noise performance.

Figure 1-(a) shows a cascode-type LNA topology, which is one of the most popular topology due to its wide bandwidth, high gain, and high reverse isolation. In the given example, the selection of the cascode topology simplifies the analysis, and the gate-drain capacitance can be neglected.

Fig. 1-(b) shows the simplified small-signal equivalent circuit of the cascode amplifier for the noise analysis including the intrinsic transistor noise model. In Fig. 1-(b), the effects of the common-gate transistor M_2 on the noise and frequency response are neglected [3], [8], as well as the

parasitic resistances of gate, body, source, and drain terminal.

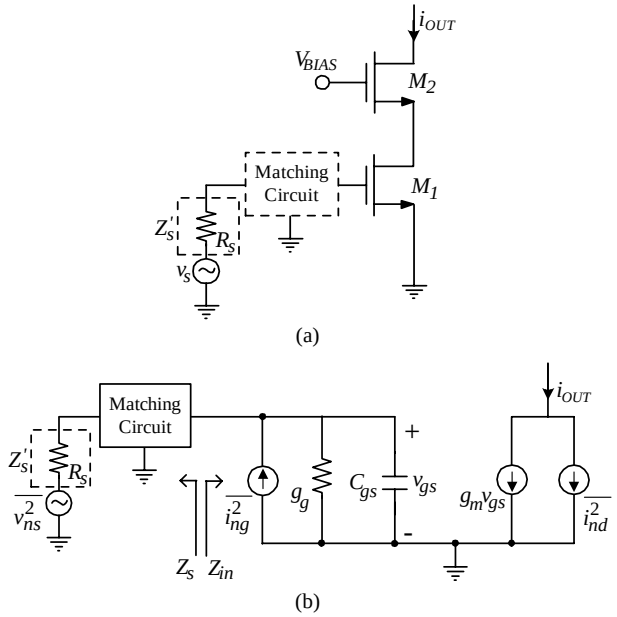

Fig. 1. The schematic of a cascode LNA topology adopted to apply the CNM technique (a) and its small-signal equivalent circuit (b).

In Fig. 1-(b), $\overline{i_{nd}^2}$ represents the mean-squared channel thermal noise current, which is given by [9]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{1}$$

where g_{do} is the drain-source conductance at zero drain-source voltage V_{DS} and k the Boltzmann constant, T the absolute temperature, and Δf the bandwidth, respectively. The parameter γ has a value of unity at zero V_{DS} and 2/3 in saturation mode operation with long channel devices. The value of γ increases at high V_{GS} and V_{DS} and can be more than two in short-channel devices.

The fluctuating channel potential due to the channel noise current shown in Eq. (1) couples capacitively into the gate terminal, leading to a noisy gate current. As in [9], the mean-squared gate-induced noise current is given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2}$$

where
$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{3}$$

In Eq. (2), δ is a constant with value of 4/3 in long-channel devices, and C_{gs} represents the gate-source capacitance of the input transistor. Like γ, the value of δ also increases in short-channel devices and at high V_{GS} and V_{DS}. Since the gate-induced noise current has correlation with the channel noise current, a correlation coefficient is defined as follows [9]

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \tag{4}$$

With long channel devices, c can be predicted theoretically as j0.395 [9]. The value of c is purely imaginary reflecting the capacitive coupling between the channel and gate-induced noise sources. After some lengthy algebraic derivations [3], the noise parameters for the cascode amplifier shown in Fig. 1-(a) can be expressed as

$$R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{5}$$

$$Y_{opt}^o = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{6}$$

$$F_{min}^o = 1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{7}$$

where R_n^o represents the noise resistance, Y_{opt}^o the optimum noise admittance, $F_{\min}^o$ the minimum noise factor, respectively. In Eq. (7) the cutoff frequency ω_T is equal to g_m/C_{gs}, and $\alpha \equiv g_m/g_{do}$ is unity for long-channel devices and decreases as channel length scales down. In Eqs. (5) - (7), the superscripted zero is adopted as a differentiation with other cases.

Note that, from Fig. 1-(b), the input admittance is purely capacitive, i.e. $Y_{in}^o = j\omega C_{gs}$. By comparing the complex conjugate of Y_{in}^o with Eq. (6), it can be seen that the optimum source admittance for input matching is inherently different from that of the noise matching in both real and imaginary parts. Thus, with the given example, one cannot obtain both input matching and minimum noise figure simultaneously. This is the main limitation of the CNM technique when applied to the LNA topology shown in Fig. 1-(a). Note that the imaginary component of Eq. (6) is inductive, but the frequency response is like that of a capacitor. Hence, there is a fundamental limitation in achieving a broadband noise matching.

B. Simultaneous Noise and Input Matching (SNIM) Technique

Feedback techniques are often adopted in designing low-noise amplifiers in order to shift the optimum noise impedance Z_{opt} to the desired point. Parallel feedback has been applied for wideband [10]-[12] and better input/output matching [13]. Series feedback has been preferred to obtain simultaneous noise and input matching without the degradation of NF [14]-[17]. Especially, the series feedback with inductive source degeneration, which is applied to the common-source or cascode topology, is widely used for narrow band applications [5], [18]-[24].

Fig. 2-(a) and (b) show a cascode LNA with inductive source degeneration and the simplified small-signal equivalent circuit.

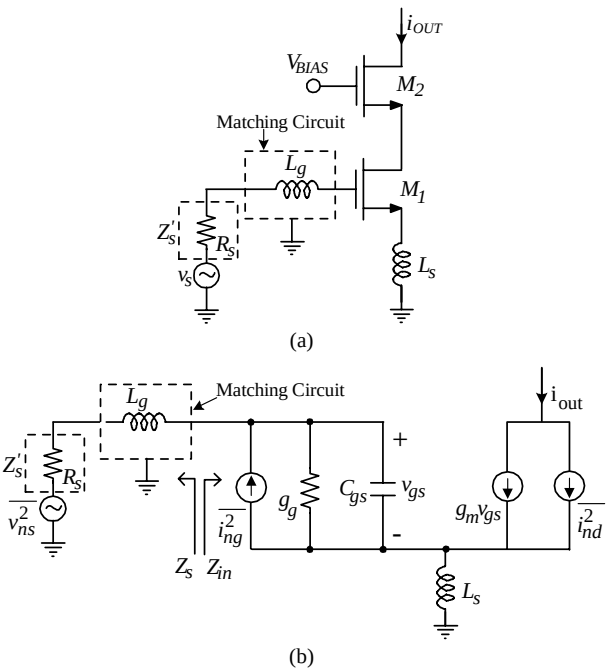

Fig. 2. The schematic of a cascode LNA topology adopted to apply the SNIM technique (a) and its small-signal equivalent circuit (b).

In Fig. 2-(b), the same simplifications are applied as in Fig. 1-(b). The following are the ways to obtain the noise parameter expressions of a MOSFET with series feedback: noise transformation formula using noise parameters [25], using the noise matrix [26], [27], or KCL/KVL with noise current sources [3], [6]. Like Eqs. (5)-(7), the noise parameters seen into the gate of the circuit shown in Fig. 2-(b) can be obtained. The procedures described in [3] and [6] are used in this work. The derivation is somewhat tedious, but the result is simple enough to provide useful insights. The detailed derivations are summarized in the APPENDIX assuming the inductors are lossless. In the APPENDIX, to simply the derivation, it is assumed that the matching circuit is implemented by a series inductor L_g, and $Z_s^{'} = R_s$. As shown in the APPENDIX, the noise factor and noise parameters can be given by

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + s^2 C_{gs} \left(L_g + L_s \right) \left(1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}} \right) \right]^2 \\ -\left(sC_{gs} R_s \right)^2 \left(1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}} \right)^2 \end{array} \right\} - \frac{\alpha\delta}{5} \left(1 - |c|^2 \right) g_m \left(sC_{gs} \right)^2 \left(R_s^2 - sL_g^2 \right) \right\} \tag{8}$$

$$R_n = R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{9}$$

$$Z_{opt} = Z_{opt}^o - sL_s \tag{10}$$

$$F_{min} = F_{min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{11}$$

In Eqs. (9)-(11), the noise parameters with superscripted zeros are those of the cascode amplifier with no degeneration (see Eqs. (5)-(7)). Note that Eq. (10) is expressed in impedance as it is simpler in this case and Z_{opt}^o is given by

$$Z_{opt}^o = 1/Y_{opt}^o = \frac{\alpha \sqrt{\frac{\delta}{5\gamma\left(1 - |c|^2\right)}} + j\left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma\left(1 - |c|^2\right)} + \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} \tag{12}$$

Note that, from Eqs. (9)-(11), only Z_{opt} is shifted and there is no change in R_n and F_{min}. Also, note that Eqs. (9)-(11) are valid for any arbitrary matching circuits as well as the source impedance $Z_s^{'}$ in Fig. 2. In addition, as shown in Fig. 2-(b), the input impedance Z_{in} of the given LNA can be expressed as

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} = sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \tag{13}$$

As can be seen from Eq. (13), the source degeneration generates real part at the input impedance. This is important because there is no real part in the Z_{in} without degeneration while there is in the Z_{opt}. Therefore, if not excessive, L_s helps to reduce the discrepancy between the real parts of the Z_{opt} and the Z_{in} of LNA. Furthermore, from Eq. (13), the imaginary part of Z_{in} is changed by sL_s, and this is followed by the same change in Z_{opt} as shown in Eq. (10). From Eq. (12), Eq. (10) can be re-expressed as

$$Z_{opt} = \mathrm{Re}\left[Z_{opt}^o \right] - m\frac{1}{sC_{gs}} - sL_s \tag{14}$$

where the constant m, for the typical device parameters of long channel MOSFETs, is approximately equal to 0.6. With technology scaling, the ratio δ/γ stays nearly constant at 2 [3], [9], α becomes lower than 1 [28], and c is slightly higher than 0.4 (e.g., $c \approx 0.5$ with 0.25 μm technology [29]), such that the constant m is expected to become closer to 1. Therefore, from Eqs. (13) and (14), it can be seen that the inductive source degeneration helps to bring the Z_{opt} point close to the optimum source impedance point Z_{in}^* while causing no degradation in F_{min} and R_n. This characteristic reveals the potential for the SNIM technique.

For the circuit shown in Fig. 2-(a), the condition that allows the simultaneous noise and input matching is

$$Z_{opt} = Z_{in}^* \tag{15}$$

From Eqs. (9), (10), (11), and (13), the conditions that satisfy Eq. (15) and the matching with the source impedance Z_s are as follows

$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}\left[Z_s \right] \tag{16}$$

$$\mathrm{Im}[Z_{opt}] = \mathrm{Im}\left[Z_s \right] \tag{17}$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}\left[Z_s \right] \tag{18}$$

$$\mathrm{Re}[Z_{in}] = \mathrm{Re}\left[Z_s \right] \tag{19}$$

As described above, based on Eqs. (13) and (14), Eqs. (17) and (18) are the same, especially in advanced technology.

Therefore, Eq (18) should be dropped considering the importance of the noise performance. Some amount of mismatch in the input matching has negligible effect on the LNA performance while the mismatch in Z_{opt} directly affects the NF. Now then, from Eqs. (9)-(13), the design parameters that can satisfy Eqs. (16), (17), and (19) are V_{GS}, the transistor size W (or C_{gs}), and L_s. Minimum gate length is assumed to maximize the transistor cutoff frequency ω_T. Therefore, for the given value of Z_s, Eqs. (16), (17), and (19) can be solved since three effective equations are provided with three unknowns.

Qualitatively, the LNA design based on SNIM technique can be explained as follows. Following Eqs. (16), (10), and (12), for an arbitrary signal source impedance Z_s, choose a transistor size (C_{gs}) which satisfies $\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s]$. For the given transistor size C_{gs}, choose the degeneration inductor size L_s that satisfies Eq. (17), $\mathrm{Im}[Z_{opt}] = -\mathrm{Im}[Z_s]$. Then, for the given values of C_{gs} and L_s, the value of V_{GS} can be determined from Eq. (19), $\mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s]$. Note that, as discussed above, for the given L_s the imaginary value of the optimum noise impedance would automatically be approximately equal to that of the input impedance with an opposite sign, $\mathrm{Im}[Z_{in}] \approx -\mathrm{Im}[Z_s]$. Now, from Fig. 2-(b), if $Z_s = Z_s^{'}$, then the simultaneous noise and input matching is achieved to the signal source impedance. If not, the matching circuit shown in Fig. 2 should be added. The design methodology described above guarantees the NF of LNA equal to the F_{min} of the common-source transistor with nearly perfect input impedance matching.

The above LNA design technique suggests that by the addition of L_s, in principle, the simultaneous noise and input matching can be achieved at any values of Z_s by satisfying Eqs. (16), (17), and (19) assuming Eqs. (9)-(11) are valid. Many cases, especially those with large transistor size, high power dissipation, and high frequency of operation, Eqs. (16), (17), and (19) can be satisfied without much difficulty while Eqs. (9)-(11) stay valid. The problem occurs when the transistor size is small (hence the power dissipation is small) and the LNA operates at low frequencies. Eq. (12) indicates that the small transistor size and/or low frequency leads to high value of $\mathrm{Re}[Z_{opt}]$. Therefore, from Eq. (13), for the given bias point or ω_T, the degeneration inductor L_s has to be very large to satisfy Eq. (19). The problem is that for the L_s to be greater than some value, Eq. (11) becomes invalid and F_{min} increases significantly [30]. As a result, the minimum achievable NF of the LNA can be considerably higher than F_{min} of the common-source transistor, spoiling the idea of simultaneous noise and input matching. In other words, the SNIM technique is not applicable for the transistor sizes and bias levels (or the power dissipation levels) as $\mathrm{Re}[Z_{opt}]$ becomes greater than $\mathrm{Re}[Z_{in}]$ for the value of L_s, which does not degrade the F_{min} of the LNA. The inaccuracy of Eq. (11) for large L_s might be caused by the negligence of C_{gd}. With large L_s, the transconductance of the common-source stage can degrade significantly and the feedback signal through C_{gd} could become non-negligible. As a practical design technique, the minimum value of L_s, which does not degrade the F_{min}, can be identified by monitoring the F_{min} of the LNA as a function of L_s in simulation.

Note that from Eq. (13), even with a small transistor, low power, and low frequency, the input matching can still be satisfied by proper selection of the degeneration inductance. It was found that for the small amount of power dissipation where the SNIM technique is not applicable, there exists an optimum transistor size that provides minimum NF while satisfying input matching [6]. However the achievable minimum NF is higher than F_{min} of the common-source transistor. This power-constrained LNA optimization technique is the subject of the topic that will be discussed in the following section.

C. Power-Constrained Noise Optimization (PCNO) Technique

With a constrained amount of power dissipation, the simultaneous gain and noise matching approach can still be useful. At any given amount of power dissipation, Eqs. (18) and (19) can be satisfied by the proper selection of L_s for the given C_{gs}, with the help of the matching circuit shown in Fig. 2 which is typically implemented by a series inductance L_g. It can be shown that, under fixed drain current and while satisfying Eqs. (18) and (19), there exists a transistor size where the NF of the amplifier becomes minimum [6]. From [3], this optimum transistor size is given by

$$W_{opt} \approx \frac{1}{3\omega C_{ox} R_s Q_{in,opt}} \tag{20}$$

where

$$Q_{in,opt} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{21}$$

In Eq. (20), C_{ox} represents the gate-oxide capacitance of the MOSFET per unit area. The minimum noise figure in this case F_{minP} can be given by [3]

$$F_{minP} \approx 1+2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right] \tag{22}$$

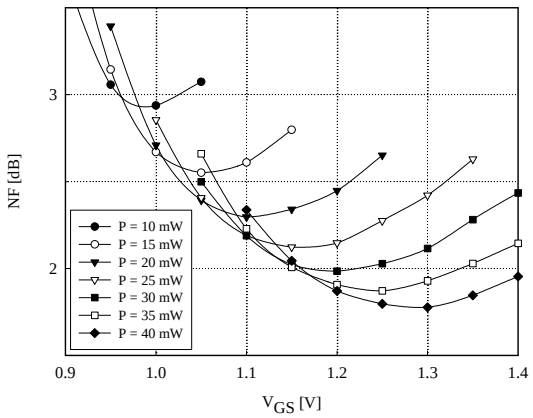

Fig. 3. The simulated NF of a cascode LNA with inducting degeneration as function of power dissipation and transistor size. A 0.8 μm high-resistivity-substrate CMOS technology is used for the simulation at 2 GHz.

As described in [3], F_{minP} is higher than F_{min}, the minimum noise figure of the common-source transistor. The reason for $F_{minP} > F_{min}$ is due to the mismatch between Z_s and Z_{opt} and/or the high values of L_s which leads to higher F_{min} as discussed previously. Fig. 3 shows the noise figure of a cascoded LNA with inductive degeneration as a function of power dissipation and transistor size. In Fig. 3, the simulation is done at 2 GHz based on a 0.8 μm high-resistivity-substrate CMOS technology and the inductors are assumed ideal. As can be seen in Fig. 3, at each level of power dissipation, there exists a transistor size that provides minimum NF. The PCNO technique will eventually converge to the SNIM technique as the power dissipation increases and therefore satisfies Eqs. (16), (17), and (19).

D. Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) Technique

As described in section B and C, the SNIM and PCNO techniques do not allow simultaneous noise and input matching at low power implementations. However, the need for low power implementation of radio transceiver is one of the inevitable technical trends. Fig. 4-(a) shows a cascoded amplifier topology that can satisfy the simultaneous noise and input matching at low power. Note that the difference in Fig. 4-(a) compare to the LNA shown in Fig. 2-(a) is one additional capacitor C_{ex}. Fig. 4-(b) shows the simplified small-signal equivalent circuit of Fig. 4-(a). Again, in Fig. 4-(b), the same simplifications are applied as in Fig. 1-(b) and Fig. 2-(b). For the given small-signal circuit shown in Fig. 4-(b), following the similar approach as described in the APPENDIX, rather simple sets of noise parameter equations can be derived by replacing Eq. (2) with the following expression

$$\overline{i_{ng}^2} = 4kT\delta_{eff}\frac{\omega^2 C_t^2}{5g_{do}}\Delta f \tag{23}$$

where $\delta_{eff} = \delta.\left(C_{gs}^2/C_t^2\right)$ and $C_t = C_{gs} + C_{ex}$. Eq. (23) is the same expression as Eq. (2), but is just rewritten for the simpler mathematics. The noise parameters can be given by

$$R_n = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{24}$$

$$Z_{opt} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}} + j\left(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{25}$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2}} \tag{26}$$

Interestingly, as can be seen from Eqs. (24) and (26), the noise resistance R_n and the minimum noise figure F_{min} are not affected by the addition of C_{ex}, the same as the cases shown in Fig. 1 and 2. From Fig. 4-(b), the input impedance of the LNA can be given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \tag{27}$$

Now then, it can be seen that the Eqs. (24)-(27) are similar to the Eqs. (9)-(11) and (13). As discussed in section B, the Eqs. (24)-(26) are valid for rather small values of L_s.

Now, like the LNA topology shown in Fig. 2-(a), for the simultaneous noise and input matching of the circuit shown in Fig. 4-(a), Eq. (15) needs to be satisfied, and that means that the conditions shown in Eqs. (16)-(19) should be satisfied. From Eqs. (25) and (27), Eqs. (16)-(19) can be re-expressed as follows

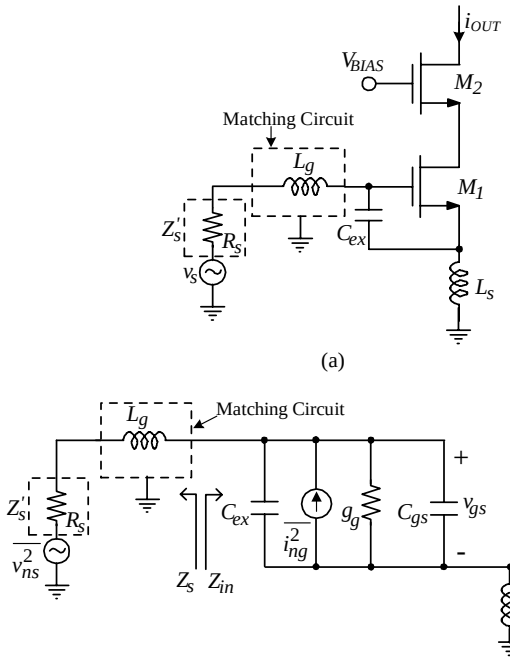

Fig. 4. The schematic of a cascode LNA topology adopted to apply the PCSNIM technique (a) and its small-signal equivalent circuit (b).

$$\frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s] \tag{28}$$

$$\frac{j\left(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{gs}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = \mathrm{Im}[Z_s] \tag{29}$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \tag{30}$$

$$\frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \tag{31}$$

As discussed in section B, for the typical values of advanced CMOS technology parameters, Eq. (29) is

approximately equal to Eq. (30). Therefore, Eq. (30) can be dropped, which means that, as in section B, for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with an opposite sign, $\mathrm{Im}[Z_{in}] \approx -\mathrm{Im}[Z_s]$ automatically,. Now then, the design parameters that can satisfy Eqs. (28), (29), and (31) are V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, Eqs. (28), (29), and (31) can be solved for an arbitrary value of Z_s, by fixing the value of one of the design parameters. Therefore, in the PCSNIM LNA design technique, by the addition of an extra capacitor C_{ex}, the simultaneous noise and input matching can be achieved at any level of power dissipation.

Note that, like the case of SNIM technique, Eqs. (24)-(26) are derived assuming L_s is not very large. The validity of this assumption in low power LNA can be investigated. From Eqs. (28) and (31), the following approximated relation can be made

$$L_s \approx \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega\omega_T C_t} \tag{32}$$

Eq. (32) indicates that L_s is a function of C_t and ω_T (which is a function of V_{GS}). In comparison, for the SNIM technique, a similar relation can be obtained from Eqs. (10), (14), (16), and (19) as

$$L_s \approx \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega\omega_T C_{gs}} \tag{33}$$

By comparing Eqs. (32) and (33), it can be seen that in the PCSNIM technique applied for the low power design, where C_{gs} is small, the required degeneration inductance, L_s, can be reduced by the addition of C_{ex}. In fact, by applying the PCSNIM technique to the SNIM technique-based LNA, the required degeneration inductance L_s can be reduced below what the SNIM technique requires.

The qualitative description of the PCSNIM design process would be as follows. First, choose the DC bias, V_{GS}, for example, the bias point that provides minimum F_{min}. Then, choose the transistor size W based on the power constraint P_D. Now choose the additional capacitance C_{ex} as well as the degeneration inductance L_s to satisfy Eqs. (28) and (31) simultaneously. The value of C_{ex} should be chosen considering the compromise between the size of L_s and the available power gain. As described before, too much L_s can lead to the increase in F_{min}, while large C_{ex} leads to the gain reduction due to the degradation of the effective cut-off frequency of the composite transistor (transistor including C_{ex}). At this point, the simultaneous noise and input matching is achieved. As the last step, if there exists any mismatch between Z_{in} and $Z_s^{'}$, as shown in Fig. 4(b), an impedance matching circuit can be added.

The limitation of the PCSIM technique is the high value of noise resistance. From Eq. (24), the noise resistance R_n of the proposed topology is not affected by the addition of C_{ex} but depends only on the value of g_m. Therefore, the small transistor size and low power dissipation can lead to very high R_n. High R_n can be a serious limitation for the practical high yield LNA design. Fig. 5 shows the simulated *NF* and input return loss S_{11} as a function of frequency for the LNA topology shown in Fig. 4-(a) for three transistor sizes. In Fig. 5, the simulation is based on 0.25 μm CMOS technology with the supply voltage of 1.25 V. The amount of power dissipation is varied by changing the transistor size, which leads to the supply current of 1.6, 4.8 and 9.6 mA, for a given value of gate-source voltage. As can be seen in Fig. 5, in addition to the good input matching, for all power levels, the NF of the designed LNAs coincides with the F_{min} of the transistor at the frequency of interest. Note that, as explained above, with reduction in the amount of power dissipation (smaller transistor size), due to the larger R_n, the NF of LNAs increases sharply at the frequencies away from the optimum point.

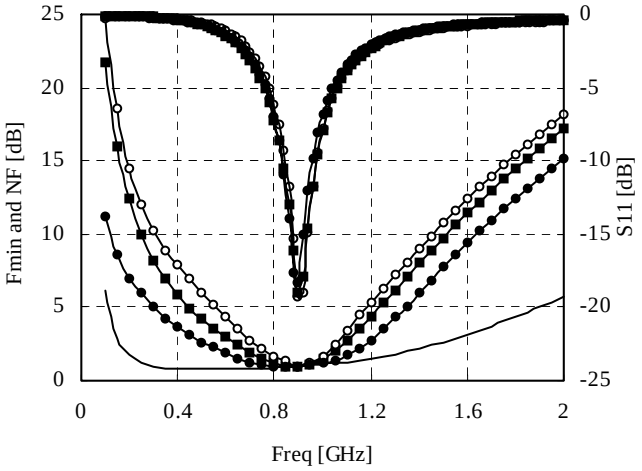

Fig. 5. The simulated NF, Fmin, and S11 of the LNA shown in Fig. 4 following the PCSNIM technique as a function of frequency. The simulation includes LNA design for three levels of power dissipation based on 0.25 μm CMOS technology.

Considering the relationship between the cut-off frequency (f_T) and the total input capacitance, the addition of C_{ex} leads to power gain degradation. For example, if $C_{ex} = 3C_{gs}$, the f_T of LNA is expected to be reduced by the factor of 4. This would lead to the reduction of the maximum oscillation frequency (f_{max}) by the factor of $\sqrt{2}$, 71%, due to the square-root functional dependence of the f_{max} on f_T. Therefore, it could be considered that the power gain is slow function of C_{ex}. From the simulation of the case shown in Fig. 5, the maximum available gain of LNA is degraded by 1 dB for $C_{ex} = 1.5\ C_{gs}$ at 900 MHz.

Table I summarizes and compares the advantages and disadvantages of the four LNA design techniques discussed in Section II. As can be seen in Table I, the PCSNIM technique offers a new prospect in low power LNA design.

Table I. Summary of the characteristics for the four LNA design techniques

Parameters	CNM [4]	SNIM [5]	PCNO [6]	PCSNIM [7]
Power-Constrained	Yes	Yes, at rather high power dissipation	Yes	Yes
Input matching	Typically No	Yes	Yes	Yes
NF = F_{min}	Yes	Yes	Mostly no	Yes

III. LNA DESIGN

The LNA designs following the CNM, SNIM, and PCNO techniques have been confirmed through the fabrications and measurements [30]- [33]. However, none of the measurement results have been reported following the design principles of the PCSNIM technique. Fig. 6 shows a folded cascode type LNA topology that is chosen to apply the PCSNIM technique. The LNA shown in Fig. 6 is designed based on 0.25 μm CMOS technology for 900 MHz Zigbee application [34], which requires very low power dissipation and low supply voltage. In Fig. 6, the folding of the common-gate transistor helps to extend the cut-off frequency of the common-source transistor. Furthermore, the parasitic capacitances at the drain node of the common-source transistor can easily be eliminated by the resonance with the inductance at the supply pin L_d. The elimination or the reduction of this parasitic capacitance helps to suppress the noise contribution of the common-gate transistor at the output and avoid the signal loss into the silicon substrate [32]. In Fig. 6, the size of C_{ex} and L_s are chosen following the design principle of the PCSNIM technique, and L_g is inserted for the input matching to the signal source impedance of 50 Ω. In this design, the value of L_d is 33 nH, and L_s is 3.9 nH, which is implemented by combining off-chip inductor and wire bonding. The size of transistor M_1 is 0.25μm x160μm. The values of C_{ex} and L_g are 500 fF and 33 nH, respectively. A simple L-C network using an off-chip inductor L_o and an on-chip capacitor C_o are used to match the output of the LNA. The high-Q and 20 nH off-chip inductor L_o helps to improve the linearity of the LNA [35]. In Fig. 6, the LNA dissipates the total current of 1.6 mA from the supply voltage of 1.25 V where the common-source and common-gate stages consume 0.7 and 0.9 mA, respectively. Considering the linearity, the higher amount of current is allocated at the common-gate stage.

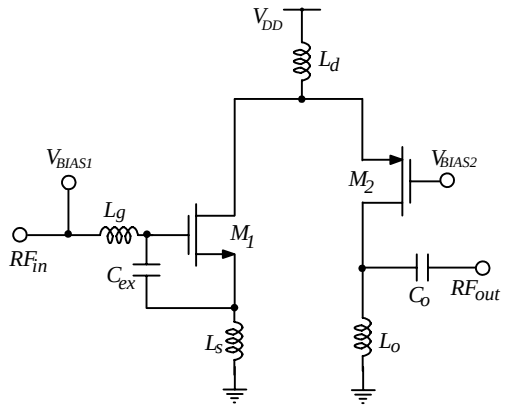

Fig. 6. The schematic of a folded cascode LNA, which adopts the PCSNIM technique.

Fig. 7 shows the measurement results of the LNA shown in Fig. 6. As can be seen in Fig. 7, the LNA shows power gain of 12 dB, NF of 1.35 dB, and S_{11} of –18 dB, respectively, at 910 MHz. Note that in Fig. 7, the F_{min} of the LNA is also shown as a function of frequency, and it can be seen that the NF of the LNA coincides with F_{min} very well at the frequencies of interest showing good agreement with what was expected theoretically. From Fig. 5, the simulated NF and S_{11} of the same circuit at 910 MHz are 1.05 dB and –19 dB, respectively. Fig. 8 shows the measured IIP3 of – 4 dBm and Fig. 9 shows the microphotograph of the LNA. Table II summarizes the measured performances of the LNA.

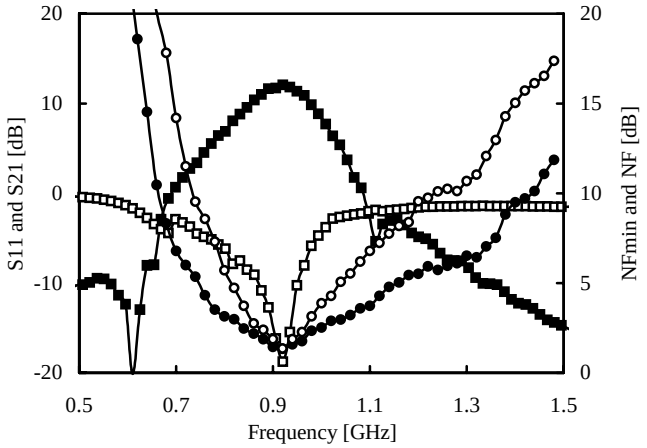

Fig. 7. The measured NF, F_{min}, power gain, and S_{11} of the LNA shown in Fig. 6 as a function of frequency

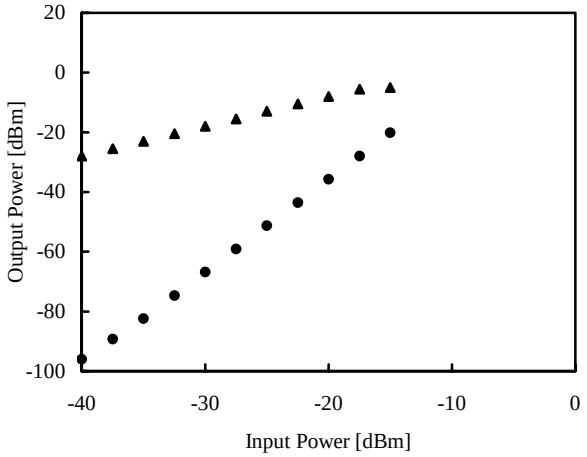

Fig. 8. The measured IIP3 of the LNA shown in Fig. 6.

TABLE II SUMMARY OF THE MEASURED 900 MHz LNA PERFORAMCNES

Parameters	**Values**
Operating frequency [MHz]	900
Power Gain [dB]	12
Noise Figure [dB]	1.35

IIP3 [dBm]	-4
Technology [μm]	0.25
Power dissipation [mW]	1.6x1.25

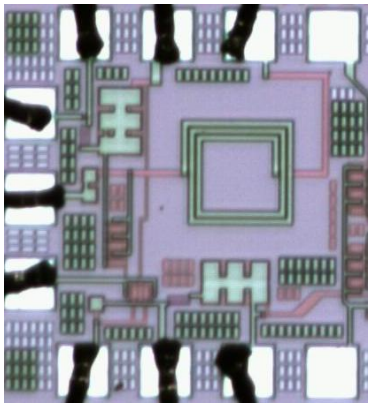

Fig. 9. The microphotograph of the LNA shown in Fig. 6.

IV. Conclusion

Four well-known LNA design optimization techniques: the classical noise matching (CNM), simultaneous noise and input matching (SNIM), power-constrained noise optimization (PCNO), and power-constrained simultaneous noise and input matching (PCSNIM) techniques are reviewed and analyzed. Very simple and insightful sets of noise parameter expressions are newly introduced for the cases of the SNIM and the PCSNIM techniques. Based on the noise parameter expressions, the design principles, advantages, and limitations of each technique are discussed. With the CNM technique, the LNA can be designed for the minimum noise figure F_{min} of the given technology at any given amount of power dissipation. However, the LNA typically experiences inherent input mismatch problems. With the SNIM technique, the condition for the simultaneous noise and input matching can be satisfied by the proper selection of the transistor sizes and the degeneration inductances. This technique, in principle, can be applied for any levels of power dissipation as long as Re[Z_{opt}] = Re[Z_{in}] is satisfied and the F_{min} of the LNA is not degraded by the degeneration inductance. However, with low power application, the SNIM technique is not useful. With low power design, the increase in the value of the degeneration inductance to force the condition of Re[Z_{opt}] = Re[Z_{in}] leads to the degradation of F_{min}. In this situation, the PCNO technique can be applied. The PCNO technique, which is proposed as a low power LNA design technique, provides an optimum transistor size that can obtain minimum noise figure for the given amount of power dissipation. However, with PCNO technique, the noise figure of the LNA is higher than the F_{min} of the LNA. As an alternative, the PCSNIM technique can be used for the low power design. The PCSNIM technique allows the same performance advantages as the SNIM technique, i.e., simultaneous noise and input matching at the power level where the SNIM technique cannot be applied. The disadvantages of the PCSNIM technique are the higher value of noise resistance R_n and the lower value of effective cut-off frequency. With the production development, higher R_n can be the source of lower yield. Overall, based on the noise parameter equations, this work provides clear understanding of the design principles, the fundamental limitations, and the advantages of the reported LNA design techniques so that the designers can get the general LNA design perspective.

As a demonstration for the proposed design principle of the PCSNIM technique, a very low power folded-cascode LNA is fabricated based on 0.25 μm CMOS technology for 900 MHz Zigbee applications. Measurement results show the noise figure of 1.35 dB, power gain of 12 dB, and IIP3 of –4 dBm while dissipating 1.6 mA from 1.25 V supply. The NMOS input stage of the LNA dissipates only 0.7 mA. The overall behavior of the implemented LNA shows good agreement with the proposed design principle.

Appendix

As can be seen in Fig. 2-(b), the mean-squared output noise current of the source terminal is given by

$$\overline{i_{o,ns}^2} = \left|\frac{R_s}{D}\cdot g_m\right|^2 \cdot \overline{i_{ns}^2} \qquad \text{(A1)}$$

Here the denominator D is

$$D = 1 + s^2 C_{gs}\left(L_g + L_s\right) + s\left(C_{gs}R_s + g_m L_s\right) \qquad \text{(A2)}$$

When the admittance of the source termination is purely resistive, the source admittance is expressed as $Y_s = G_s = (R_s)^{-1}$, so that the mean-squared noise current by the source is $\overline{i_{ns}^2} = 4kTG_s\Delta f$.

The mean-squared output noise current by the gate induced noise source is

$$\overline{i_{o,ng}^2} = \left|\frac{R_s + s\left(L_g + L_s\right)}{D}\cdot g_m\right|^2 \cdot \overline{i_{ng}^2} \qquad \text{(A3)}$$

Since the mean-squared output noise current by the channel noise source is changed by the feedback source inductance L_s, so that the expression is

$$\overline{i_{o,nd}^2} = \left|\frac{1 + s^2 C_{gs}(L_g + L_s) + sC_{gs}R_s}{D}\right|^2 \cdot \overline{i_{nd}^2} \qquad \text{(A4)}$$

At the resonance condition for the matching, the reactance of the input impedance is zero, therefore, the first two terms in the denominator of (A2) and the numerator of (A4) are summed to zero, i.e., $1 - \omega C_{gs}(\omega L_g + \omega L_s) = 0$. Considering the correlation between the gate-induced and the channel noise sources, the gate induced noise current is expressed as the sum of uncorrelated and correlated components. The mean-squared expression of the induced-gate noise is

$$\overline{i_{ng}^2} = \overline{i_{ngu}^2} + \overline{i_{ngc}^2} = 4kT\delta g_g(1 - |c|^2) + 4kT\delta g_g |c|^2 \qquad \text{(A5)}$$

Here the coefficient of the correlation between gate-induced and channel noise sources is

$$\frac{i_{ngc}}{i_{nd}} = j\,|\,c\,|\,\frac{\sqrt{\overline{i_{ng}^2}}}{\sqrt{\overline{i_{nd}^2}}} \tag{A6}$$

The total output noise current consists of the output current from the resistive source termination, the gate-induced noise, and the channel noise sources. Considering correlation, the total output noise current is expressed as

$$|\,i_{o,total}\,|^2 = |\,i_{o,ns} + i_{o,ng} + i_{o,nd}\,|^2 = |\,i_{o,ns}\,|^2 + |\,i_{o,ngc} + i_{o,nd}\,|^2 + |\,i_{o,ngu}\,|^2 \tag{A7}$$

The noise factor (F) is defined as the ratio between total mean-squared output noise current and the mean-squared output noise current due to input source only, i.e.,

$$F \equiv \frac{|\,i_{o,total}\,|^2}{|\,i_{o,ns}\,|^2} \tag{A8}$$

Therefore, by using (A1)-(A8) the noise factor can be given by

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \begin{array}{l} \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + s^2 C_{gs} \left(L_g + L_s \right) \left(1 + |\,c\,| \alpha \sqrt{\frac{\delta}{5\gamma}} \right) \right]^2 \\ -\left(sC_{gs} R_s \right)^2 \left(1 + |\,c\,| \alpha \sqrt{\frac{\delta}{5\gamma}} \right)^2 \end{array} \right\} \\ -\frac{\alpha\delta}{5} \left(1 - |\,c\,|^2 \right) g_m \left(sC_{gs} \right)^2 \left(R_s^2 - sL_g^2 \right) \end{array} \right\} \tag{A9}$$

In general, F can be expressed as follows [4],

$$F = F_{min} + \frac{R_n\,|\,Y_s - Y_{opt}\,|^2}{G_s} \tag{A10}$$

The noise resistance, R_n, can be obtained by comparing (A9) with (A10). The optimum source impedance Z_{opt} can be obtained by solving the zero solutions after differentiating (A10) with respect to R_s and L_g, respectively. Now by inserting Z_{opt} expression into (A9), F_{min} can be obtained. After some tedious calculations, the noise parameters can be derived as follows

$$R_n = R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{A11}$$

$$Z_{opt} = Z_{opt}^o - sL_s \tag{A12}$$

$$F_{min} = F_{min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |\,c\,|^2)} \tag{A13}$$

Here the superscripted zero is adopted to represent the corresponding noise parameters of the common-source amplifier with no degeneration (see Eqs (5)-(8)).

In (A12), the optimum noise impedance without source degeneration is equal to

$$Z_{opt}^o = 1/Y_{opt}^o = \frac{\alpha \sqrt{\frac{\delta}{5\gamma(1 - |\,c\,|^2)}} + j\left(1 + \alpha\,|\,c\,| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma(1 - |\,c\,|^2)} + \left(1 + \alpha\,|\,c\,| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} \tag{A14}$$

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