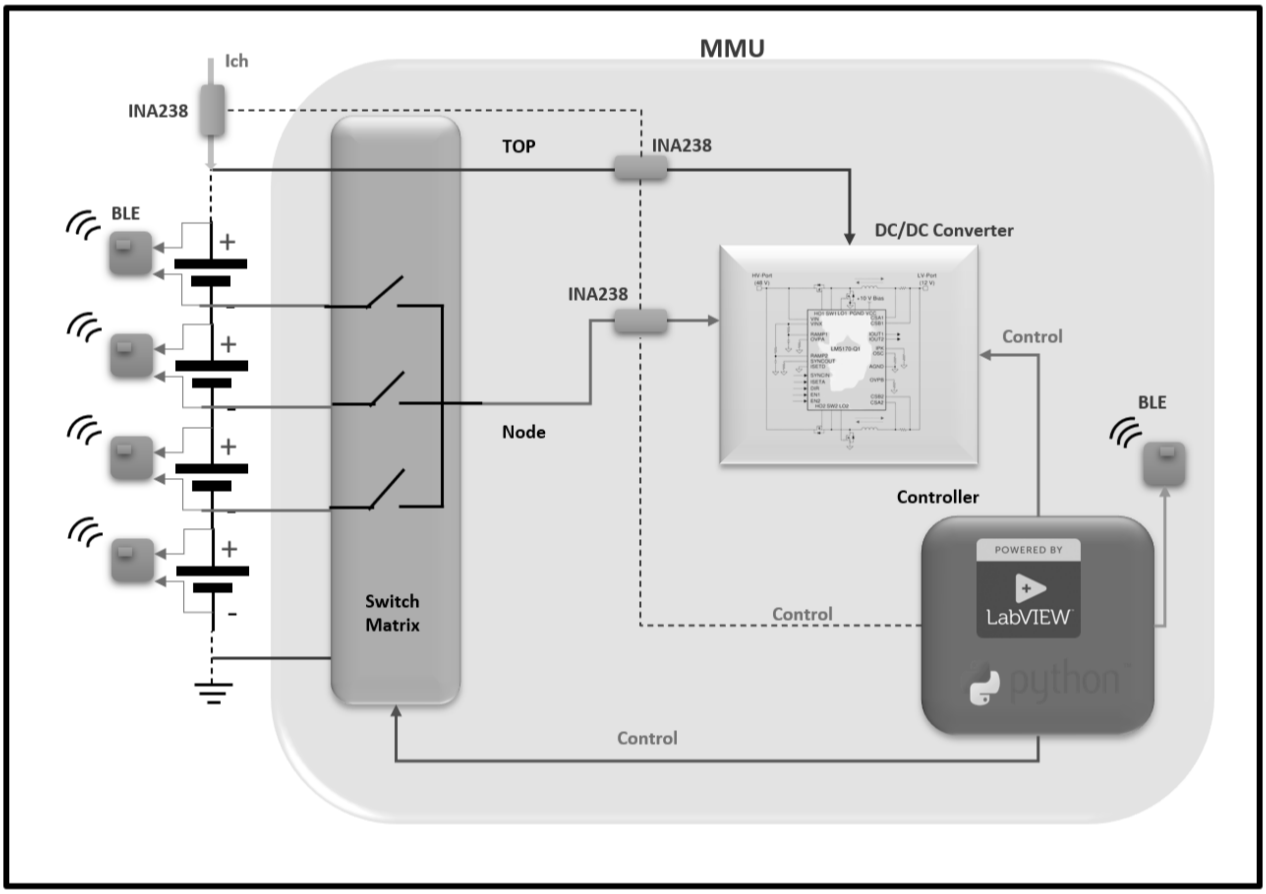
SOC and SOH estimation in BMS based on Wireless Communication Network



UNIVERSITA' DI PAVIA

Department of Electrical, Computer and Biomedical Engineering
University of Pavia

SOC and SOH estimation in BMS based on Wireless Communication Network

Dissertation submitted in partial fulfillment

of the requirements for the degree of

Master of Science

in

Microelectronics

by

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based on research carried out

under the supervision of

Prof. Piero Malcovati

and

Prof. Domenico Granozio

UNIVERSITA' DI PAVIA

December, 2022

Department of Electrical, Computer and Biomedical Engineering
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To

My Beloved Mother Miss.Kalavathi Shivaramappa ...

Acknowledgment

First and foremost, I express my deep appreciation and gratitude to my advisor, *Prof. Piero Malcovati* for his active support and crucial guidance throughout my master's Thesis program. It's his guidance that provided me with perspective and intuitive skills along with analytical capabilities that helped me to improve my technical understanding. His constructive approach and passion for his job are very inspirational to me. His positive words and encouragement always cheered me up, to gain productivity and proactiveness.

I also like to extend my gratitude to acknowledge my co-advisor and Manager of the Application Team in *Inventvm*, *Eng. Domenico Granozio* for his association and active collaboration from Inventvm. The challenging tasks assigned to me enhance and outreach my potential. His supervision and suggestions always helped me to set and organize the agenda, follow it systematically, and accomplish the tasks within the specified time.

Further, I would like to thank *INVENTVM*, Pavia, for providing me with the resources and the opportunity to execute my Thesis idea. During the Master Thesis, while I spent 11 months in the Inventvm, *Luigi Pinna* was always there to help me out, in terms of instrument setup and lab activity challenges, so I also thank him for his great contribution to the project.

A Significant contribution from my colleagues in the Inventvm application team must be acknowledged at this moment, and everyone has been part of my one-year thesis programmable, and they made me the happiest person in the work environment. Every colleague in the inventvm application team made my work more productive with healthy discussions and performances. *Riccardo, Flavio*, and *Antonino* were there to have a conversation full of amusement. So on and so forth I have thanked every colleague who is directly related to my thesis program, but there is one specific person that I must thank, though he is not directly part of the project. *Musico' Marco* , IT support and coordinator deserves my most friendly appreciation and thanks, because of his social interaction and humble nature of explaining nativity of things made me very much comfortable over my journey...so thank you *Marco* you deserve it!.

Last but not least, I would like to thank my beloved parents, who fostered me by teaching me the value of education, for their unconditional love and support towards me, for encouraging me in every crucial step of my life and for believing in me. Thanks to my gorgeous sister *Ashwini* who gives me a feeling of myself being her pride, for her immense support.

Harish Kumar Shivaramappa
University of Pavia
December 2022

Abstract

Determining the SOC ad SOH of the Li-Ion batteries by employing the Conventional Coloumb count method and sophisticated Kalman filter algorithms in a wireless communication network(BLE). With the help of a Battery Emulator, The proposed Architecture measures synchronized current and voltage for SOC and SOH calculation by ensuring safety and adaptivity. By employing the Most Robust and Elegant Wireless Communication Network(BLE) in BMS, the architecture mitigates the problem of bulky and wired setups.

***Keywords*: *BMS*; *SOC*; *SOH*; *BLE*; *Coloumb-Count*; *Kalman Filter*; *Battery Emulator*.**

Contents

List of Figures

List of Tables

Chapter 1

Preface

When started my Microelectronics master's program at the University of Pavia, I was wondering about the future of microelectronics in the domain of electric vehicle and sustainable energy management because I have witnessed personally how world leaders are crumbling to fix global warming and climate change. The idea of making global warming free through sustainable energy drove me to explore electrical vehicles and power management. As I was intensively researching my self about electrical vehicles and battery management systems, I got an opportunity to enroll LM+ program at the university of Pavia which is doing an internship through the university in corporate companies for one year.

Among the LM+ opportunities, I have noticed that Inventvm a dynamic young Italian company is doing research on Battery management systems for electrical vehicles. Since my interest is to work in power management and sustainable energy management, the Inventvm BMS project became a cherry on the pie for me. During the process, I met Eng. Domenico (Inventvm project BMS project manager), his idea of an elaboration made me more curious about the project and I stretched my legs immediately to the Inventvm on Feb 2020.

As I was stepping into Inventvm I started to experience the radiation of the knowledge from the engineers because they are not kids like me. As a young rookie in technology, I start to learn more about the hardware and software of the project because the bus(project) is already started way before I join to the company. That was ok! because at the age of 10 I smoked the LED placing it in 230V mains, what ??????? YES that's right, for sure the led did not glow bright, but my brain became to dig into why LED got burned despite the black smoke on the face while LED burned. Anyway, later I was educated by my father(of course he is an electrician) that LED needs some kind of electronic circuit to make it glow. when my father made LED glow, That was WoW, ”astonishing”! LED was not too much bright enough though. This idea of making education by failure became fascinating this same strategy worked for me to understand this in the industry too quickly not to miss the bus. There are always my colleagues who gave me a shoulder to shoulder when I was stuck in some technological part.

Before my Master’s, I worked with Analog Device Inc as IoT application Engineer and System Testing Engineer for Highpower circuits In NEXTGEN computers helped in my current project to understand the Wireless communication environment and power management. My experience in these two prime companies laid the foundation for analytical skills and problem-picking skills throughout the project. Nevertheless, the key motivation was my father and all my teachers who educated me throughout my life to contribute well to nature and humanity. Nonetheless, Prof malcovati has been a gem among all my honorable teacher’s treasury who shined bright in my way. Thanks......!

Chapter 2

Introduction

Chapter 3

Bluetooth Module Design

3.1 Introduction

An Antenna design and analysis are crucial in a wireless network that transmits and receives information through electromagnetic wave radiation in open space. Modern Antenna and RF design techniques more often testified against size, power, flexibility, radiation patterns, efficiency, etc... It is very unusual to use a wide variety of RF fundamental design techniques even though the usage of silicon and power is different because the fundamentals of RF design are most rigorous and robust from decades, hence RF fundamentals and design techniques remain intact. Nevertheless, modern RF applications demand to emphasize efficiency and power requirements, so this requirement needs some special RF Design treatments. Chapter .3 gives the extravagance of PCB antenna design practices, general guidelines for grounding, PCB stacking, spacings and via holes, etc. Matching networks in RF design are extremely important to increase the efficiency of the Antenna and RF line, so it is also explored in the same chapter how to pick the passive components for RF Antenna matching such as capacitors and inductors.

3.2 Antenna Basics :

An Antenna is a piece of metal exposed to free space. A piece of conductor behaves like an antenna when its length is a certain ratio or multiple of the wavelength of the signal.

This scenario is expressed as ”resonance”, where the antenna radiates the electrical energy to the open space.

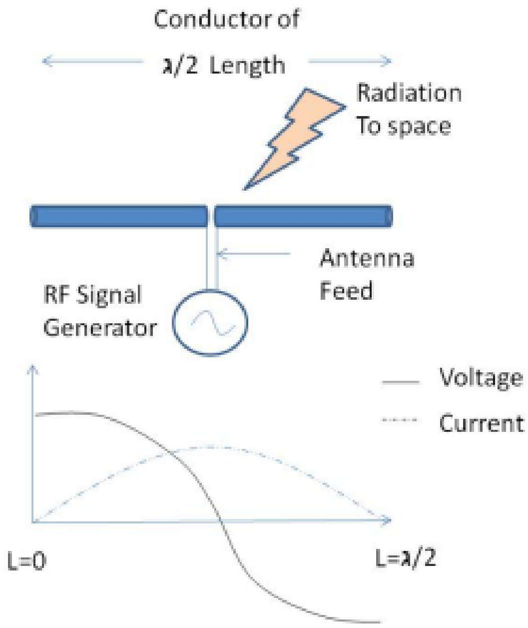


Figure 3.1: Basic Diploe Antenna

Fig.1 shows the diploe antenna whose length is $\lambda/2$ and the fed has an input impedance of 50Ω. Dipole antennas are the most basic antennas that have been used for broadcasting. In the Millennial age of technology, dipole antennas have been bulky and heavy, thanks to the PCB technology, which made diploe antennas extremely simple in construction and this became the center of attraction for the Bluetooth application in the modern era. Although diploe antennas are extremely comfortable for PCB we still face hurdles to manage proper grounding for the antenna..which can be addressed through quarter-wave antennas. The quarter-wave antennas have half of the length of the dipole antennas $\lambda/4$ their popularity became exponential because of the fed which can be single-ended. A single-ended feed to the antenna made life much easier to make a wide range of ground planes and better matching.

3.2.1 Antenna Types:

As discussed in the previous section quarter wavelength antennas can be more effective on the PCB because of their fed and ground plane management on PCB. Depending on the antenna dimensions and the shape antennas fall into different technologies namely FM, AM, Bluetooth, and wifi son on. Since the eccentric part of this chapter discusses the Bluetooth antenna design and guidelines, we can broadly classify three types of antennas. as Follows :

3.2.1.a Wire Antenna :

These types of antennas are just a piece of wire extended over the PCB in open space, whose length is matched to $\frac{\lambda}{4}$ on the ground plane. In general, these antennas are fed by a 50Ω matching transmission line, a Wire antenna gives a top-notch performance and supports a wide range of frequencies because of its three-dimensional exposure in open space. The shape of the wire antennas can be loop, wire, or helix.. depending on the application the shape is changed.

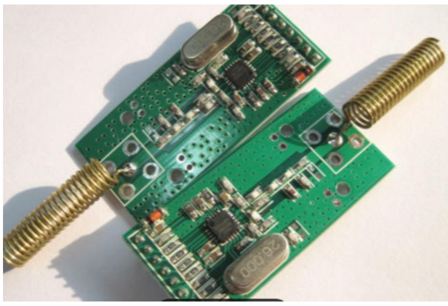


Figure 3.2: Wire Antenna

3.2.1.b PCB Antenna :

Constructively this type of antenna is copper traces that are etched on the PCB. The Traces can be Zig-Zag, straight, MIFA, Meandered type, F-type, or Zip track so on., the shape of the antenna is chosen based on the antenna type and the space constraints on the PCB. PCB Antennas have only two-dimensional freedom, therefore certain guidelines are needed for the PCB antenna design due to the space constraints and poor quality of PCB stack-up. The space constraints of the PCB antennas lead to less efficiency compared with wire antennas nonetheless PCB antennas are cost-effective. In short manufacturing comfortability and its wireless range is ravishing for Bluetooth applications.

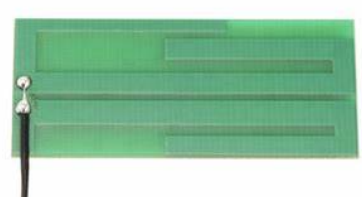


Figure 3.3: PCB Antenna

3.2.1.c Chip Antenna :

This is a Small form factor IC that is in-house with a ceramic package or some metal case. These antennas are handier in terms of space management on the board and internally their impendence is very well managed. A chip antenna can also take an advantage of three-dimensional freedom for radiation similar to wire antennas. Refer to figure 10 for the Nordic Bluetooth module having a chip antenna. It's true that chip antennas can gain upper hand in size and radion pattern on the contrary power handling capacity of the chip antenna is very minimal.

Figure 3.4: Chip Antenna

3.2.2 Antenna Parameters

The following section gives some key antenna performance parameters.

3.2.2.a Return loss :

The return loss of an antenna signifies how well the antenna is matched to the 50-Ω transmission line (TL), shown as a signal feed in Figure 3.5. The TL characteristic impedance is typically 50 Ω, although it could be a different value. The industry standard for commercial antennas and testing equipment is 50-Ω impedance, so it is most convenient to use this value [5].

Return loss indicates how much of the incident power is reflected by the antenna due to mismatch (Equation 3.1). An ideal antenna when perfectly matched will radiate the entire energy without any reflection. If the return loss is infinite, the antenna is said to be perfectly matched to the TL, as shown in Figure 3.5. S11 is the negative return loss expressed in decibels. In most cases, a return loss ≥ 10 dB (equivalently, S11 ≤ –10 dB) is considered sufficient. Table 3.1 relates the return loss (dB) to the power reflected from the antenna (percent). A return loss of 10 dB signifies that 90% of the incident power goes into the antenna for radiation [5].

$$Returnloss(db) = 10 \times \log(\frac{Pincident}{Preflected}) \tag{3.1}$$

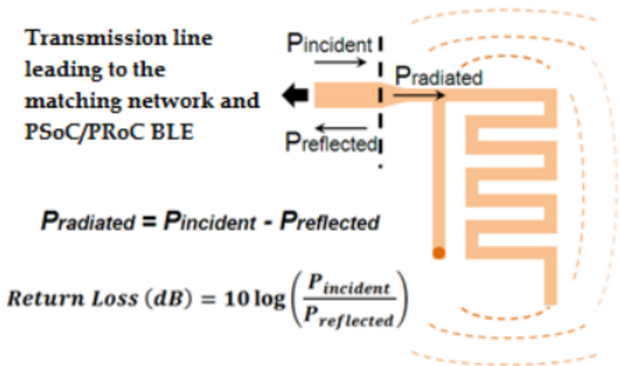


Figure 3.5: Antenna Return loss

S11 (dB)	Return Loss (dB)	Preflected/Pincident (%)	Pradiated/Pincident (%)
–20	20	1	99
–3	3	50	50
–10	10	10	90
–1	1	79	21

Table 3.1: Return Loss and Power reflected from antenna

3.2.2.b Bandwidth :

Bandwidth indicates the frequency response of an antenna. It signifies how well the antenna is matched to the 50-Ω transmission line over the entire band of interest, that is, between 2.40 GHz and 2.48 GHz for BLE applications [5].

As Figure 3.6 shows, the return loss is greater than 10 dB from 2.33 GHz to 2.55 GHz. Therefore, the bandwidth of interest is around 200 MHz. Wider bandwidth is preferred in most cases, because it minimizes the effect of detuning resulting from the changes in the environments around the antenna in actual uses of the product (e.g. mouse placed on wood/metal/plastic table, hand kept around the mouse, etc.) [5]

3.2.2.c Radiation efficiency:

A portion of the non-reflected power (see Figure 3.1) gets dissipated as heat or as thermal loss in the antenna. Thermal loss is due to the dielectric loss in the FR4 substrate and the conductor loss in the copper trace. This information is characterized as radiation

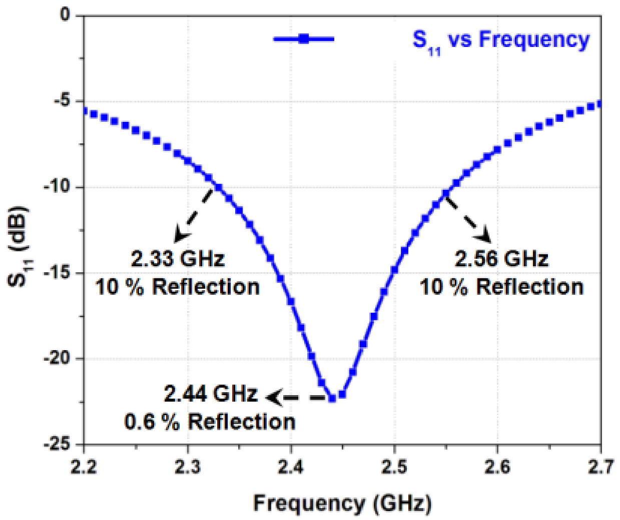


Figure 3.6: Antenna Bandwidth

efficiency. The radiation efficiency of 100 percent indicates that all non-reflected power is radiated to free space. For a small-form-factor PCB, the heat loss is minimal [5].

3.2.2.d Radiation pattern:

Radiation pattern indicates the directional property of radiation, that is, which directions have more radiation and which have less. This information helps to orient the antenna properly in an application [5].

An isotropic dipole antenna radiates equally in all directions in the plane perpendicular to the antenna axis. However, most antennas deviate from this ideal behavior. See the radiation pattern of a PCB antenna shown in Figure 3.7 as an illustration. Each data point represents RF field strength, measured by the received signal strength indicator (RSSI) in the receiver. As expected, the contours are not exactly circular, as the antenna is not isotropic [5].

3.2.2.e Gain :

Gain indicates the radiation in the direction of interest compared to the isotropic antenna, which radiates uniformly in all directions. This is expressed in terms of dBi—how strong the radiation field is compared to an ideal isotropic antenna [5].

3.3 Motivation for Designing BLE Modules

One of the core ideas of the Inventvm BMS team is to make the BMS project in a wireless communication environment, therefore the team has decided to use Bluetooth as the communication tool. Hence finding the big sharks (Bluetooth Hardware and stack)

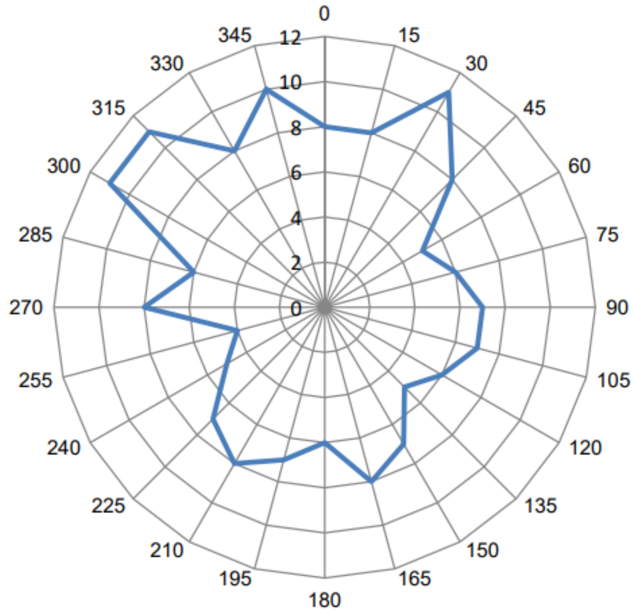


Figure 3.7: Antenna Radiation Pattren

in the Bluetooth world took quite some time, after a long investigation; we concluded to pick two important pies in the Bluetooth cake such as STM BLUeNRG-355mc [6] and Nordic nRF52840 [7]. BlueEnergy-355mc is the jewel of our projects because it owes the advantages of very low power consumption: 3.4 mA, Receiver sensitivity, Bluetooth low energy data extensions, high data rate so on... despite having these many advantages STM does not manufacture the Bluetooth modules other than eval boards. Henceforth team has been paralyzed to outsource the required Bluetooth modules, later in the same path we found MDARTRONICS the company that manufactures the Bluetooth modules using the STM BLUeNRGgy-355mc hardware named STORMY. Stormy is a such cutie pie, at least it helps at some extent in R and D to prove the Wireless communication BMS architecture, but in the long run, we have experienced some the discomforts such as lack of documentation and market supply...to overcome all these issues team has decided to make inventive proprietary level Bluetooth modules fr BMS project. This gave me the perfect timing and to opportunity design RF Bluetooth modules for the project, as part of my thesis which is dedicated to wireless communication BMS.

Nordic nRF52840[7] is another Bluetooth hardware similar to the BlueEnergy-355Mc reason behind picking the Nordic is the open BLE stack and Robust hardware. Nordic is much more comfortable in terms of different data rates, on-chip power converters, 32-bit ARM Cortex M4F @64MHz so and forth. Nordic has also a dedicated BLE stack [8] that handles all power management resources on-chip, which attracts low-power automobile applications. In a much broader sense, Nordic is additional Bluetooth hardware that we can provide to the customer according to the application's need.

Though picking the Bluetooth hardware and stack is a boiling task, choosing the antenna and RF layout also takes prime place. Though, There are plenty of antennas for the 2.4GHz band, most Bluetooth manufacturers recommend two types of PCB antennas, meanders inverted antennas (MIFA) and inverted-F antenna (IFA), which are characterized and simulated exclusively for the low-power Bluetooth applications.However, MIFA (PIFA) is peculiar for most automobile applications because of its pointed directional properties.

, However, we can choose any type of antenna and hardware for Bluetooth, admittedly the antenna, hardware, and RF layout design described in the following modules are classified for the BMS project.

The Low Data rate and bandwidth requirement in Bluetooth applications make IFA and MIFA make these two antennas most attractive for BLE. Manufacturing these antennas is extremely easy because they are part of the PCB design. Certainly, these antennas are inexpensive as they are part of PCB and they provide good bandwidth in ranges for BLE in terms of 150 to 250 MHZ.MIFA is most preferable for smaller form factor PCBs such as a wireless mouse, wearable watches, handy IoT devices.... etc. IFA antennas are recommended for applications such as one of the dimensions is needed to be smaller than the other for example heart rate monitor. following modules explain MIFA and IFA antennas construction and functionalities:

3.4 PCB Meandered Inverted-F Antenna (PIFA/MIFA)

PIFA antennas are much more popular in Bluetooth Low Energy stack because of the small size, low profile and cost-effective compared to the conventional dipole and ceramic chip antennas. The proposed structure (PIFA/MIFA) Figure 3.9 of the PIFA antenna is routed to gain all these advantages. Replacing the conventional PCB trace in PIFA with the meandering line and meandering shorting strip improves the efficiency of the PIFA as well as the bandwidth.

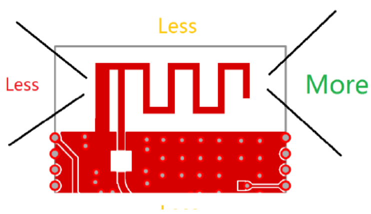


Figure 3.8: MIFA/PIFA antenna radiation direction

Figure 3.9 Taking the meandered shape on one side and connecting meandered terminal to the ground makes the radiation lobe a more directional Figure3.8 that implicates the radiation of the meandered antenna.Meandered side of the antenna radiates very less power because the Menderes terminal is connected to the ground which nullifies most of the radiation on the backward side. This kind of feature is highly needed in extremely noisy environments such as automobiles, power grid applications, data servers....etc. As a case study, the design and measurement results of the proposed MIFA/PIFA are presented [9] in Figure3.9.

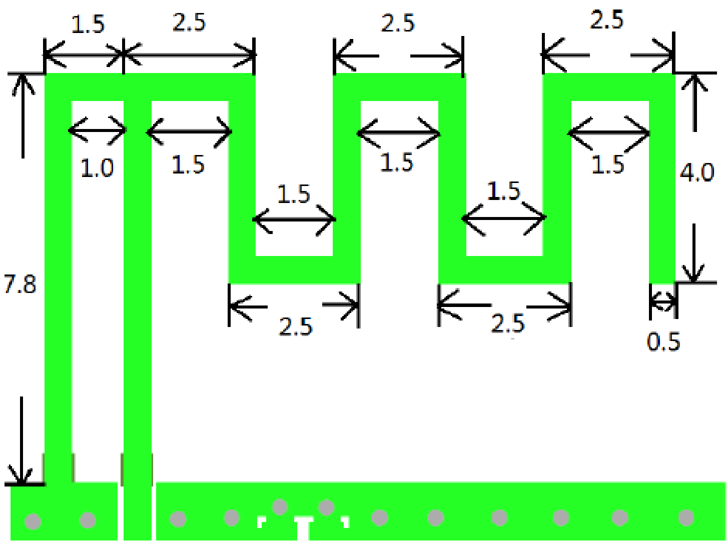


Figure 3.9: PCB Inverted Meandered F type Antenna [1]

3.4.1 Antenna used in Inventvm BLE modules :

I got an opportunity complete the Inventvm BLE module antenna simulation Figure3.9 to depict the typical board shape and the antenna placement [10]. The RF shield housing has been removed for testing purposes, usually, Bluetooth modules provide RF housing to protect the BLE from external interference.

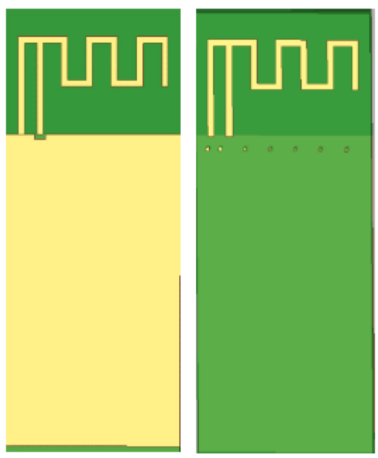


Figure 3.10: BLE module PCB with the MIFA/PIFA antenna placement

Some MIFA/PIFA antenna and PCB parameters that are used for the simulation are shown in the table 3.2.

Antenna parameters	Value	Unit
PCB substrate permittivity	4.6	—
PCB substrate H	1.0	mm
Length of PCB substrate	35.5	mm
Width of PCB substrate	14	mm
Length of TOP PCB ground	25.5	mm
Width of TOP PCB ground	14	mm
Length of BOT PCB grounD	25.5	mm
Width of BOT PCB ground	14	mm
Width of antenna trace	0.5	mm

Table 3.2: MIFA/PIFA antenna simulation parameters [1]

3.4.2 S11 of the MIFA/PIFA antenna

Figure3.11 shows the MIFA/PIFA antenna s11 parameter simulation results. The Bluetooth frequency bandwidth ranges from 2402 to 2483.5 MHz. The return loss of the antenna in the Bluetooth frequency band is less than the -10db.

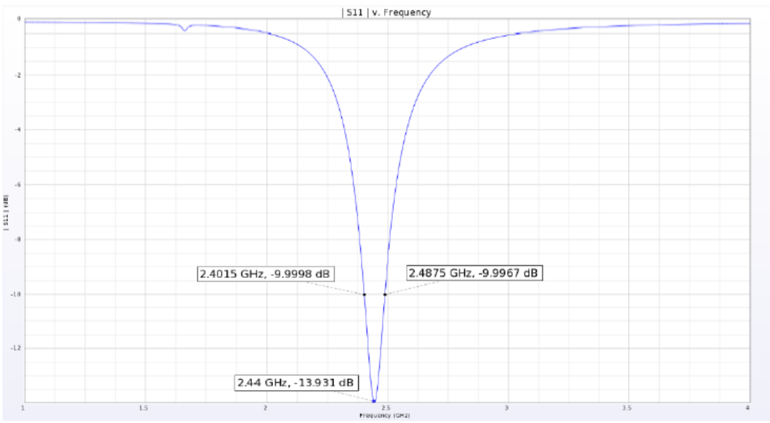
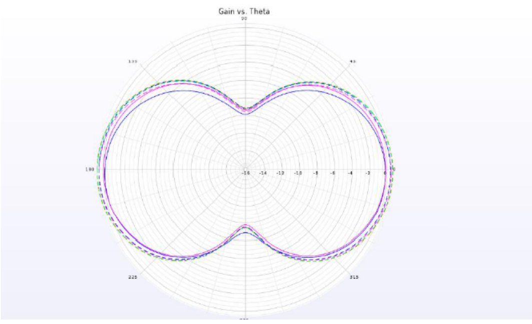


Figure 3.11: MIFA/PIFA antenna S11 return loss

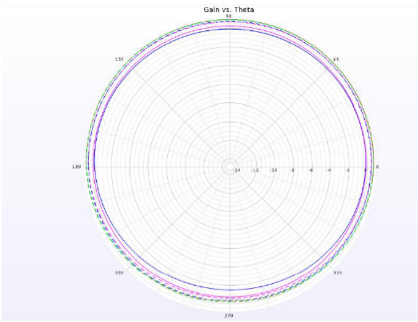
3.4.3 MIFA/PIFA antennas 3D pattern :

3.5 Inverterd-F Antenna:

The inverted F antenna is also one of the popular antennae, recommended for the Low power stack BLE applications. IFA antennas host similar features to what MIFA/PIFA antennas offer but MIFA antennas are more recommended where is a space constraint and power radiation is in one direction. IFA antennas have bidirectional power radiation rather than mono-directional. Nordic Recommends in all designs to use the IFA antennas. Figure 3.15 educates the typical design of the IFA antenna and simulation parameters are pretty much the same as it is used for the MIFA antenna Table 3.2.



(a) MIFA antenna Gain Radiation pattern @ϕ = 90 deg



(b) MIFA antenna Gain Radiation pattern @$\phi = 0$ deg

Figure 3.12: MIFA Antenna Gain Radiation Pattren

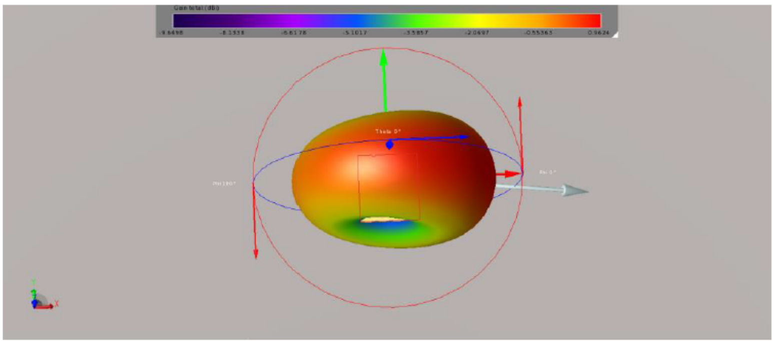


Figure 3.13: MIFA/PIFA antenna 3D radiation Pattren

By the constructional nature of the IFA antennas are easy to match we can see that in the Figure 3.16 IFA antenna is very well-matched at 2.4GHz. The S11 is quite impressive because it has a reflection coefficient at 2.4GHz is -27db and bandwidth at -9db is 160MHz. IFA antenna matching can be further tuned by varying the hinges, and length of the antennas, on contrary we need to compromise with power and resonant frequencies. Figure 3.17shows the relative length and hinge width changes of the design Figure 3.15 caused different frequency shfit, but they keep giving the best performance in matching.

3.6 BLE Schematic and PCB layout

The Schematic of the Inventvm BLE modules is inherited directly from the vendors, which are BluEnergy-355MC[6] and Nordic nRF52840[7]. The Figure3.18 shows the pinout and shape of the BLE module, which is multi-purpose because of same shape and pinout from both the BluEnergy-355MC and Nordic nRF52840 modules. By having the Same pinout and shape with different Bluetooth hardware, customers can use different Bluetooth hardware stacks with the same BMS solution. This approach is nothing but the daughter and motherboard approach where the Bluetooth module becomes the daughter

Frequency (GHz)	Available power (W)	Input power (W)	Radiated power (W)	System efficiency	Radiation efficiency
1	0.0025	6.09E-05	4.24E-06	0.17 %	6.96 %
1.6	0.0025	1.00E-04	3.23E-05	1.29 %	32.19 %
1.66	0.0025	2.22E-04	6.56E-05	2.63 %	29.51 %
1.72	0.0025	1.22E-04	4.94E-05	1.98 %	40.35 %
2.08	0.0025	3.67E-04	2.46E-04	9.84 %	67.07 %
2.26	0.0025	1.02E-03	7.63E-04	30.50 %	74.76 %
2.44	0.0025	2.40E-03	1.86E-03	74.44 %	77.58 %
2.54	0.0025	1.85E-03	1.43E-03	57.32 %	77.41 %
2.64	0.0025	1.12E-03	8.54E-04	34.17 %	76.35 %
2.83	0.0025	4.83E-04	3.50E-04	14.00 %	72.46 %
3.22	0.0025	1.91E-04	1.18E-04	4.70 %	61.58 %
4	0.0025	8.62E-05	3.18E-05	1.27 %	36.87 %

Figure 3.14: MIFA/PIFA antenna efficiency Simulation Results

board and BMS MMU board and CMU boards become motherboards.

3.6.1 BluEnergy-355MC

BLUENRG-355MC[6] BLE module includes BlueNRG-LP BLE low energy system on chip (QFN48 package), Associated with BlueNRG-LP development software stack from STM. The BlueNRG-LP features a 64 MHz, 32-bit Arm®Cortex®-M0+core, a 256 KB programmable flash memory, a 64 KB SRAM, an MPU, and an extensive peripheral set (6x PWM, 2x I²C, 2x SPI/I2S, SPI, USART, UART, PDM, and 12-bit ADC SAR)[6]. It is compliant with the Bluetooth® LE specification and supports master, slave, and simultaneous master-and-slave roles. It features data length extension, 2 Mbps, long-range, extended advertising and scanning, as well as periodic advertising, periodic advertising sync transfer, LE L2CAP connection-oriented channel, and LE power control and path loss monitoring[6]. For more technical details refer STM BLUENRG-355MC datahseet [6].

3.6.1.a BluEnergy-355MC RF Schematic:

The Figure3.19 refers to the core circuit of the BLUeNRG circuit for the Bluetooth, the pi network matching topology used to match the Ic and antennas, and refer 3.19 circuit between the RF net and the ANT net in the schematic. All the discrete components are selected 0402 packages to make the Bluetooth module as sophisticated as possible, for more insight into the component selection for the schematic 3.19 refer to BOM[11].

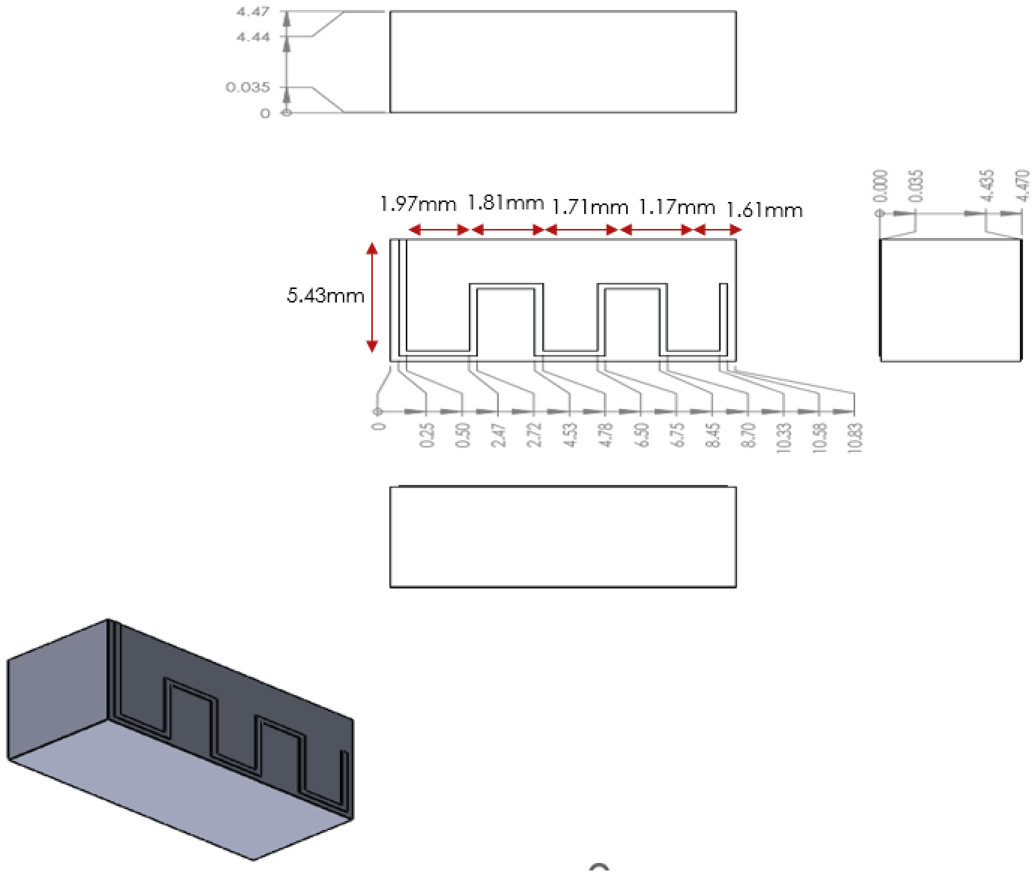


Figure 3.15: IFA antenna design and the placement

3.6.1.b BluEnergy-355MC RF Layout:

The BLE module designed for the BMS application in Inventvm is the four-layer PCB, among four layers bottom layer is entirely dedicated to the ground. The bottom layer ground of the module is the analog ground it is differentiated from the power ground of the BMS from a small indictor to make sure the RF circuit gets less noise from the power ground.

By referring to the layout Figure 3.20of the RF module you can recognize that the shape of the power plane in the layer is pretty much weird, there is an RF technique behind making this kind of shape to avoid as much as the ground and power plane over a lap to decrease the capacitive parasitic effect. parasitic components on PCB are the plague of the RF circuit, they can kill RF signal. Hence it is always a good idea to avoid power and ground planes overlap as much as possible and also make separate ground for the RF layout apart from the power ground.

place as many as vias possible from the top to bottom ground layer to enhance the ground layer capacity, and making sure to have equal space for antenna and RF feed line from the ground enhances the matching capability of the antenna. The following extinctions can give a detailed view of RF layout design:.

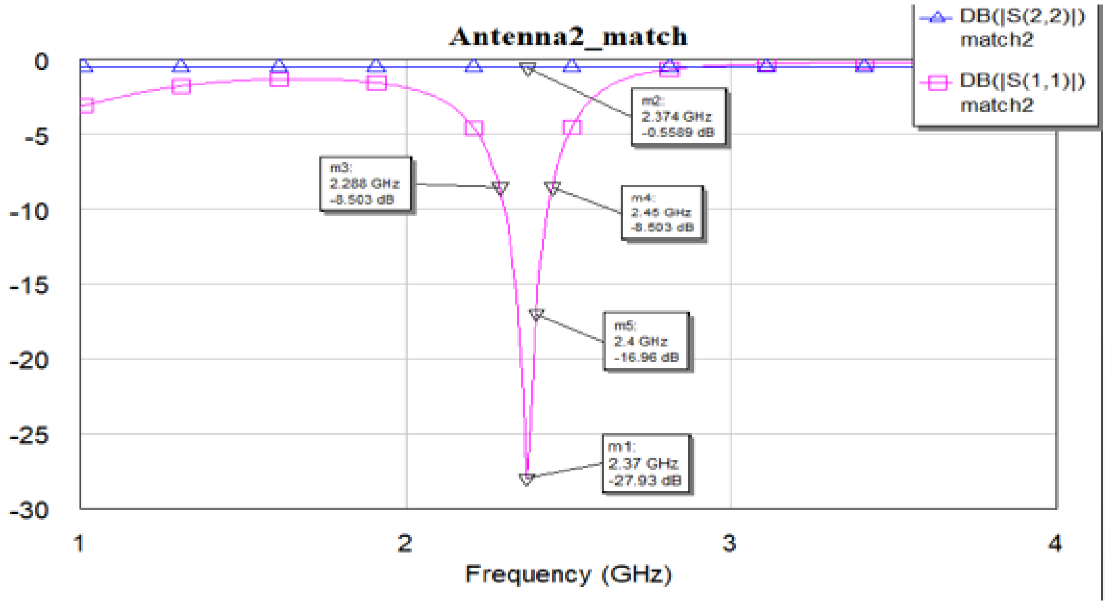


Figure 3.16: IFA antenna S11 and S22

- **Power plane and Grounding :**The power and Ground plane's overlap needs to be decreased as much as possible to avoid the parasitic capacitance effect. The Figure 3.20 refers to the power supply plane in the layer and the ground in the bottom layer.

- **Equal Clearance to Antenna Feed :** It is essential to keep the same clearance throughout the RF feed line from the ground. This strategy helps to make equal parasitic capacitance from the ground. With an equal parasitic capacitance from the opposite side, the RF sanding wave reflections can be nullified. Figure3.21 depicts one such example of designing the RF feed line.

  –

- **Isolate Power Ground from Analog/RF ground :**It is the most common practice while RF layout designing, The RF layout is isolated from the Power circuit. For this approach I have few intuitions behind the two-fold, those are :

  1. RF-related noise is confined within the RF/Analog ground of the PCB.
  2. This will isolate noise from the digital circuitry with the DC power supply and High power switching circuit on the BMS board.
  3. RF circuit protected from direct current flow from DC supply if there are any power surges in supply. So on....

3.6.1.b Such mentioned benefits can be obtained by placing an inductor between the Power Ground/RF ground. Choosing Inductor for such functionality follows

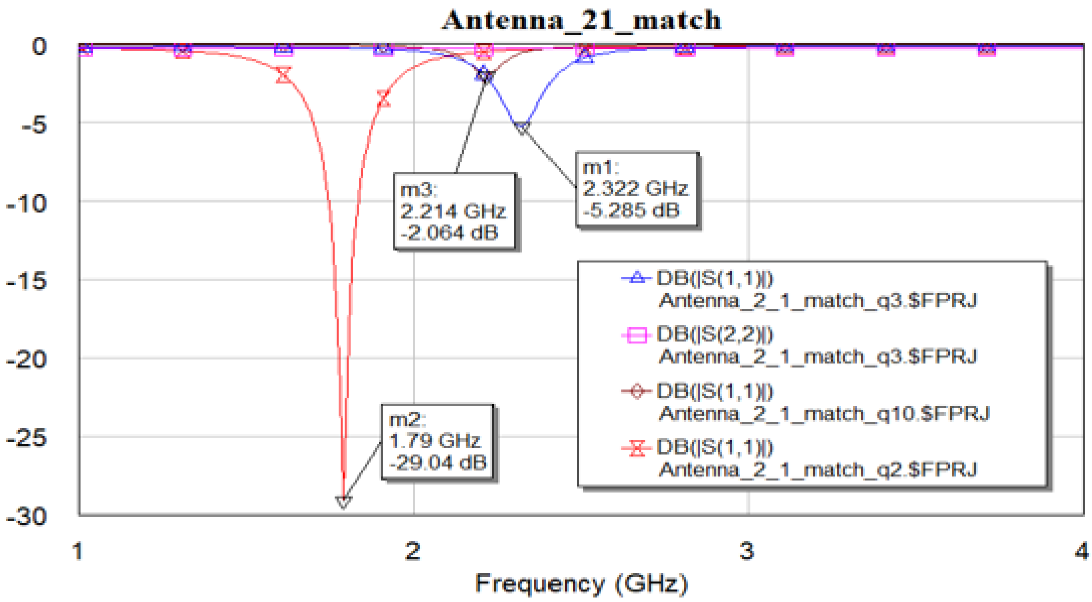


Figure 3.17: IFA antenna S11 Variation by changing the length and hinge width

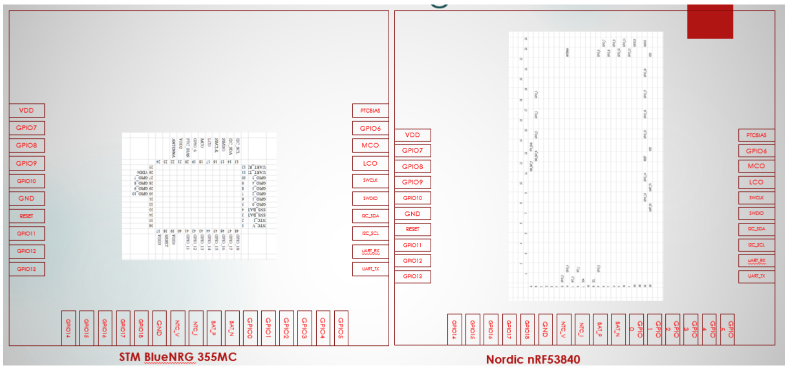


Figure 3.18: BluEnergy-355MC(right) and Nordic Modules(left)

that the inductor will not allow sudden current spikes $L \times \frac{di}{dt}$, on the benefit it can also provide a high current ratio when the current is stable,reference 3.22..

- **RF feed line shape :**It is common practice to keep the rf feed line with the known shape. Since Bluetooth operates at 2.4GHz, even one millimeter can give a large amount of resonant frequency drift in antenna reflections. The simplest approach to mitigate such issues is to keep the RF feed and the RF IC, both on the same axis. To avoid unnecessary parasitics by an irregular shape of the antenna, make a feed trace from the ic to Antenna with the same width as the antenna feed has. Figure 3.23 shows the approach that I have followed to design the Antenna feed and the RF trace, The Figure shows the nonregular shape of the antenna.

  –

- **Grounding Via's :** Keep always clean ground and this can be achieved by placing as many vias from the top layer to the dedicated RF/Analog ground in the bottom

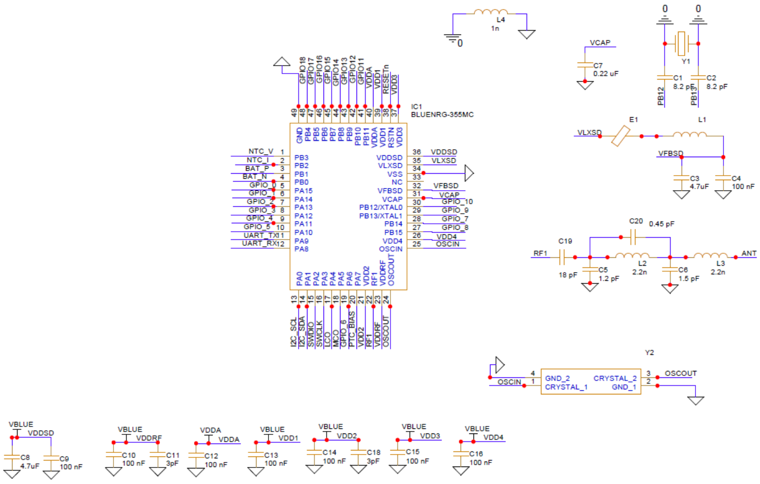
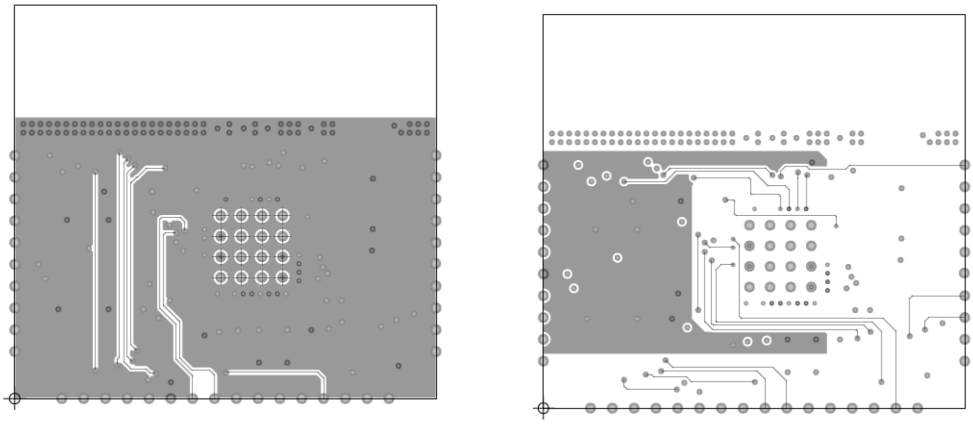


Figure 3.19: BluEnergy-355MC Module Core circuit



(a) Ground plane ”Bottom layer”

(b) Power Plane ”Layer 1”

Figure 3.20: BLE PCB ground and power planes

layer. It is recommended in the PCB design to place the Vias with equal distance, Figure 3.23 refers to Vias placement from the top layer to the bottom layer with equal distance. There should not be any ground under the RF antenna, because the ground under the RF antenna again makes, Antenna just an RF trace instead of allowing open radiation.

–

- **Antenna placement :** Do not place any component in the Antenna Keep out area, make the strict keep-out area for the antenna to prevent any external components' noise interference. It is always good placement to avoid any of the plastic components around the antenna because the plastic can behave like a dielectric and this will change the antenna characteristics. Antenna placement on they should end of the PCB where the PCB notch is pointed out. See Figure3.20 the antenna has been placed on the edge of the PCB and there are no plastic or high-frequency switching circuits around it.

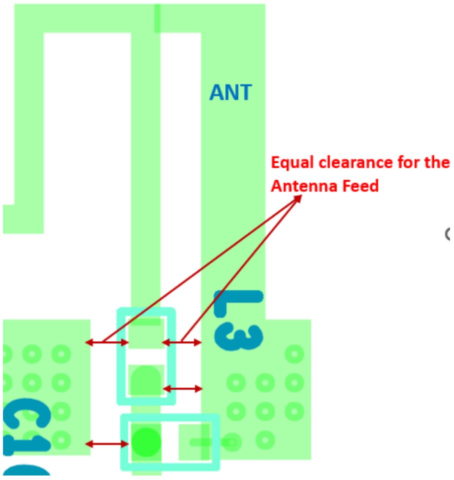


Figure 3.21: Antenna Feed Line clearence

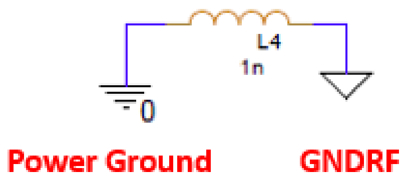
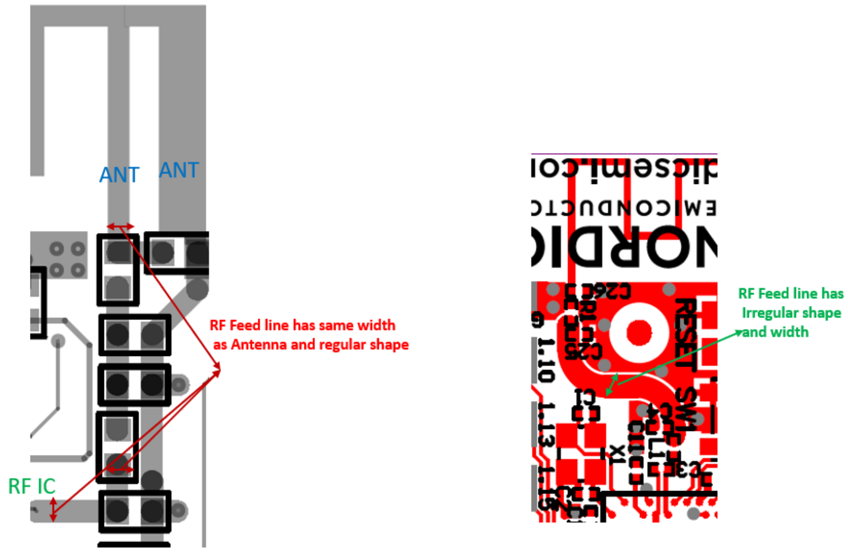


Figure 3.22: Power Ground and RF Ground Isolated with Inductor

3.6.1.c Power Supply Decoupling Layout Considerations[5]

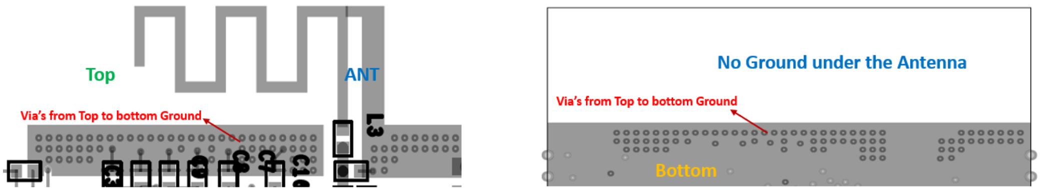
Note the following best practices when laying out the power supply traces:

- Place the components as close to the supply pin as possible [5].
- Place the smallest-value capacitor closest to the power supply pin [5].
- Place the decoupling capacitor on the same layer as the IC. If it is not possible to place all the capacitors on the same layer, give priority to smaller values [5].
- The power supply should flow through the decoupling capacitors to the power supply pin of the IC. Avoid using
- supply vias between the component and the pin [5].
- Use separate vias to ground for each decoupling capacitor. Do not share vias[5].
- For four-layer boards with a separate power plane, use separate vias for each power supply pin to the power plane [5].
- It is recommended not to share the vias [5].
- Some of the commonly made layout issues related to power supply decoupling are shown in [5] Figure 3.25.



(a) Regular shape and Antenna feed (b) Irregular Antenna shape and Antenna feed

Figure 3.23: Antenna Feed Shape



(a) Top Layer Vias (b) Bottom Layer Vias

Figure 3.24: Vias placement on BLE board

3.6.1.d BluEnergy-355MC RF Matching Circuit Layout:

It is always a good approach to have the matching circuit as tight as possible you can refer to the Figure3.26 the matching circuit is placed as close as possible, to avoid any additional track length to create some extra RF stub effects. Don't ever run any of the signal lines across the RF feed line and always make sure to place the IC and RF in the same direction this approach will avoid any strange track shapes which can cause parasitics. It is a good way to make sure the RF feed line to the antenna through the IC has the same width across the track length this will avoid any unnecessary filtering effect. The figure refers to all of above-mentioned RF layout design hints. Figure3.26 shows that matching components are tightly packed, and no signals run across the RF feed.

We can place the components even overruling the component outline. Until we do not make the pads overlap, to achieve this we might have to bypass some PCB DRCs.

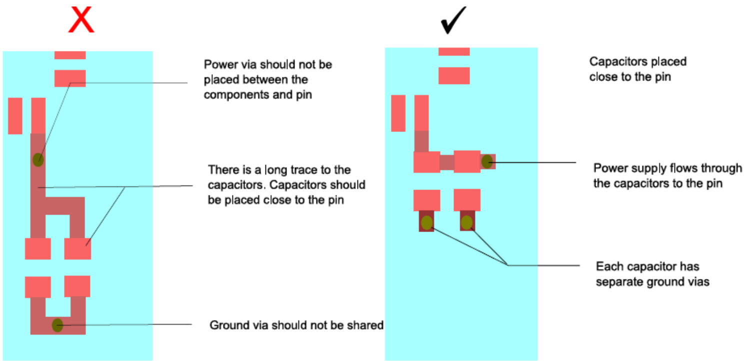
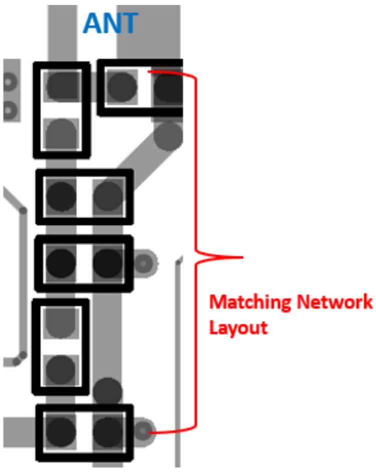
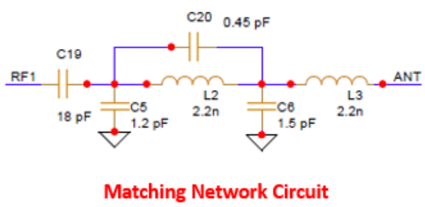


Figure 3.25: Power Supply Decoupling



(a) Matching Network Layout



(b) Matching Network Schematic

Figure 3.26: BLE Antenna Matching Network

3.6.2 Summery of the RF layout Design guidelines :

1. Keep Ground clearance as much as possible around the antenna.
2. Make equi clearance on both sides of the antenna and RF feed line.
3. Do not make a strange shape of the antenna feed line.
4. Do not run any of the signal lines under the antenna or RF feed line.
5. Make more vias from the top layer to the bottom layer for pure ground.
6. Keep capacitive filters as near as possible to the power supply pins.
7. Pack antenna matching network as close to antenna and IC RF feed.
8. Place antennae in less clumsy are from other circuitry on the PCB.
9. Make less overlap of the ground plane and power plane.
10. Avoid high-frequency circuits around the RF feed.

11. Always places the antenna at the edge of the PCB.

12. Always chooses a standard pattern for the ground around the antenna.

13. Never places any components, screws, mounting holes, or planes in the keep-out area of the antenna.

14. The antenna must house with a Metalic shield to avoid external interference.

15. There should not be direct ground under the antenna.

16. The Orientation of the antenna should be inlined with the final PCB.

17. When using the passive matching circuit try to have multiple components matching this can help at the debugging stage to tune the matching circuit.

3.7 Conclusion of the Chapter 3

The simulation and design of both the MIFA and IFA antennas are successful the results have been presented in Chapter3. Both the MIFa and IFa antennas are well performed in the sense of the results and design, because of the industry standards and Bluetooth stack recommendations, from vendors I have opted MIFA for Inventvm Bluetooth modules. The Layout is also quite impressive considering all norms of RF PCB layout guidelines, which are mentioned in the chapter3. In the chapter3 I have not stressed the theoretical calculation for the MIFA/IFA antenna because the calculations are pretty much the same as the standard MIFA and IFA antennas, The goal is to bring up the sophisticated RF BLE layout according to the application with a standard approach. Yet reference papers [[12],[13]] give more insight into the theocratical design of the MIFA / IFA antenna and I have taken fewer opportunities to explain the nordic architecture, because of the RF layout out-wise and in the antenna sense, I have followed the same guidelines as I did for the BLUeNRG-355mc. The Complete layout of the BLUeNRG and Nordic is attached in the chapter5 , Figures (5.1,5.3).

Chapter 4

Architecture of Wireless Communication Active Balancing BMS

4.1 Introduction

There are plenty of topologies dedicated to the BMS active balancing, for instance, cell-to-cell charge balancing, cell-to-stack or stack-to-cell charge sharing, and stack charge sharing. Among such wide techniques cell to stack and stack-cell, charge-sharing techniques gain the upper hand because of their robustness and safety measures against the battery.

4.2 Active Balancing Topologies for BMS

4.2.1 *Type Ia* : Combination of Buck and Boost Converter

4.2.2 *Type Ia* : Combination of the Buck/Boost Converter :

The figure4.1 illustrates the Type Ia balancing method for a battery system with n series-connected cells. The description is stack-to-cells-to-stack in accordance with the accepted nomenclature. A buck converter serves as a charging unit that distributes charge from the stack to the chosen cells. A boost converter reverses the process of discharge.

The boost converter's input and output voltage ranges must be large enough to accommodate cells with voltages ranging from 1 to n-1. All cells can be actively charged and discharged up to the top level of the stack in this manner. It is only possible for nearby cells to balance numerous cells at once. Access to all cells below the topmost cell is used to balance that cell.
This section explains the balancing procedure shown in Figure 4.1. The buck converter feeds Cell 1 with energy from the stack through switch S_wA1. The converter output current I_{Buck} is used to charge Cell 1. With the converter input current boost, the boost converter simultaneously discharges Cell 1 and Cell 2 through S_wB2. The sum of the current in Cell 1 is 0A since $I_{Buck} = -I_{Boost} = I_{Bal}$, while Cell 2 discharges with I_{boost}A (negative balancing or "discharge mode"). The buck converter is often connected higher than the boost converter Batteries in Charging Mode. Discharging is done in the opposite order.

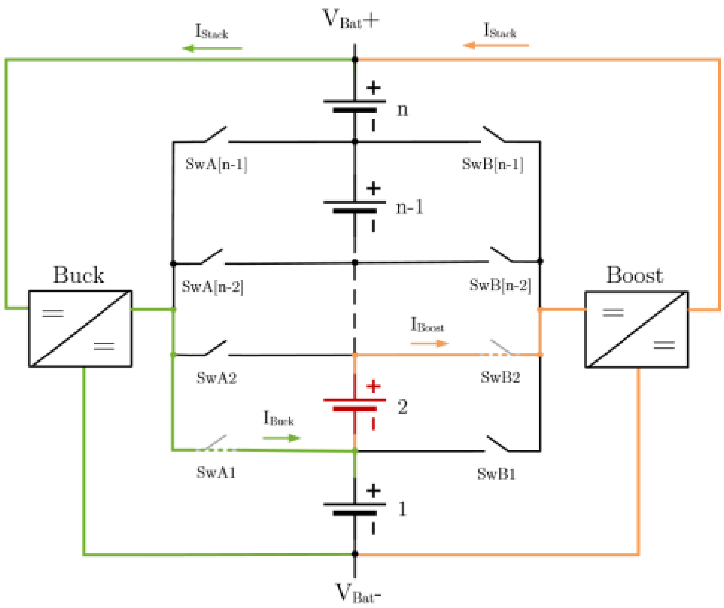


Figure 4.1: *Type Ia*: Active Battery Balancing

The idle cell currents can be expressed as a vector following 4.2. It accounts for the balancing currents, both positive and negative, as well as the resulting stack current.

$$\vec{I_{Cell}} = I_{stack} + \vec{I_n} \cdot I_{Bal} - \vec{OUT} \cdot I_{Bal} \tag{4.1}$$

$$I_{stack} = I_{Bal}(\frac{1}{\eta}\sum \vec{I_n} - \eta \sum \vec{Out}) \tag{4.2}$$

$$\vec{OUT} = \begin{pmatrix} S_{B1} \\ \vdots S_{B[n-1]} \end{pmatrix}, S_x = \{0 \cdots 1\}, \vec{I_n} = \begin{pmatrix} S_{A1} \\ \vdots S_{A[n-1]} \end{pmatrix} \tag{4.3}$$

where $\vec{I_n}$ and $\vec{OUT}$ are the vectors of the switch signals $S_{A[x]}$ and $S_{B[x]}$, respectively. The converter power and overall losses depend on the stack's n cells and the location of the balanced cell inside it. They rise as the position and the number of cells increases. *I* = *J* when a single cell is in balance, In the absence of that, *I* stands for the bottom cell of the balancing group and *j* for the top one. As a result, *I* and *j* is always true.

The necessary converters can be the traditional buck and boost converters depicted in Figures 4.2 and 4.3. A synchronous design can be adopted, in which the diode is replaced with an actively regulated MOSFET to eliminate losses and to improve the efficiency of the converters across the whole operating range.

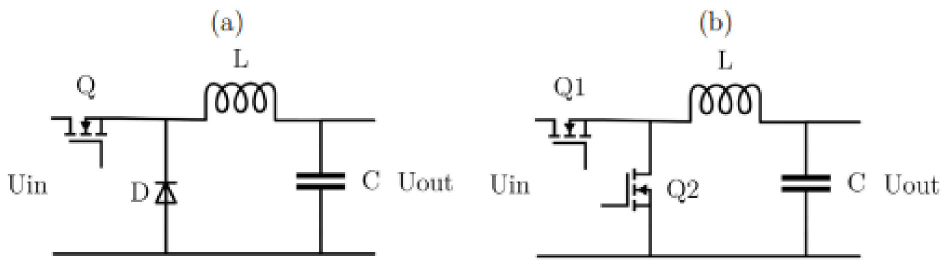


Figure 4.2: Conventional Buck (a) and synchronous Buck(b) Conveter

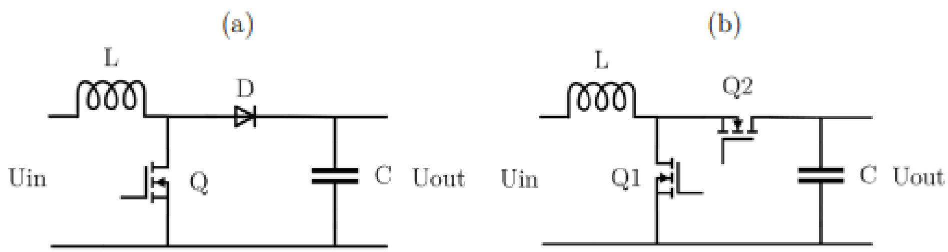


Figure 4.3: Conventional Boost (a) and synchronous Boost(b) Conveter

4.2.3 *Type Ib* : *Type Ia* with a bidirectional converter :

In terms of balancing routes, *Type Ib* is comparable to *Type Ia*. Bidirectional converters are used in place of unidirectional ones. Figure 5.9 depicts the schematic for potential hardware implementation.

4.2.4 *Type IIa* : Buck-boost converter :

The Type IIa of the discussed balancing techniques is shown in Figure 50. Once more, n cells are arranged in series to make up the battery system. The description is cells-to-cells following the accepted nomenclature. This approach is comparable to cell bypassing if the load current and balancing current are the same. In discharge mode, a buck converter moves charge from one cell or many neighboring cells to its subjacent cells in the stack. A boost converter transfers charge in the other direction when it is in charge mode. A single bidirectional buck-boost converter can be created by combining the two converters. A

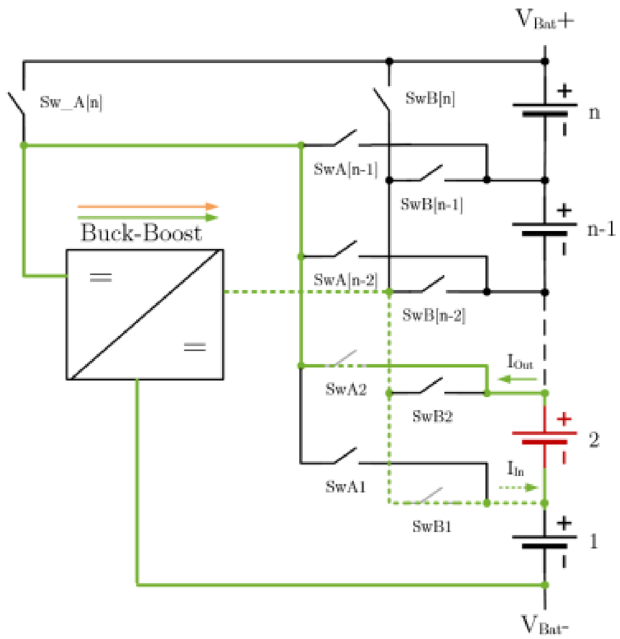


Figure 4.4: *Type IIa* : Buck-boost converter

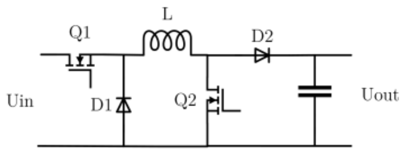
bidirectional buck-boost converter made up of both converters is possible. To support 1 to n cells, the buck-boost converter's input and output voltage ranges must be sufficiently broad. Only cells that are close to one another can balance numerous cells at once.

The explanation for the balancing procedure shown in Figure 4.4 is given in the paragraphs that follow. Switches $S_{wA[2]}$ and $S_{wB[1]}$ in the buck converter allow the energy from Cells 1 and 2 to be transferred to Cell 1. it releases cells 1 and 2. The converter output current I_{In} charges cell number one. In turn, Cell 1 is charged with $(I_{In} - I_{Out})$ A while Cell 2 is discharged with I_{Out} A (negative balancing). I_{Out} becomes I_{Bal}. In most cases, charging occurs when the DC/DC converter is connected in parallel to the desired cells and is in boost mode. However, in buck mode, discharge is performed in the same manner. Same charge and discharge operations as with *Type I* are possible through switches $S_{wA[n]}$ and $S_{wB[n]}$.
Depending on the number of balanced cells, the resulting cell current can be expressed

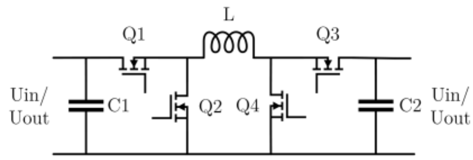
as a vector:

$$\vec{I_{Cell}} = \vec{I_n} \cdot I_{Bal} + \eta \cdot \frac{\sum \vec{I_n}}{\sum \vec{I_{Out}}} \cdot \vec{I_{Out}} \cdot I_{Bal} \tag{4.4}$$

$$\vec{OUT} = \begin{pmatrix} S_{B1} \\ \vdots S_{Bn} \end{pmatrix}, S_x = \{0 \cdots 1\}, \vec{I_n} = \begin{pmatrix} S_{A1} \\ \vdots S_{An} \end{pmatrix} \tag{4.5}$$



(a) Conventional Buck-Boost Converter



(b) Synchronous Buck-Boost Converter

Figure 4.5: Typical Buck-Boost Converters

Figure 4.5(a) depicts a potential buck-boost converter implementation. The N-MOSFET Q2 is disabled for buck mode, and Q1 is turned on and off. Q1 is constantly on in boost mode while Q2 is actively switched. The four-switch buck-boost converter from Figure 4.5(b) may be used instead to enable synchronous mode.

4.2.5 *Type IIb* : Bidirectional buck-boost converter :

In terms of balancing routes, *Type IIb* is comparable to *Type IIa*. A bidirectional buck-boost converter is employed instead of a traditional (unidirectional) one. Because not every cell level requires a connection to both input and output, the number of MOSFETs needed in the switch-matrix is decreased. The same equations and exact operations are true for *Type IIa* as well. Figure 4.6 displays the diagram and the power paths[4][p. 60]. A four-switch buck-boost converter similar to the one in Figure4.5(b) can be used to realize the necessary bidirectional buck-boost converter. The ability to run the converter in a synchronous mode in both directions is a benefit of this design.

4.2.6 *Type IIIa* : High - and low-side buck-boost converters :

The system's implementation using high- and low-side buck-boost converters are shown in Figure 4.7. Similar to *Type I*, the operation involves the transfer of charge sequentially rather than simultaneously. There are two phases to the balancing process: one for the boost operation and one for the buck operation. The description is stack-to-cells-to-stack following accepted nomenclature. The high-side converter and low-side converter shouldn't work in the same direction at the same time to maintain a low average stack current throughout the two phases. To demonstrate how the high-side converter works in this example, balancing routes for *Cell [n-1]* are also given in

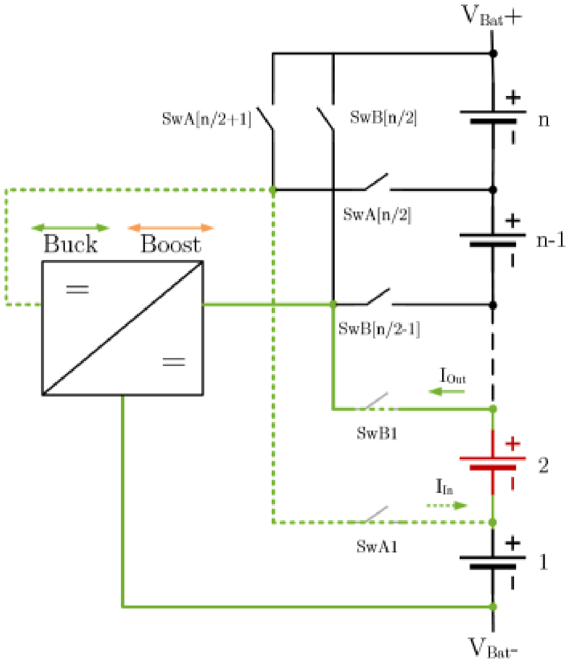


Figure 4.6: *Type IIb* active balancing architecture

addition to *Cell 2*[4][p. 62]. Four converters, which can carry out the two phases concurrently, are used in an expanded version of this architecture[4]. There are more conceivable combinations: Another high-performance variant can be created by fusing the Type II concept with the Type III high-side converter.

During Phase 1, the low-side converter functions as a boost converter, discharging *Cells 1* and 2 through S_{wA} with the converter's input current IBal, identical to Example 4.7. *Cell [n-1]* and *Cell [n]* are simultaneously charged with IBal by the high-side converter while operating in buck mode. Phase 2 involves charging Cell 1 in buck mode and discharging *Cell [n]* in boost mode to achieve the same balancing results as in Section (Results will be published in the upcoming chapters). I_{Bal} is used to charge and discharge *Cell [n-1]* and *Cell 2*.
A common ground connection allows the low-side converter to access all cells up to the middle of the battery stack, including *Cell [n/2]*. It can be executed as depicted in Figure 5.10. The design is made simpler by the fact that the two operating modes are only required in one direction. To enable synchronous operation for both modes, only two MOSFETs are required. If switch Q1 is not controlled, the MOSFET's intrinsic antiparallel diode enables normal operation albeit with lower efficiency.
The remaining cells are connected to the high-side converter through a shared V_{Bat+} link. It is similar to the common ground converter in terms of design, but it has a distinct structure (see Figure 4.7).

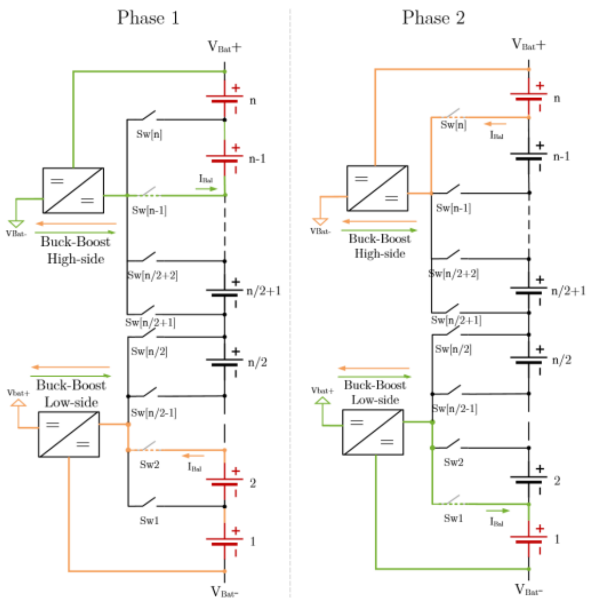


Figure 4.7: *Type IIIa* active balancing architecture

4.3 Proposed Active Balancing Method

4.4 Overview of Active balancing BMS Architecture

4.5 Retrospect of BMS Hardware

4.5.1 Multiphase Bidirectional DC/DC Current Controller LM5170-Q1

The LM5170-q1[14] controller is a high precision dual channel bidirectional converter applicated in automotive 48 Volts and 12Volts dual battery systems. Depending on the Direction Signal DC/DC converter regulates the average current. The Regulated current through the DC/DC converter can be programmed by analog or Digital PWM inputs.

The LM5170-q1[14] has a dedicated dual channel differential current sense amplifier to monitor the current flowing through the Dc/Dc converter, which can achieve 1% current sense accuracy. It has a Robust Gate driver to drive half the bridge. The Internal gate driver of the LM5170 has the capability of driving parallel MOSFET switches with a capacity of 500Watts. The synchronous diode emulation mode prevents the dc to dc converter from the negative currents and also enables the discontinuous mode of operation. This property enhances the DC/DC converter efficiency tremendously. The Controller can offer benefits of cycle-by-cycle current limitation, overVoltage protection at both low side and high side ports, Temperature protection and Mosfet failure so on...

An innovative average current mode control scheme maintains constant loop gain,

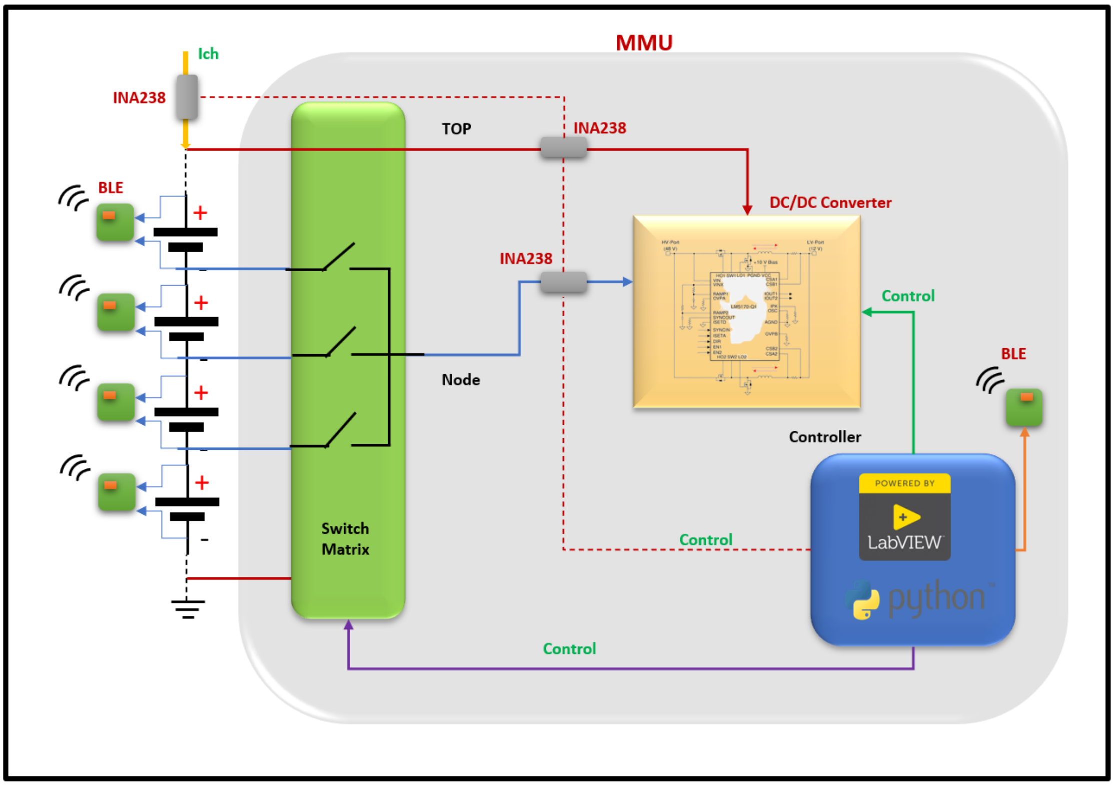


Figure 4.8: BMS Architecture

allowing a single R-C network to compensate both buck and boost conversion[14, p .2],[3]. The oscillator is adjustable up to 500 kHz and can synchronize to an external clock. Multiphase parallel operation is achieved by connecting two LM5170 controllers for 3- or 4-phase operation, or by synchronizing multiple controllers to phase-shifted clocks for a higher number of phases. A low state on the UVLO pin disables the LM5170 in a low current shutdown mode[14].

4.5.1.a Definition of IC LM5170 Operation Modes:

- **Shutdown Mode:** When the UVLO pin is < 1.25 V, VCC < 8 V, or default < 1.25 V, the LM5170 is in shutdown mode with all gate drivers in the low state, all internal logic reset, and the VINX pin disconnected from the VIN pin. When UVLO < 1.25 V, the IC draws < 20 µA through the VIN and VCC pins[14].

- **Initialization Mode:** When the UVLO pin is > 1.5 V but < 2.5 V, VCC > 8.5 V, and nFAULT > 2 V, the LM5170 establishes proper internal logic states and prepares for circuit operation[14].

- **Standby Mode:** When the UVLO pin is > 2.5 V, VCC > 8.5 V, and nFAULT > 2 V, the LM5170 first performs fault detection for 2 to 3 ms. During this time, the external power MOSFETs are each checked for drain-to-source short-circuit conditions. If a fault is detected, the LM5170 returns to shutdown mode and is latched in shutdown until reset through the UVLO or VCC pins. If no failure is detected, the LM5170 is ready to operate. The circuit breaker MOSFETs are turned on and the oscillator and ramp generators are activated, but the four gate drive outputs remain off until the EN1 or EN2 initiate the power delivery mode[14].

- **Power Delivery Mode:** When the UVLO pin > 2.5 V, VCC > 8.5 V, nFAULT > 2 V, EN1 or EN2 > 2 V, DIR is valid (> 2 V or < 1 V), and ISETA > 0 V, the SS capacitor is released and the LM5170 regulates the DC current at the level set at the ISETA pin[14].

4.5.1.b Bench setup and operation of the DC/DC Converter :

Although LM5170 can perform full bridge operation, we need only the half-bridge with a full current rating for our application. Figure4.9 only the high side bridge is used for buck and boost operations. The Figure shows the typical setup to operate the DC/DC converter in the bidirectional power system environment. The combination of the Load on the High side is the Battery pack Top and on the Low side, the is Battery pack node. A current Can flow from the High side to the low side or vice versa depending on the direction. The direction of the current flow depends on the BMS algorithm. A BMS algorithm decides which no needs to be balanced depending on batteries voltage difference.

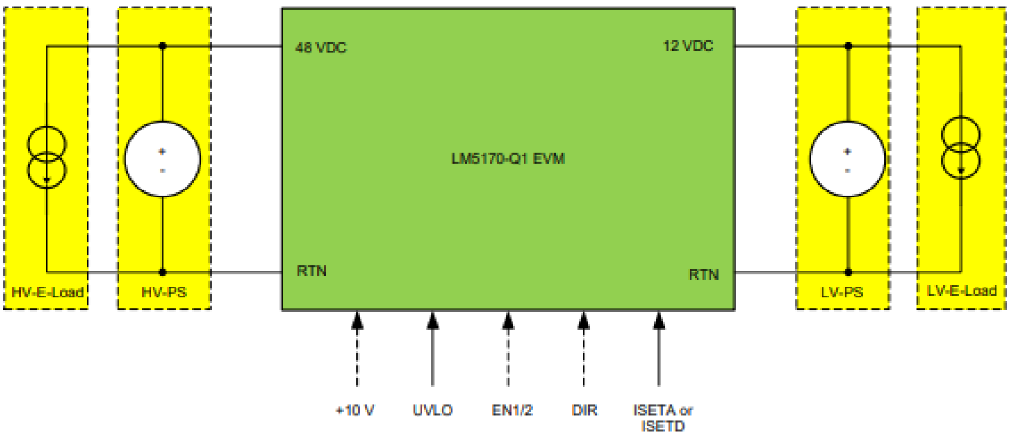


Figure 4.9: LM5170 DC/DC Converter Operation Setup [2],[3]

4.5.1.c The operation of the DC converter is as follows (The Figure 4.9) :

- Connect the High side and Low side Battery pack nodes (Low or High side could be electronics loads also).

- Apply a voltage > 2.5 V and < 6 V to the UVLO pin to release it from the shutdown mode.

- Select the EN1 or EN2 to enable the dc to dc converter output, for instance, EN1 is the output enable signal for Channel1 and EN2 is the output enable signal for Channel 2.

- Depending on the mode of operation Apply DIR pin voltages. Direction command input. Pulling DIR above 2 V sets the converter to buck mode, which commands the current to flow from the HV-Port to LV-Port. Pulling DIR below 1 V sets the converter to boost mode, which commands the current to flow from the LV-Port to HV-Port. If the DIR pin is left open, the LM5170 detects an invalid command and disables both channels with the MOSFET gate drivers in the low state[3, p .5].

- Use the ISETA signal to set the current.ISETA is the analog current programming pin. The inductor DC is proportional to the ISETA voltage. Use either ISETA or ISETD but not both for channel current programming. When ISETA is not used, connect a 100-pF to 0.1-µF capacitor from ISETA to AGND[3, p .5].

- If the ISETD is used, The PWM current programming pin. The inductor DC level is proportional to the PWM duty cycle. Use either ISETA or ISETD but not both for channel current programming. When ISETD is not used, short ISETD to AGND [3, p .6].

4.5.1.d Summery of the DC/DC Converter:

Although DC/DC Converter LM5170 is capable to use the dual channel in a full bridge, we have limited the DC/DC converter to the single channel with full bridge operation according to the Type ii BMS DC/DC converter configuration. Depending on the user's need user can use ISETA or ISETD to setting the current flowing in the dc to dc converter. For Instance, if the user uses a microcontroller it is much more convenient to use the PWM, so the ISETD is a natural choice, If the user opts Central pc/ Labview application it is much better to use ISETA through some analog supply. Ultimately ISETD (PWM) converted to the Analog voltage to set the current.

4.5.2 Switch Matrix :

Automotive BMS applications demand sophisticated and robust switch matrices, as in the market there are no switch matrix will available according to the application. There has been specific knowledge used to pick this switching component. Switching components are more unlikely than the conventional components, such a vote for picking the switching components always registered for the high power MOSFETs because of various technological advantages over conventional electro-mechanical switches. Since the component choice is entirely left to the design engineer, it is always a good practice to design these switch matrix boards from scratch to have full control over the system.

The following sections will give more insights into the switch matrix. Single or

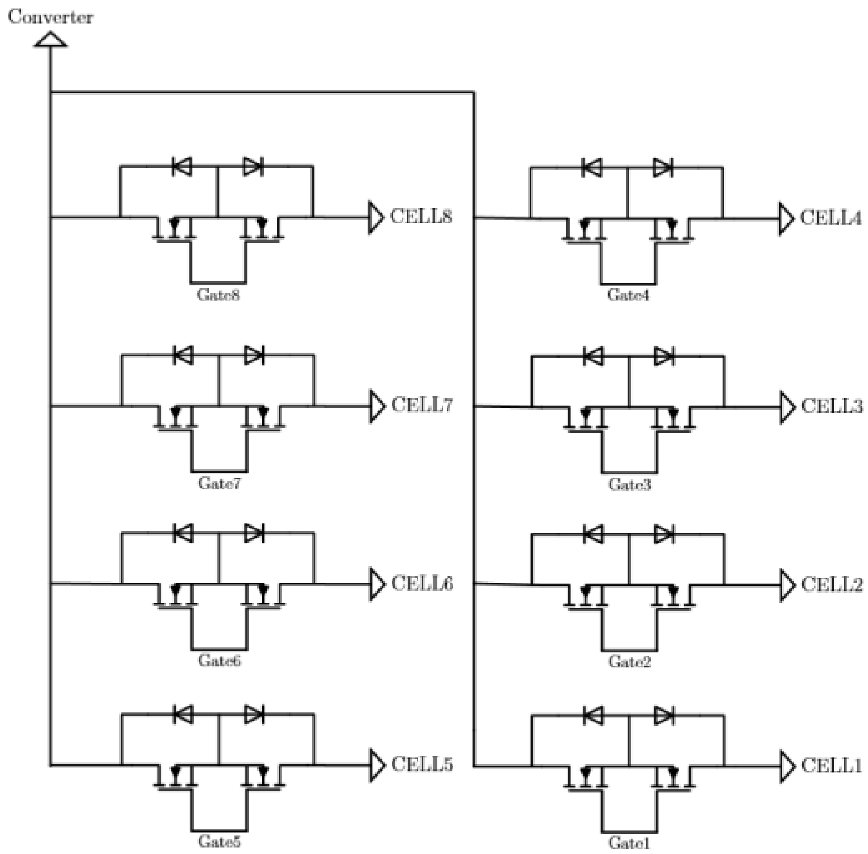


Figure 4.10: Typical Mosfet switch matrix for 8 batteries [4]

double back-to-back FETS are used for the switch matrix, back to back MOSFETS are two MOSFETs housed in a single package or externally by connecting the gates of FETs are common. The Figure4.10 implicates one such example of a switch matrix using the back-to-back MOSFETs.

4.5.2.a The initiative understanding behind choosing the switch matrix MOSFET:

- Low Rds ON; low on-state resistance implicates that MOSFET can carry high DC with lower dissipation.

- High Blocking voltage; High blocking voltage between the drain and the source ensures the breakdown safety of the MOSFET against the full Battery pack voltage.

- Low gate area - to drive the FET faster, and it cost less than the current budget for the FET's gate driver.

- Low gate drive voltage. So-and-so forth.

By analyzing the criteria mentioned in the section, the choice is made to use STD20NF06L for the switch matrix. The component specification is as follows : STD20NF06[15] is the high-power MOSFET that has been developed for automotive applications to handle the High current with very low input gate capacitance. The FET has perfect dv/dt. STD20NF06 is DPACK package which is quite big compared to SMD package and single package dual back-to-back FET's, yet the FET is opted for because of the following benefits. The back-to-back FET arrangement is made externally as shown in Figure 4.10. for more insights into the component refer to the MOSFET Datasheet [15].

STD20NF06L Datasheet			
Symbol	Parameter	Value	Unit
V_{ds}	Drain-source voltage	60	V
V_{gs}	Gate-source voltage	$\pm$ 18	V
I_d	Drain current (continuous) at $TC = 25 \deg C$	24	A
P_{Tot}	Total power dissipation at $TC = 25 \deg C$	60	W
$\frac{dv}{dt}$	Peak diode recovery voltage slope	10	V/ns
C_{iss}	Input capacitance VDS = 25 V, f = 1 MHz, VGS = 0 V,	660	C
$R_{ds(on)}$	Static drain-source on-resistanc	@VGS = 10V,@ID = 12A, 32	Ω

4.5.3 Matrix Switch Gate Driver :

Modern BMS application is suffocated by the hot swapping of the Batteries for balancing. When the battery node is switched in the battery pack to balance the battery node matrix(switching circuit) the MMU will see an immense current that is flowing from the battery [16]. when the switch matrix is switched to a particular node of the battery pack. The battery Node will be directly connected to the output node of the DC/DC converter (The low side of the DC/DC Converter refers to the circuit 5.6 @low side), which will be having reservoir capacitor that will sink an immense amount of the current from the battery in very short time this will cause switching FET to burn, so it essential to switch FET very carefully. such technique is called "Hot Swap". "Hot Swap" is FET switching technique Figure4.10, more often used in live power switch applications. The technique allows the gate driver circuit to monitor the current flowing through the switch circuit by the input sense resistance. By any chance Hot swap circuit doesn't allow the rapid surge of the load current in the switch circuit [16].

4.5.3.a LTC4231 :

LTC4231 is an Analog Device Inc Micro power hot-swap controller that is employed to face circuit board insertion and abrupt live power supply. An internal high-side switch driver controls the gate of an external N-channel MOSFET. Back-to-back MOSFETs can be used for reverse supply protection down to –40V [16].

The LTC4231 provides a debounce delay and allows the GATE to be ramped up at an adjustable rate. After startup, the LTC4231's quiescent current drops to 4µA during normal operation with output active. UVL, UVH, OV, and GNDSW monitor overvoltage and Undervoltage periodically, keeping total quiescent current low. Pulling SHDN low shuts down the LTC4231 and the quiescent current drops to 0.3µA.

During an overcurrent fault, the LTC4231 actively limits current while running an adjustable timer [16]. The LTC4231-1 remains off after a current fault while the LTC4231-2 automatically reapplies power after a cool-down period[16].

A typical circuit diagram and the operational waveforms of the LTC4231 are described in the Figure5.8. For more technical details refer to the ADI LTC4231 datasheet[16].

4.5.3.b Inrush Current Control by LTC4231 :

In most, automotive applications keeping the inrush current low and in control is essential to avoid catastrophic damage to the switching circuits. LTC4231 takes a golden hand in controlling the inrush current by startup method (Timer Delay varying). The equations 4.6 implicate the Inrush current controlled by the LTC, the Inrush current highly depends on the gate capacitance of the switch, and the output capacitance of the DC/DC capacitance (load Capacitance C_L). A capacitor C_G of the Gate to the GND can be used to control the gate voltage slew rate for the Inrush current in the Switch.

$$I_{InRsush} = \frac{C_L}{C_G} \times 10\mu A \tag{4.6}$$

The V_{GATE} of the switch raise with the slope of $10\mu A/C_G$. Once V_{GATE} crosses the Vth, status goes high impedance. see the figure4.11 which explains the Inrush current protection when the $\Delta V_{Th(GATE)}$ crosses the gate voltage threshold.

The Design Example in the Chapter5 explains, how to pick the design parameters to design the inrush current limit and gate driver, please follow. LTC4231 holds a wide range of advantages compared to the gate driver that is available in the market such Wide Operating Voltage Range: 2.7V to 36V, Reverse Supply Protection to –40V n Adjustable

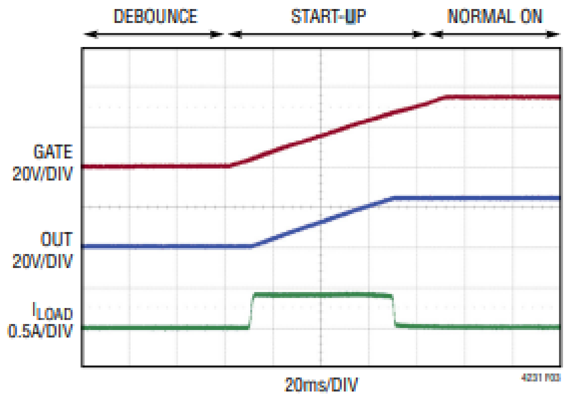


Figure 4.11: Inrush Control by Limiting V_{GATE} Slew

Analog Current Limit with Circuit Breaker n Automatic Retry or Latchoff on Current Fault n Overvoltage and Undervoltage Monitoring n Controls Single or Back-to-Back N-Channel MOSFETs [16]. By considering all the facts we have picked the LTC4321 as the gate driver for the switch matrix.

4.5.4 Current Sense :

As elaborated in the BMS architecture High precision current sensors are used to monitor the BMS Currents. The currents are mainly monitored by the sensor charging current that is entering through the Battery pack Top and balancing current that is entering or leaving from the DC to Dc convert to the Balancing node from Battery pack TOP.

For Inventvm active balancing BMS application, The team has selected INA238 Current sensor from Texas instruments. The chapter(Current and Voltage Synchronization for BMS application) gives an extensive explanation for choosing the INA238[17] and the application.

4.5.5 Wireless Communication Hardware :

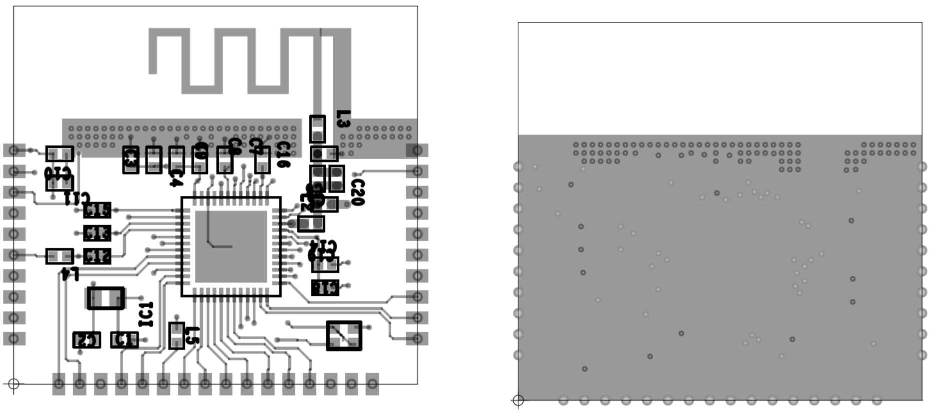
The Bed Rock Idea behind the Inventvm active balancing BMS is to make the BMS architecture in the Wireless Communication Environment. The wireless communication architecture will reduce the immense pain of hard wires for communication in modern smart EVs. The Wireless Communication picked for the project is the Bluetooth stack, Chapter 3 takes the privilege to explain the Bluetooth Hardware choosing criteria, and design the proprietary Bluetooth solution for the projects. The BLUeNRG-355MC[6] and the Nordic[7] are the Bluetooth solutions employed in the project.

Chapter 5

Misellaneous

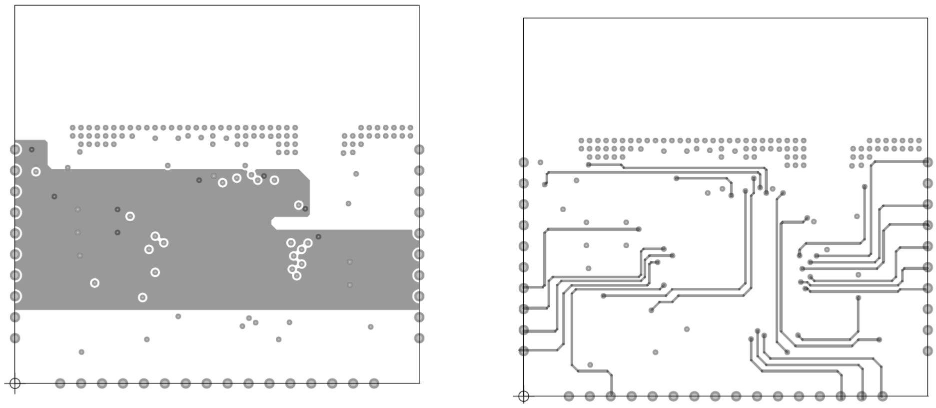
5.1 Chapter 3

5.1.0.a BLUeNRG-355mc BLE module Layout :



(a) Top layer (b) Bottom Layer

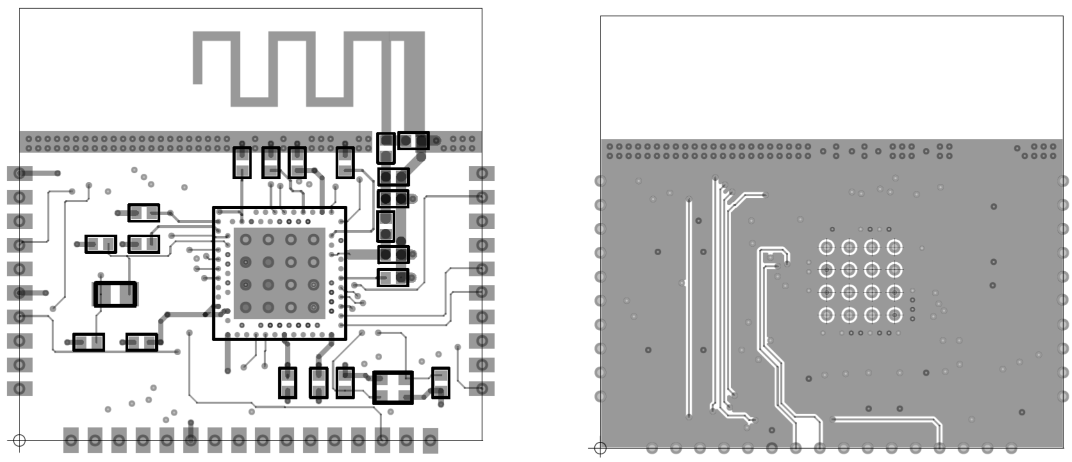
Figure 5.1: BLUeNRG-355mc BLE Module Layout



(a) Power Supply Layer-1 (b) Signals Layer-2

Figure 5.2: BLUeNRG-355mc BLE Module Layout

5.1.0.b Nordic nrf52840 BLE module Layout :



(a) Top layer (b) Bottom Layer

Figure 5.3: Nordic nrf52840 BLE module Layout

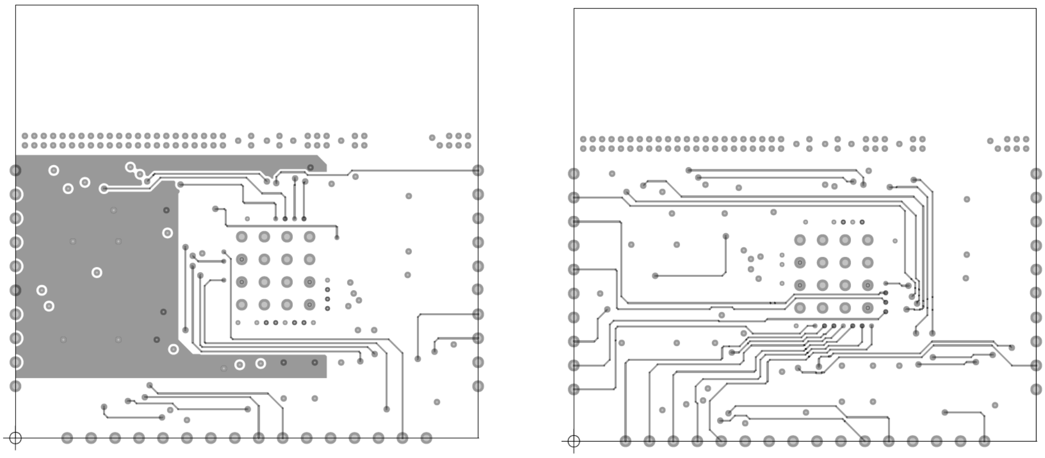
5.2 Chapter 4

5.2.0.a Design Example for the LTC4321 Gate Driver :

As Design takes the following specifications for the Figure5.8 application circuit. The application is rated for a max battery pack voltage of 24V at 5A, $C_L = 100\mu F$. UV raising=23V, UV falling = 22V, OV rising = 26V.

Sense Resistor :

$$R_{sense} = \frac{\Delta V_{sense(CB)(MIN)}}{I_{Inrush}} = \frac{(47mV)}{(2A)} = (23.5m\Omega) \tag{5.1}$$



(a) Power Supply Layer-1 (b) Signals Layer-2

Figure 5.4: Nordic nrf52840 BLE module Layout

Use RSENSE = 22.5mΩ for margin. Worst case analog current limit:

$$I_{LIMIT(MIN)} = \frac{\Delta V_{sense(ACL)(MIN)}}{R_{sense}} = \frac{(65mV)}{(23.5m\Omega)} = (2.89A) \tag{5.2}$$

$$I_{LIMIT(MAX)} = \frac{\Delta V_{sense(ACL)(MAX)}}{R_{sense}} = \frac{(90mV)}{(23.5m\Omega)} = (4A) \tag{5.3}$$

Calculate the worst-case time it takes to charge up CL analog current limit:

$$t_{CHARGE(MAX)} = \frac{C_L \times V_{IN}}{I_{LIMIT(MIN)}} = \frac{(100\mu F \times 24V)}{(2.89A)} = (0.9ms) \tag{5.4}$$

For inrush control using analog current limit, $t_{CHARGE(MAX)}$ must be less than the circuit breaker delay (tCB) for a proper start-up [16].

The worst-case power dissipation in MOSFET M1 occurs ”

$$P_{DISS} = V_{IN} \times I_{LIMIT(MAX)} = (24V \times 4A) = (96W) \tag{5.5}$$

during a severe overcurrent fault when the current is controlled by analog current limit for the duration of tCB:

$$C_T = \frac{t_{Cb}}{24V} = \frac{(2mS)}{(24V)} = (82nF) \tag{5.6}$$

If a low inrush current ($< \ \Delta V_{SENSE(CB)}$) is preferred, refer to the Figure 5.8 application circuit which uses a gate capacitor CG to limit the inrush current. Choose IINRUSH = 0.5A which is set using C_G [16]:

$$C_G = \frac{C_l \times 10\mu A}{I_{Inrush}} = \frac{(100\mu F \times 10\mu A)}{(2.89A)} = (20nF) \tag{5.7}$$

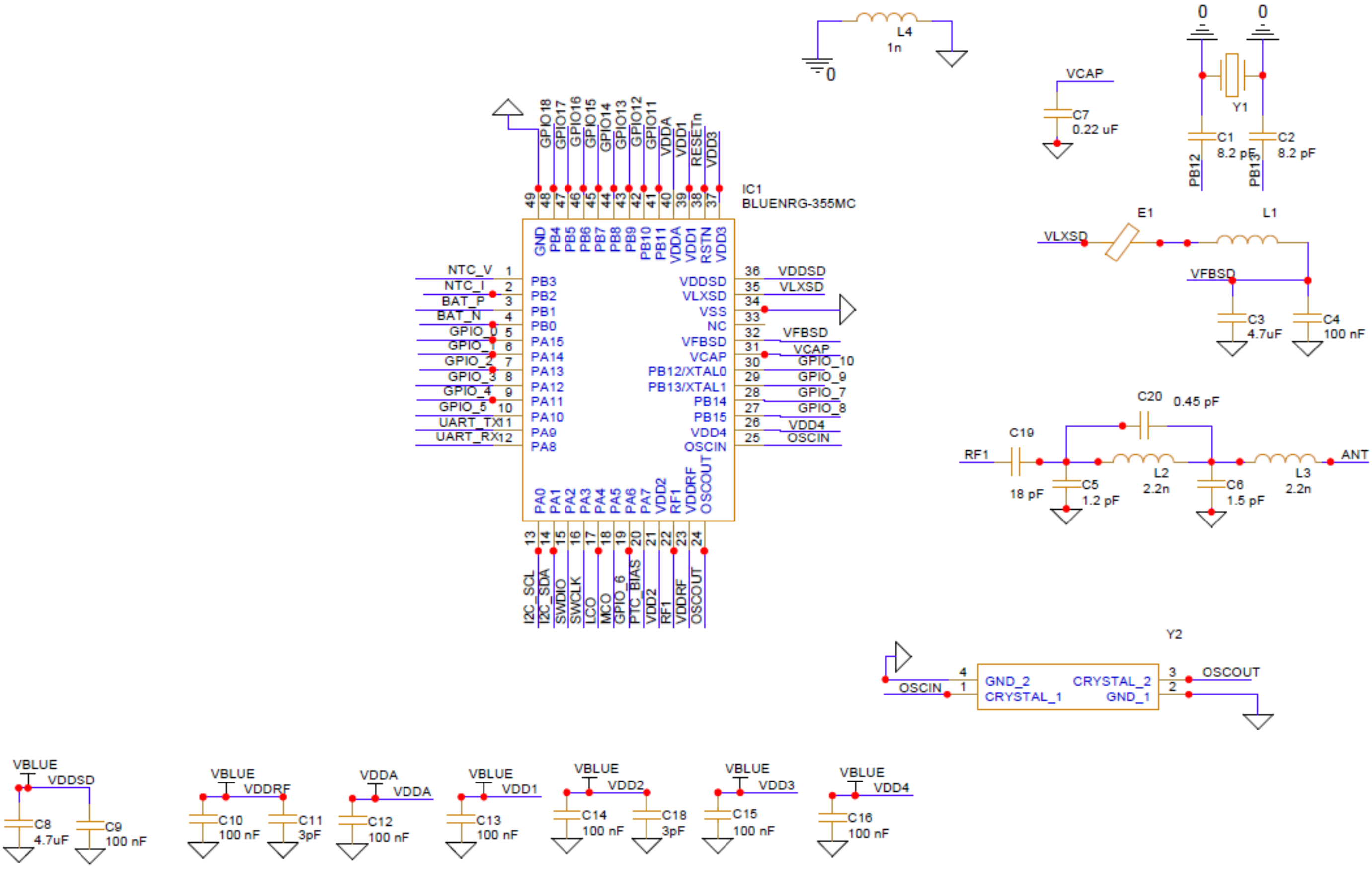


Figure 5.5: BLUeNRG-355mc BLE Complete Schematic

The time to charge up CL with 0.5A is:

$$t_{CHARGE(MAX)} = \frac{C_L \times V_{IN}}{I_{Inrush}} = \frac{(100\mu F \times 24V)}{(0.5A)} = (48ms) \tag{5.8}$$

The average power dissipation in the MOSFET M1 during this start-up is:

$$P_{DISS} = V_{IN} \times I_{LIMIT(MAX)} = (24V \times 0.5A) = (6W) \tag{5.9}$$

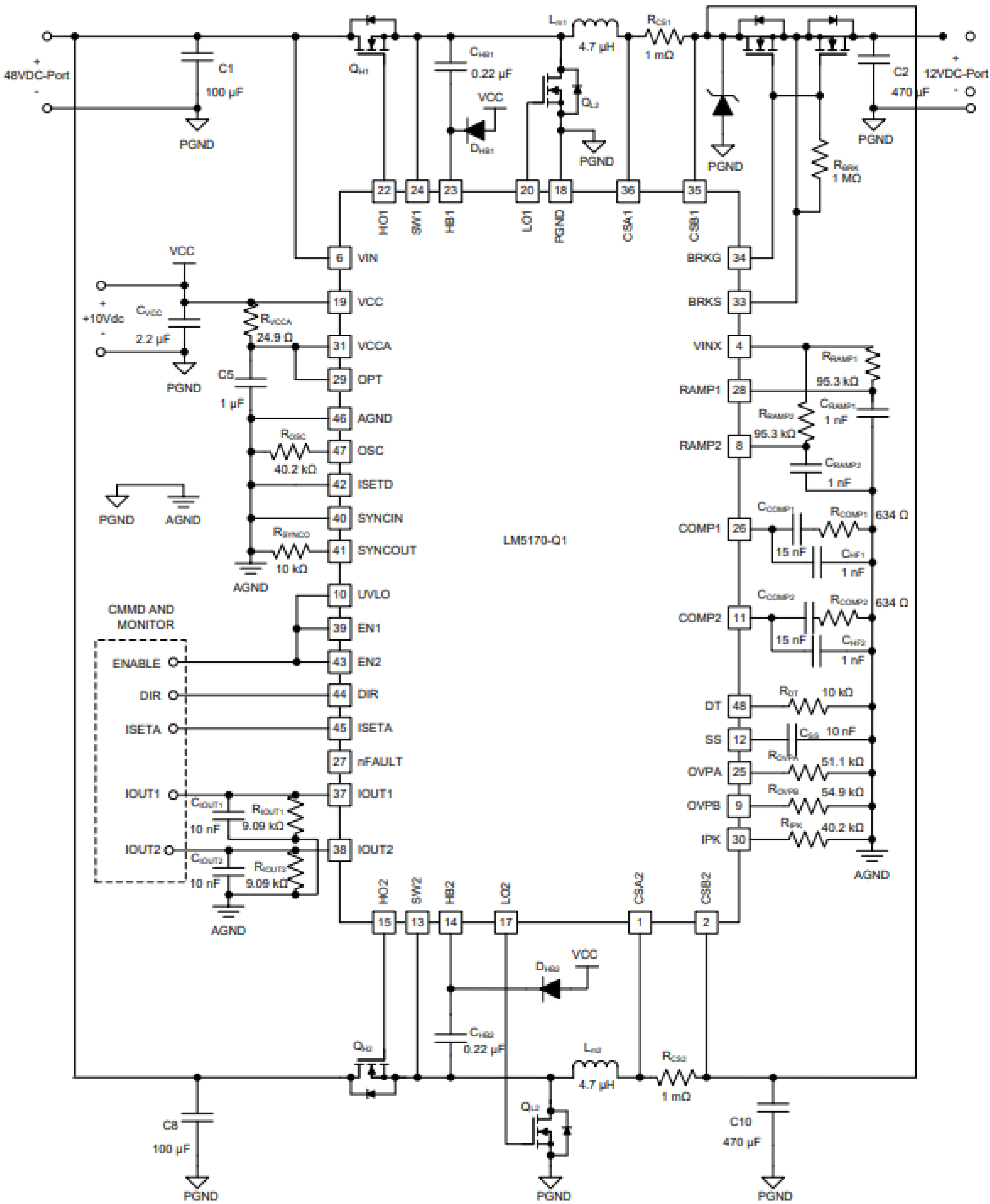


Figure 5.6: Typical Bidirectional circuit of the LM5170

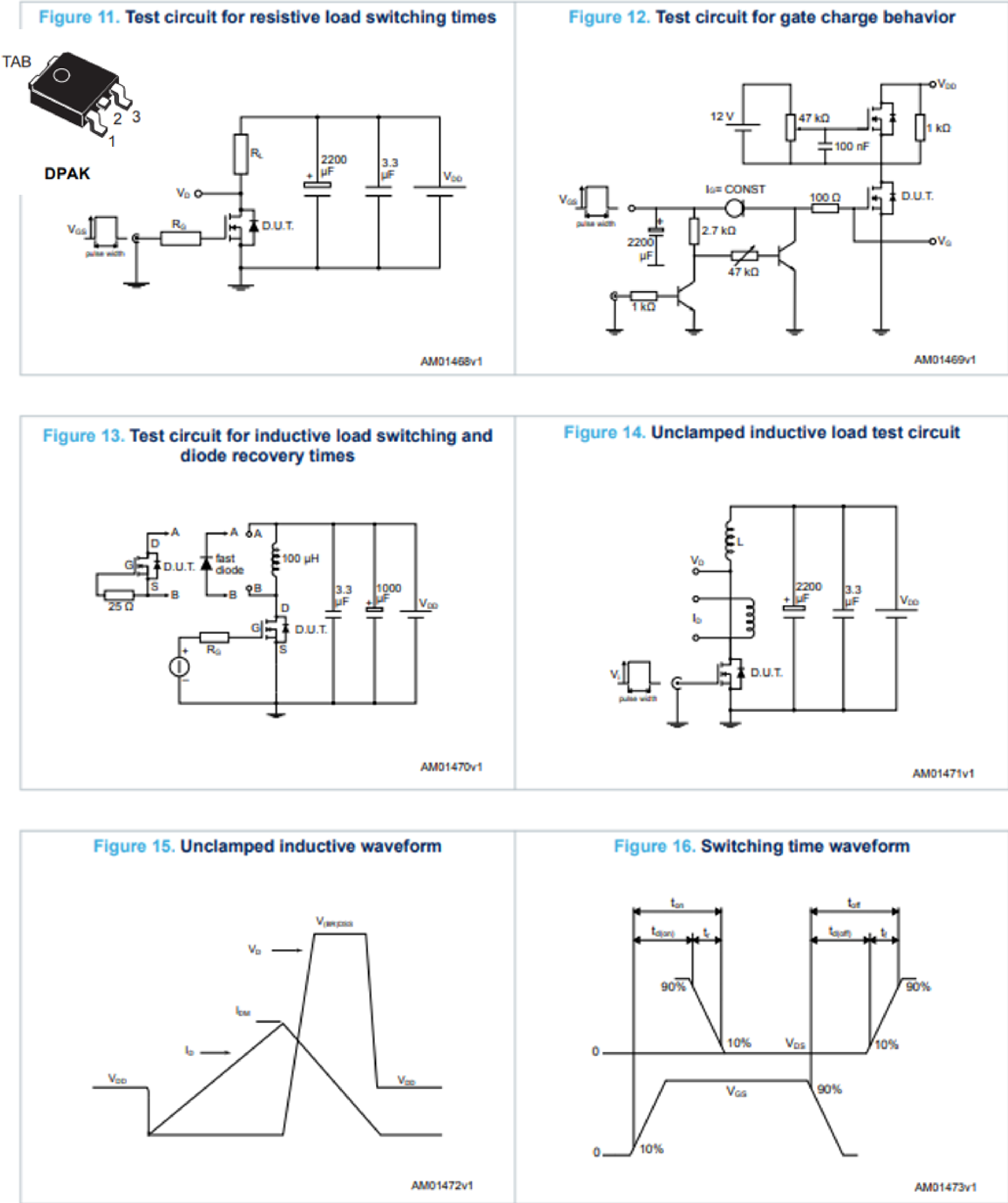


Figure 5.7: STD20NF06L Application typical circuit and package

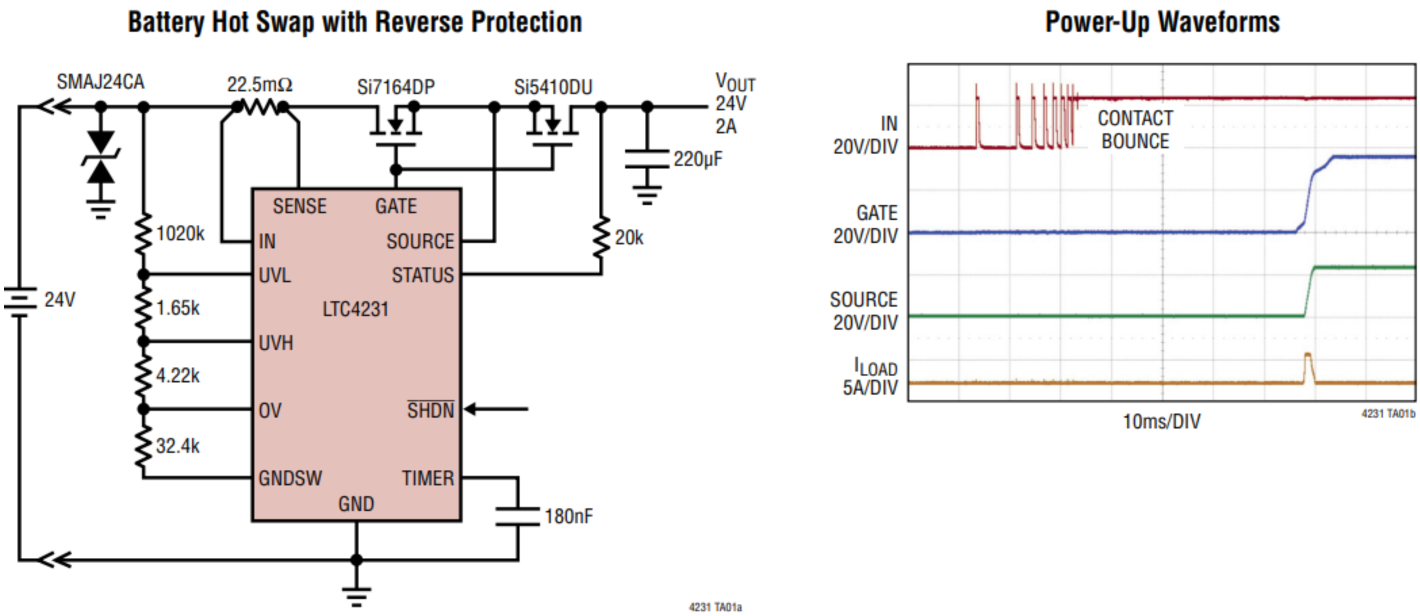


Figure 5.8: LTC4231 Application circuit and the Operational waveform

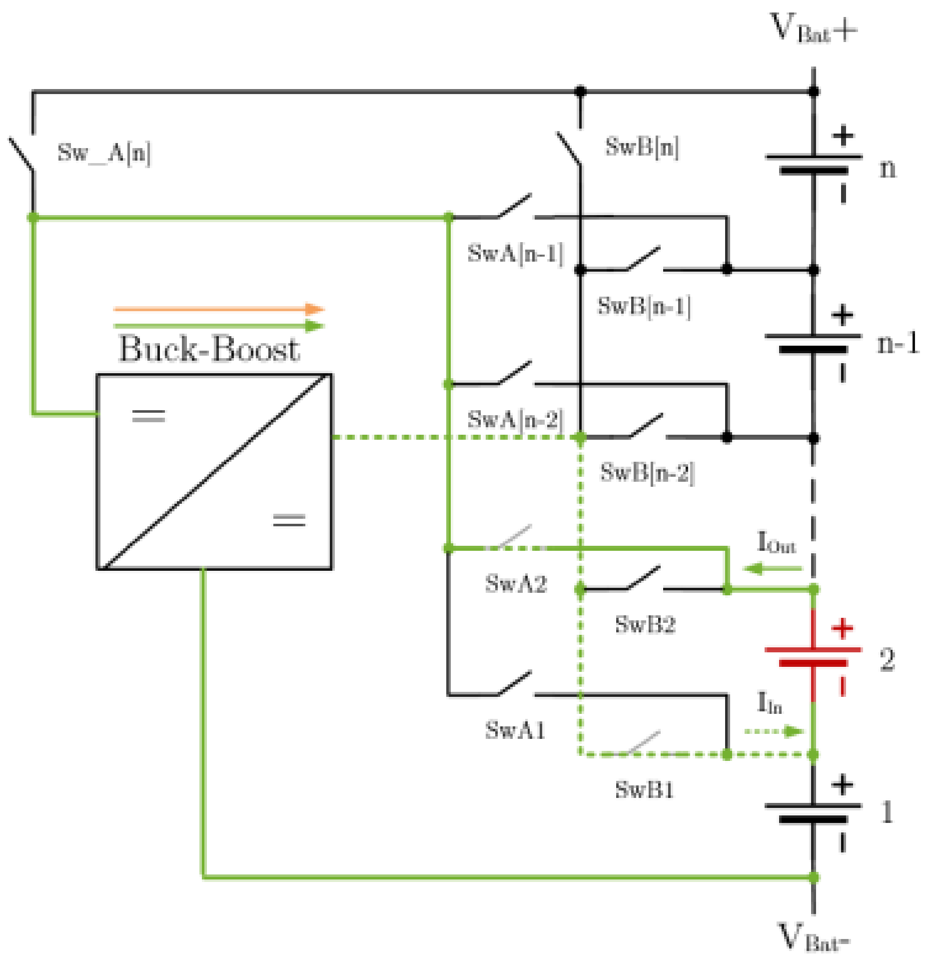


Figure 5.9: *Type Ib* Active Balancing Circuit

(a) Single operation bidirectional buck-boost converter (Low-side)

(b) Single operation bidirectional buck-boost converter (High-side)

Figure 5.10: Typical Schematics of the Low side and High Side buck-boost Converter

Bibliography

[1] N. B. Applications, “An11994qn908x ble antenna design guide,” *NXP Annual Conference journals*, vol. Rev 1.0, June 2017. [Online]. Available: https://www.nxp.com/docs/en/nxp/application-notes/AN11994

[2] T. d. Shaurya, “Designing anaccurate multifunction li-ion battery-testing solution,” *TI DC/DC switching regulator applications*, vol. Rev 1.0, September 2020. [Online]. Available: https://www.ti.com/lit/wp/slpy010/slpy010.pdf

[3] SNVU543A, “Lm5170-q1 evm user guide,” *TI APIs Automation Integration forum*, vol. Rev 1.0, November 2016. [Online]. Available: https://www.ti.com/lit/ug/snvu543a/snvu543a.pdf

[4] M. Räber, “New active charge balancing methods and algorithms for lithium-ion battery systems,” Ph.D. dissertation, Université de Haute-Alsace, 24-Jan-2019. [Online]. Available: https://doi.org/10.21256/zhaw-17244

[5] G. T. Tapan Pattnayak, “Antenna design and rf layout guidelines,” *Cypress Conference journals*. [Online]. Available: http://www.cypress.com/go/AN91445

[6] S. microelectronics application team, “Evaluvation platform based on the bluenrg-355mc system-on-chip,” *STM IoT Applications*, vol. REv 2.0, no. STEVAL-IDB011V2, 2021. [Online]. Available: https://www.st.com/en/evaluation-tools/steval-idb011v2.html

[7] N. application team, “nrf52840 system-on-chip multiprotocol bluetooth 5.3 soc supporting bluetooth low energy, bluetooth mesh, nfc, thread and zigbee,” *Nordic Applicatin guides*, vol. REv 3.0, no. nRF52840. [Online]. Available: https://www.nordicsemi.com/Products/nRF52840

[8] N. software team, “nrf5 sdk v17.1.0,” *Nordic software stack guides*, vol. REv 17.1.0, no. nRF5 SDK, 2022/07/28. [Online]. Available: www.nordicsemi.com/eng/Products/Bluetooth-low-energy/nRF5-SDK

[9] . Cheuk Yin Cheung, 1 Joseph S. M. Yuen and S. W. Y. Mung, “Miniaturized printed inverted-f antenna for internet of things: Adesign on pcb with a meandering line

and shorting strip," *Hindawi International Journal of Antennas and Propagation*, 26 March 2018. [Online]. Available: https://doi.org/10.1155/2018/5172960

[10] N. B. Applications, "Ble antenna design guide," *NXP Annual Conference journals*, May 2018. [Online]. Available: https://www.nxp.com/docs/en/user-guide/UM10992

[11] S. microelectronics application team, "Bluenrg-355mc system-on-chip steval-idb011v2 bill of materials," *STM IoT Applications*, vol. REv 2.0, no. STEVAL-IDB011V2, 2021. [Online]. Available: https://www.st.com/en/evaluation-tools/steval-idb011v2_bom

[12] O. Losito, V. Dimiccoli, and D. Barletta, "Meander-line inverted f antenna designed using a transmission line model," in *The 8th European Conference on Antennas and Propagation (EuCAP 2014)*, 2014, pp. 1370–1373.

[13] R. Kanan, "Compact double meandered line inverted-f antenna for outdoor parking wireless car detector," in *2014 IEEE Asia Pacific Conference on Wireless and Mobile*, 2014, pp. 30–35.

[14] SNVSAQ6D, "Lm5170 multiphase bidirectional current controller," *TI DC/DC switching regulator products*, vol. Rev 2.0, Novemeber 2016. [Online]. Available: https://www.ti.com/lit/ds/symlink/lm5170.pdf

[15] S. Applications, "Std20nf06l datasheet," *ST PowerManagement and Discrete Components*, vol. Rev 1.0, 29 Apr 2022. [Online]. Available: https://www.st.com/en/power-transistors/std20nf06l.html#documentation

[16] A. Applications, "Ltc4231 micropower hot swap controller," *ADI and LT PMIC*, vol. Rev B, 2018. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/LTC4231.pdf

[17] SLY025A, "Ina238 85-v, 16-bit, high-precision power monitor with i2c interface," *TI Current/Voltage/Power Monitors*, vol. Rev 2.0, MAY 2022. [Online]. Available: https://www.ti.com/lit/ds/slys025a/slys025a.pdf