# Module Three Introduction and Learning Objectives

## Welcome to the Processor Microarchitecture & Design Module!

To implement the MIPS ISA, we design processor microarchitectures according to its specification. A particular architecture, such as MIPS, may have many different microarchitectures, each with different trade-offs of performance, cost, and complexity. They all run the same programs (i.e., instructions), but their internal designs vary widely. In this module, we will learn the datapath and control unit for two different implementations of the MIPS instruction set. Before learning this module, you might think that building a processor could be very complicated. However, if you follow the progress of this module, you will find that its idea is actually quite straightforward. And you will be able to build a processor on your own with the knowledge of this module.

## Learning Objectives

By the end of the module, you will be able to

1. Know the basic design of the single-cycle and pipelined MIPS processor.
2. Understand how different instructions execute in the MIPS processor.
3. Understand the constraints of pipelined processor design (e.g., hazards) and their solutions (e.g., branch prediction).

## How to Achieve the Objectives

You can achieve this module's learning objective by accomplishing the following:

### Readings

1. Chapter 4 of the textbook: **COD_Chapter4.pdf (https://sjsu.instructure.com/courses/1491749/files/69324406?wrap=1)**

2. Extra reading: **DDCA_Chapter7.pdf (https://sjsu.instructure.com/courses/1491749/files/69324405?wrap=1)**

### Lectures

Check the module for the latest lecture slides.

### Assignments

There will be a series of assignments related to this module. Check the Assignments under this module for the latest assignment.

### Discussions

Module discussion: **Module Three General Discussion (https://sjsu.instructure.com/courses/1491749/discussion_topics/4728253)**

## How You Will Demonstrate Your Achievement of the Learning Objectives

1. Quiz.
2. Extra practice questions.