**ABOUT THE AUTHORS**

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I am *Saiteja* and I am from Hyderabad, India. I completed my bachelors in Electronics and Communication Engineering from Gokaraju Rangaraju Institute of Engineering and Technology with a CGPA of 9.97/10 in the year 2019. I received a Gold Medal for the academic excellence from my university. Right after that, I got an opportunity to work for Tata Consultancy Services as a Systems Engineer and have worked for 3 years until July 2022. I speak English, Hindi, and Telugu where the last of these is my first language. My interests include but not limited to Cricket, Table-Tennis and learning new languages. Currently I am pursuing my master’s in Computer Engineering at San Jose State University.

**TABLE OF CONTENTS**

[LIST OF FIGURES \ TABLES 3](#_Toc118392193)

[INTRODUCTION: 4](#_Toc118392194)

[MY GROUP: 4](#_Toc118392195)

[GIVEN TASK: 4](#_Toc118392196)

[STEPS TAKEN TO COMPLETE THE TASK: 4](#_Toc118392197)

[DISCUSSION SECTION: 5](#_Toc118392198)

[1) Datapath Explanation: 5](#_Toc118392199)

[2) Control Path Explanation: 10](#_Toc118392200)

[3) Simulating in Vivado: 12](#_Toc118392201)

[COLLABORATION SECTION: 14](#_Toc118392202)

[CONCLUSION: 14](#_Toc118392203)

[APPENDIX 15](#_Toc118392204)

[1) Datapath of the Enhanced (shown in red color) Single-Cycle MIPS Processor: 15](#_Toc118392205)

[2) Source Code – tb\_mips\_top.v (TestBench module for the design) 15](#_Toc118392206)

[3) Source Code – mips\_top.v (Top module for the design) 17](#_Toc118392207)

[4) Source Code – mips.v (Top module for the datapath and controlpath) 18](#_Toc118392208)

[5) Source Code – datapath.v (Top module for the datapath) 19](#_Toc118392209)

[6) Source Code – adder.v (Module for the adder unit) 23](#_Toc118392210)

[7) Source Code – alu.v (Module for the ALU unit) 23](#_Toc118392211)

[8) Source Code – dreg.v (Module for the Program Counter unit) 24](#_Toc118392212)

[9) Source Code – mux2.v (Module for the 2x1 Multiplexer unit) 24](#_Toc118392213)

[10) Source Code – regfile.v (Module for the Register File) 24](#_Toc118392214)

[11) Source Code – signext.v (Module for the Sign Extending Unit) 25](#_Toc118392215)

[12) Source Code – mux4.v (Module for the 4x1 Multiplexer unit) 25](#_Toc118392216)

[13) Source Code – mult\_inf.v (Module for the 32-bit Multiplier unit) 26](#_Toc118392217)

[14) Source Code – HiLo\_reg.v (Module for the Hi-Lo storage register) 27](#_Toc118392218)

[15) Source Code – controlunit.v (Module for the Control unit) 28](#_Toc118392219)

[16) Source Code – maindec.v (Module for the Main decoder) 29](#_Toc118392220)

[17) Source Code – auxdec.v (Module for the Auxiliary decoder) 30](#_Toc118392221)

[18) Source Code – imem.v (Module for the Instruction memory) 30](#_Toc118392222)

[19) Source Code – dmem.v (Module for the Data memory) 31](#_Toc118392223)

[20) Source Code – memfile.dat (Memory dump for factorial.asm in hexadecimal format) 31](#_Toc118392224)

# LIST OF FIGURES \ TABLES

Table5.1 – Signal-Description table for the D-Register

Table5.2 – Signal-Description table for the 32-bit adder

Table5.3 – Signal-Description table for the 2x1 multiplexer

Table5.4 – Signal-Description table for the Sign Extension Unit

Table5.5 – Signal-Description table for the Register File

Table5.6 – Signal-Description table for the ALU

Table5.7 – Truth-Table observed in alu.v file

Table5.8 – Signal-Description table for the 4x1 multiplexer

Table5.9 – Signal-Description table for the HiLo register

Table5.10 – Signal-Description table for the multiplier

Figure 5.11 – Enhanced Datapath of the Single-cycle MIPS Processor

Table5.12 – Signal-Description table for the Main Decoder

Table5.13 – Signal-Description table for the Auxilary Decoder

Table5.14 – Modified Truth-Table for the Main Decoder

Table5.15 – Modified Truth-Table for the Auxiliary Decoder

Figure5.16 – Waveform after verifying the Enhanced Single-cycle MIPS Processor

Figure5.17 – Waveform after verifying the Enhanced Single-cycle MIPS Processor

# INTRODUCTION:

This activity is to extend the initial design of the single-cycle MIPS processor (from Assignment #5) to support more MIPS instructions. Apart from that, we learn the basic technique for functionally verifying a processor.

# MY GROUP:

**Name:** Student\_Team 6

**Members:** Harish Marepalli (016707314), Tirumala Saiteja Goruganthu (016707210),

# GIVEN TASK:

The task is to carefully enhance the single-cycle MIPS processor’s functionality by extending its instruction set (add, sub, and, or, slt, lw, sw, beq, j, addi) to cover the following additional instructions: MULTU, MFHI, MFLO, JR, JAL, SLL, SLR: This report must contain the following:

1. Memory dump of factorial.asm program from MARS simulator.
2. Enhanced Datapath of the single-cycle MIPS processor.
3. Modified tables of the control unit decoders.
4. The simulation logs and testbench.
5. Corresponding waveforms and the verilog source code.

Note that any microarchitecture changes (modification and/or extension) to the initial design (figure and source code) must be in a different color and clearly noted.

# STEPS TAKEN TO COMPLETE THE TASK:

1. Spent time to understand the question carefully.
2. First, using the MARS simulator, get the machine code of the *factorial.asm* file.
3. To get the dump, go to *File -> Dump to memory* and select *Hexadecimal\_text* as the dump option.
4. Divided the work of adding new instructions between us where, I worked on MULTU, MFHI and MFLO instructions and *Saiteja* worked on JR, JAL, SLL, SLR instructions.
5. After completing the assertions on the new instructions, we drew a rough datapath on the paper first to get the clear working idea of the enhanced datapath.
6. Simultaneously, the truth tables of the control unit decoders i.e., the auxiliary and main decoder tables are modified to send the correct control signals to the above mentioned enhanced datapath.
7. To test the design, we created a new project in vivado and imported the initial single-cycle MIPS processor archive into the project to act as a base.
8. The desired code is written in the existing files and new files are created wherever required.
9. After that, we simulated the design and verified the output waveforms for the design correctness.
10. Finally, after getting the desired output, the whole enhanced datapath is drawn using the Visio tool.

# DISCUSSION SECTION:

## Datapath Explanation:

From the Verilog file “*datapath.v*”, we can observe that nine leaf-level modules are used to instantiate the whole datapath (albeit some modules may be used multiple times). In this section, we will try to visually (in the form of tables) show the input-output structure of each leaf-level module and then we traverse our way back up to the datapath module.

1. The D-Register module named “*dreg*” contains three inputs and one output. The main logic here is that for every positive clock edge and positive reset edge we will start the execution. If the reset (*rst*) signal is asserted, then assign logic ‘*0*’ to the output (*q*), else assign the input (*d*) to the output (*q*). The following table (*Table5.1*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| clk | Clock signal (Input) |
| rst | Reset Signal (Input) |
| d[31:0] | Input Signal (Input) |
| q[31:0] | Output Signal (Output) |

*Table5.1 – Signal-Description table for the D-Register*

1. The 32-bit adder module named “*adder*” contains two inputs and one output. The main logic here is written in behavioral way where just a single instruction (*y = a+b*) is enough to realize a 32-bit adder. The following table (*Table5.2*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[31:0] | Operand 1 (Input) |
| b[31:0] | Operand 2 (Input) |
| y[31:0] | Result (Output) |

*Table5.2 – Signal-Description table for the 32-bit adder*

c. The 2x1 multiplexer module named “*mux2*” contains two inputs, one output and one selection line to select the required input line. The main logic here is written in behavioral way using the ternary operator (*y = sel ? b : a*) is enough to realize a 2x1 multiplexer. The following table (*Table5.3*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[7:0] | Operand at 0 port (Input) |
| b[7:0] | Operand at 1 port (Input) |
| sel | Selection line (Input) |
| y[7:0] | Output Signal (Output) |

*Table5.3 – Signal-Description table for the 2x1 multiplexer*

d. The sign extension module named “*signext*” contains one input and one output. The main logic here is to get the MSB of the input, duplicate this bit 16 times and append the new 16-bit string to the already existing 16-bit input (*a*) to form a 32-bit number as output (*y*). The following table (*Table5.4*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[15:0] | 16-bit Input (Input) |
| y[31:0] | 32-bit Output (Output) |

*Table5.4 – Signal-Description table for the Sign Extension Unit*

e. The Register file module named “*regfile*” contains eight inputs and three outputs. Each register in this register file can hold 32-bit data. We realize this using a two-dimensional array. Initialize all the register values to zero and initialize “*sp*” value to 32-bit “b’*100*” value. The main logic here is that for every positive edge of the clock, if write enable signal (*we*) is enabled then write the data (*wd*) into the provided write address (*wa*). After that, output all three read-data ports (*rd1, rd2, rd3*) by assigning them with the content at addresses (*ra1, ra2, ra3*). The following table (*Table5.5*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| clk | Clock signal (Input) |
| we | Write Enable (Input) |
| ra1[4:0] | Read Address 1 (Input) |
| ra2[4:0] | Read Address 2 (Input) |
| ra3[4:0] | Read Address 3 (Input) |
| wa[4:0] | Write Address (Input) |
| wd[31:0] | Write Data (Input) |
| rd1[31:0] | Read Data 1 (Input) |
| rd2[31:0] | Read Data 2 (Input) |
| rd3[31:0] | Read Data 3 (Input) |
| rst | Reset (Input) |

*Table5.5 – Signal-Description table for the Register File*

f. The Arithmetic and Logical Unit (ALU) module named “*alu*” has four inputs and two outputs. The main logic here is that depending on the “*op*” value, the operation is determined. So, we use switch case to realize the ALU. Apart from that, a “*zero*” flag is set as output to the ALU which will be de-asserted only if the ALU result is logic low. The following table (*Table5.6*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[31:0] | Operand 1 (Input) |
| b[31:0] | Operand 2 (Input) |
| op[3:0] | Operation Select (Input) |
| zero | Zero Flag (Output) |
| y[31:0] | Result (Output) |
| shamt[4:0] | Shift amount (Input) |

*Table5.6 – Signal-Description table for the ALU*

The following Truth-Table (*Table5.7*) observed from the given Verilog code is as follows:

|  |  |
| --- | --- |
| **op value** | **Corresponding Operation** |
| 0000 | AND |
| 0001 | OR |
| 0010 | ADD |
| 0110 | SUB |
| 0111 | SLT |
| 1001 | SLL |
| 1010 | SLR |

*Table5.7 – Truth-Table observed in alu.v file*

g. The 4x1 multiplexer module named “*mux4*” contains four inputs, one output and one selection line to select the required input line. The main logic here is written in behavioral way using the switch case which is enough to realize a 4x1 multiplexer. The following table (*Table5.8*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[7:0] | Operand at 0 port (Input) |
| b[7:0] | Operand at 1 port (Input) |
| c[7:0] | Operand at 2 port (Input) |
| d[7:0] | Operand at 3 port (Input) |
| sel | Selection line (Input) |
| y[7:0] | Output Signal (Output) |

*Table5.8 – Signal-Description table for the 4x1 multiplexer*

h. A register module named “*HiLo\_reg.v*” is created to store the contents of both higher order and lower bits after the multiplication operation. This module consists of five inputs and two outputs. The main logic here is that if the positive edge of the clock and the positive edge of the reset occurs and when the write enable of this register is asserted, then the contents of *hi* and *lo* will be passed on to *hi\_out* and *lo\_out* output lines. The following table (*Table5.9*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| clk | Clock signal (Input) |
| rst | Reset signal (Input) |
| we | Write enable (Input) |
| hi[31:0] | Higher order bit port (Input) |
| lo[31:0] | Lower order bit port (Input) |
| hi\_out[31:0] | Higher order bit port (Output) |
| lo\_out[31:0] | Lower order bit port (Output) |

*Table5.9 – Signal-Description table for the HiLo register*

i. A multiplier module named “mult\_inf.v” is created to perform the multiplication operation between two operands. This module consists of two inputs and one output. The main logic is realized using the behavioral modelling of the elements i.e., (out <= a\*b). The following table (*Table5.10*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| a[31:0] | Operand 1 (Input) |
| b[31:0] | Operand 2 (Input) |
| out[63:0] | Result (Output) |

*Table5.10 – Signal-Description table for the multiplier*

j. Finally, the whole datapath is realized in a module named “*datapath.v*.” We use one or more of the leaf-level to achieve the required datapath.

The D-Register (*pc\_reg*) is used to store the program counter value with every positive edge of the clock cycle.

The adder (*pc\_plus\_4*) is used to add number 4 to the current program counter to point to the next instruction.

The adder (*pc\_plus\_br*) is used to add pc\_plus\_4 and the branch address (calculated by multiplying the signImm value with 4).

The multiplexer (*pc\_src\_mux*) is used to select either next instruction program counter or the new branch target address.

The multiplexer (*pc\_jmp\_mux*) is used to select either next instruction program counter or the new jump target address.

The multiplexer (*rf\_wa\_mux*) is used to select either the Rd destination register or Rt destination register depending on the type of instruction.

The Register File (*rf*) is used to as a 32 32-bit register container used for processor operations.

The Sign Extension Unit (*se*) is used to extend the 16-bit input using the MSB and replicating the MSB 16 more times before appending to the original 16-bit input to form a 32-bit output.

The multiplexer (*alu\_pb\_mux*) is used to select either the data from the register file or the sign extension unit depending on the type of instruction.

The Alu (*alu*) is used to perform operations such as add, sub, and, or and slt where these operations are controlled by the op[2:0] bits.

The multiplexer (*rf\_wd\_mux*) is used to select either the data from the memory or the alu output depending on the type of instruction.

The multiplexer (*jr\_mux*) is used to select either the PC value coming from the jump/branch instruction, or the return address stored in the $31 register of the register file.

The 4x1 multiplexer (*hilo\_mux*) is used to select either *lo* or *hi* or the output from the *rf\_wd\_mux* multiplexer.

The register (*hi\_lo\_reg*) is used to store the *hi* and *lo* contents of a multiplication operation.

The multiplier (*mult\_inf*) is used to perform the multiplication operation which outputs a 64-bit value. Therefore, these 64 bits are stored into two 32-bit registers realized using above *hi\_lo\_reg* register.

The 2x1 multiplexer (*jal\_wd\_mux*) is used to select either the data output from the *hilo\_mux* or the *pc\_plus4* value using a select line called *jal\_wd\_mux\_sel*.

The 2x1 multiplexer (*jal\_wa\_mux*) is used to select either the data output from the *rf\_wa\_mux* or the *address of ra i.e., $31* value using a select line called *jal\_wa\_mux\_sel*.

The following figure (*Figure 5.11*) will illustrate the datapath for the enhanced (shown in red color) version:

Diagram, schematic

Description automatically generated

*Figure 5.11 – Enhanced Datapath of the Single-cycle MIPS Processor*

## 2) Control Path Explanation:

From the Verilog file “*controlunit.v*”, it is observed that the whole control unit is divided into two categories.

1. A main decoder to generate all the control signals such as mux selects, branch and jump using the opcode part of the instruction machine code and it also outputs a 2-bit *alu\_op* signal which controls the second *auxiliary* or ALU decoder. In addition, to support the JAL instruction, two additional control signals are defined. They are *jal\_wa\_mux\_sel* and *jal\_wd\_mux\_sel*. Depending upon the opcode bits, the corresponding operation is selected. The following table (*Table 5.12*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| opcode[5:0] | Opcode from the Machine Code (Input) |
| branch | Branch Control (Output) |
| jump | Jump Control (Output) |
| reg\_dst | Destination Register Select (Output) |
| we\_reg | Write Enable Register (Output) |
| alu\_src | ALU Source Steering (Output) |
| we\_dm | Write Enable to Data Memory (Output) |
| dm2reg | Data Memory to RF (Output) |
| alu\_op[1:0] | 2-bit ALU Result (Output) |
| jal\_wa\_mux\_sel | JAL Write Address Mux Select |
| jal\_wd\_mux\_sel | JAL Write Data Mux Select |

*Table5.12 – Signal-Description table for the Main Decoder*

1. An Auxiliary or ALU decoder is another module which takes two inputs and sends out four outputs. Depending on the *funct* field and the *alu\_op* signal, the corresponding operation is realized. If *alu\_op* is either 00 or 01, then the operation is add or subtract, else, the *funct* field is used to realize a particular operation. The following table (*Table 5.13*) will illustrate the Signal-Description relationship.

|  |  |
| --- | --- |
| **Signal Name** | **Description (Input / Output)** |
| alu\_op[1:0] | ALU Input from Main Decoder |
| funct[5:0] | Function bits from the Machine Code |
| alu\_ctrl[3:0] | ALU Control bits to ALU Module |
| hilo\_mux\_ctrl[1:0] | Hilo Mux Select |
| hilo\_we | Hilo Register Write Enable |
| jr\_mux\_ctrl | Jump Return Mux Select |

*Table5.13 – Signal-Description table for the Auxiliary Decoder*

1. The modified truth-table of the main decoder contains two additional columns to control the *wa* and *wd* ports of the register file when JAL instruction is getting executed. These lines control two separate multiplexers and will only be asserted if the JAL instruction is being executed. The following table (*Table 5.14*) will illustrate the modified truth-table for the main decoder of the control unit.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Main Decoder** | | | | | | | | | | | |
| **Instr** | **Op5:0** | **branch** | **jump** | **reg\_dst** | **we\_reg** | **alu\_src** | **we\_dm** | **dm2reg** | **alu\_op1:0** | **jal\_wa\_mux** | **jal\_wd\_mux** |
| R-type | 00\_0000 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 10 | 0 | 0 |
| addi | 00\_1000 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 00 | 0 | 0 |
| beq | 00\_0100 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 01 | 0 | 0 |
| j | 00\_0010 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 00 | 0 | 0 |
| jal | 00\_0011 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00 | 1 | 1 |
| sw | 10\_1011 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 00 | 0 | 0 |
| lw | 10\_0011 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 00 | 0 | 0 |

*Table5.14 – Modified Truth-Table for the Main Decoder*

1. The modified truth-table of the auxiliary decoder contains three additional columns to control the *hilo\_mux* select line, *hilo\_we* and *jr\_mux* select line. The following table (*Table 5.15*) will illustrate the modified truth-table for the auxiliary decoder of the control unit.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Auxilary Decoder** | | | | | | |
| **Instr** | **alu\_op** | **funct** | **alu\_ctrl** | **hilo\_mux\_ctrl** | **hilo\_we** | **jr\_mux\_ctrl** |
| and | 10 | 10\_0100 | 0000 | 00 | 0 | 0 |
| or | 10 | 10\_0101 | 0001 | 00 | 0 | 0 |
| add | 10 | 10\_0000 | 0010 | 00 | 0 | 0 |
| sub | 10 | 10\_0010 | 0110 | 00 | 0 | 0 |
| slt | 10 | 10\_1010 | 0111 | 00 | 0 | 0 |
| multu | 10 | 01\_1000 | xxxx | 00 | 1 | 0 |
| mfhi | 10 | 01\_0000 | xxxx | 11 | 0 | 0 |
| mflo | 10 | 01\_0010 | xxxx | 01 | 0 | 0 |
| sll | 10 | 00\_0000 | 1001 | 00 | 0 | 0 |
| srl | 10 | 00\_0010 | 1010 | 00 | 0 | 0 |
| jr | 10 | 00\_1000 | xxxx | 00 | 0 | 1 |

*Table5.15 – Modified Truth-Table for the Auxiliary Decoder*

## 3) Simulating in Vivado:

A test-bench file has already been given in the assignment archive which has been imported into the simulation sources of the Vivado Xilinx tool. After that, when the “*Run Simulation*” button is clicked, the waveforms will appear in the tool. The following figures (*Figure5.16* and *Figure5.17*) constitute the waveforms.

Graphical user interface

Description automatically generated with low confidence

*Figure5.16 – Waveform after verifying the Enhanced Single-cycle MIPS Processor*

**A picture containing graphical user interface

Description automatically generated**

*Figure5.17 – Waveform after verifying the Enhanced Single-cycle MIPS Processor*

# COLLABORATION SECTION:

1. Divided the work of adding new instructions between us where, I worked on the JR, JAL, SLL, SLR instructions and *Harish* completed MULTU, MFHI and MFLO instructions.
2. Worked together on the Datapath block diagram designs using Microsoft Visio tool.
3. Worked together to enhance the control unit decoder truth tables to support the above-mentioned additional instructions.
4. Collaborated to complete the decoder truth tables and used Microsoft Excel to draw them.
5. By collaborating with each other, imported the given base source files into Vivado and observed the output waveforms after the simulation.
6. Worked together to devise the test plan to add the required instructions to the already existing single-cycle MIPS processor.
7. Collaborated in extracting the memfile.dat file from the MARS simulator using Dump to memory option.

# CONCLUSION:

In conclusion, we end the report by extending the initial version of the single-cycle MIPS processor to handle more instructions. We also were able to test the logic that we wrote by executing a factorial program and after successful simulation, we were able draw datapath block diagram (using Visio) and control-unit decoder truth tables (using MS Excel) for the modified processor.

# 

# APPENDIX

## Datapath of the Enhanced (shown in red color) Single-Cycle MIPS Processor:

Diagram, schematic

Description automatically generated

## Source Code – tb\_mips\_top.v (TestBench module for the design)

*module tb\_mips\_top;*

*reg clk;*

*reg rst;*

*wire we\_dm;*

*wire [31:0] pc\_current;*

*wire [31:0] instr;*

*wire [31:0] alu\_out;*

*wire [31:0] wd\_dm;*

*wire [31:0] rd\_dm;*

*wire [31:0] DONT\_USE;*

*integer i;*

*mips\_top DUT (*

*.clk (clk),*

*.rst (rst),*

*.we\_dm (we\_dm),*

*.ra3 (5'h0),*

*.pc\_current (pc\_current),*

*.instr (instr),*

*.alu\_out (alu\_out),*

*.wd\_dm (wd\_dm),*

*.rd\_dm (rd\_dm),*

*.rd3 (DONT\_USE)*

*);*

*task tick;*

*begin*

*clk = 1'b0; #5;*

*clk = 1'b1; #5;*

*end*

*endtask*

*task reset;*

*begin*

*rst = 1'b0; #5;*

*rst = 1'b1; #5;*

*rst = 1'b0;*

*end*

*endtask*

*initial begin*

*reset;*

*for(i = 0; i < 13; i = i + 1)*

*begin*

*tick;*

*end*

*reset;*

*while(pc\_current != 32'h58) tick;*

*$finish;*

*end*

*endmodule*

## Source Code – mips\_top.v (Top module for the design)

*module mips\_top (*

*input wire clk,*

*input wire rst,*

*input wire [4:0] ra3,*

*output wire we\_dm,*

*output wire [31:0] pc\_current,*

*output wire [31:0] instr,*

*output wire [31:0] alu\_out,*

*output wire [31:0] wd\_dm,*

*output wire [31:0] rd\_dm,*

*output wire [31:0] rd3*

*);*

*wire [31:0] DONT\_USE;*

*mips mips (*

*.clk (clk),*

*.rst (rst),*

*.ra3 (ra3),*

*.instr (instr),*

*.rd\_dm (rd\_dm),*

*.we\_dm (we\_dm),*

*.pc\_current (pc\_current),*

*.alu\_out (alu\_out),*

*.wd\_dm (wd\_dm),*

*.rd3 (rd3)*

*);*

*imem imem (*

*.a (pc\_current[7:2]),*

*.y (instr)*

*);*

*dmem dmem (*

*.clk (clk),*

*.we (we\_dm),*

*.a (alu\_out[7:2]),*

*.d (wd\_dm),*

*.q (rd\_dm),*

*.rst (rst)*

*);*

*endmodule*

## Source Code – mips.v (Top module for the datapath and controlpath)

*module mips (*

*input wire clk,*

*input wire rst,*

*input wire [4:0] ra3,*

*input wire [31:0] instr,*

*input wire [31:0] rd\_dm,*

*output wire we\_dm,*

*output wire [31:0] pc\_current,*

*output wire [31:0] alu\_out,*

*output wire [31:0] wd\_dm,*

*output wire [31:0] rd3*

*);*

*wire branch;*

*wire jump;*

*wire reg\_dst;*

*wire we\_reg;*

*wire alu\_src;*

*wire dm2reg;*

*wire [3:0] alu\_ctrl;*

*wire hilo\_we;*

*wire [1:0] hilo\_mux\_ctrl;*

*wire jr\_mux\_ctrl;*

*wire jal\_wd\_mux\_sel;*

*wire jal\_wa\_mux\_sel;*

*datapath dp (*

*.clk (clk),*

*.rst (rst),*

*.branch (branch),*

*.jump (jump),*

*.reg\_dst (reg\_dst),*

*.we\_reg (we\_reg),*

*.alu\_src (alu\_src),*

*.dm2reg (dm2reg),*

*.alu\_ctrl (alu\_ctrl),*

*.ra3 (ra3),*

*.instr (instr),*

*.rd\_dm (rd\_dm),*

*.pc\_current (pc\_current),*

*.alu\_out (alu\_out),*

*.wd\_dm (wd\_dm),*

*.rd3 (rd3),*

*.hilo\_we (hilo\_we),*

*.hilo\_mux\_ctrl (hilo\_mux\_ctrl),*

*.jr\_mux\_ctrl (jr\_mux\_ctrl),*

*.jal\_wa\_mux\_sel (jal\_wa\_mux\_sel),*

*.jal\_wd\_mux\_sel (jal\_wd\_mux\_sel)*

*);*

*controlunit cu (*

*.opcode (instr[31:26]),*

*.funct (instr[5:0]),*

*.branch (branch),*

*.jump (jump),*

*.reg\_dst (reg\_dst),*

*.we\_reg (we\_reg),*

*.alu\_src (alu\_src),*

*.we\_dm (we\_dm),*

*.dm2reg (dm2reg),*

*.alu\_ctrl (alu\_ctrl),*

*.hilo\_we (hilo\_we),*

*.hilo\_mux\_ctrl (hilo\_mux\_ctrl),*

*.jr\_mux\_ctrl (jr\_mux\_ctrl),*

*.jal\_wa\_mux\_sel (jal\_wa\_mux\_sel),*

*.jal\_wd\_mux\_sel (jal\_wd\_mux\_sel)*

*);*

*endmodule*

## Source Code – datapath.v (Top module for the datapath)

*module datapath (*

*input wire clk,*

*input wire rst,*

*input wire branch,*

*input wire jump,*

*input wire reg\_dst,*

*input wire we\_reg,*

*input wire alu\_src,*

*input wire dm2reg,*

*input wire [3:0] alu\_ctrl,*

*input wire [4:0] ra3,*

*input wire [31:0] instr,*

*input wire [31:0] rd\_dm,*

*//New Additions for Enhanced Single-Cycle MIPS Processor*

*input wire hilo\_we,*

*input wire [1:0] hilo\_mux\_ctrl,*

*input wire jr\_mux\_ctrl,*

*input wire jal\_wd\_mux\_sel,*

*input wire jal\_wa\_mux\_sel,*

*output wire [31:0] pc\_current,*

*output wire [31:0] alu\_out,*

*output wire [31:0] wd\_dm,*

*output wire [31:0] rd3*

*);*

*wire [4:0] rf\_wa;*

*wire pc\_src;*

*wire [31:0] pc\_plus4;*

*wire [31:0] pc\_pre;*

*wire [31:0] pc\_next\_1, pc\_next\_final;*

*wire [31:0] sext\_imm;*

*wire [31:0] ba;*

*wire [31:0] bta;*

*wire [31:0] jta;*

*wire [31:0] alu\_pa;*

*wire [31:0] alu\_pb;*

*wire [31:0] wd\_rf;*

*wire zero;*

*//New Additions for Enhanced Single-Cycle MIPS Processor*

*wire [31:0] wd\_rf\_1, wd\_rf\_out;*

*wire [31:0] mult\_hi, mult\_lo;*

*wire [31:0] hi\_out, lo\_out;*

*wire [31:0] rd1\_out, rd2\_out;*

*wire [31:0] hilo\_mux\_out;*

*wire [4:0] rf\_wa\_mux\_out;*

*wire [31:0] jal\_wd\_mux\_out;*

*wire [4:0] jal\_wa\_mux\_out;*

*assign pc\_src = branch & zero;*

*assign ba = {sext\_imm[29:0], 2'b00};*

*assign jta = {pc\_plus4[31:28], instr[25:0], 2'b00};*

*//New Additions for Enhanced Single-Cycle MIPS Processor*

*assign wd\_dm = rd2\_out;*

*// --- PC Logic --- //*

*dreg pc\_reg (*

*.clk (clk),*

*.rst (rst),*

*.d (pc\_next\_final),*

*.q (pc\_current)*

*);*

*adder pc\_plus\_4 (*

*.a (pc\_current),*

*.b (32'd4),*

*.y (pc\_plus4)*

*);*

*adder pc\_plus\_br (*

*.a (pc\_plus4),*

*.b (ba),*

*.y (bta)*

*);*

*//PC Mux for Branch Instructions*

*mux2 #(32) pc\_src\_mux (*

*.sel (pc\_src),*

*.a (pc\_plus4),*

*.b (bta),*

*.y (pc\_pre)*

*);*

*//PC Mux for Jump Instructions*

*mux2 #(32) pc\_jmp\_mux (*

*.sel (jump),*

*.a (pc\_pre),*

*.b (jta),*

*.y (pc\_next\_1)*

*);*

*// --- RF Logic --- //*

*mux2 #(5) rf\_wa\_mux (*

*.sel (reg\_dst),*

*.a (instr[20:16]),*

*.b (instr[15:11]),*

*.y (rf\_wa\_mux\_out)*

*);*

*regfile rf (*

*.clk (clk),*

*.we (we\_reg),*

*.ra1 (instr[25:21]),*

*.ra2 (instr[20:16]),*

*.ra3 (ra3),*

*.wa (jal\_wa\_mux\_out),*

*.wd (jal\_wd\_mux\_out),*

*.rd1 (rd1\_out),*

*.rd2 (rd2\_out),*

*.rd3 (rd3),*

*.rst (rst)*

*);*

*signext se (*

*.a (instr[15:0]),*

*.y (sext\_imm)*

*);*

*// --- ALU Logic --- //*

*mux2 #(32) alu\_pb\_mux (*

*.sel (alu\_src),*

*.a (rd2\_out),*

*.b (sext\_imm),*

*.y (alu\_pb)*

*);*

*alu alu (*

*.op (alu\_ctrl),*

*.a (rd1\_out),*

*.b (alu\_pb),*

*.zero (zero),*

*.y (alu\_out),*

*.shamt (instr[10:6])*

*);*

*// --- MEM Logic --- //*

*mux2 #(32) rf\_wd\_mux (*

*.sel (dm2reg),*

*.a (alu\_out),*

*.b (rd\_dm),*

*.y (wd\_rf\_1)*

*);*

*//New Additions for Enhanced Single-Cycle MIPS Processor*

*// --- JR Logic --- //*

*mux2 #(32) jr\_mux (*

*.sel (jr\_mux\_ctrl),*

*.a (pc\_next\_1),*

*.b (rd1\_out),*

*.y (pc\_next\_final)*

*);*

*// --- HI/LO Mux --- //*

*mux4 #(32) hilo\_mux (*

*.sel (hilo\_mux\_ctrl),*

*.a (wd\_rf\_1),*

*.b (lo\_out),*

*.c (hi\_out),*

*.y (hilo\_mux\_out)*

*);*

*// --- Hi and Lo Registers --- //*

*HiLo\_reg #(32) hi\_lo\_reg (*

*.clk (clk),*

*.hi (mult\_hi),*

*.lo (mult\_lo),*

*.rst (rst),*

*.we (hilo\_we),*

*.hi\_out (hi\_out),*

*.lo\_out (lo\_out)*

*);*

*mult\_inf #(32) mult (*

*.a (rd1\_out),*

*.b (rd2\_out),*

*.out ({mult\_hi, mult\_lo})*

*);*

*mux2 #(32) jal\_wd\_mux (*

*.a (hilo\_mux\_out),*

*.b (pc\_plus4),*

*.y (jal\_wd\_mux\_out),*

*.sel (jal\_wd\_mux\_sel)*

*);*

*mux2 #(5) jal\_wa\_mux (*

*.sel (jal\_wa\_mux\_sel),*

*.a (rf\_wa\_mux\_out),*

*.b (5'd31),*

*.y (jal\_wa\_mux\_out)*

*);*

*endmodule*

## Source Code – adder.v (Module for the adder unit)

*module adder (*

*input wire [31:0] a,*

*input wire [31:0] b,*

*output wire [31:0] y*

*);*

*assign y = a + b;*

*endmodule*

## Source Code – alu.v (Module for the ALU unit)

*module alu (*

*input wire [3:0] op,*

*input wire [31:0] a,*

*input wire [31:0] b,*

*input wire [4:0] shamt,*

*output wire zero,*

*output reg [31:0] y, hi, lo*

*);*

*assign zero = (y == 0);*

*always @ (op, a, b) begin*

*case (op)*

*4'b0000: y <= a & b;*

*4'b0001: y <= a | b;*

*4'b0010: y <= a + b;*

*4'b0110: y <= a - b;*

*4'b0111: y <= (a < b) ? 1 : 0;*

*4'b1001: y <= b << shamt;*

*4'b1010: y <= b >> shamt;*

*endcase*

*end*

*endmodule*

## Source Code – dreg.v (Module for the Program Counter unit)

*module dreg # (parameter WIDTH = 32) (*

*input wire clk,*

*input wire rst,*

*input wire [WIDTH-1:0] d,*

*output reg [WIDTH-1:0] q*

*);*

*always @ (posedge clk, posedge rst) begin*

*if (rst) q <= 0;*

*else q <= d;*

*end*

*endmodule*

## Source Code – mux2.v (Module for the 2x1 Multiplexer unit)

*module mux2 #(parameter WIDTH = 8) (*

*input wire sel,*

*input wire [WIDTH-1:0] a,*

*input wire [WIDTH-1:0] b,*

*output wire [WIDTH-1:0] y*

*);*

*assign y = (sel) ? b : a;*

*endmodule*

## Source Code – regfile.v (Module for the Register File)

*module regfile (*

*input wire clk,*

*input wire we,*

*input wire [4:0] ra1,*

*input wire [4:0] ra2,*

*input wire [4:0] ra3,*

*input wire [4:0] wa,*

*input wire [31:0] wd,*

*output wire [31:0] rd1,*

*output wire [31:0] rd2,*

*output wire [31:0] rd3,*

*input wire rst*

*);*

*reg [31:0] rf [0:31];*

*integer n;*

*initial begin*

*for (n = 0; n < 32; n = n + 1) rf[n] = 32'h0;*

*rf[29] = 32'h100; // Initialze $sp*

*end*

*always @ (posedge clk, posedge rst) begin*

*if (rst) begin*

*for (n = 0; n < 32; n = n + 1) rf[n] = 32'h0;*

*rf[29] = 32'h100; // Initialze $sp*

*end*

*else if (we) rf[wa] <= wd;*

*end*

*assign rd1 = (ra1 == 0) ? 0 : rf[ra1];*

*assign rd2 = (ra2 == 0) ? 0 : rf[ra2];*

*assign rd3 = (ra3 == 0) ? 0 : rf[ra3];*

*endmodule*

## Source Code – signext.v (Module for the Sign Extending Unit)

*module signext (*

*input wire [15:0] a,*

*output wire [31:0] y*

*);*

*assign y = {{16{a[15]}}, a};*

*endmodule*

## Source Code – mux4.v (Module for the 4x1 Multiplexer unit)

*`timescale 1ns / 1ps*

*//////////////////////////////////////////////////////////////////////////////////*

*// Company:*

*// Engineer: Tirumala Saiteja Goruganthu*

*//*

*// Create Date: 11/01/2022 08:08:29 PM*

*// Design Name:*

*// Module Name: mux4*

*// Project Name:*

*// Target Devices:*

*// Tool Versions:*

*// Description:*

*//*

*// Dependencies:*

*//*

*// Revision:*

*// Revision 0.01 - File Created*

*// Additional Comments:*

*//*

*//////////////////////////////////////////////////////////////////////////////////*

*module mux4 #(parameter WIDTH = 8) (*

*input wire [1:0] sel,*

*input wire [WIDTH-1:0] a,*

*input wire [WIDTH-1:0] b,*

*input wire [WIDTH-1:0] c,*

*input wire [WIDTH-1:0] d,*

*output reg [WIDTH-1:0] y*

*);*

*always @ (\*)*

*begin*

*case (sel)*

*2'b00: y <= a;*

*2'b01: y <= b;*

*2'b10: y <= c;*

*2'b11: y <= d;*

*endcase*

*end*

*endmodule*

## Source Code – mult\_inf.v (Module for the 32-bit Multiplier unit)

*`timescale 1ns / 1ps*

*//////////////////////////////////////////////////////////////////////////////////*

*// Company:*

*// Engineer: Tirumala Saiteja Goruganthu*

*//*

*// Create Date: 11/01/2022 08:47:11 PM*

*// Design Name:*

*// Module Name: mult\_inf*

*// Project Name:*

*// Target Devices:*

*// Tool Versions:*

*// Description:*

*//*

*// Dependencies:*

*//*

*// Revision:*

*// Revision 0.01 - File Created*

*// Additional Comments:*

*//*

*//////////////////////////////////////////////////////////////////////////////////*

*module mult\_inf #(parameter WIDTH = 32)(*

*input wire [WIDTH - 1:0] a, b,*

*output reg [2\*WIDTH - 1:0] out*

*);*

*always @ (a, b) begin*

*out <= a \* b;*

*end*

*endmodule*

## Source Code – HiLo\_reg.v (Module for the Hi-Lo storage register)

*`timescale 1ns / 1ps*

*//////////////////////////////////////////////////////////////////////////////////*

*// Company:*

*// Engineer: Tirumala Saiteja Goruganthu*

*//*

*// Create Date: 11/01/2022 08:21:34 PM*

*// Design Name:*

*// Module Name: HiLo\_reg*

*// Project Name:*

*// Target Devices:*

*// Tool Versions:*

*// Description:*

*//*

*// Dependencies:*

*//*

*// Revision:*

*// Revision 0.01 - File Created*

*// Additional Comments:*

*//*

*//////////////////////////////////////////////////////////////////////////////////*

*module HiLo\_reg# (parameter WIDTH = 32) (*

*input wire clk, rst, we,*

*input wire [WIDTH - 1:0] hi, lo,*

*output reg [WIDTH - 1:0] hi\_out, lo\_out*

*);*

*always @ (posedge clk, posedge rst)*

*begin*

*if (rst) {hi\_out, lo\_out} <= 0;*

*else if (we) {hi\_out, lo\_out} <= {hi,lo};*

*else {hi\_out, lo\_out} <= {hi\_out, lo\_out};*

*end*

*endmodule*

## Source Code – controlunit.v (Module for the Control unit)

*module controlunit (*

*input wire [5:0] opcode,*

*input wire [5:0] funct,*

*output wire branch,*

*output wire jump,*

*output wire reg\_dst,*

*output wire we\_reg,*

*output wire alu\_src,*

*output wire we\_dm,*

*output wire dm2reg,*

*output wire [3:0] alu\_ctrl,*

*output wire [1:0] hilo\_mux\_ctrl,*

*output wire hilo\_we,*

*output wire jr\_mux\_ctrl,*

*output wire jal\_wd\_mux\_sel,*

*output wire jal\_wa\_mux\_sel*

*);*

*wire [1:0] alu\_op;*

*wire [1:0] hilo\_mux\_temp;*

*maindec md (*

*.opcode (opcode),*

*.branch (branch),*

*.jump (jump),*

*.reg\_dst (reg\_dst),*

*.we\_reg (we\_reg),*

*.alu\_src (alu\_src),*

*.we\_dm (we\_dm),*

*.dm2reg (dm2reg),*

*.alu\_op (alu\_op),*

*.jal\_wa\_mux\_sel (jal\_wa\_mux\_sel),*

*.jal\_wd\_mux\_sel (jal\_wd\_mux\_sel)*

*);*

*auxdec ad (*

*.alu\_op (alu\_op),*

*.funct (funct),*

*.alu\_ctrl (alu\_ctrl),*

*.hilo\_mux\_ctrl (hilo\_mux\_temp),*

*.hilo\_we (hilo\_we),*

*.jr\_mux\_ctrl (jr\_mux\_ctrl)*

*);*

*assign hilo\_mux\_ctrl = (hilo\_mux\_temp) ? hilo\_mux\_temp : 2'b0;*

*endmodule*

## Source Code – maindec.v (Module for the Main decoder)

*module maindec (*

*input wire [5:0] opcode,*

*output wire branch,*

*output wire jump,*

*output wire reg\_dst,*

*output wire we\_reg,*

*output wire alu\_src,*

*output wire we\_dm,*

*output wire dm2reg,*

*output wire [1:0] alu\_op,*

*output wire jal\_wa\_mux\_sel,*

*output wire jal\_wd\_mux\_sel*

*);*

*reg [10:0] ctrl;*

*assign {branch, jump, reg\_dst, we\_reg, alu\_src, we\_dm, dm2reg, alu\_op, jal\_wa\_mux\_sel, jal\_wd\_mux\_sel} = ctrl;*

*always @ (opcode) begin*

*case (opcode)*

*6'b00\_0000: ctrl = 11'b0\_0\_1\_1\_0\_0\_0\_10\_0\_0; // R-type*

*6'b00\_1000: ctrl = 11'b0\_0\_0\_1\_1\_0\_0\_00\_0\_0; // ADDI*

*6'b00\_0100: ctrl = 11'b1\_0\_0\_0\_0\_0\_0\_01\_0\_0; // BEQ*

*6'b00\_0010: ctrl = 11'b0\_1\_0\_0\_0\_0\_0\_00\_0\_0; // J*

*6'b10\_1011: ctrl = 11'b0\_0\_0\_0\_1\_1\_0\_00\_0\_0; // SW*

*6'b10\_0011: ctrl = 11'b0\_0\_0\_1\_1\_0\_1\_00\_0\_0; // LW*

*6'b00\_0011: ctrl = 11'b0\_1\_0\_1\_0\_0\_0\_00\_1\_1; // JAL //Enhanced*

*default: ctrl = 11'bx\_x\_x\_0\_x\_0\_x\_xx\_x\_x;*

*endcase*

*end*

*endmodule*

## Source Code – auxdec.v (Module for the Auxiliary decoder)

*module auxdec (*

*input wire [1:0] alu\_op,*

*input wire [5:0] funct,*

*output wire [3:0] alu\_ctrl,*

*output wire [1:0] hilo\_mux\_ctrl,*

*output wire hilo\_we,*

*output wire jr\_mux\_ctrl*

*);*

*reg [7:0] ctrl;*

*assign {alu\_ctrl, hilo\_mux\_ctrl, hilo\_we, jr\_mux\_ctrl} = ctrl;*

*always @ (alu\_op, funct) begin*

*case (alu\_op)*

*2'b00: ctrl = 8'b0010\_00\_0\_0; // ADD*

*2'b01: ctrl = 8'b0110\_00\_0\_0; // SUB*

*default: case (funct)*

*6'b10\_0100: ctrl = 8'b0000\_00\_0\_0; // AND*

*6'b10\_0101: ctrl = 8'b0001\_00\_0\_0; // OR*

*6'b10\_0000: ctrl = 8'b0010\_00\_0\_0; // ADD*

*6'b10\_0010: ctrl = 8'b0110\_00\_0\_0; // SUB*

*6'b10\_1010: ctrl = 8'b0111\_00\_0\_0; // SLT*

*6'b01\_1001: ctrl = 8'bxxxx\_00\_1\_0; // MULTU*

*6'b01\_0000: ctrl = 8'b0000\_11\_0\_0; // MFHI*

*6'b01\_0010: ctrl = 8'b0000\_01\_0\_0; // MFLO*

*6'b00\_0000: ctrl = 8'b1001\_00\_0\_0; // SLL*

*6'b00\_0010: ctrl = 8'b1010\_00\_0\_0; // SRL*

*6'b00\_1000: ctrl = 8'b0000\_00\_0\_1; // JR*

*default: ctrl = 8'bxxxx\_xx\_x\_x;*

*endcase*

*endcase*

*end*

*endmodule*

## Source Code – imem.v (Module for the Instruction memory)

*module imem (*

*input wire [5:0] a,*

*output wire [31:0] y*

*);*

*reg [31:0] rom [0:63];*

*initial begin*

*$readmemh ("H:\\Masters\\Semester1\\CMPE200\\Assignment6\\memfile.dat", rom);*

*end*

*assign y = rom[a];*

*endmodule*

## Source Code – dmem.v (Module for the Data memory)

*module dmem (*

*input wire clk,*

*input wire we,*

*input wire [5:0] a,*

*input wire [31:0] d,*

*output wire [31:0] q,*

*input wire rst*

*);*

*reg [31:0] ram [0:63];*

*integer n;*

*initial begin*

*for (n = 0; n < 64; n = n + 1) ram[n] = 32'hFFFFFFFF;*

*end*

*always @ (posedge rst) begin*

*end*

*always @ (posedge clk, posedge rst) begin*

*if (rst) for (n = 0; n < 64; n = n + 1) ram[n] = 32'hFFFFFFFF;*

*else if (we) ram[a] <= d;*

*end*

*assign q = ram[a];*

*endmodule*

## Source Code – memfile.dat (Memory dump for factorial.asm in hexadecimal format)

201d0030

20040004

0c000005

00408020

08000016

23bdfff8

afa40004

afbf0000

20080002

0088402a

11000003

20020001

23bd0008

03e00008

2084ffff

0c000005

8fbf0000

8fa40004

23bd0008

00820019

00001012

03e00008