Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

SCHOOL OF COMPUTING
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Academic Year 2020-21 : Winter Semester

1151CS118 - MICROPROCESSORS AND CONTROLLERS

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Department of CSE

Slot No : G1,S4,S5

COURSE CONTENT

UNIT I- THE 8086 MICROPROCESSOR (9)

Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

UNIT II 8086 SYSTEM BUS STRUCTURE (9)

8086 signals – Basic configurations – System bus timing –System design using 8086 – IO programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, closely coupled and loosely Coupled configurations – Introduction to Pentium family processors.

UNIT III 8051 ARCHITECTURE (9)

Architecture – memory organization –I/O ports and circuits-Timers - Interrupts –serial communication – Addressing modes –Instruction set.

COURSE CONTENT

UNIT IV PERIPHERAL DEVICES (10)

Parallel peripheral Interface (8255) - Timer / Counter (8253) - Keyboard and Display Controller (8279) - USART (8251) - Interrupt Controller (8259)- DMA Controller (8237).

UNITVMICROCONTROLLER APPLICATIONS & ADVANCED PROCESSOR (8)

Temperature control system- Motor speed control system – Traffic light System – Elevator system - Introduction to architecture of PIC, ARM, ATMEGA processors

Total: 45 Periods

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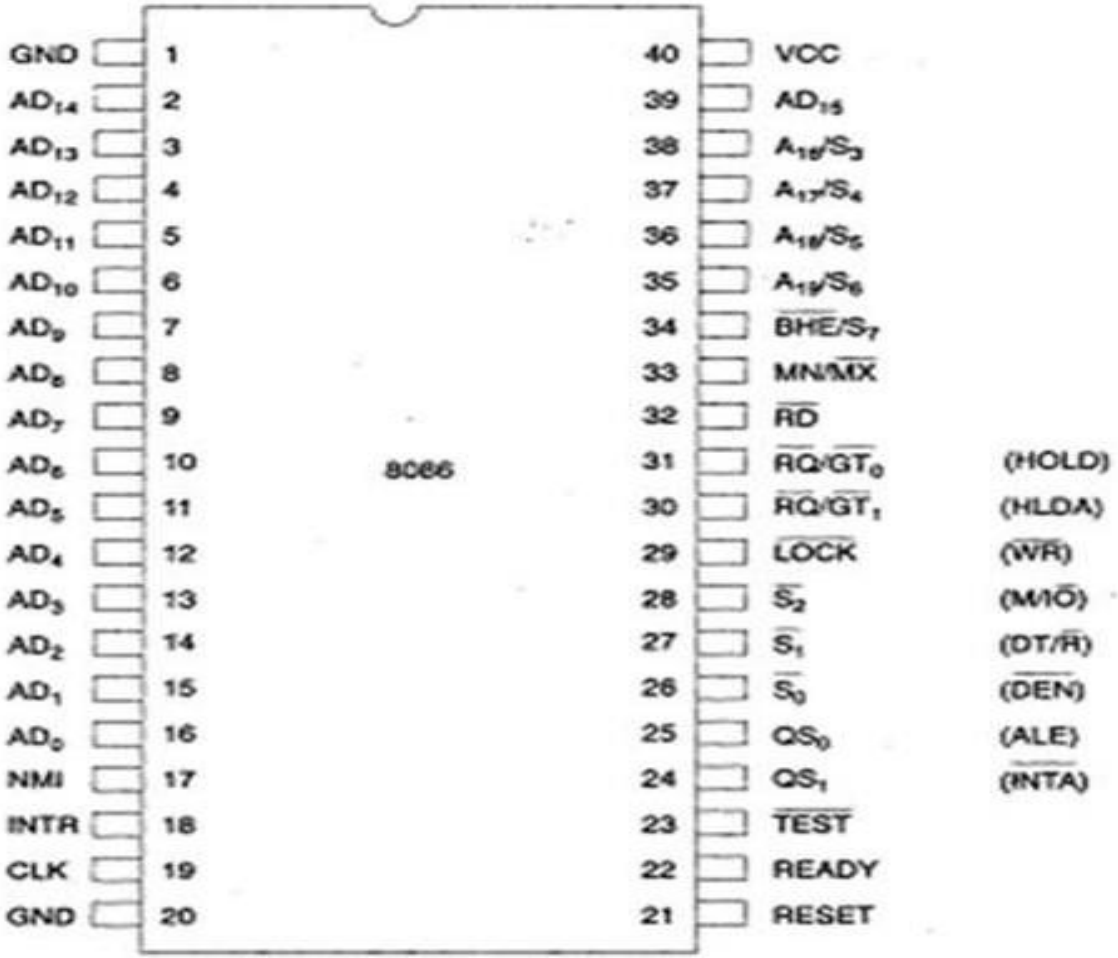
Pins and Signals

8086 Pin Diagram



8086 Signals

Power supply and frequency signals

- V_{CC} pin 40
- V_{SS} pin 1 and 20 - Ground

Clock signal

- Pin-19.
- Frequency - 5MHz, 8MHz and 10MHz.

Address/data bus

- AD0-AD15
- 16 address/data bus.
- AD0-AD7 - low order byte data
- AD8 - AD15 - higher order byte data.
- First clock cycle - 16-bit address
- 16-bit data.

Address/status bus

- A16-A19/S3-S6.
- 4 address/status buses.
- First clock cycle - 4-bit address
- carries status signals.

S7/BHE

- BHE -Bus High Enable.
- pin 34
- Transfer of data using data bus D8-D15.
- Low - first clock cycle, thereafter it is active.

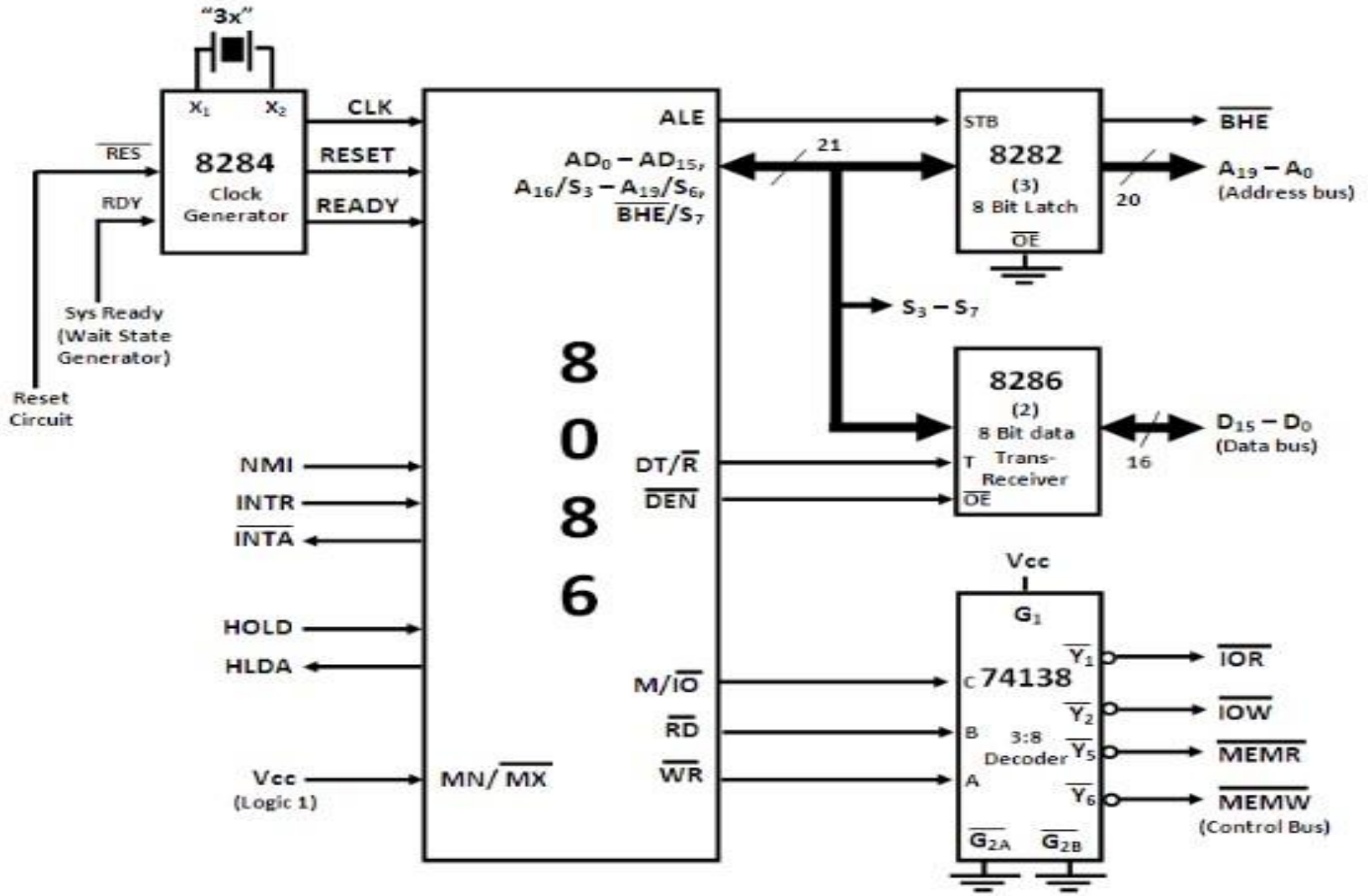
Read(RD)

- pin 32
- read signal -Read operation.

Minimum Mode & Maximum Mode

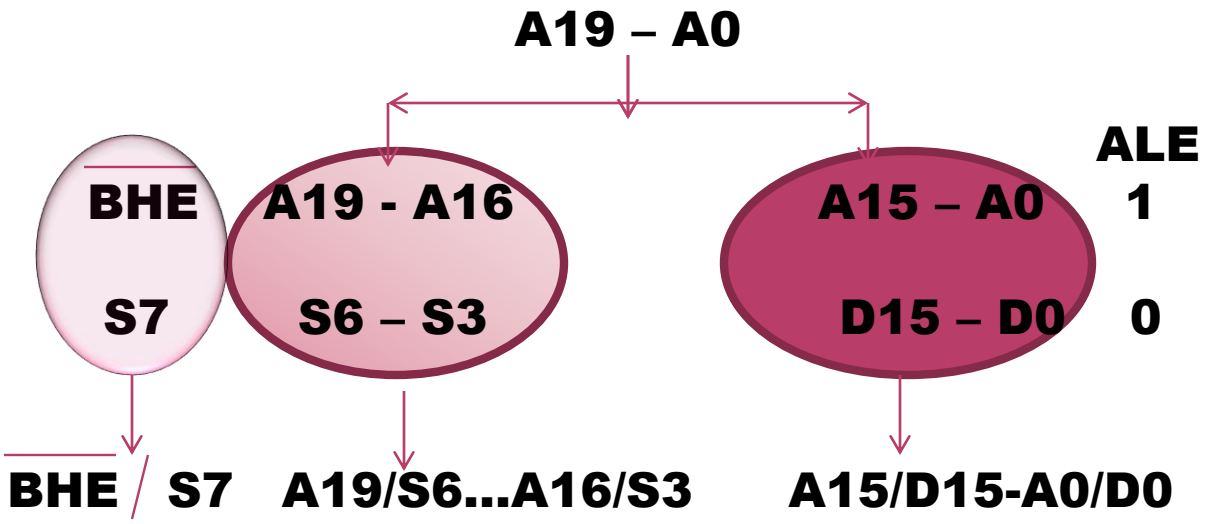
- Minimum Mode
  - One Processor
- Maximum Mode
  - Multiple Processors

Block Diagram for Minimum Mode



- What is Multiplexing? Advantages of Multiplexing?
- Demulti plexing the addressing and data bus
- Memory Banking
  - Odd Banking
    - Higher Bank(BHE)
  - Even Banking
    - Lower Bank(A0)

Minimum Mode



S4	S3	SEGMENT
0	0	EXTRA SEGMENT
0	1	STACK SEGMENT
1	0	CODE SEGMENT
1	1	DATA SEGMENT

MINIMUM MODE

S5=0 -> IF=0
1 -> IF=1

S6=0 -> 8086 BUS
1 -> OTHER

S7 -> RESERVED

•Data Trans – Receiver

•8286 – Data Trans receiver
•$\overline{DEN}$ – Data Enable
•Actively Low signal
•Active when 0

DEN	DT/R	Action
1	X	
0	1	Transmits the data
0	0	Receives the data

Decoder

- Decoder 74138
- Input output ratio - 3:8

000	Y0
001	Y1
010	Y2
011	Y3
100	Y4
101	Y5
110	Y6
111	Y7

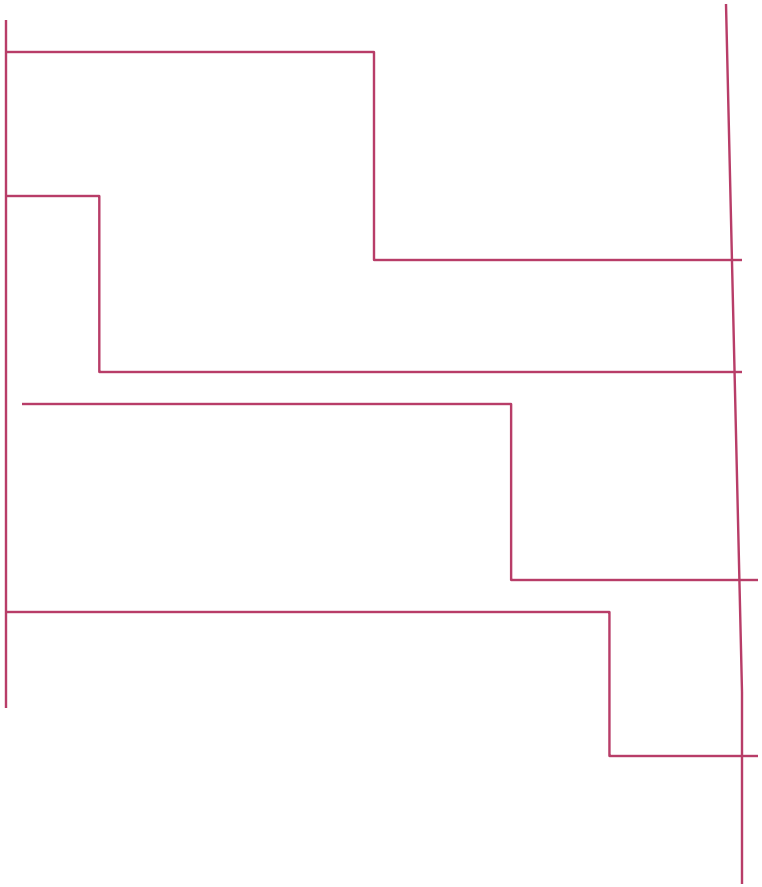
Control Bus

Table 2.5 Read write cycle

M/IO	RD	WR	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

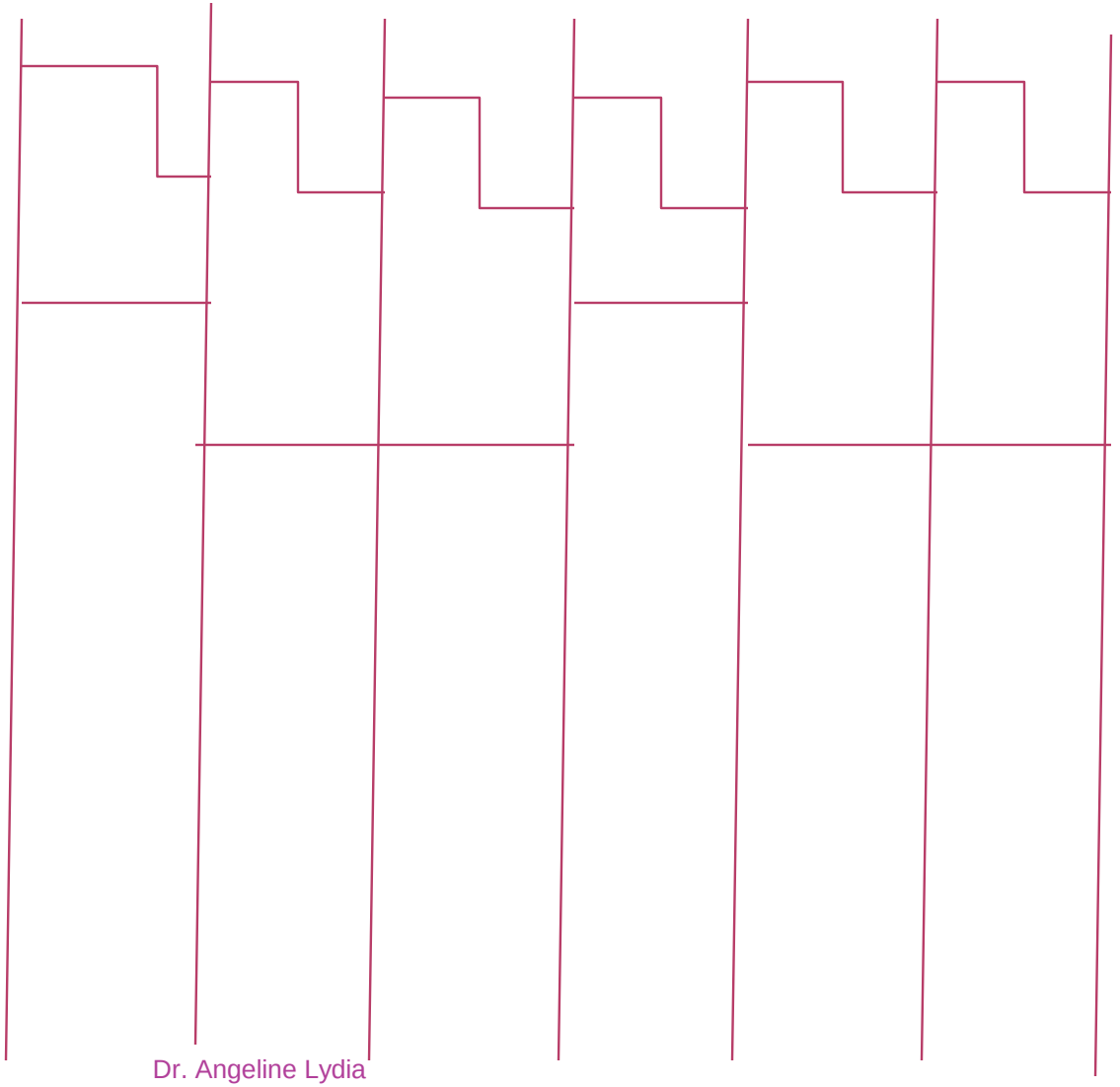
Clock

- 8284 Clock generator
- 33% duty cycle



X1,x2

33% duty cycle



Timing Diagram

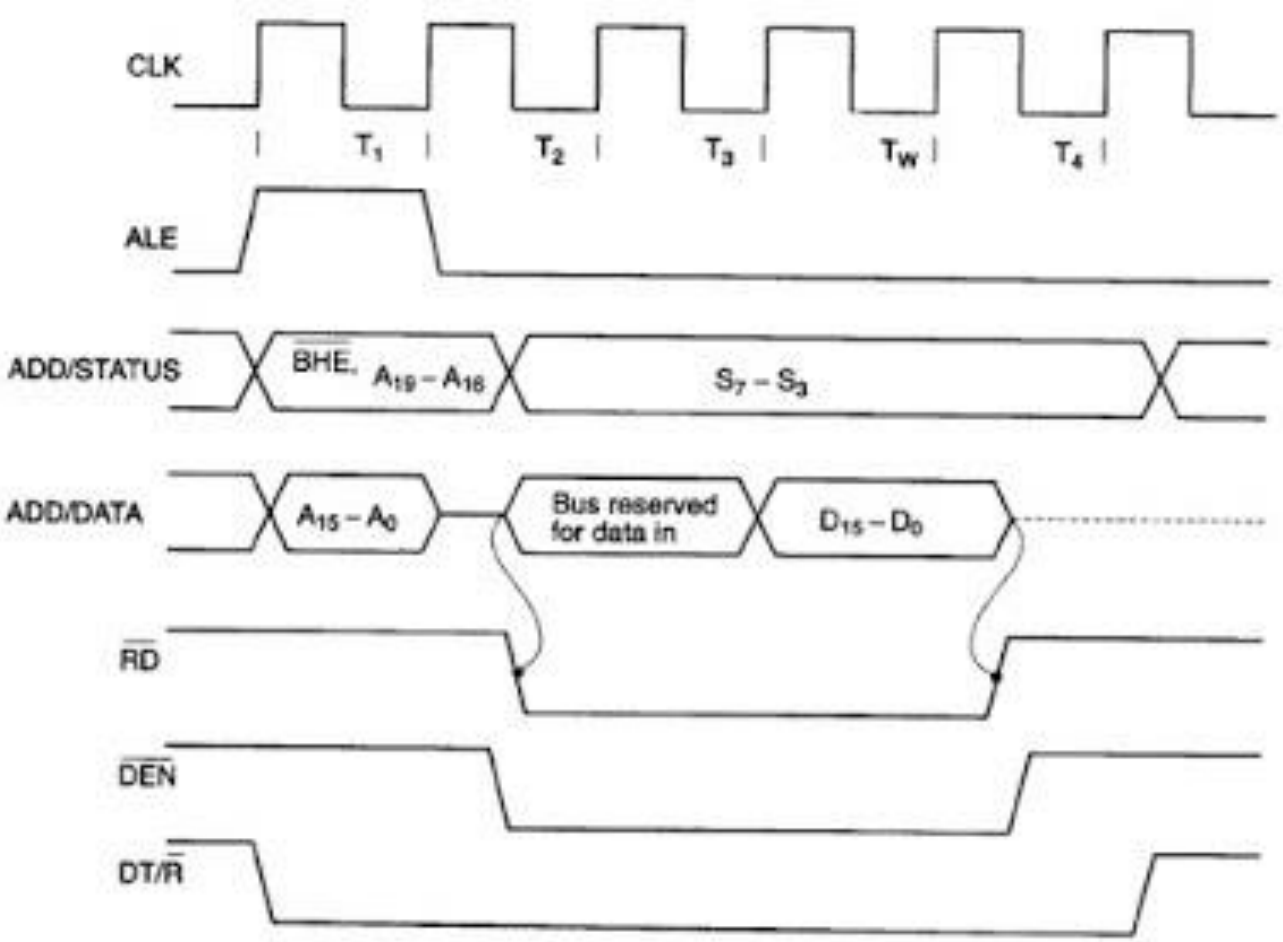
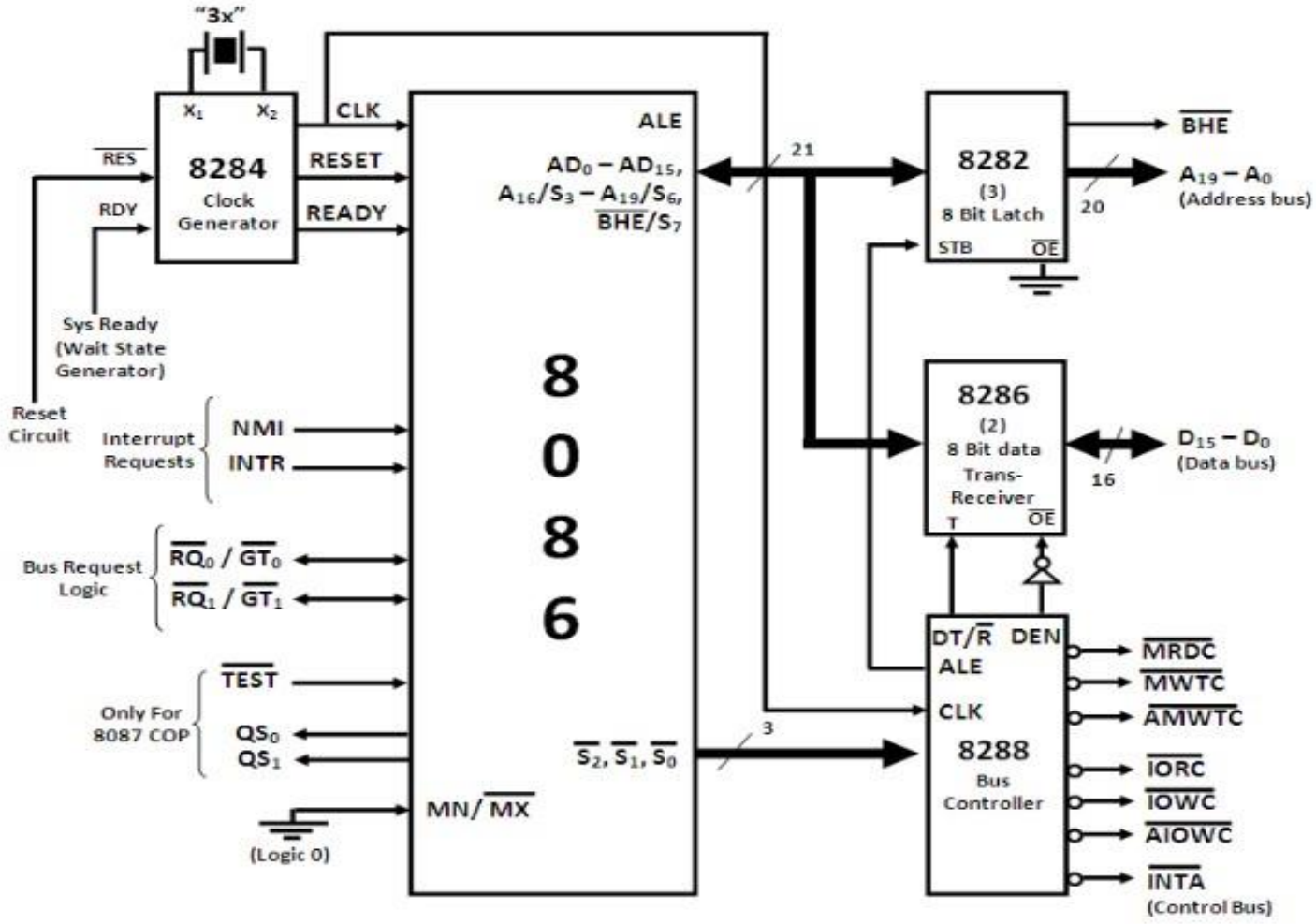
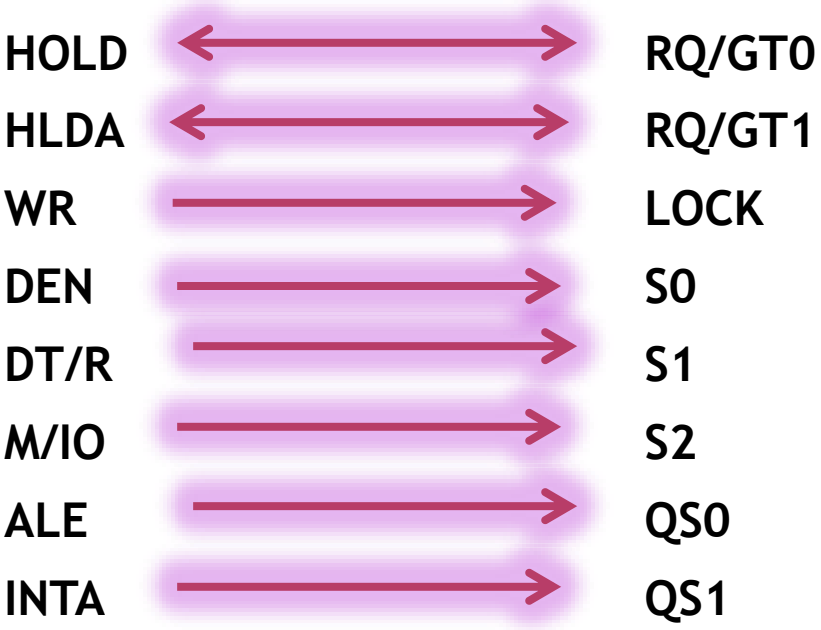


Fig. 1.9(a) *Read Cycle Timing Diagram for Minimum Mode*

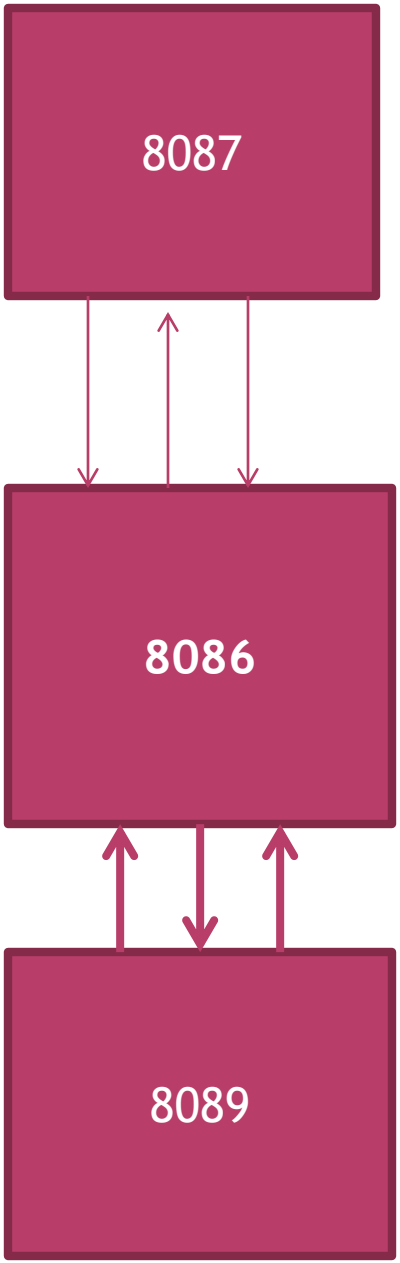
Maximum Mode of 8086

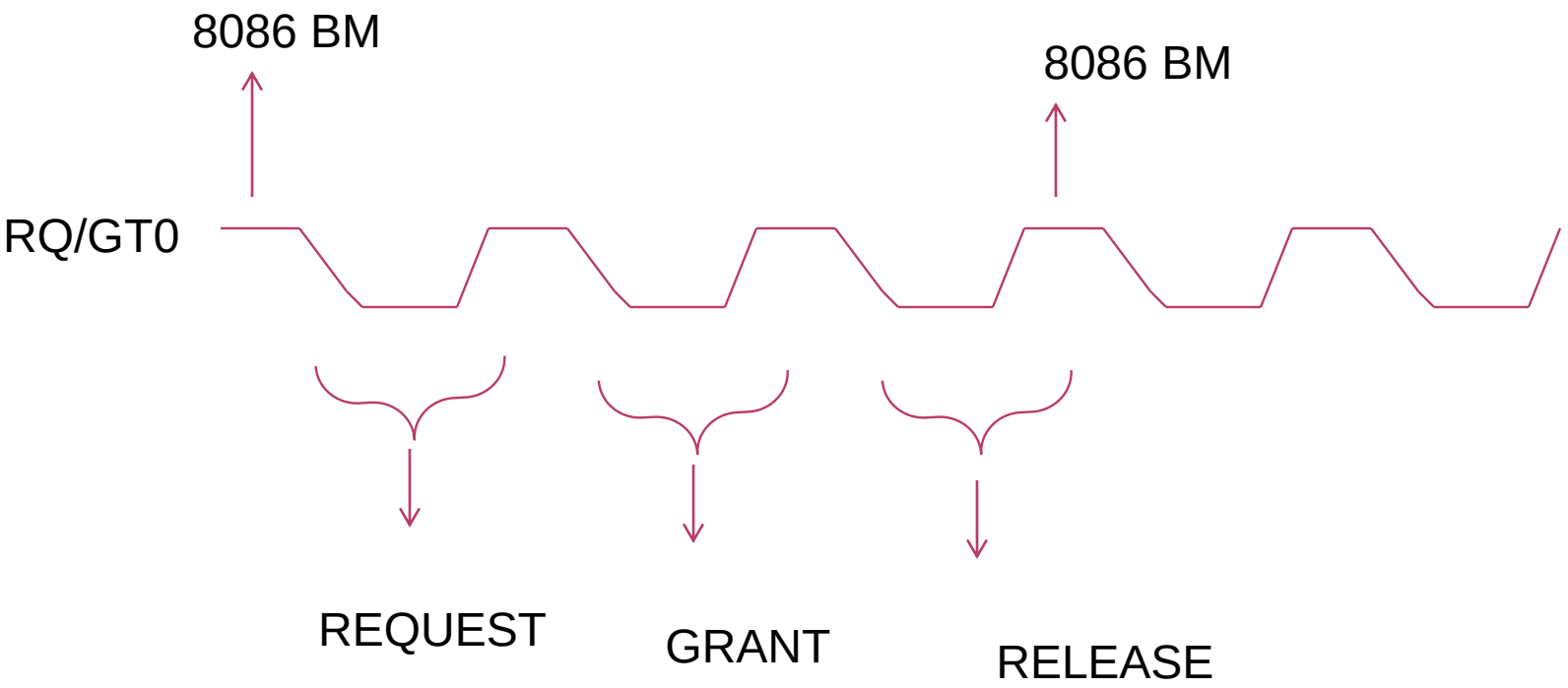




Maximum Mode Signals

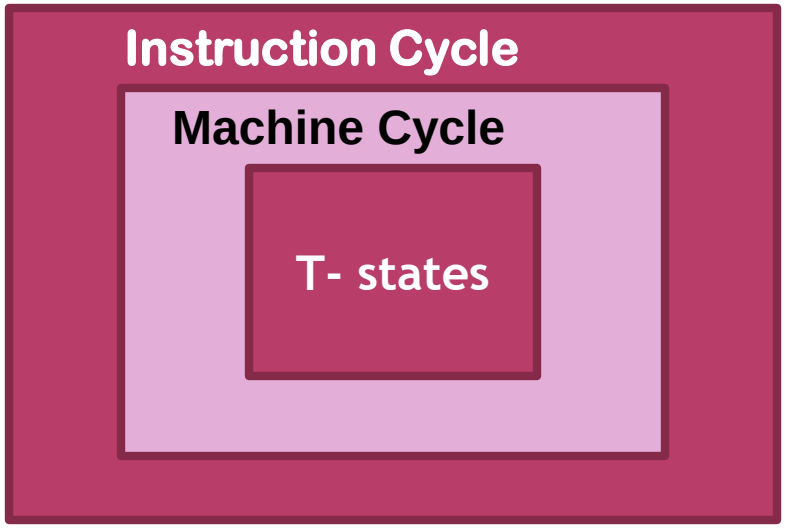
Multiple Processors connected to 8086

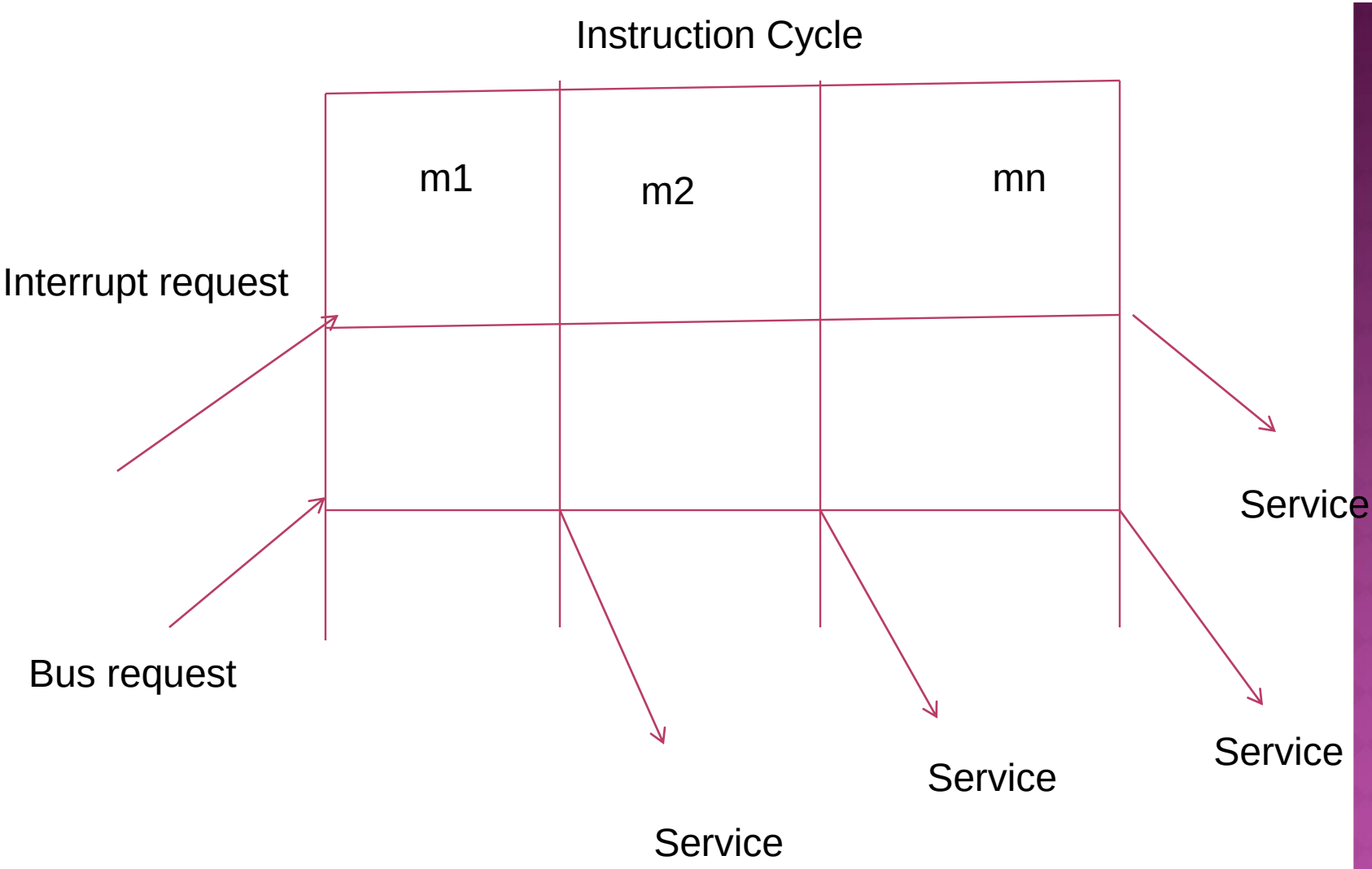




Bus transfer from one processor to another

Organization of the Machine Cycle




Instruction Cycle
m1
m2
mn
Interrupt request
Service
Bus request
Service
Service
Service

Lock

Lock MOV CX, [5000H}

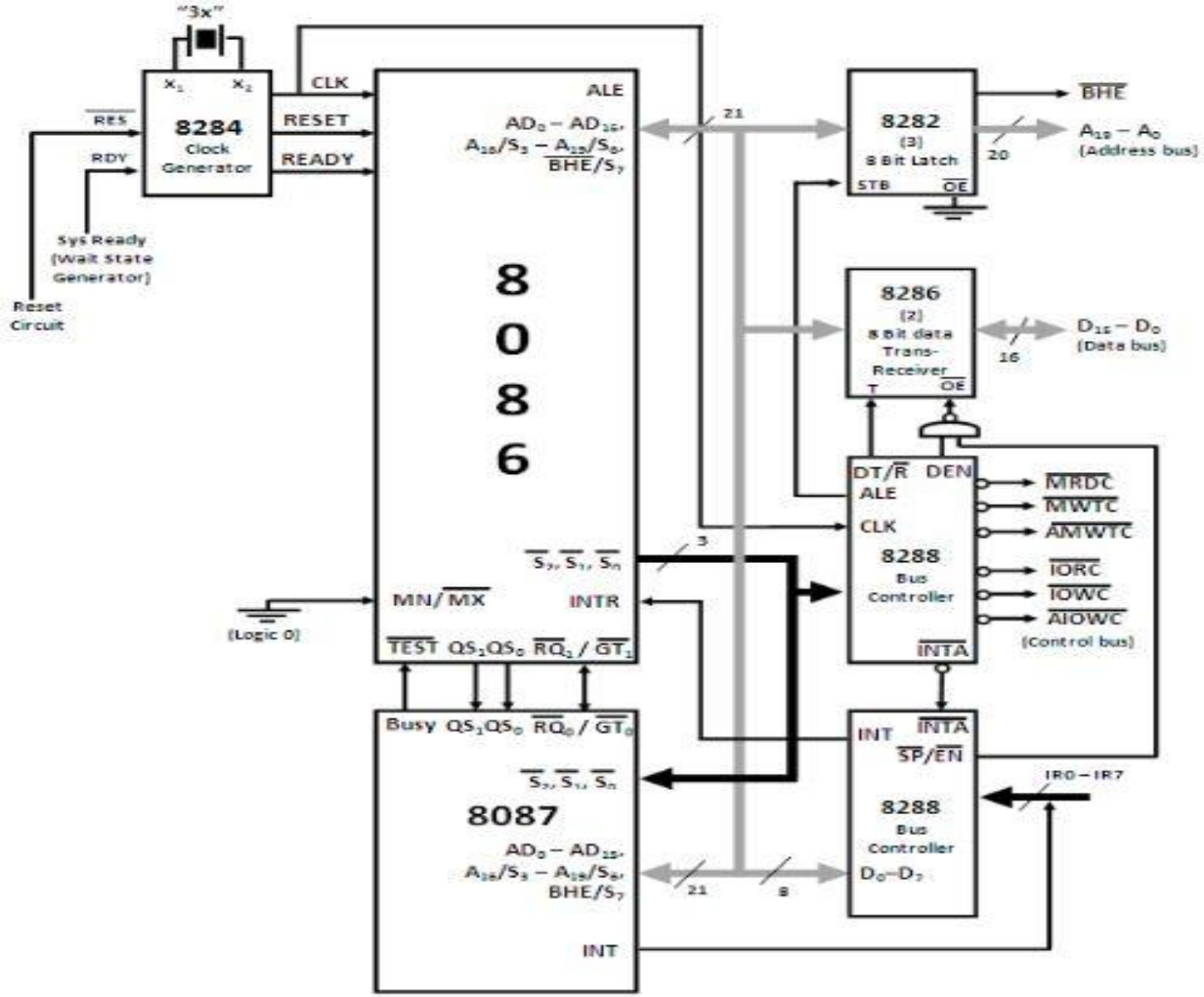
LOCK =0

REP- Repeating the String instructions

Status Signals

S2	S1	S0	Operation
0	0	0	INTA
0	0	1	IOREAD
0	1	0	IOWRITE
0	1	1	HALT
1	0	0	INSTRUCTION FETCH
1	0	1	MEMORY READ
1	1	0	MEMORY WRITE
1	1	1	IDLE

Co Processor Configuration



QS_1	QS_0	8087 Operation
0	0	NOP
0	1	8087 removes Opcode from Queue and compares 5 MSB bits with 11011.
1	0	8087 clears its queue.
1	1	8087 removes operand if earlier comparison with Opcode is successful.

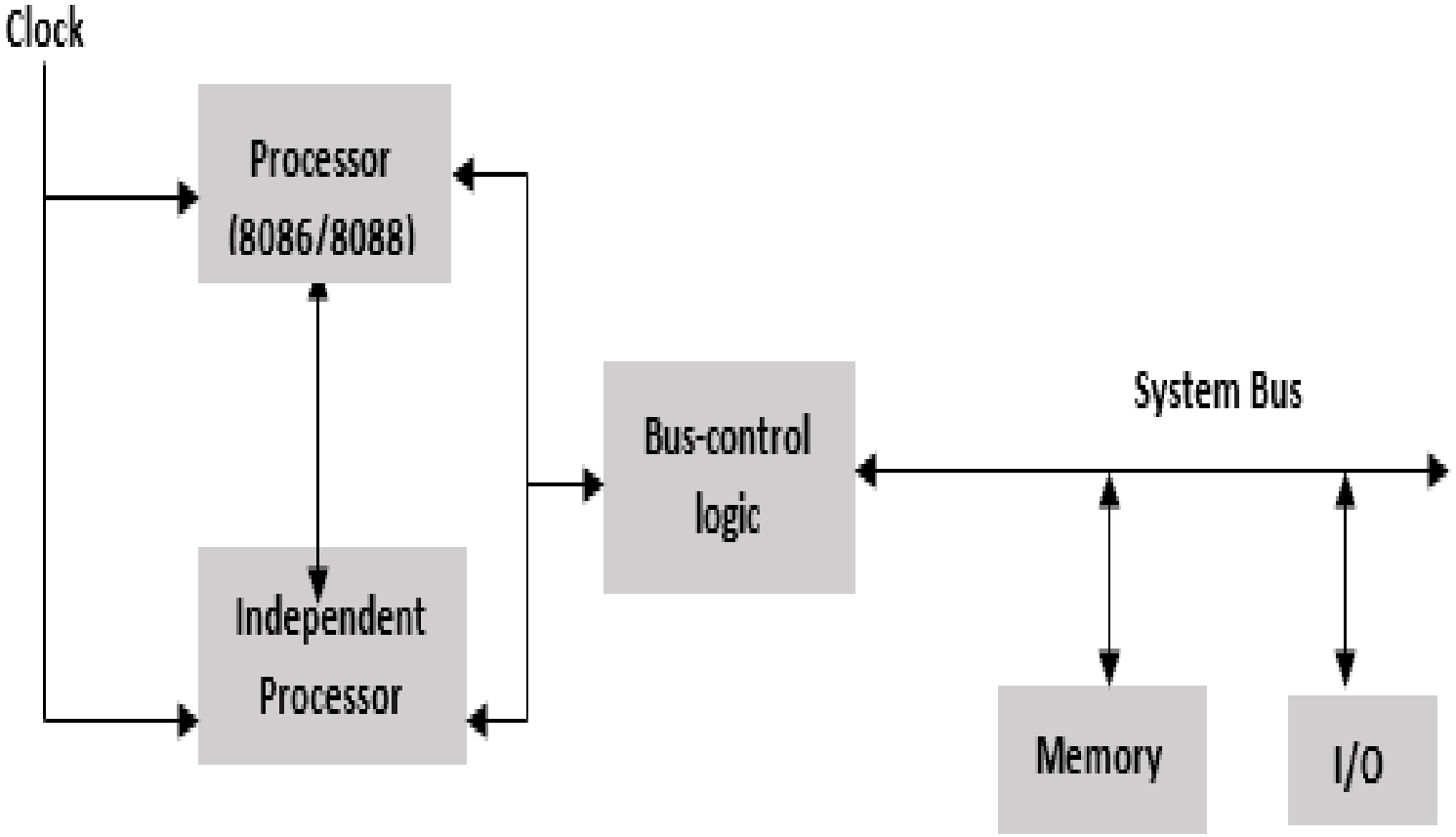
Multi Processor Configuration

- Multiple Processors – Execute the instructions simultaneously
And communicate with each other
- Maximum mode of 8086
    1. Coprocessor (8087) Configuration
    2. Closely Coupled (8089) Configuration
    3. Loosely Coupled (Multibus) Configuration

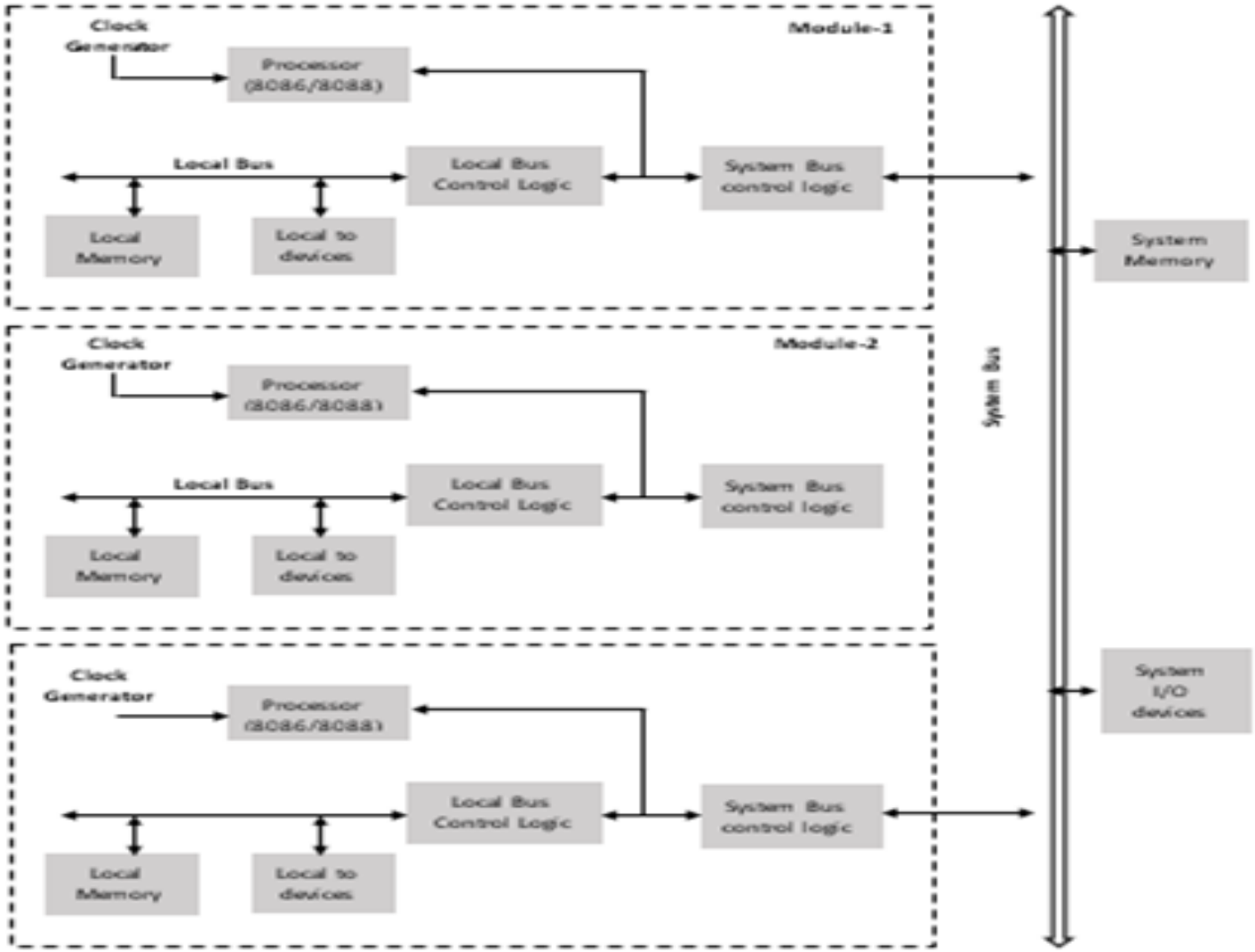
Coprocessor and closely coupled Processor

- Coprocessor and Closely Coupled Processor
  - Both similar
  - External Processor shares
    - Memory
    - I/O devices
    - Bus
    - Bus control Logic
    - Clock generator

Closely Coupled Configuration



Loosely Coupled Configuration



Pentium, Family of microprocessors developed by Intel Corp.

- Introduced in 1993 as the successor to Intel's
- The Pentium quickly became the processor of choice for personal computers.
- It was superseded by ever faster and more powerful processors, the Pentium Pro (1995), the Pentium II (1997), the Pentium III (1999), and the Pentium 4 (2000).

Thank You