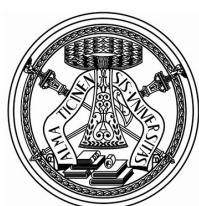
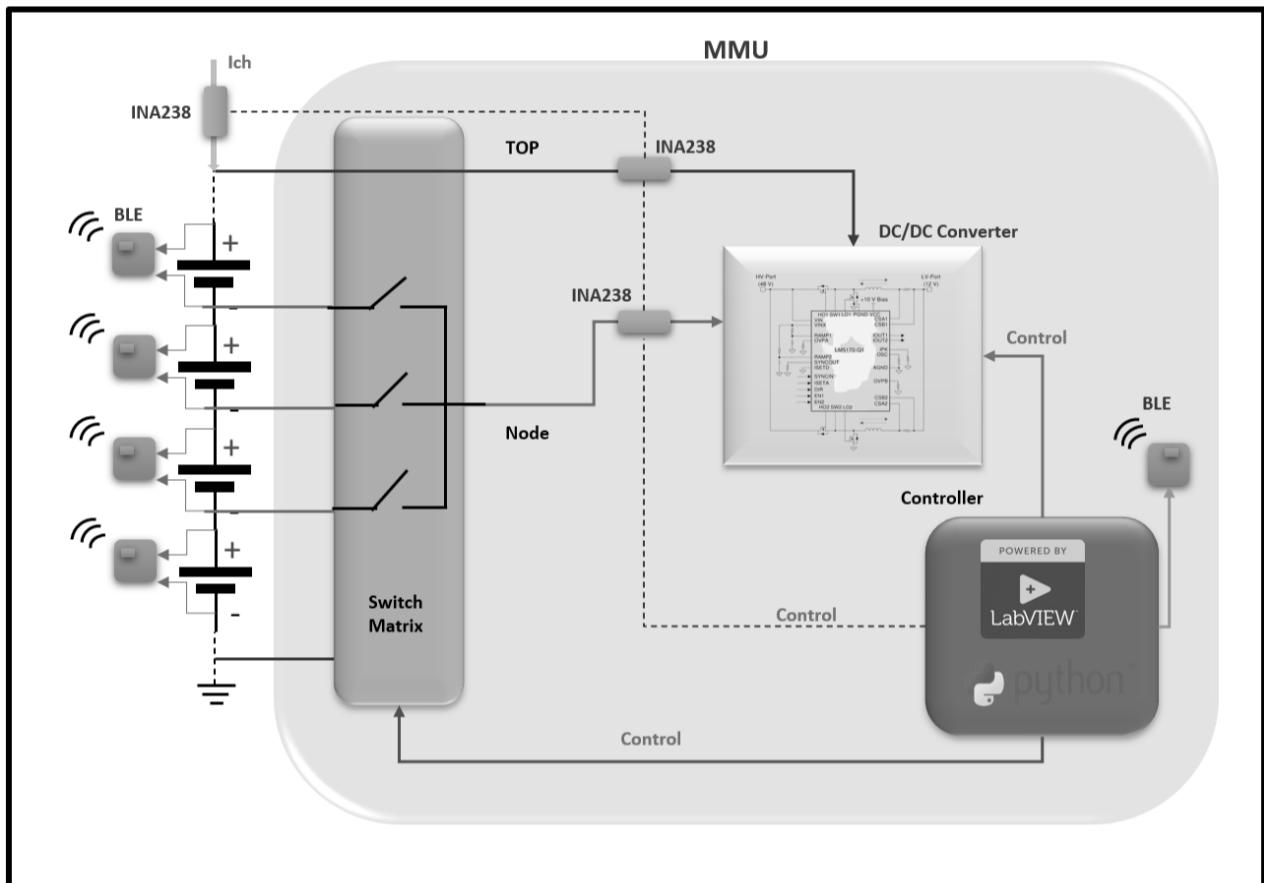


SOC and SOH estimation in BMS based on Wireless Communication Network



Department of Electrical, Computer and Biomedical Engineering
University of Pavia

SOC and SOH estimation in BMS based on Wireless Communication Network

Dissertation submitted in partial fulfillment

of the requirements for the degree of

Master of Science

in

Microelectronics

by

Harish Kumar Shivaramappa

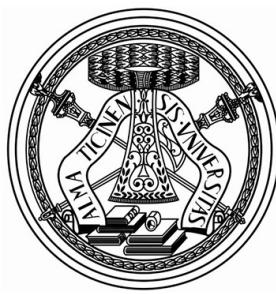
based on research carried out

under the supervision of

Prof. Piero Malcovati

and

Prof. Domenico Granozio



UNIVERSITA' DI PAVIA

December, 2022

Department of Electrical, Computer and Biomedical Engineering
University of Pavia

To

My Beloved Mother Miss.Kalavathi Shivaramappa ...

Acknowledgment

First and foremost, I express my deep appreciation and gratitude to my advisor, *Prof. Piero Malcovati* for his active support and crucial guidance throughout my master's Thesis program. It's his guidance that provided me with perspective and intuitive skills along with analytical capabilities that helped me to improve my technical understanding. His constructive approach and passion for his job are very inspirational to me. His positive words and encouragement always cheered me up, to gain productivity and proactiveness.

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A Significant contribution from my colleagues in the Inventvm application team must be acknowledged at this moment, and everyone has been part of my one-year thesis programmable, and they made me the happiest person in the work environment. Every colleague in the inventvm application team made my work more productive with healthy discussions and performances. *Riccardo*, *Flavio*, and *Antonino* were there to have a conversation full of amusement. So on and so forth I have thanked every colleague who is directly related to my thesis program, but there is one specific person that I must thank, though he is not directly part of the project. *Musico' Marco* , IT support and coordinator deserves my most friendly appreciation and thanks, because of his social interaction and humble nature of explaining nativity of things made me very much comfortable over my journey...so thank you *Marco* you deserve it!.

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Harish Kumar Shivaramappa

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Abstract

Determining the SOC ad SOH of the Li-Ion batteries by employing the Conventional Coloumb count method and sophisticated Kalman filter algorithms in a wireless communication network(BLE). The proposed Architecture measures synchronized current and voltage for SOC and SOH calculation by ensuring safety and adaptivity. By employing the Most Robust and Elegant Wireless Communication Network(BLE) in BMS, the architecture mitigates the problem of bulky and wired setups.

Keywords: **BMS; SOC; SOH; BLE; Coloumb-Count; Kalman Filter.**

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Preface

When started my Microelectronics master's program at the University of Pavia, I was wondering about the future of microelectronics in the domain of electric vehicle and sustainable energy management because I have witnessed personally how world leaders are crumbling to fix global warming and climate change. The idea of making global warming free through sustainable energy drove me to explore electrical vehicles and power management. As I was intensively researching myself about electrical vehicles and battery management systems, I got an opportunity to enroll LM+ program at the university of Pavia which is doing an internship through the university in corporate companies for one year.

Among the LM+ opportunities, I have noticed that Inventvm a dynamic young Italian company is doing research on Battery management systems for electrical vehicles. Since my interest is to work in power management and sustainable energy management, the Inventvm BMS project became a cherry on the pie for me. During the process, I met Eng. Domenico (Inventvm project BMS project manager), his idea of an elaboration made me more curious about the project and I stretched my legs immediately to the Inventvm on Feb 2020.

As I was stepping into Inventvm I started to experience the radiation of the knowledge from the engineers because they are not kids like me. As a young rookie in technology, I start to learn more about the hardware and software of the project because the bus(project) is already started way before I join to the company. That was ok! because at the age of 10 I smoked the LED placing it in 230V mains, what ?????? YES that's right, for sure the led did not glow bright, but my brain became to dig into why LED got burned despite the black smoke on the face while LED burned. Anyway, later I was educated by my father(of course he is an electrician) that LED needs some kind of electronic circuit to make it glow. when my father made LED glow, That was WoW, "astonishing"! LED was not too much bright enough though. This idea of making education by failure became fascinating this same strategy worked for me to understand this in the industry too quickly not to miss the bus. There are always my colleagues who gave me a shoulder to shoulder when I was stuck in some technological part.

Before my Master's, I worked with Analog Device Inc as IoT application Engineer and System Testing Engineer for Highpower circuits in NEXTGEN computers. The

knowledge gained from these two institutions, helped in my current project to understand the Wireless communication environment and power management. My experience in these two prime companies laid the foundation for analytical skills and problem-picking skills throughout the project. Nevertheless, the key motivation was my father and all my teachers who educated me throughout my life to contribute well to nature and humanity. Nonetheless, *Prof. Malcovati* has been a gem among all my honorable teacher's treasury who shined bright in my way. Thanks.....!

Introduction

Chapter 1

Bluetooth Module Design

1.1 Introduction

Antenna design and analysis are crucial in a wireless network that transmits and receives information through electromagnetic wave radiation in open space. Modern Antenna and RF design techniques are more often testified against size, power, flexibility, radiation patterns, efficiency, etc... It is very unusual to use a wide variety of RF fundamental design techniques even though the usage of silicon and power is different because the fundamentals of RF design are most rigorous and robust from decades, hence RF fundamentals and design techniques remain intact. Nevertheless, modern RF applications demand to emphasize efficiency and power requirements, so this requirement needs some special RF Design treatments. Chapter .3 gives the extravagance of PCB antenna design practices, general guidelines for grounding, PCB stacking, spacings and via holes, etc. Matching networks in RF design are extremely important to increase the efficiency of the Antenna and RF line, so it is also explored in the same chapter how to pick the passive components for RF Antenna matching such as capacitors and inductors.

1.2 Antenna Basics :

An Antenna is a piece of metal exposed to free space. A piece of conductor behaves like an antenna when its length is a certain ratio or multiple of the wavelength of the signal.

This scenario is expressed as "resonance", where the antenna radiates the electrical energy to the open space.

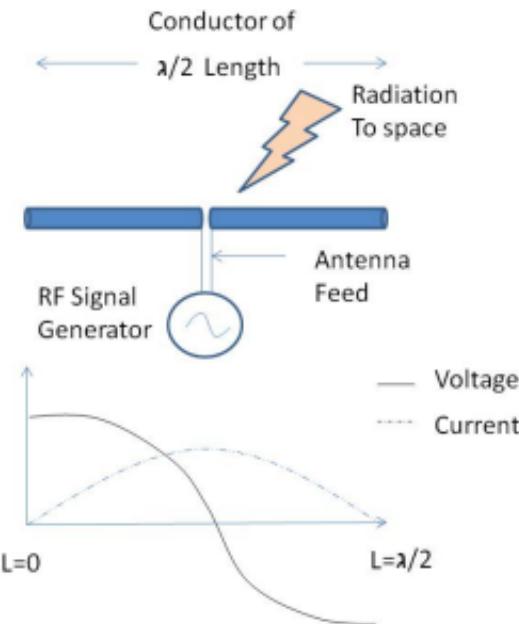


Figure 1.1: Basic dipole Antenna

Fig.1 shows the dipole antenna whose length is $\lambda/2$ and the fed has an input impedance of 50Ω . Dipole antennas are the most basic antennas that have been used for broadcasting. In the Millennial age of technology, dipole antennas have been bulky and heavy, thanks to the PCB technology, which made dipole antennas extremely simple in construction and this became the center of attraction for the Bluetooth application in the modern era. Although dipole antennas are extremely comfortable for PCB we still face hurdles to manage proper grounding for the antenna..which can be addressed through quarter-wave antennas. The quarter-wave antennas have half of the length of the dipole antennas $\lambda/4$, their popularity became exponential because of the fed which can be single-ended. A single-ended feed to the antenna made life much easier to make a wide range of ground planes and better matching.

1.2.1 Antenna Types:

As discussed in the previous section quarter wavelength antennas can be more effective on the PCB because of their fed and ground plane management on PCB. Depending on the antenna dimensions and the shape of antennas fall into different technologies namely FM, AM, Bluetooth, Wi-Fi and so on. Since the eccentric part of this chapter discusses the Bluetooth antenna design and guidelines, we can broadly classify three types of antennas. As follows :

1.2.1.a Wire Antenna :

These types of antennas are just a piece of wire extended over the PCB in open space, whose length is matched to $\frac{\lambda}{4}$ on the ground plane. In general, these antennas are fed by a 50Ω matching transmission line, a Wire antenna gives a top-notch performance and supports a wide range of frequencies because of its three-dimensional exposure in open space. The shape of the wire antennas can be loop, wire, or helix.. depending on the application the shape is changed.

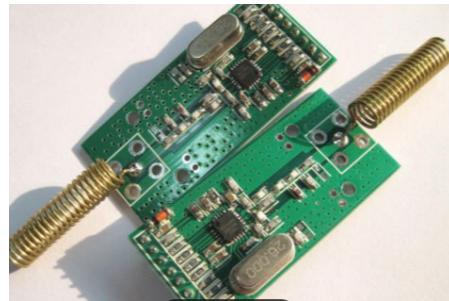


Figure 1.2: Wire Antenna

1.2.1.b PCB Antenna :

Constructively this type of antenna is copper traces that are etched on the PCB. The Traces can be Zig-Zag, straight, MIFA, Meandered type, F-type, or Zip track so on., the shape of the antenna is chosen based on the antenna type and the space constraints on the PCB. PCB Antennas have only two-dimensional freedom, therefore certain guidelines are needed for the PCB antenna design due to the space constraints and poor quality of PCB stack-up. The space constraints of the PCB antennas lead to less efficiency compared with wire antennas nonetheless PCB antennas are cost-effective. In short manufacturing comfortability and its wireless range is ravishing for Bluetooth applications.

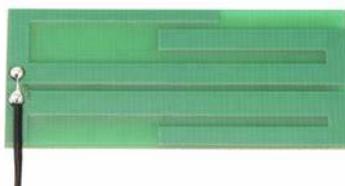


Figure 1.3: PCB Antenna

1.2.1.c Chip Antenna :

This is a Small form factor IC that is in-house with a ceramic package or some metal case. These antennas are handier in terms of space management on the board and internally

their impedance is very well managed. A chip antenna can also take an advantage of three-dimensional freedom for radiation similar to wire antennas. Refer to figure 10 for the Nordic Bluetooth module having a chip antenna. Chip antennas can indeed gain upper hand in size and radion pattern on the contrary power handling capacity of the chip antenna is very minimal.



Figure 1.4: Chip Antenna

1.2.2 Antenna Parameters

The following section gives some key antenna performance parameters.

1.2.2.a Return loss :

The return loss of an antenna signifies how well the antenna is matched to the $50\text{-}\Omega$ transmission line (TL), shown as a signal feed in Figure ???. The TL characteristic impedance is typically $50\ \Omega$, although it could be a different value. The industry standard for commercial antennas and testing equipment is $50\text{-}\Omega$ impedance, so it is most convenient to use this value [7].

Return loss indicates how much of the incident power is reflected by the antenna due to mismatch (Equation 1.1). An ideal antenna when perfectly matched will radiate the entire energy without any reflection. If the return loss is infinite, the antenna is said to be perfectly matched to the TL, as shown in Figure 1.5. S₁₁ is the negative return loss expressed in decibels. In most cases, a return loss $\geq 10\text{ dB}$ (equivalently, $S_{11} \leq -10\text{ dB}$) is considered sufficient. Table 1.1 relates the return loss (dB) to the power reflected from the antenna (percent). A return loss of 10 dB signifies that 90% of the incident power goes into the antenna for radiation [7].

$$\text{Returnloss}(db) = 10 \times \log\left(\frac{P_{\text{incident}}}{P_{\text{reflected}}}\right) \quad (1.1)$$

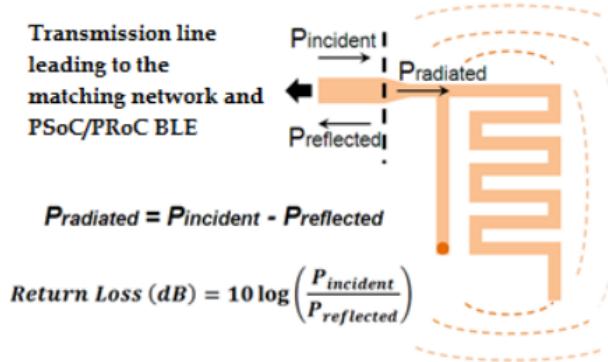


Figure 1.5: Antenna Return loss

S11 (dB)	Return Loss (dB)	$\Gamma_{\text{ref}}/\Gamma_{\text{inc}} (\%)$	$\Gamma_{\text{rad}}/\Gamma_{\text{inc}} (\%)$
-20	20	1	99
-3	3	50	50
-10	10	10	90
-1	1	79	21

Table 1.1: Return Loss and Power reflected from antenna

1.2.2.b Bandwidth :

Bandwidth indicates the frequency response of an antenna. It signifies how well the antenna is matched to the $50\text{-}\Omega$ transmission line over the entire band of interest, that is, between 2.40 GHz and 2.48 GHz for BLE applications [7].

As Figure 1.6 shows, the return loss is greater than 10 dB from 2.33 GHz to 2.55 GHz. Therefore, the bandwidth of interest is around 200 MHz. Wider bandwidth is preferred in most cases, because it minimizes the effect of detuning resulting from the changes in the environments around the antenna in actual uses of the product (e.g. mouse placed on wood/metal/plastic table, hand kept around the mouse, etc.) [7]

1.2.2.c Radiation efficiency:

A portion of the non-reflected power (see Figure 1.1) gets dissipated as heat or as thermal loss in the antenna. Thermal loss is due to the dielectric loss in the FR4 substrate and the conductor loss in the copper trace. This information is characterized as radiation

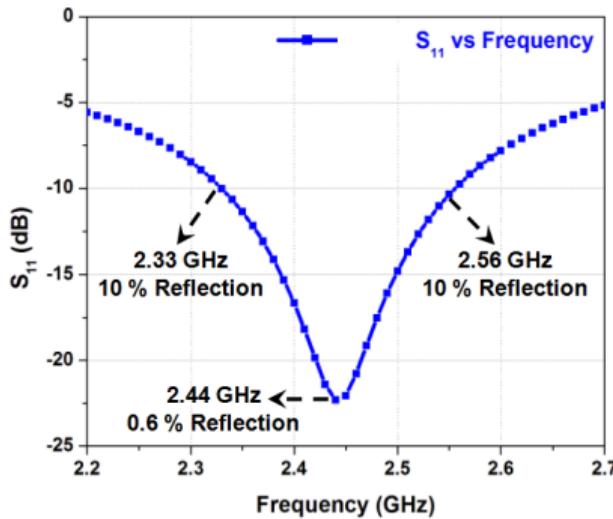


Figure 1.6: Antenna Bandwidth

efficiency. The radiation efficiency of 100 percent indicates that all non-reflected power is radiated to free space. For a small-form-factor PCB, the heat loss is minimal [7].

1.2.2.d Radiation pattern:

Radiation pattern indicates the directional property of radiation, that is, which directions have more radiation and which have less. This information helps to orient the antenna properly in an application [7].

An isotropic dipole antenna radiates equally in all directions in the plane perpendicular to the antenna axis. However, most antennas deviate from this ideal behavior. See the radiation pattern of a PCB antenna shown in Figure 1.7 as an illustration. Each data point represents RF field strength, measured by the received signal strength indicator (RSSI) in the receiver. As expected, the contours are not exactly circular, as the antenna is not isotropic [7].

1.2.2.e Gain :

Gain indicates the radiation in the direction of interest compared to the isotropic antenna, which radiates uniformly in all directions. This is expressed in terms of dBi—how strong the radiation field is compared to an ideal isotropic antenna [7].

1.3 Motivation for Designing BLE Modules

One of the core ideas of the Inventvm BMS team is to make the BMS project in a wireless communication environment, therefore the team has decided to use Bluetooth as the communication tool. Hence, finding the big sharks (Bluetooth Hardware and stack)

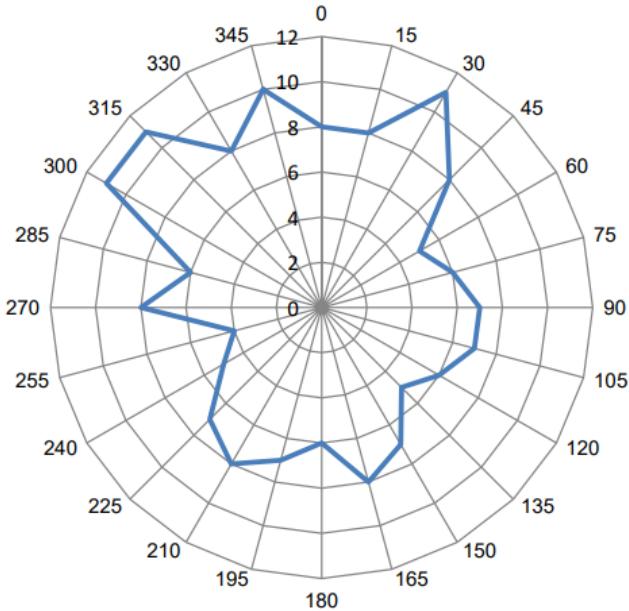


Figure 1.7: Antenna Radiation Pattern

in the Bluetooth world took quite some time, after a long investigation; we concluded to pick two important pies in the Bluetooth cake such as STM BLUeNRG-355mc [8] and Nordic nRF52840 [9]. BlueEnergy-355mc is the jewel of our projects because it owes the advantages of very low power consumption: 3.4 mA, Receiver sensitivity, Bluetooth low energy data extensions, high data rate so on... despite having these many advantages STM does not manufacture the Bluetooth modules other than eval boards. Henceforth, the team has been paralyzed to outsource the required Bluetooth modules, later in the same path we found MIDARTRONICS the company that manufactures the Bluetooth modules using the STM BLUeNRGgy-355mc hardware named STORMY. Stormy is a such cutie pie, at least it helps to some extent in R and D to prove the Wireless communication BMS architecture, but in the long run, we have experienced some the discomforts such as lack of documentation and market supply...to overcome all these issues team has decided to make inventive proprietary level Bluetooth modules for BMS project. This gave me the perfect timing and to opportunity design RF Bluetooth modules for the project, as part of my thesis which is dedicated to wireless communication BMS.

Nordic nRF52840[9] is another Bluetooth hardware similar to the BlueEnergy-355Mc reason behind picking the Nordic is the open BLE stack and Robust hardware. Nordic is much more comfortable in terms of different data rates, on-chip power converters, 32-bit ARM Cortex M4F @64MHz so and forth. Nordic has also a dedicated BLE stack [10] that handles all power management resources on-chip, which attracts low-power automobile applications. In a much broader sense, Nordic is additional Bluetooth hardware that we can provide to the customer according to the

application's need.

Though picking the Bluetooth hardware and stack is a boiling task, choosing the antenna and RF layout also takes prime place. Though, there are plenty of antennas for the 2.4GHz band, most Bluetooth manufacturers recommend two types of PCB antennas, meanders inverted antennas (MIFA) and inverted-F antenna (IFA), which are characterized and simulated exclusively for the low-power Bluetooth applications. However, MIFA (PIFA) is peculiar for most automobile applications because of its pointed directional properties.

, However, we can choose any type of antenna and hardware for Bluetooth, admittedly the antenna, hardware, and RF layout design described in the following modules are classified for the BMS project.

The Low Data rate and bandwidth requirement in Bluetooth applications make IFA and MIFA the two most attractive antennas for BLE. Manufacturing these antennas is extremely easy because they are part of the PCB design. Certainly, these antennas are inexpensive as they are part of PCB and they provide good bandwidth in ranges for BLE in terms of 150 to 250 MHZ.MIFA is most preferable for smaller form factor PCBs such as a wireless mouse, wearable watches, handy IoT devices.... etc. IFA antennas are recommended for applications such as one of the dimensions is needed to be smaller than the other for example heart rate monitor. The following modules explain MIFA and IFA antennas construction and functionalities:

1.4 PCB Meandered Inverted-F Antenna (PIFA/MIFA)

PIFA antennas are much more popular in Bluetooth Low Energy stack because of the small size, low profile and cost-effective compared to the conventional dipole and ceramic chip antennas. The proposed structure (PIFA/MIFA) Figure 1.9 of the PIFA antenna is routed to gain all these advantages. Replacing the conventional PCB trace in PIFA with the meandering line and meandering shorting strip improves the efficiency of the PIFA as well as the bandwidth.

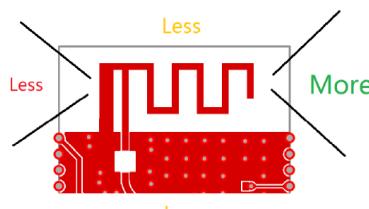


Figure 1.8: MIFA/PIFA antenna radiation direction

Figure 1.9 Taking the meandered shape on one side and connecting meandered terminal to the ground makes the radiation lobe a more directional Figure1.8 that implicates the radiation of the meandered antenna.Meandered side of the antenna radiates

very less power because the Menderes terminal is connected to the ground which nullifies most of the radiation on the backward side. This kind of feature is highly needed in extremely noisy environments such as automobiles, power grid applications, data servers....etc. As a case study, the design and measurement results of the proposed MIFA/PIFA are presented [11] in Figure 1.9.

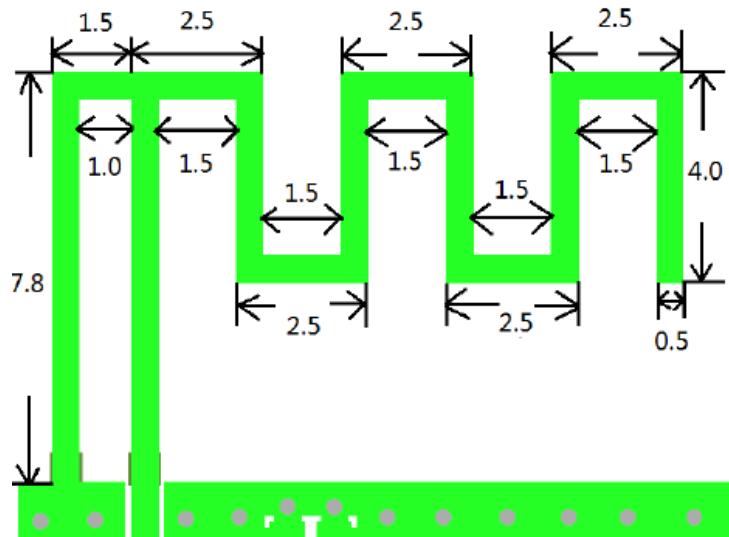


Figure 1.9: PCB Inverted Meandered F type Antenna [1]

1.4.1 Antenna used in Inventvm BLE modules :

I got an opportunity complete the Inventvm BLE module antenna simulation Figure 1.9 to depict the typical board shape and the antenna placement [12]. The RF shield housing has been removed for testing purposes, usually, Bluetooth modules provide RF housing to protect the BLE from external interference.

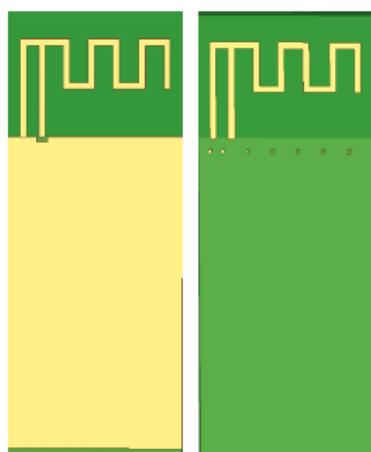


Figure 1.10: BLE module PCB with the MIFA/PIFA antenna placement

Some MIFA/PIFA antenna and PCB parameters that are used for the simulation are shown in the table 1.2.

Antenna parameters	Value	Unit
PCB substrate permittivity	4.6	—
PCB substrate H	1.0	mm
Length of PCB substrate	35.5	mm
Width of PCB substrate	14	mm
Length of TOP PCB ground	25.5	mm
Width of TOP PCB ground	14	mm
Length of BOT PCB ground	25.5	mm
Width of BOT PCB ground	14	mm
Width of antenna trace	0.5	mm

Table 1.2: MIFA/PIFA antenna simulation parameters [1]

1.4.2 S11 of the MIFA/PIFA antenna

Figure 1.11 shows the MIFA/PIFA antenna s11 parameter simulation results. The Bluetooth frequency bandwidth ranges from 2402 to 2483.5 MHz. The return loss of the antenna in the Bluetooth frequency band is less than the -10db.

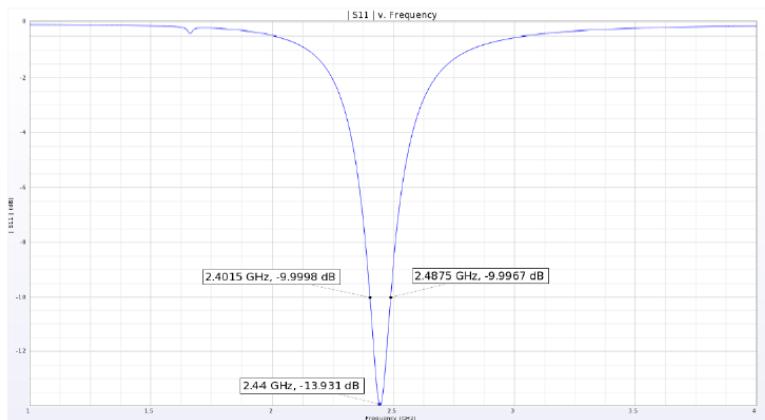


Figure 1.11: MIFA/PIFA antenna S11 return loss

1.4.3 MIFA/PIFA antennas 3D pattern :

1.5 Inverted-F Antenna:

The inverted F antenna is also one of the popular antennae, recommended for the Low power stack BLE applications. IFA antennas host similar features to what MIFA/PIFA antennas offer but MIFA antennas are more recommended where there is a space constraint and power radiation is in one direction. IFA antennas have bidirectional power radiation

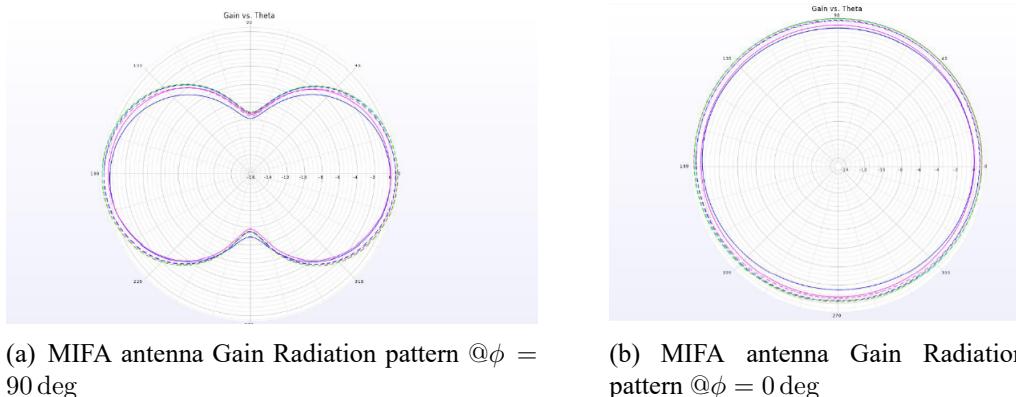


Figure 1.12: MIFA Antenna Gain Radiation Patten

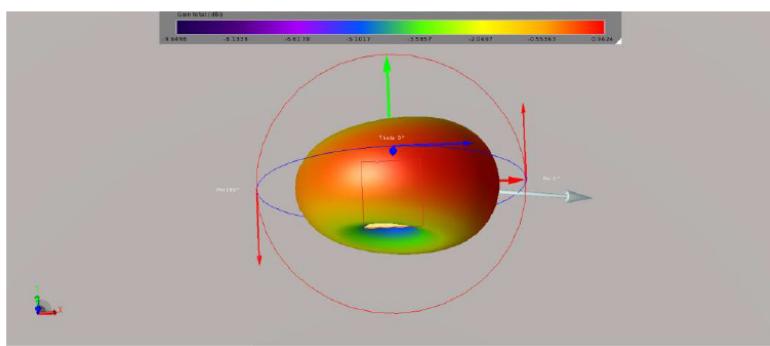


Figure 1.13: MIFA/PIFA antenna 3D radiation Patten

rather than mono-directional. Nordic Recommends in all designs to use the IFA antennas. Figure 1.15 educates the typical design of the IFA antenna and simulation parameters are pretty much the same as it is used for the MIFA antenna Table 1.2.

By the constructional nature of the IFA antennas are easy to match we can see that in the Figure 1.16 IFA antenna is very well-matched at 2.4GHz. The S11 is quite impressive because it has a reflection coefficient at 2.4GHz is -27db and bandwidth at -9db is 160MHz. IFA antenna matching can be further tuned by varying the hinges, and length of the antennas, on contrary we need to compromise with power and resonant frequencies. Figure 1.17 shows the relative length and hinge width changes of the design Figure 1.15 caused different frequency shfit, but they keep giving the best performance in matching.

1.6 BLE Schematic and PCB layout

The Schematic of the Inventvm BLE modules is inherited directly from the vendors, which are BluEnergy-355MC[8] and Nordic nRF52840[9]. The Figure1.18 shows the pinout and shape of the BLE module, which is multi-purpose because of same shape and pinout from both the BluEnergy-355MC and Nordic nRF52840 modules. By having the

Frequency (GHz)	Available power (W)	Input power (W)	Radiated power (W)	System efficiency	Radiation efficiency
1	0.0025	6.09E-05	4.24E-06	0.17 %	6.96 %
1.6	0.0025	1.00E-04	3.23E-05	1.29 %	32.19 %
1.66	0.0025	2.22E-04	6.56E-05	2.63 %	29.51 %
1.72	0.0025	1.22E-04	4.94E-05	1.98 %	40.35 %
2.08	0.0025	3.67E-04	2.46E-04	9.84 %	67.07 %
2.26	0.0025	1.02E-03	7.63E-04	30.50 %	74.76 %
2.44	0.0025	2.40E-03	1.86E-03	74.44 %	77.58 %
2.54	0.0025	1.85E-03	1.43E-03	57.32 %	77.41 %
2.64	0.0025	1.12E-03	8.54E-04	34.17 %	76.35 %
2.83	0.0025	4.83E-04	3.50E-04	14.00 %	72.46 %
3.22	0.0025	1.91E-04	1.18E-04	4.70 %	61.58 %
4	0.0025	8.62E-05	3.18E-05	1.27 %	36.87 %

Figure 1.14: MIFA/PIFA antenna efficiency Simulation Results

Same pinout and shape with different Bluetooth hardware, customers can use different Bluetooth hardware stacks with the same BMS solution. This approach is nothing but the daughter and motherboard approach where the Bluetooth module becomes the daughter board and BMS MMU board and CMU boards become motherboards.

1.6.1 BluEnergy-355MC

BLUENRG-355MC[8] BLE module includes BlueNRG-LP BLE low energy system on chip (QFN48 package), Associated with BlueNRG-LP development software stack from STM. The BlueNRG-LP features a 64 MHz, 32-bit Arm®Cortex®-M0+core, a 256 KB programmable flash memory, a 64 KB SRAM, an MPU, and an extensive peripheral set (6x PWM, 2x I²C, 2x SPI/I2S, SPI, USART, UART, PDM, and 12-bit ADC SAR)[8]. It is compliant with the Bluetooth® LE specification and supports master, slave, and simultaneous master-and-slave roles. It features data length extension, 2 Mbps, long-range, extended advertising and scanning, as well as periodic advertising, periodic advertising sync transfer, LE L2CAP connection-oriented channel, and LE power control and path loss monitoring[8]. For more technical details refer STM BLUENRG-355MC datahseet [8].

1.6.1.a BluEnergy-355MC RF Schematic:

The Figure1.19 refers to the core circuit of the BLUeNRG circuit for the Bluetooth, the pi network matching topology used to match the Ic and antennas, and refer 1.19 circuit between the RF net and the ANT net in the schematic. All the discrete components are selected 0402 packages to make the Bluetooth module as sophisticated as possible, for

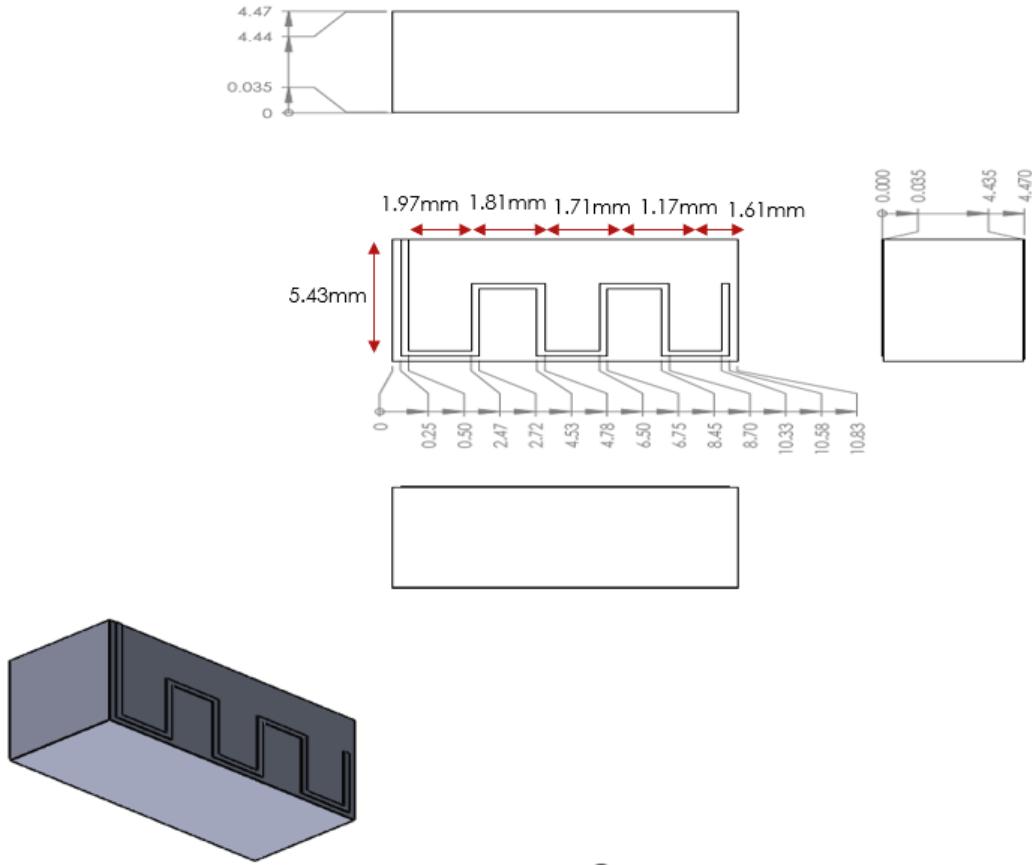


Figure 1.15: IFA antenna design and the placement

more insight into the component selection for the schematic 1.19 refer to BOM[13].

1.6.1.b BluEnergy-355MC RF Layout:

The BLE module designed for the BMS application in Inventvm is the four-layer PCB, among four layers bottom layer is entirely dedicated to the ground. The bottom layer ground of the module is the analog ground it is differentiated from the power ground of the BMS from a small inductor to make sure the RF circuit gets less noise from the power ground.

By referring to the layout Figure 1.20 of the RF module you can recognize that the shape of the power plane in the layer is pretty much weird, there is an RF technique behind making this kind of shape to avoid as much as the ground and power plane over a lap to decrease the capacitive parasitic effect. Parasitic components on PCB are the plague of the RF circuit, they can kill RF signal. Hence it is always a good idea to avoid power and ground planes overlap as much as possible and also make separate ground for the RF layout apart from the power ground.

Place as many as vias possible from the top to bottom ground layer to enhance the ground layer capacity, and making sure to have equal space for antenna and RF feed line from the ground enhances the matching capability of the antenna. The following

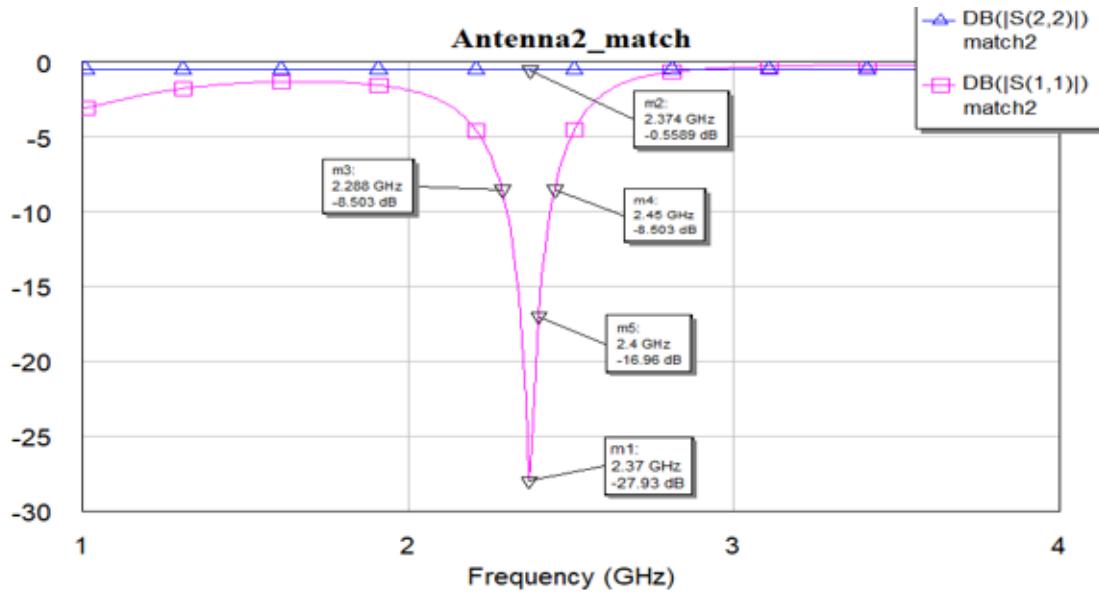


Figure 1.16: IFA antenna S11 and S22

extinctions can give a detailed view of RF layout design:..

- **Power plane and Grounding :** The power and Ground plane's overlap needs to be decreased as much as possible to avoid the parasitic capacitance effect. The Figure 1.20 refers to the power supply plane in the layer and the ground in the bottom layer.

- **Equal Clearance to Antenna Feed :** It is essential to keep the same clearance throughout the RF feed line from the ground. This strategy helps to make equal parasitic capacitance from the ground. With an equal parasitic capacitance from the opposite side, the RF standing wave reflections can be nullified. Figure 1.21 depicts one such example of designing the RF feed line.

-
- **Isolate Power Ground from Analog/RF ground :** It is the most common practice while RF layout designing, The RF layout is isolated from the Power circuit. For this approach I have few intuitions behind the two-fold, those are :
 1. RF-related noise is confined within the RF/Analog ground of the PCB.
 2. This will isolate noise from the digital circuitry with the DC power supply and High power switching circuit on the BMS board.
 3. RF circuit protected from direct current flow from DC supply if there are any power surges in supply. So on....

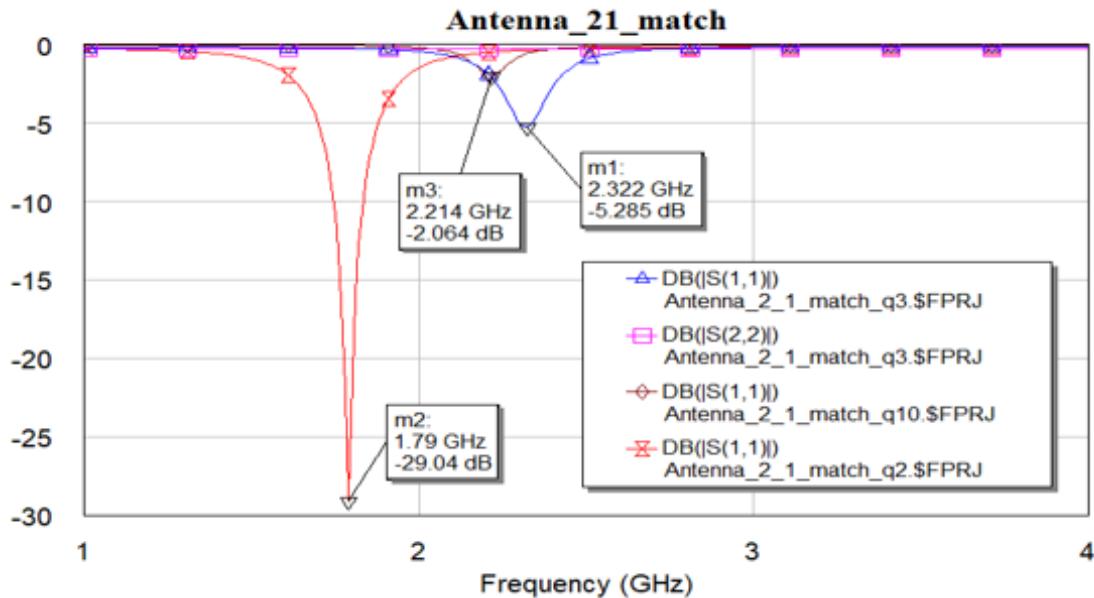


Figure 1.17: IFA antenna S11 Variation by changing the length and hinge width

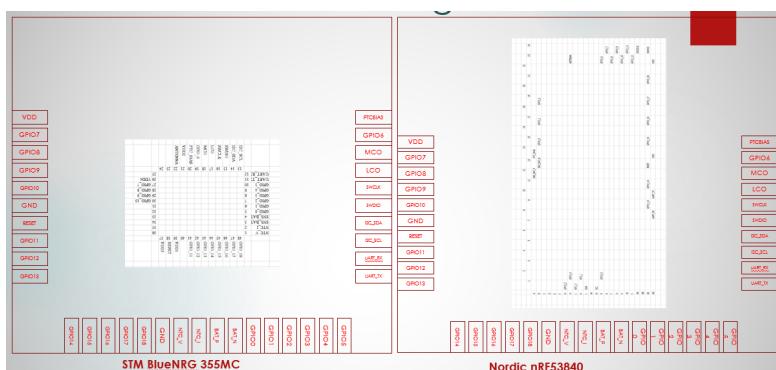


Figure 1.18: BluEnergy-355MC(right) and Nordic Modules(left)

1.6.1.b Such mentioned benefits can be obtained by placing an inductor between the Power Ground/RF ground. Choosing Inductor for such functionality follows that the inductor will not allow sudden current spikes $L \times \frac{di}{dt}$, on the benefit it can also provide a high current ratio when the current is stable,reference 1.22..

- **RF feed line shape :** It is common practice to keep the rf feed line with the known shape. Since Bluetooth operates at 2.4GHz, even one millimeter can give a large amount of resonant frequency drift in antenna reflections. The simplest approach to mitigate such issues is to keep the RF feed and the RF IC, both on the same axis. To avoid unnecessary parasitics by an irregular shape of the antenna, make a feed trace from the ic to Antenna with the same width as the antenna feed has. Figure 1.23 shows the approach that I have followed to design the Antenna feed and the RF trace, The Figure shows the nonregular shape of the antenna.

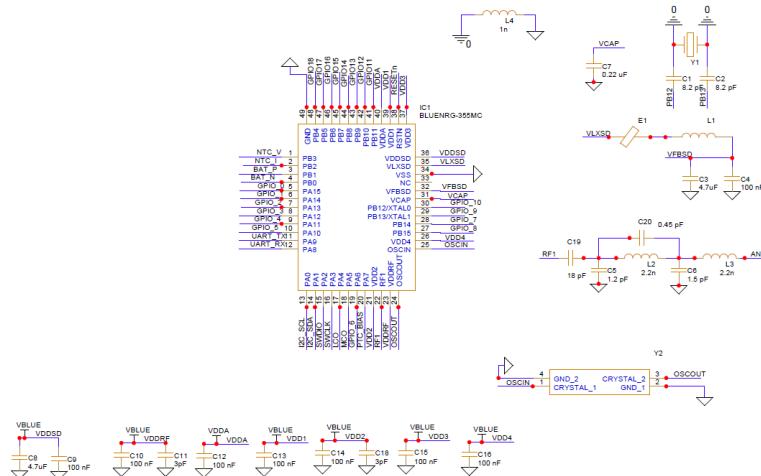


Figure 1.19: BluEnergy-355MC Module Core circuit

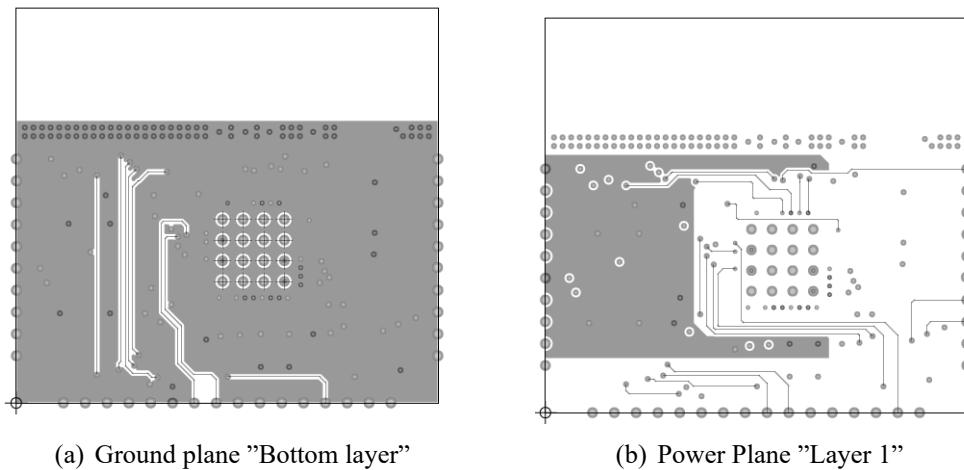


Figure 1.20: BLE PCB ground and power planes

- **Grounding Via's :** Keep always clean ground and this can be achieved by placing as many vias from the top layer to the dedicated RF/Analog ground in the bottom layer. It is recommended in the PCB design to place the Vias with equal distance, Figure 1.23 refers to Vias placement from the top layer to the bottom layer with equal distance. There should not be any ground under the RF antenna, because the ground under the RF antenna again makes, Antenna just an RF trace instead of allowing open radiation.

—

- **Antenna placement :** Do not place any component in the Antenna Keep out area, make the strict keep-out area for the antenna to prevent any external components' noise interference. It is always good placement to avoid any of the plastic components around the antenna because the plastic can behave like a dielectric and this will change the antenna characteristics. Antenna placement on they should end of the PCB where the PCB notch is pointed out. See Figure 1.20 the antenna

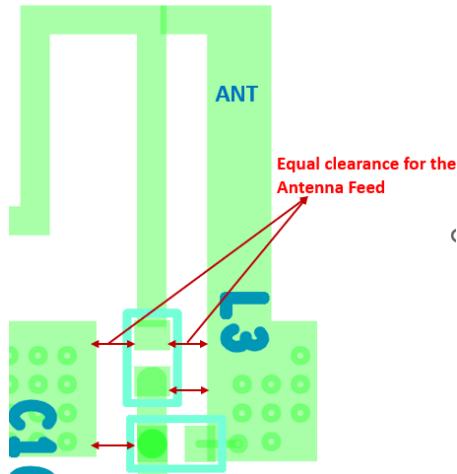


Figure 1.21: Antenna Feed Line clearance

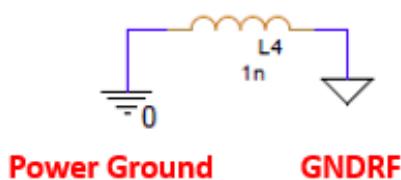


Figure 1.22: Power Ground and RF Ground Isolated with Inductor

has been placed on the edge of the PCB and there are no plastic or high-frequency switching circuits around it.

1.6.1.c Power Supply Decoupling Layout Considerations[7]

Note the following best practices when laying out the power supply traces:

- Place the components as close to the supply pin as possible [7].
- Place the smallest-value capacitor closest to the power supply pin [7].
- Place the decoupling capacitor on the same layer as the IC. If it is not possible to place all the capacitors on the same layer, give priority to smaller values [7].
- The power supply should flow through the decoupling capacitors to the power supply pin of the IC. Avoid using
 - supply vias between the component and the pin [7].
 - Use separate vias to ground for each decoupling capacitor. Do not share vias[7].
- For four-layer boards with a separate power plane, use separate vias for each power supply pin to the power plane [7].
- It is recommended not to share the vias [7].

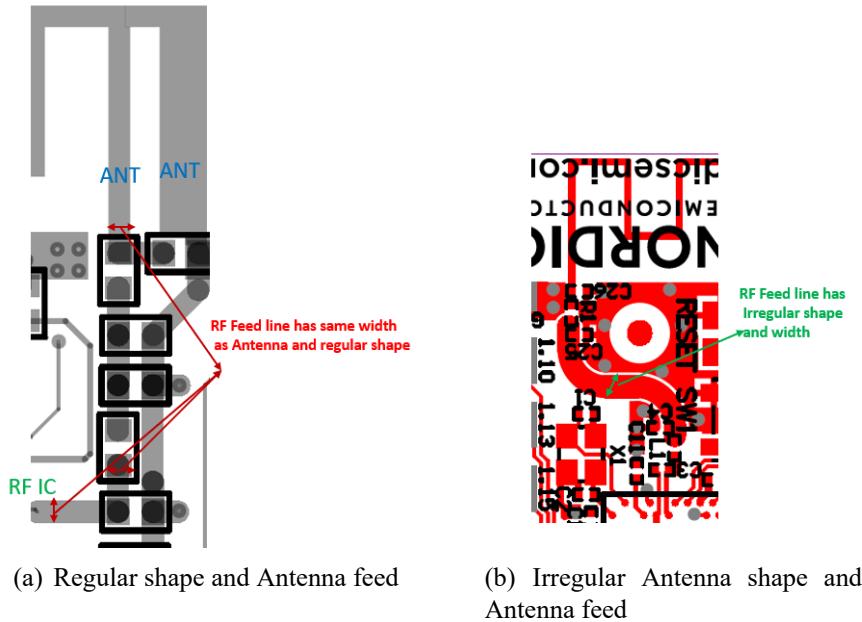


Figure 1.23: Antenna Feed Shape

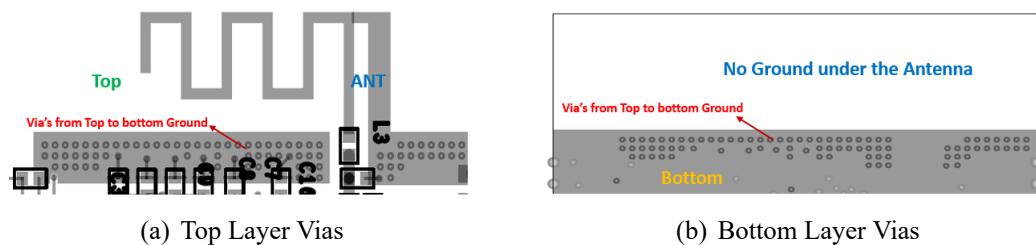


Figure 1.24: Vias placement on BLE board

- Some of the commonly made layout issues related to power supply decoupling are shown in [7] Figure 1.25.

1.6.1.d BluEnergy-355MC RF Matching Circuit Layout:

It is always a good approach to have the matching circuit as tight as possible you can refer to the Figure 1.26 the matching circuit is placed as close as possible, to avoid any additional track length to create some extra RF stub effects. Don't ever run any of the signal lines across the RF feed line and always make sure to place the IC and RF in the same direction this approach will avoid any strange track shapes which can cause parasitics. It is a good way to make sure the RF feed line to the antenna through the IC has the same width across the track length this will avoid any unnecessary filtering effect. The figure refers to all of above-mentioned RF layout design hints. Figure 1.26 shows that matching components are tightly packed, and no signals run across the RF feed.

We can place the components even overruling the component outline. Until we do

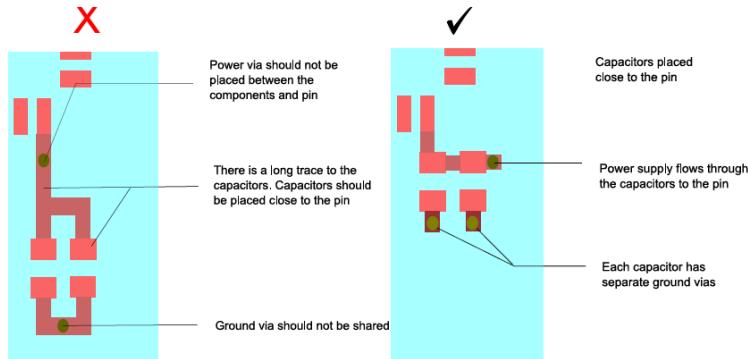


Figure 1.25: Power Supply Decoupling

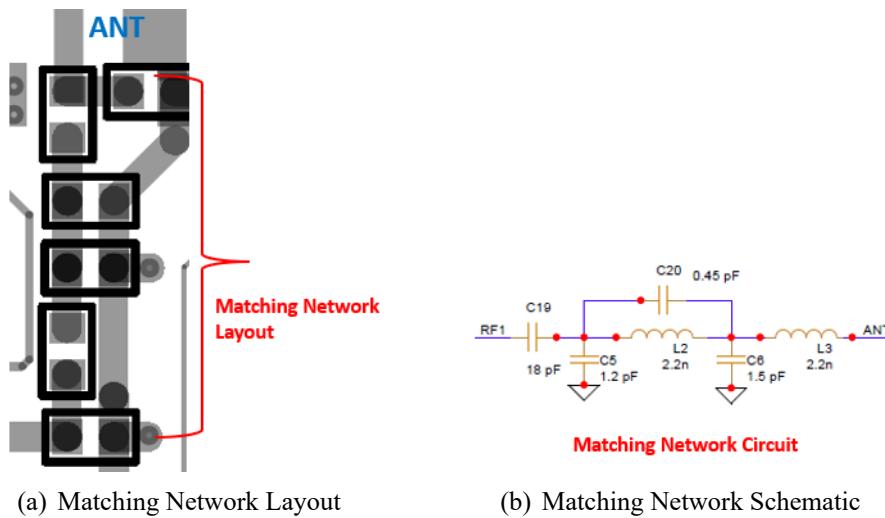


Figure 1.26: BLE Antenna Matching Network

not make the pads overlap, to achieve this we might have to bypass some PCB DRCs.

1.6.2 Summary of the RF layout Design guidelines :

1. Keep Ground clearance as much as possible around the antenna.
2. Make equi clearance on both sides of the antenna and RF feed line.
3. Do not make a strange shape of the antenna feed line.
4. Do not run any of the signal lines under the antenna or RF feed line.
5. Make more vias from the top layer to the bottom layer for pure ground.
6. Keep capacitive filters as near as possible to the power supply pins.
7. Pack antenna matching network as close to antenna and IC RF feed.
8. Place antennae in less clumsy area from other circuitry on the PCB.
9. Make less overlap of the ground plane and power plane.

10. Avoid high-frequency circuits around the RF feed.
11. Always places the antenna at the edge of the PCB.
12. Always chooses a standard pattern for the ground around the antenna.
13. Never places any components, screws, mounting holes, or planes in the keep-out area of the antenna.
14. The antenna must house with a Metalic shield to avoid external interference.
15. There should not be direct ground under the antenna.
16. The Orientation of the antenna should be inlined with the final PCB.
17. When using the passive matching circuit try to have multiple components matching this can help at the debugging stage to tune the matching circuit.

1.7 Conclusion of the Chapter 1

The simulation and design of both the MIFA and IFA antennas are successful the results have been presented in Chapter1. Both the MIFa and IFa antennas are well performed in the sense of the results and design, because of the industry standards and Bluetooth stack recommendations, from vendors I have opted MIFA for Inventvm Bluetooth modules. The Layout is also quite impressive considering all norms of RF PCB layout guidelines, which are mentioned in the chapter1. In the chapter1 I have not stressed the theoretical calculation for the MIFA/IFA antenna because the calculations are pretty much the same as the standard MIFA and IFA antennas, The goal is to bring up the sophisticated RF BLE layout according to the application with a standard approach. Yet reference papers [[14],[15]] give more insight into the theocratical design of the MIFA / IFA antenna and I have taken fewer opportunities to explain the nordic architecture, because of the RF layout out-wise and in the antenna sense, I have followed the same guidelines as I did for the BLUeNRG-355mc. The Complete layout of the BLUeNRG and Nordic is attached in the chapter6 , Figures (6.1,6.3).

Chapter 2

Architecture of Wireless Communication Active Balancing BMS

2.1 Introduction

There are plenty of topologies dedicated to the BMS active balancing, for instance, cell-to-cell charge balancing, cell-to-stack or stack-to-cell charge sharing, and stack charge sharing. Among such wide techniques cell to stack and stack-cell, charge-sharing techniques gain the upper hand because of their robustness and safety measures against the battery.

2.2 Active Balancing Topologies for BMS

2.2.1 *Type Ia : Combination of Buck and Boost Converter*

2.2.2 *Type Ia : Combination of the Buck/Boost Converter :*

The figure2.1 illustrates the Type Ia balancing method for a battery system with n series-connected cells. The description is stack-to-cells-to-stack in accordance with the accepted nomenclature. A buck converter serves as a charging unit that distributes charge from the stack to the chosen cells. A boost converter reverses the process of discharge.

The boost converter's input and output voltage ranges must be large enough to accommodate cells with voltages ranging from 1 to n-1. All cells can be actively charged and discharged up to the top level of the stack in this manner. It is only possible for nearby cells to balance numerous cells at once. Access to all cells below the topmost cell is used to balance that cell.

This section explains the balancing procedure shown in Figure 2.1. The buck converter feeds Cell 1 with energy from the stack through switch S_wA1 . The converter output current I_{Buck} is used to charge Cell 1. With the converter input current boost, the boost converter simultaneously discharges Cell 1 and Cell 2 through S_wB2 . The sum of the current in Cell 1 is 0A since $I_{Buck} = -I_{Boost} = I_{Bal}$, while Cell 2 discharges with I_{boostA} (negative balancing or "discharge mode"). The buck converter is often connected higher than the boost converter Batteries in Charging Mode. Discharging is done in the opposite order.

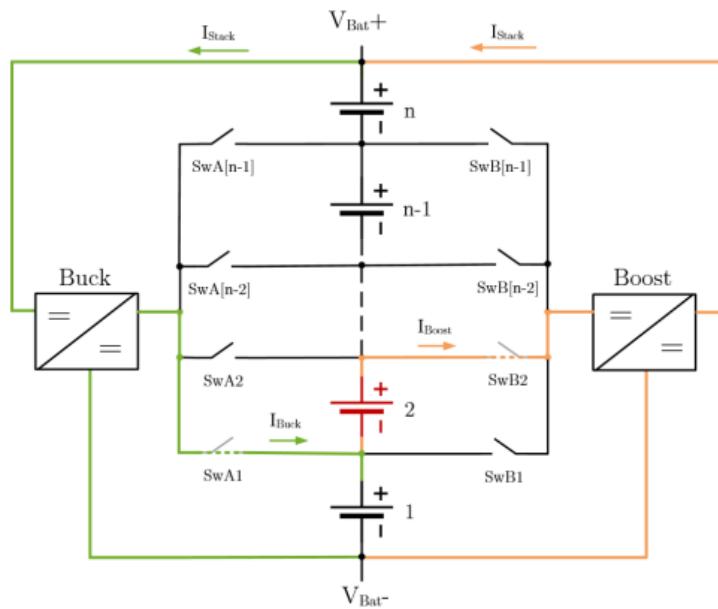


Figure 2.1: Type Ia: Active Battery Balancing

The idle cell currents can be expressed as a vector following 2.2. It accounts for the balancing currents, both positive and negative, as well as the resulting stack current.

$$\vec{I}_{Cell} = \vec{I}_{stack} + \vec{I}_n \cdot I_{Bal} - O\vec{U}T \cdot I_{Bal} \quad (2.1)$$

$$I_{stack} = I_{Bal} \left(\frac{1}{\eta} \sum \vec{I}_n - \eta \sum \vec{O}ut \right) \quad (2.2)$$

$$O\vec{U}T = \begin{pmatrix} S_{B1} \\ \vdots \\ S_{B[n-1]} \end{pmatrix}, S_x = \{0 \dots 1\}, \vec{I}_n = \begin{pmatrix} S_{A1} \\ \vdots \\ S_{A[n-1]} \end{pmatrix} \quad (2.3)$$

where \vec{I}_n and $O\vec{U}T$ are the vectors of the switch signals $S_{A[x]}$ and $S_{B[x]}$, respectively. The converter power and overall losses depend on the stack's n cells and the location of the balanced cell inside it. They rise as the position and the number of cells increases. $I = J$ when a single cell is in balance, In the absence of that, I stands for the bottom cell of the balancing group and j for the top one. As a result, I and j is always true.

The necessary converters can be the traditional buck and boost converters depicted in Figures 2.2 and 2.3. A synchronous design can be adopted, in which the diode is replaced with an actively regulated MOSFET to eliminate losses and to improve the efficiency of the converters across the whole operating range.

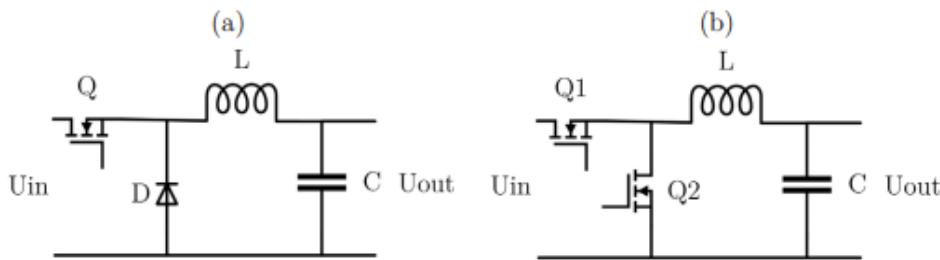


Figure 2.2: Conventional Buck (a) and synchronous Buck(b) Conveter

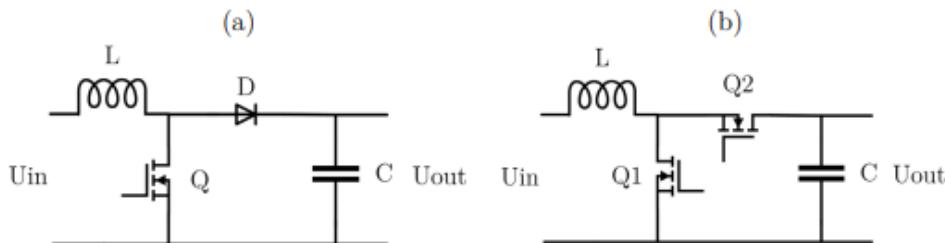


Figure 2.3: Conventional Boost (a) and synchronous Boost(b) Conveter

2.2.3 Type Ib : Type Ia with a bidirectional converter :

In terms of balancing routes, *Type Ib* is comparable to *Type Ia*. Bidirectional converters are used in place of unidirectional ones. Figure 6.9 depicts the schematic for potential hardware implementation.

2.2.4 Type IIa : Buck-boost converter :

The Type IIa of the discussed balancing techniques is shown in Figure 50. Once more, n cells are arranged in series to make up the battery system. The description is cells-to-cells following the accepted nomenclature. This approach is comparable to cell bypassing if the load current and balancing current are the same. In discharge mode, a buck converter moves charge from one cell or many neighboring cells to its subjacent cells in the stack. A boost converter transfers charge in the other direction when it is in charge mode. A single bidirectional buck-boost converter can be created by combining the two converters. A

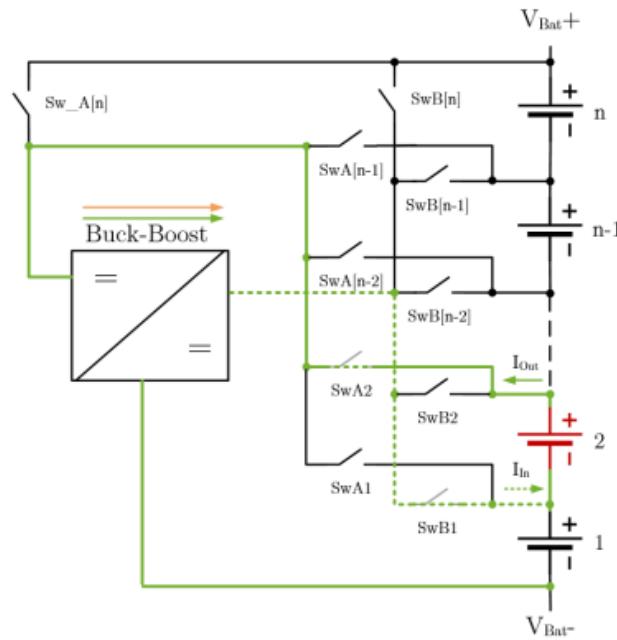


Figure 2.4: Type IIa : Buck-boost converter

bidirectional buck-boost converter made up of both converters is possible. To support 1 to n cells, the buck-boost converter's input and output voltage ranges must be sufficiently broad. Only cells that are close to one another can balance numerous cells at once.

The explanation for the balancing procedure shown in Figure 2.4 is given in the paragraphs that follow. Switches $S_{wA[2]}$ and $S_{wB[1]}$ in the buck converter allow the energy from Cells 1 and 2 to be transferred to Cell 1. It releases cells 1 and 2. The converter output current I_{In} charges cell number one. In turn, Cell 1 is charged with $(I_{In} - I_{Out})$ A while Cell 2 is discharged with I_{Out} A (negative balancing). I_{Out} becomes I_{Bal} . In most cases, charging occurs when the DC/DC converter is connected in parallel to the desired cells and is in boost mode. However, in buck mode, discharge is performed in the same manner. Same charge and discharge operations as with Type I are possible through switches $S_{wA[n]}$ and $S_{wB[n]}$.

Depending on the number of balanced cells, the resulting cell current can be expressed

as a vector:

$$\vec{I}_{Cell} = \vec{I}_n \cdot I_{Bal} + \eta \cdot \frac{\sum \vec{I}_n}{\sum I_{Out}} \cdot \vec{I}_{Out} \cdot I_{Bal} \quad (2.4)$$

$$O\vec{U}T = \begin{pmatrix} S_{B1} \\ \vdots \\ S_{Bn} \end{pmatrix}, S_x = \{0 \dots 1\}, \vec{I}_n = \begin{pmatrix} S_{A1} \\ \vdots \\ S_{An} \end{pmatrix} \quad (2.5)$$

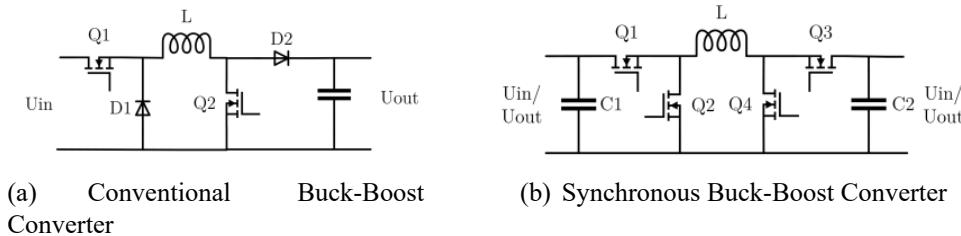


Figure 2.5: Typical Buck-Boost Converters

Figure 2.5(a) depicts a potential buck-boost converter implementation. The N-MOSFET Q2 is disabled for buck mode, and Q1 is turned on and off. Q1 is constantly on in boost mode while Q2 is actively switched. The four-switch buck-boost converter from Figure 2.5(b) may be used instead to enable synchronous mode.

2.2.5 Type IIb : Bidirectional buck-boost converter :

In terms of balancing routes, *Type IIb* is comparable to *Type IIa*. A bidirectional buck-boost converter is employed instead of a traditional (unidirectional) one. Because not every cell level requires a connection to both input and output, the number of MOSFETs needed in the switch-matrix is decreased. The same equations and exact operations are true for *Type IIa* as well. Figure 2.6 displays the diagram and the power paths[4][p. 60]. A four-switch buck-boost converter similar to the one in Figure 2.5(b) can be used to realize the necessary bidirectional buck-boost converter. The ability to run the converter in a synchronous mode in both directions is a benefit of this design.

2.2.6 Type IIIa : High - and low-side buck-boost converters :

The system's implementation using high- and low-side buck-boost converters are shown in Figure 2.7. Similar to *Type I*, the operation involves the transfer of charge sequentially rather than simultaneously. There are two phases to the balancing process: one for the boost operation and one for the buck operation. The description is stack-to-cells-to-stack following accepted nomenclature. The high-side converter and low-side converter shouldn't work in the same direction at the same time to maintain a low average stack current throughout the two phases. To demonstrate how the high-side converter works in this example, balancing routes for *Cell [n-1]* are also given in

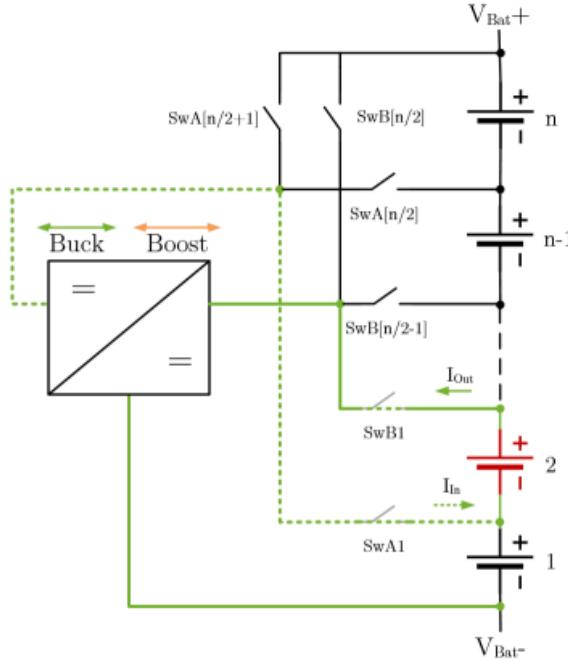


Figure 2.6: Type IIb active balancing architecture

addition to *Cell 2*[4][p. 62]. Four converters, which can carry out the two phases concurrently, are used in an expanded version of this architecture[4]. There are more conceivable combinations: Another high-performance variant can be created by fusing the Type II concept with the Type III high-side converter.

During Phase 1, the low-side converter functions as a boost converter, discharging *Cells 1* and *2* through S_{wA} with the converter's input current I_{Bal} , identical to Example 2.7. *Cell [n-1]* and *Cell [n]* are simultaneously charged with I_{Bal} by the high-side converter while operating in buck mode. Phase 2 involves charging *Cell 1* in buck mode and discharging *Cell [n]* in boost mode to achieve the same balancing results as in Section (Results will be published in the upcoming chapters). I_{Bal} is used to charge and discharge *Cell [n-1]* and *Cell 2*.

A common ground connection allows the low-side converter to access all cells up to the middle of the battery stack, including *Cell [n/2]*. It can be executed as depicted in Figure 6.10. The design is made simpler by the fact that the two operating modes are only required in one direction. To enable synchronous operation for both modes, only two MOSFETs are required. If switch Q1 is not controlled, the MOSFET's intrinsic antiparallel diode enables normal operation albeit with lower efficiency.

The remaining cells are connected to the high-side converter through a shared V_{Bat+} link. It is similar to the common ground converter in terms of design, but it has a distinct structure (see Figure 2.7).

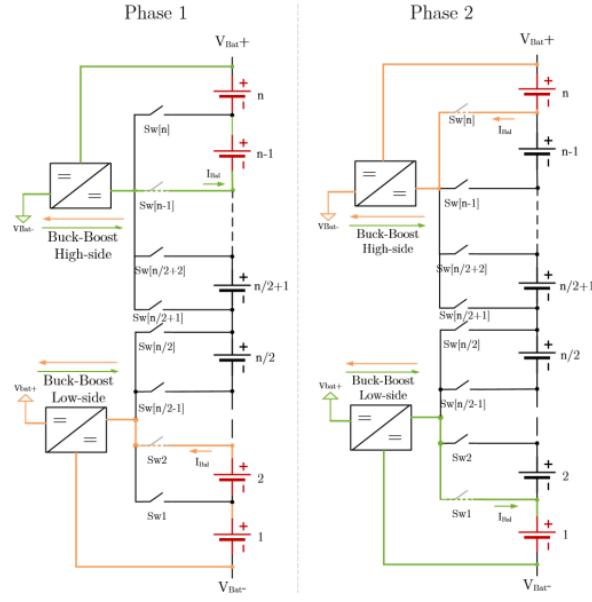


Figure 2.7: Type IIIa active balancing architecture

2.3 Proposed Active Balancing Method

The proposed architecture for the BMS active balancing is very similar to the *type IIa* and *IIb* active balancing. In the proposed topologies the charge is transferred either from imbalance cell to stack or vice versa. A bidirectional high and low-side buck-boost converter is used in the proposed architecture in place of the typical (unidirectional) buck-boost converter. Refer 2.9 to the Architecture to see how the switch matrix is set up to connect each battery node to the DC/DC converter's low side. The top of the battery pack is directly attached to the high side of the DC/DC converter. The

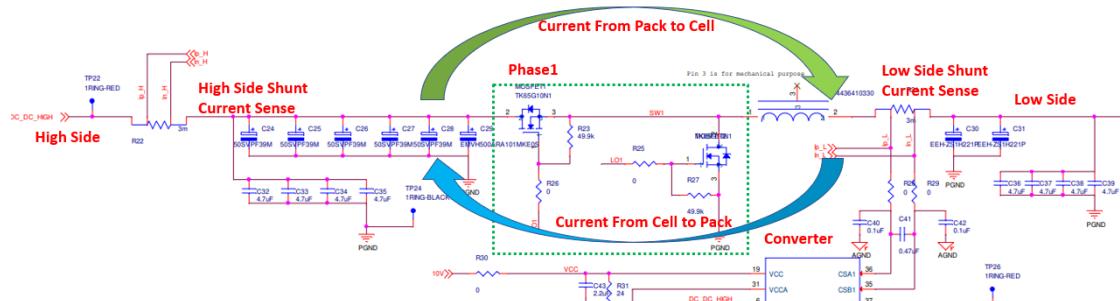


Figure 2.8: Shematic of the High/Low side DC/DC converter

proposed architecture 2.8 gives more control over the balancing current that is flowing in the DC/DC controller. One of the acute advantages of the input (With High side shunt Resistance) and output current (With Low side shunt Resistance) to the DC/DC converter. The section gives a more elaborate description and technical details of this configuration.

2.4 Overview of Active balancing BMS Architecture

Figure 2.9 shows the overview of the Inventvm wireless BMS architecture. From the Hardware point of view, the Architecture is separated into two parts one Cell Management Unit (CMU) which sits on each battery. The other one is MMU which is on the main motherboard to control the overall functionality of the BMS. The working procedure of the architecture is as follows

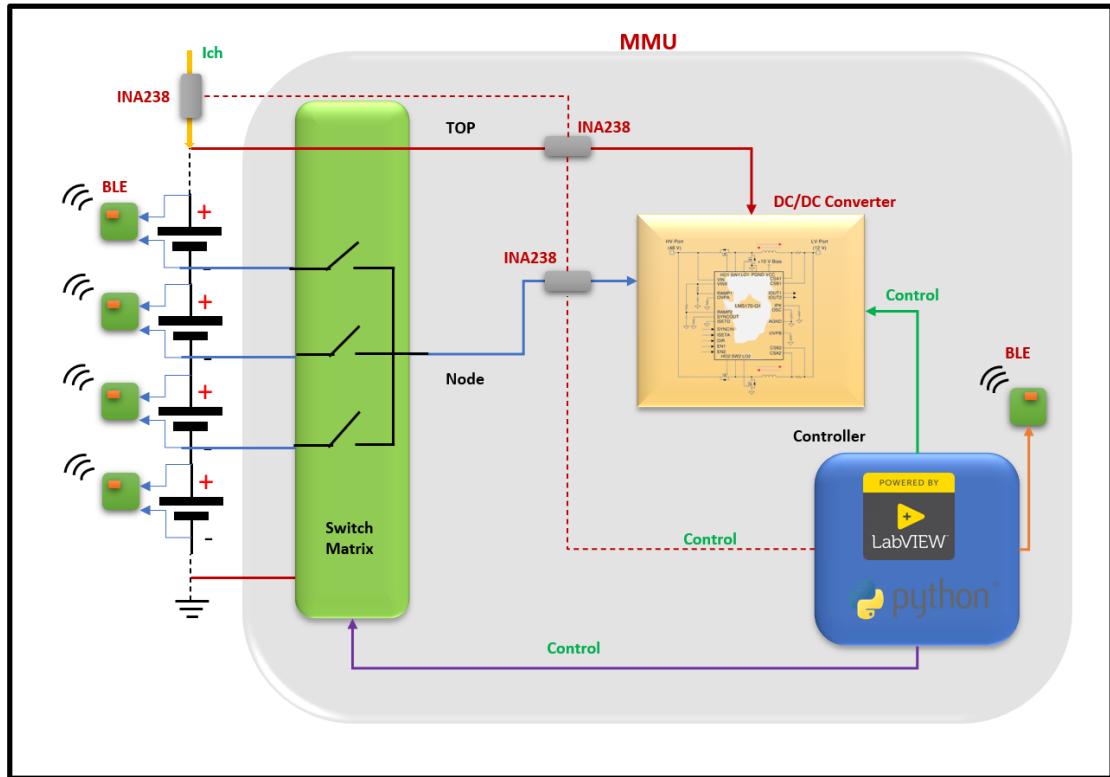


Figure 2.9: BMS Architecture

- The CMUs of each battery contains Bluetooth modules, for our applications we have used BLUENRG-355mc which will sense the live battery voltage and the temperature of the battery(using NTC).
- CMUs will synchronize with the master present on the MMU. According to the master request, all the CMUs Bluetooth will send the data to the Master in the given time slot.
- On request of the controller, the master(BLE on MMU) will collect packets from all the slaves(CMUs) and hand over the decoded data (Voltages of the Batteries and Temperature measurements) to the Controller on the MMU.
- The controller in this project is the PC, it could be a microcontroller also. The controller will be responsible for running all the BMS algorithms and detecting which node needs to be balanced depending on the CMU's battery voltages.

- In this particular project, the controller will use LabVIEW and python to build a complete BMS model and algorithm.
- Through the open circuit voltage(Battery voltages) received from the CMU, the controller will calculate the initial SoC(The open circuit voltage directly proportional initial SoC of the battery "manufacturer open circuit voltage to SoC curve").
- Once the controller finds the imbalance node through the initial SoC estimation from the open circuit voltages of the battery, the switch matrix is switched to the imbalance node and directly connected to the low side(Output) of the DC/DC converter.
- Depending on the battery imbalance the controller will configure the DC/DC converter either in buck or boost mode.
- During the Balancing, the input and output current of the DC/DC is monitored to calculate the balancing current, if the balancing current reached the threshold the DC/DC converter current is dropped.
- If the batteries are charging during the balancing the charging current I_{ch} (Figure 2.9) is also monitored through the pack current sensor.

2.5 Retrospect of BMS Hardware

2.5.1 Multiphase Bidirectional DC/DC Current Controller LM5170-Q1

The LM5170-q1[16] controller is a high precision dual phase bidirectional converter applied in automotive 48 Volts and 12Volts dual battery systems. Depending on the Direction Signal DC/DC converter regulates the average current. The Regulated current through the DC/DC converter can be programmed by analog or Digital PWM inputs.

The LM5170-q1[16] has a dedicated dual phase differential current sense amplifier to monitor the current flowing through the Dc/Dc converter, which can achieve 1% current sense accuracy. It has a Robust Gate driver to drive half the bridge. The Internal gate driver of the LM5170 has the capability of driving parallel MOSFET switches with a capacity of 500Watts. The synchronous diode emulation mode prevents the dc to dc converter from the negative currents and also enables the discontinuous mode of operation. This property enhances the DC/DC converter efficiency tremendously. The Controller can offer benefits of cycle-by-cycle current limitation, overVoltage protection at both low side and high side ports, Temperature protection and Mosfet failure so on...

An innovative average current mode control scheme maintains constant loop gain, allowing a single R-C network to compensate both buck and boost conversion[16, p .2],[3]. The oscillator is adjustable up to 500 kHz and can synchronize to an external clock. Multiphase parallel operation is achieved by connecting two LM5170 controllers for 3- or 4-phase operation, or by synchronizing multiple controllers to phase-shifted clocks for a higher number of phases. A low state on the UVLO pin disables the LM5170 in a low current shutdown mode[16].

2.5.1.a Definition of IC LM5170 Operation Modes:

- **Shutdown Mode:** When the UVLO pin is < 1.25 V, $VCC < 8$ V, or default < 1.25 V, the LM5170 is in shutdown mode with all gate drivers in the low state, all internal logic reset, and the VINX pin disconnected from the VIN pin. When $UVLO < 1.25$ V, the IC draws $< 20 \mu A$ through the VIN and VCC pins[16].
- **Initialization Mode:** When the UVLO pin is > 1.5 V but < 2.5 V, $VCC > 8.5$ V, and $nFAULT > 2$ V, the LM5170 establishes proper internal logic states and prepares for circuit operation[16].
- **Standby Mode:** When the UVLO pin is > 2.5 V, $VCC > 8.5$ V, and $nFAULT > 2$ V, the LM5170 first performs fault detection for 2 to 3 ms. During this time, the external power MOSFETs are each checked for drain-to-source short-circuit conditions. If a fault is detected, the LM5170 returns to shutdown mode and is latched in shutdown until reset through the UVLO or VCC pins. If no failure is detected, the LM5170 is ready to operate. The circuit breaker MOSFETs are turned on and the oscillator and ramp generators are activated, but the four gate drive outputs remain off until the EN1 or EN2 initiate the power delivery mode[16].
- **Power Delivery Mode:** When the UVLO pin > 2.5 V, $VCC > 8.5$ V, $nFAULT > 2$ V, $EN1$ or $EN2 > 2$ V, DIR is valid (> 2 V or < 1 V), and $ISETA > 0$ V, the SS capacitor is released and the LM5170 regulates the DC current at the level set at the ISETA pin[16].

2.5.1.b Bench setup and operation of the DC/DC Converter :

Although LM5170 can perform full bridge operation, we need only the half-bridge with a full current rating for our application. Figure2.10 only the high side bridge is used for buck and boost operations. The Figure shows the typical setup to operate the DC/DC converter in the bidirectional power system environment. The combination of the Load on the High side is the Battery pack Top and on the Low side, the is Battery pack node. A current Can flow from the High side to the low side or vice versa depending on the direction. The direction of the current flow depends on the BMS algorithm. A

BMS algorithm decides which no needs to be balanced depending on batteries voltage difference.

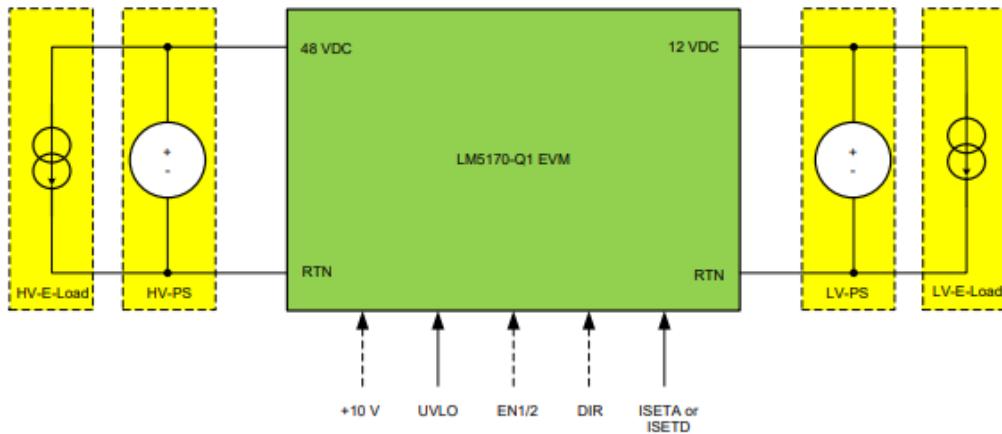


Figure 2.10: LM5170 DC/DC Converter Operation Setup [2],[3]

2.5.1.c The operation of the DC converter is as follows (The Figure 2.10) :

- Connect the High side and Low side Battery pack nodes (Low or High side could be electronics loads also).
- Apply a voltage $> 2.5 \text{ V}$ and $< 6 \text{ V}$ to the UVLO pin to release it from the shutdown mode.
- Select the EN1 or EN2 to enable the dc to dc converter output, for instance, EN1 is the output enable signal for phase1 and EN2 is the output enable signal for phase 2.
- Depending on the mode of operation Apply DIR pin voltages. Direction command input. Pulling DIR above 2 V sets the converter to buck mode, which commands the current to flow from the HV-Port to LV-Port. Pulling DIR below 1 V sets the converter to boost mode, which commands the current to flow from the LV-Port to HV-Port. If the DIR pin is left open, the LM5170 detects an invalid command and disables both phases with the MOSFET gate drivers in the low state[3, p .5].
- Use the ISETA signal to set the current.ISETA is the analog current programming pin. The inductor DC is proportional to the ISETA voltage. Use either ISETA or ISETD but not both for phase current programming. When ISETA is not used, connect a 100-pF to 0.1- μF capacitor from ISETA to AGND[3, p .5].
- If the ISETD is used, The PWM current programming pin. The inductor DC level is proportional to the PWM duty cycle. Use either ISETA or ISETD but not both for phase current programming. When ISETD is not used, short ISETD to AGND [3, p .6].

2.5.1.d Summary of the DC/DC Converter:

Although DC/DC Converter LM5170 is capable to use the dual phases, we have limited the DC/DC converter to the single phase according to the Type ii BMS DC/DC converter configuration. Depending on the user's need user can use ISETA or ISETD to setting the current flowing in the dc to dc converter. For Instance, if the user uses a microcontroller it is much more convenient to use the PWM, so the ISETD is a natural choice, If the user opts Central pc/ Labview application it is much better to use ISETA through some analog supply. Ultimately ISETD (PWM) converted to the Analog voltage to set the current.

2.5.2 Switch Matrix :

Automotive BMS applications demand sophisticated and robust switch matrices, as in the market there are no switch matrix will available according to the application. There has been specific knowledge used to pick this switching component. Switching components are more unlikely than the conventional components, such a vote for picking the switching components always registered for the high power MOSFETs because of various technological advantages over conventional electro-mechanical switches. Since the component choice is entirely left to the design engineer, it is always a good practice to design these switch matrix boards from scratch to have full control over the system. The following sections will give more insights into the switch matrix. Single or double back-to-back FETS are used for the switch matrix, back to back MOSFETs are two MOSFETs housed in a single package or externally by connecting the gates of FETs are common. The Figure2.11 implicates one such example of a switch matrix using the back-to-back MOSFETs.

2.5.2.a The initiative understanding behind choosing the switch matrix MOSFET:

- Low R_{ds} ON; low on-state resistance implicates that MOSFET can carry high DC with lower dissipation.
- High Blocking voltage; High blocking voltage between the drain and the source ensures the breakdown safety of the MOSFET against the full Battery pack voltage.
- Low gate area - to drive the FET faster, and it cost less than the current budget for the FET's gate driver.
- Low gate drive voltage. So-and-so forth.

By analyzing the criteria mentioned in the section, the choice is made to use STD20NF06L for the switch matrix. The component specification is as follows : STD20NF06[17] is the high-power MOSFET that has been developed for automotive

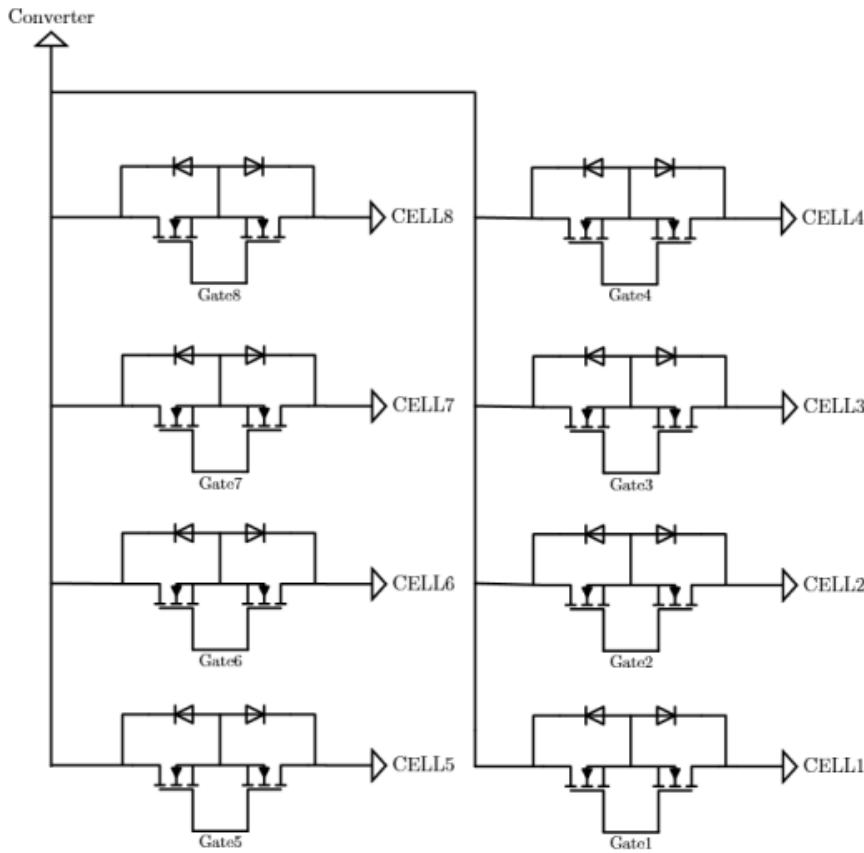


Figure 2.11: Typical Mosfet switch matrix for 8 batteries [4]

applications to handle the High current with very low input gate capacitance. The FET has perfect dv/dt. STD20NF06 is DPACK package which is quite big compared to SMD package and single package dual back-to-back FET's, yet the FET is opted for because of the following benefits. The back-to-back FET arrangement is made externally as shown in Figure 2.11. for more insights into the component refer to the MOSFET Datasheet [17].

STD20NF06L Datasheet			
Symbol	Parameter	Value	Unit
V_{ds}	Drain-source voltage	60	V
V_{gs}	Gate-source voltage	± 18	V
I_d	Drain current (continuous) at $TC = 25 \text{ deg C}$	24	A
P_{Tot}	Total power dissipation at $TC = 25 \text{ deg C}$	60	W
$\frac{dv}{dt}$	Peak diode recovery voltage slope	10	V/ns
C_{iss}	Input capacitance VDS $= 25 \text{ V}, f = 1 \text{ MHz}, VGS$ $= 0 \text{ V},$	660	C
$R_{ds(on)}$	Static drain-source on-resistance	@VGS = 10V, @ID = 12A, 32	Ω

2.5.3 Matrix Switch Gate Driver :

Modern BMS application is suffocated by the hot swapping of the Batteries for balancing. When the battery node is switched in the battery pack to balance the battery node matrix(swapping circuit) the MMU will see an immense current that is flowing from the battery [18]. when the switch matrix is switched to a particular node of the battery pack. The battery Node will be directly connected to the output node of the DC/DC converter (The low side of the DC/DC Converter refers to the circuit 6.6 @low side), which will be having reservoir capacitor that will sink an immense amount of the current from the battery in very short time this will cause switching FET to burn, so it essential to switch FET very carefully. such technique is called "Hot Swap". "Hot Swap" is FET switching technique Figure2.11, more often used in live power switch applications. The technique allows the gate driver circuit to monitor the current flowing through the switch circuit by the input sense resistance. By any chance Hot swap circuit doesn't allow the rapid surge of the load current in the switch circuit [18].

2.5.3.a LTC4231 :

LTC4231 is an Analog Device Inc Micro power hot-swap controller that is employed to face circuit board insertion and abrupt live power supply. An internal high-side switch driver controls the gate of an external N-channel MOSFET. Back-to-back MOSFETs can be used for reverse supply protection down to -40V [18].

The LTC4231 provides a debounce delay and allows the GATE to be ramped up at

an adjustable rate. After startup, the LTC4231's quiescent current drops to $4\mu A$ during normal operation with output active. UVL, UVH, OV, and GNDSW monitor overvoltage and Undervoltage periodically, keeping total quiescent current low. Pulling SHDN low shuts down the LTC4231 and the quiescent current drops to $0.3\mu A$.

During an overcurrent fault, the LTC4231 actively limits current while running an adjustable timer [18]. The LTC4231-1 remains off after a current fault while the LTC4231-2 automatically reapplies power after a cool-down period[18].

A typical circuit diagram and the operational waveforms of the LTC4231 are described in the Figure6.8. For more technical details refer to the ADI LTC4231 datasheet[18].

2.5.3.b Inrush Current Control by LTC4231 :

In most, automotive applications keeping the inrush current low and in control is essential to avoid catastrophic damage to the switching circuits. LTC4231 takes a golden hand in controlling the inrush current by startup method (Timer Delay varying). The equations 2.6 implicate the Inrush current controlled by the LTC, the Inrush current highly depends on the gate capacitance of the switch, and the output capacitance of the DC/DC capacitance (load Capacitance C_L). A capacitor C_G of the Gate to the GND can be used to control the gate voltage slew rate for the Inrush current in the Switch.

$$I_{InRush} = \frac{C_L}{C_G} \times 10\mu A \quad (2.6)$$

The V_{GATE} of the switch raise with the slope of $10\mu A/C_G$. Once V_{GATE} crosses the

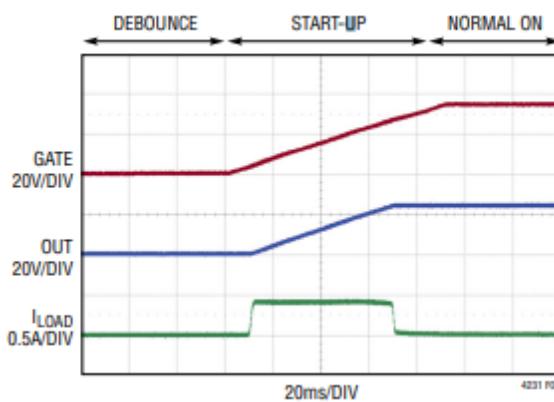


Figure 2.12: Inrush Control by Limiting V_{GATE} Slew

V_{th} , status goes high impedance. see the figure2.12 which explains the Inrush current protection when the $\Delta V_{Th(GATE)}$ crosses the gate voltage threshold.

The Design Example in the Chapter6 explains, how to pick the design parameters to design the inrush current limit and gate driver, please follow. LTC4231 holds a wide

range of advantages compared to the gate driver that is available in the market such Wide Operating Voltage Range: 2.7V to 36V, Reverse Supply Protection to -40V n Adjustable Analog Current Limit with Circuit Breaker n Automatic Retry or Latchoff on Current Fault n Overvoltage and Undervoltage Monitoring n Controls Single or Back-to-Back N-Channel MOSFETs [18]. By considering all the facts we have picked the LTC4321 as the gate driver for the switch matrix.

2.5.4 Current Sense :

As elaborated in the BMS architecture High precision current sensors are used to monitor the BMS Currents. The currents are mainly monitored by the sensor charging current that is entering through the Battery pack Top and balancing current that is entering or leaving from the DC to Dc convert to the Balancing node from Battery pack TOP.

For Inventvm active balancing BMS application, The team has selected INA238 Current sensor from Texas instruments. Chapter 3 gives an extensive explanation for choosing the INA238[5] and the application 3.4.

2.5.5 Wireless Communication Hardware :

The Bed Rock Idea behind the Inventvm active balancing BMS is to make the BMS architecture in the Wireless Communication Environment. The wireless communication architecture will reduce the immense pain of hard wires for communication in modern smart EVs. The Wireless Communication picked for the project is the Bluetooth stack, Chapter 1 takes the privilege to explain the Bluetooth Hardware choosing criteria, and design the proprietary Bluetooth solution for the projects. The BLUeNRG-355MC[8] and the Nordic[9] are the Bluetooth solutions employed in the project.

2.6 Summary of Chapter 2

The initial phase of the chapter 2 summarizes the different topologies of the BMS active balancing, more or less, many of the topologies remained on the shelf, because of the less robustness and clumsy implementation. The proposed topology2.8 for the BMS active balancing is inherited from topology *Type IIa* and topology *Type IIb*. Currently, by using the proposed methodology2.8, we can successfully perform the active balancing for batteries. The active balancing BMS architecture2.9 will give a much broader view in this chapter 2, but in this architecture2.9, I have not discussed how to calculate the SoC and SoH but following Chapters(SoC and SoH calculation chapter not yet updated) will give more extravagance on the SoC and SoH calculation and synchronization methods of the voltage and current. I have succeeded in explaining most of the BMS hardware except the current sensors because I have dedicated a separate chapter to explaining the

current acquisition and synchronization(Current and Voltage synchronization chapter not yet updated) of the measurements.

Chapter 3

Current Measurement For SoC Estimation

SoC is the most crucial parameter of the battery to estimate in the BMS. In the deal case, the SoC of the battery has to be measured continuously, well which is not feasible since we have a measuring setup (sensors) we need to discretize the time and, measure how much current flows through the battery to estimate the soc. To be precise in the current measure to estimate battery soc we need to account for all currents that flow in and outwards from the battery. In the active balancing setup, we have a minimum of three currents that need to be synchronized to estimate the battery soc, DC/DC converter input and output currents, and battery pack charging and discharging current. In an integrated circuit solution current measuring is very easy by designing all the sensors operating with a master clock and reading by an internal bus. Since the project is at a discrete solution level we have several current sensors associated with reading the currents. The following sections elaborate on a competitive solution for current reading and its usage in the project.

3.1 Current Sensing

To address the difficulties of creating an accurate current-measurement circuit for cost-effective applications, designers have a variety of choices at their disposal. The best flexibility is provided by using general-purpose operational amplifiers (op amps)

or analog-to-digital converters (ADCs), they could be standalone or embedded in a microcontroller (MCU). While also leveraging a wide range of tailored components that are specifically made for current sensing but also address challenges in a specific way [19]. Shunt resistors(Kelvin method) and/or hall sensors are the two methods more widely used methods in automotive BMS applications to measure the battery pack current(Charging/Discharging and Balancing current). The integrated solutions for measuring current is more preferable, to secure the space and power constraints in automotive applications. The following sections will give more insights into the current sense methods.

3.2 Hall Effect Current Sensors

”The Hall effect is the creation of a voltage difference (the Hall voltage) across an electrical conductor that is transverse to an applied magnetic field perpendicular to the current and an electric current in the conductor”. Well, that is a bit of a more scientific and deep mathematical explanation of the Hall effect. If I take a little leverage to explain the Hall effect in the nomenclature The Current flow in the conductor causes to induce magnetic flux inside the magnetic core, these fluxes also turn out a small potential, which can be called hall voltage. The Hall voltage dropped across the coil (Magnetic) is directionally proportional to the current flowing in the conductor. A galvanically isolated Hall effect current sensor capable of DC or AC measurement with high accuracy, excellent linearity, and temperature stability[20]. Let us explore hall sensors with some typical examples in the BMS such as the TMCS1107xx [20] series from the TI are the most popular and competitive galvanic solutions for measuring the current.

3.2.1 TMCS1107xx Sensors :

The TMCS1107-Q1 is a galvanically isolated Hall effect current sensor with high accuracy, great linearity, and temperature stability for measuring DC or AC currents. A signal chain with low drift and temperature compensation offers a 3% full-scale error over the device temperature range.

A magnetic field is created by the input current flowing through an internal 1.8-m conductor, which is monitored by an integrated Hall-effect sensor. This topology reduces design complexity and does away with external concentrators. Reduced conductor resistance decreases thermal and power loss. A 420-V lifetime working voltage and a 3-kV RMS minimal isolation between the current path and circuitry are provided by inherent galvanic insulation. Transient immunity and high common-mode rejection are made possible by integrated electrical shielding.

The output voltage is proportional to the input current. Fixed sensitivity minimizes

ratiometry errors and enhances supply noise rejection, enabling the TMCS1107-Q1 to run from a single 3-V to 5.5-V power supply. When current enters the positive input pin, it is regarded as having a positive polarity. There are options for both unidirectional and bidirectional sensing.

Input current to the TMCS1107-Q1 passes through the isolated side of the package lead

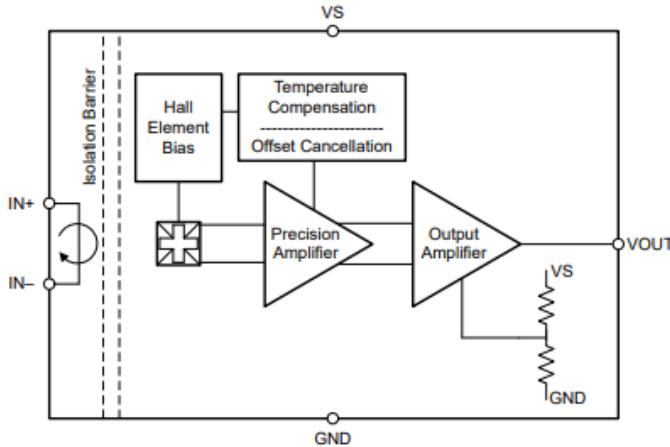


Figure 3.1: TMCS1107xx Hall sensor Block diagram

frame through the IN+ and IN– pins. The current flow through the package generates a magnetic field that is proportional to the input current and measured by a galvanically isolated, precision, Hall sensor IC. As a result of the electrostatic shielding on the Hall, sensor die, only the magnetic field generated by the input current is measured, thus limiting input voltage switching pass-through to the circuitry[20].

3.3 Shunt Resistors for Battery Current Measurement

Sensing the voltage drop across a shunt or current-sense resistor 3.2 to determine the current in the most typical way. It is necessary to look at the parametric values of both the resistor and current-sense amplifier to obtain a very precise measurement of the current. Accuracy loss must be prevented by carefully planning the connections between the current-sense amplifier and the resistor.

INA2XX series shunt current sensors are the most competitive solution offered by TI to measure the high-side and low-side shunt current with high precision. INA238 is used in this project to measure the shunt current, bus voltage, and several other parameters. Section 3.4 will talk extensively about the INA238 and the features offered by the sensor to synchronize current measurements for BMS application.

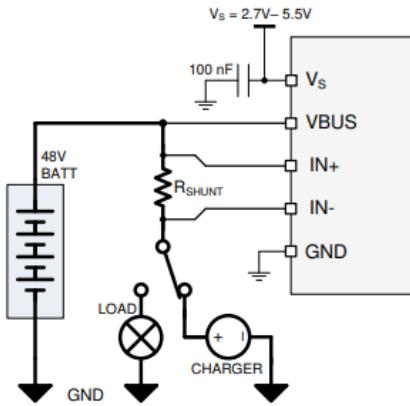


Figure 3.2: INA238 High-Side Shunt Current Sensing

3.4 INA238/INA2xx

The INA238 is a 16-bit delta-sigma ADC with an ultra-precise digital power monitor that is made primarily for current-sensing applications. With a common-mode voltage support range of -0.3 V to +85 V, the device can measure a full-scale differential input of ± 163.84 mV or ± 40.96 mV via a resistive shunt sensing element. The INA238 does the necessary calculations in the background while reporting current, bus voltage, temperature, and power. The embedded temperature sensor is useful for tracking the system's ambient temperature and has a die temperature measurement accuracy of 1°C .

The INA238 can be utilized in accurate systems without undergoing multi-temperature calibration during production thanks to its low offset and gain drift design. Additionally, a wide dynamic range is provided without considerable power dissipation losses on the sensing shunt element thanks to the extremely low offset voltage and noise. This enables use in A to kA sensing applications. Due to the device's low input bias current, bigger current-sense resistors can be used, resulting in precise current readings in the micro-amp range. The device supports samples averaging from 1x to 1024x and adjustable ADC conversion durations from $50\mu\text{ s}$ to 4.12 ms, which further reduces noise in the measured data.

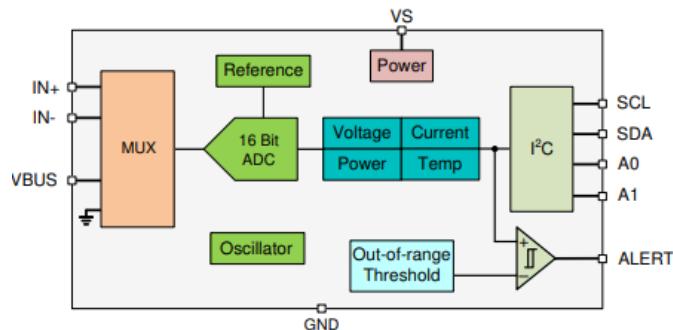


Figure 3.3: INA238 Simplified Block diagram [5]

The INA238 has a multifunctional, open-drain ALERT output pin that can be utilized to report various problems or as a sign that the ADC conversion is finished while the device is functioning in both triggered and continuous conversion mode. Every time an output value under continuous monitoring exceeds its corresponding out-of-range threshold, the diagnostics mentioned in Table 7 can be transmitted via the ALERT pin.

The diagnosis that prompted the ALERT pin can be identified by reading the DIAG ALRT register. In addition to configuring some ALERT pin functions, this register, which is depicted in Table 7, is also utilized to monitor other related diagnostics.

- Alert latch enables — In the event that the ALERT pin is activated, this feature will maintain the pin's value even after all diagnostic circumstances have been resolved. The status of the ALERT pin is reset by reading the DIAG ALRT register. By setting the ALATCH bit, this function is made available.
- Conversion ready enable — When an ADC conversion is finished and the output values are prepared to be received through the digital interface, the CONVERSION READY ENABLE signal instructs the ALERT pin to assert. Setting the CNVR bit enables this feature. Regardless of the CNVR bit set, the conversion completed events can also be read through the CNVRF bit.
- Alert comparison on averaged output — Enables comparison of the out-of-range threshold value to the ADC's averaged data values. Comparing the output data to the out-of-range threshold, this aids in further removing noise from the data to prevent false alarms brought on by noise. However, because of the time required for averaging, the diagnosis will be postponed. Setting the SLOWALERT bit activates this feature.
- Alert polarity — Allows the device to flip the ALERT pin's active state. Keep in mind that the ALERT pin is an open-drain output that requires a resistor to be pulled up. The APOL control bit can be used to change the ALERT pin's default active-low function to an active-high one.

Other diagnostic features that the ALERT pin does not report but which can be accessed by checking the DIAG ALRT register include:

- Math overflow — The MATHOF bit indicates when an arithmetic operation has resulted in an internal register overflow, which is reported.
- Memory status — The MEMSTAT bit, which monitors the non-volatile trim memory of the device, indicates the memory status. When the gadget is functioning properly, this bit should always be set to '1'.

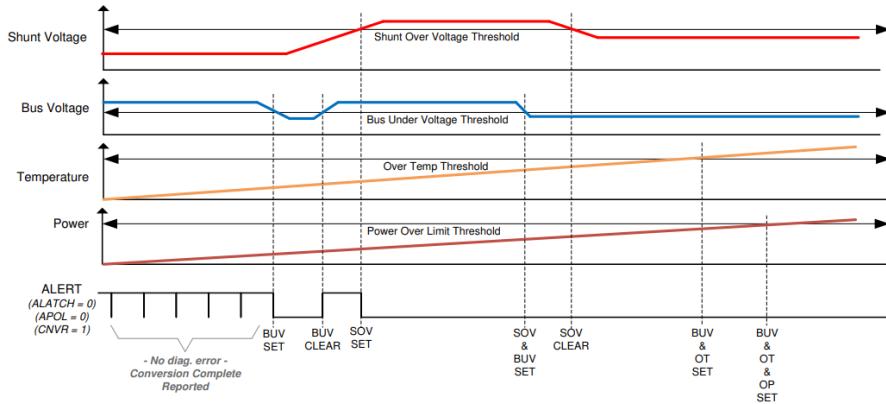


Figure 3.4: INA238 Multi-Alert Configuration

The ALERT pin becomes a multifunctional reporting output when set up to report the ADC conversion complete event. In the example shown in Figure 3.4, the INA238 device reports ADC conversion complete events while also experiencing shunt over-voltage (over current), bus under voltage, over temperature, and overpower limit events.

3.5 Current Measurements Synchronization

Section 3.4 described the very detailed view of INA238/INA2xx sensors, the essence of explaining INA is the most competitive solution for current measurements and it is the main pillar in this project to acquire current measurements and other several measurements(Shunt Voltage, Bus Voltage, ALERT). Among all measurements synchronizing the current measurements is the nail hitting. The following sections will brief different approaches to synchronize the current measurements.

3.5.1 Simultaneous Write and Sequential Read :

Thanks to the INA238/INA2xx multi-addressing functionality [5, p.18], INA operates through I2C and the address of the INA can be configured by address lines A0 and A1 pulling to Vdd or GND. Figure 3.5 shows the Simultaneous Write and Sequential Read approach. Configure all the INAs (Write Control register) simultaneously by keeping all the INA addresses the same. Address configuration can be done, by the controller. As soon as write is done all the INAs start current acquisitions and report measurements at the same instant. For reading the current measurements, configure sensor address lines to different addresses(for instance 0x40,0x41,0x44,0x44, and so on) and read current measurements sequentially from each INA.

"Simultaneous Write and Sequential Read" 3.5 approaches are reliable only for low precision and sequential data storage applications. SoC estimation is dealing with real-time current flowing in the battery, let's say a case where we write all sensors at the

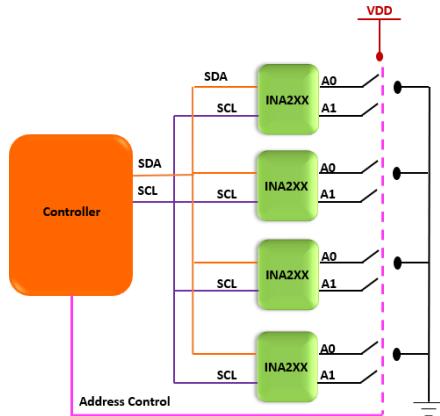


Figure 3.5: INA2xx Simultaneous Write and Sequential Read

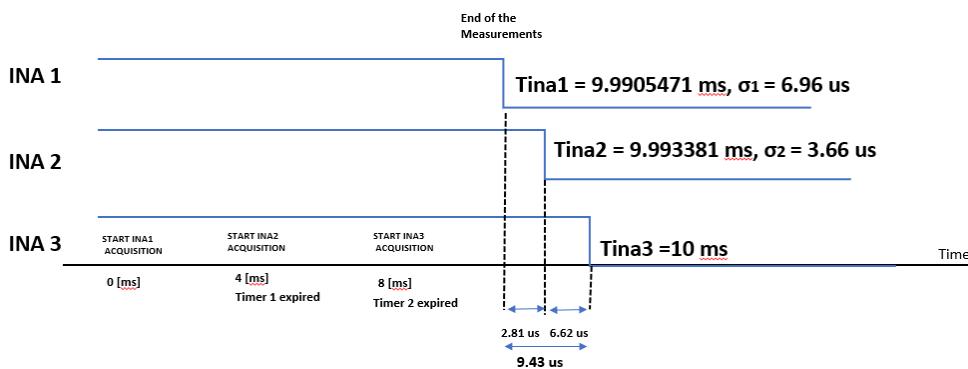


Figure 3.6: INA2xx Delayed Synchronization

same time parallelly by considering the acknowledgment but this acknowledge could be sent by any one of the sensors if any one sensor dropped in between writing the data (configuring) controller can not differentiate. The controller only gets to know the sensor is not configured or dropped after it samples the first current data. Unfortunately, by that time the battery balancing might have already started if we do not receive current measurement data from anyone's sensor we might be in deep trouble. Simultaneous Write and Sequential Read are simple to implement but it is not robust and reliable for BMS applications.

3.5.2 Synchronizing by Delayed Measurements

Depending on the MODE bits that have been specified and set in the ADC CONFIG register, the INA238 can measure the shunt voltage, bus voltage, die temperature, or any combination of these. This enables the user to further tune the monitoring function to meet the demands of the particular application by choosing modes to convert simply the shunt voltage or bus voltage.

The INA238 conversion can be delayed to synchronize with other system

components by setting the CONVDLY bits in the CONFIG register to a value between 0 (no delay) and 510 ms. The conversion delay resolution in programming is 2 ms. By default, the conversion delay is set to 0. As soon as the measurement conversion is complete the INA2xx ALERT pin asserts. Figure 3.6 shows synchronizing the 3 sensors by writing the sequential delay for instance first sensor has a conversion delay of 2ms subsequently adding other sensors' conversion delay (INA1 delay = INA2 delay + INA3 delay + 2ms). At the end of the 10ms all the sensors sample at the same time, finish the conversion and assert the alert pin. As soon as the ALERT is asserted the controller interrupts will trigger and the controller will read the data from the sensors sequentially. The point here is not reading the data sequentially or parallel important is all the sensors must sample the current at the same instance time.

3.5.2.1 Implementation of Synchronizing by Delayed Measurements Algorithm:

- Send to three INAs: the config alert command (bit 14, register Bh) and sets the CONVDLY (bits 13-6 register 0h), which is the delay for initial ADC conversion.
- When START ACQUISITION command is sent, the INA waits the time specified by CONVDLY before starting the conversion.
- CONVDLY INA 1 = 10 ms, CONVDLY INA 2 = 6 ms, CONVDLY INA 3 = 2 ms
- Two Timers are used to send the start acquisition command: Timer 1 = 4ms, Timer 2 = 4ms
- As two timers finish writing controller wait for ALERT interrupt to read data from sensors

Figure 3.6 shows the three INAs synchronize current measurement current, each INA triggered with a different delay to acquire data at the end of 10ms all the INAs are asserted alert signals. The sque of the ALERT of the INAs is quite impressive because they have responded with around 10us of sque.

So on and so forth the above sections briefed about the current sensor, features, and synchronizing methods. This section will put a more detailed view of one of the current measurement applications from BMS architecture, Power analyzer emulation, and current measurement synchronization.

3.6 Balancing Current Measurement

As discussed in chapter 2 active balancing architecture 2.9 the controller will operate the DC/DC converter either in buck or boost mode depending on the unbalanced node. The

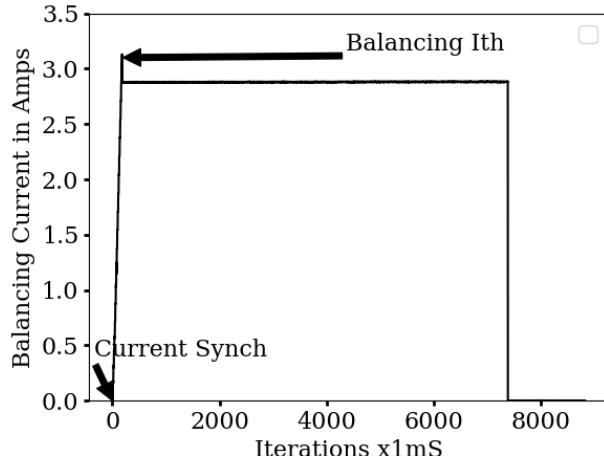


Figure 3.7: Battery Balancing Current

output current of the DC/DC converter is the total balancing current that needs to flow from the battery node to the pack or vice versa. DC/DC converter input and output both have the shunt resistor 2.9 where INAs are coupled with them to measure the current. All the currents in the architecture 2.9 are measured with the power analyzer setup as briefed in chapter 4.5.5(Measurement view), and all the INAs synchronized with the "INAs delayed measurement algorithm" approach as mentioned in section 3.5.2..1. Though, we have several currents(Charging/Discharging TOP and bottom current, DC/DC converter low and high side currents) to talk about in the architecture 2.9 I would like to stress the DC/DC output current more! 3.7. Because the output current of the DC/DC converter is the balancing current that can flow from the battery node to the battery pack or vice versa, which is one of the main currents that determine the battery SOC(charging and discharging excluded in this example). As the balancing current reaches the threshold current (shunt current threshold set by the user Figure 3.7) ALERT will be asserted by the sensor (Section 3.4) and the controller will monitor the DC/DC output shunt resistor current sensor and drop the balancing current below the threshold and maintains the same current until the balancing timer period ends.

3.7 Summery of Chapter 3

Chapter 3 provided me an opportunity to explore different kinds of current measuring sensors for the BMS application and synchronize current measurements, after a deep analysis finally we landed with INA2xx series sensors. In section 3.4, I took the advantage of explaining deeply about the current sensor, because most of the measurements and decisions are taken by the controller depend on the current sensor during the balancing for instance balancing current, balancing node voltage, balancing current thresholds, bus voltage threshold, and so on. INA current sensor ALERT signal

configuration gave an extensive chance to explore the synchronization of the current measurement estimating the battery SoC. Battery balancing current results (Figure 3.7) measured through the power analyzer model will interpolate the BMS architecture discussed in chapter 2 to the Powel Analyzer architecture in chapter 4. This chapter can also become the fundamental pillar for chapter 5 to estimate the SOC with several algorithms (synchronization with Delayed Measurements and Parallel Wite; Sequential Read).

Chapter 4

Battery Modeling and Emulation

The *Battery* is a complex composition of lethal chemicals that are very hard to handle in terms of safety and maintenance. So, is those petroleum vehicles safe? No, Not at all petroleum products and vehicles are much more dangerous not only in terms of environmental pollution it in terms of safety and measures. Then we should raise the question of what stopping modern engineers to transition from petroleum engines to Battery vehicles. And which wall stopping us from battery usage? Well, to answer all the above questions we need to look back at the evolution of vehicles, the petroleum vehicle fetus came to this world nearly a century ago. Engineers thoroughly studied and learned how to handle petroleum products and petroleum vehicles. Undoubtedly, EVs are the gift of modern technology, but it is essential to study institutionally the battery characteristics and the testing.

It is the prime responsibility of every Electrical engineer who works in EVs/Battery systems to ensure the safety of mankind. Considering all the facts, I have decided to make safety and sophisticated system for engineers to test the BMS and play with BMS without interacting with the physical batteries. The *Part I* of Chapter 4 gives more elaboration about the battery modeling and battery constructional theory. *Part II* facilitates understanding of Battery model implementation and BMS simulation through coding.

4.1 Battery Modeling

This section explains the principles of a technique for calculating the state of charge (SOC) of lithium-ion batteries using two different equivalent circuit designs. It discusses how to use typical measurements to determine these circuits' parameters. The comparison of measurement and computation results reveals good agreement. The first step ignores the effects of temperature and battery age on these parameters [6].

The Ampere-counting (Columb counting) method can be used to identify the state of charge (SOC) of a battery if a defined full charge occurs regularly. This technique is based on the amount of charge that is put into or taken out of the battery. The error in the SOC estimation can grow too big and a better solution needs to be discovered in cases where a defined full charge of the battery cannot occur frequently. A lithium-ion battery's open circuit voltage (OCV) determines the SOC; however, as shown in the figures, this method has an issue with the battery's dynamics. The electrochemical reactions that occur in a cell prevent the OCV from being measured at the battery terminals. It is necessary to theoretically model the dynamics so that the OCV or SOC may be determined by measuring simply the battery voltage and current at the terminals of the battery. It is necessary to utilize an analogous circuit design for the battery cell for this purpose, and characteristic measurements must be employed to identify the parameters. This section presents three models: the internal resistance model (IR) 4.1(a), the one-time constant model (OTC) 4.1(b), and the two-time constants model (TTC) 4.1(c). The presented models, which serve as the basis for the model-based SOC calculation, are also evaluated for validity by making comparisons between the model-based simulation data and the measured data[21].

4.1.1 Nomenclature of Battery Model

1. **Open Circuit Voltage(OCV)** : OCV is measured at the battery's open circuit terminal voltage at various SOC points when the battery is in equilibrium. A polynomial equation is used to determine the nonlinear relationship between SOC and OCV. The figure 4.2 displays an OCV subsystem. Because SOC directly affects OCV's value, the OCV subsystem includes a SOC computation component. The value of OCV controls the regulated voltage source. The voltage curve of the pulse discharge test (PDT) during relaxation can be used to determine the OCV value[22].
2. **Internal Resistance (R_0)** : Internal resistance results in a voltage drop in the equivalent circuit. Fig. 4.1(a), displays the value of the subsystem R_0 as a function of the input current and SOC. A switchable resistor utilized to transmit a resistor's internal value's physical signal. From this, one can calculate the amount of internal

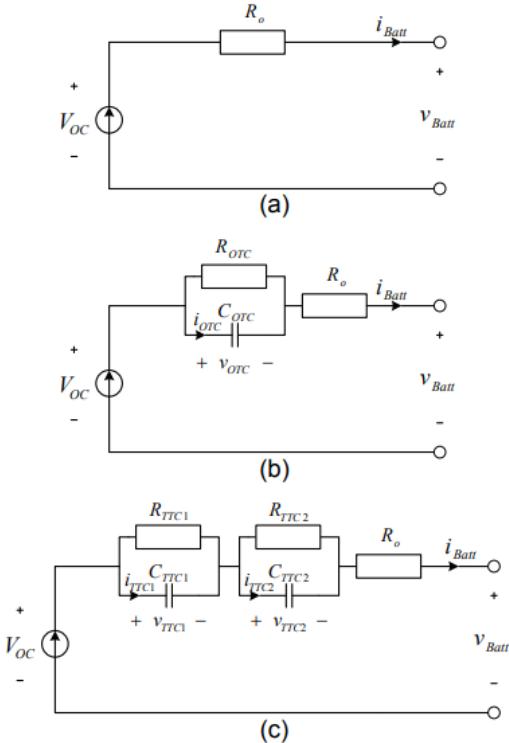


Figure 4.1: Battery equivalent circuit diagrams. (a) internal resistance model (IR), (b) one-time constant model (OTC), (c) two time constants model (TTC) [6],[6]

resistance. Instantaneous voltage following the release of the current pulse. The optimal 2-D lookup table is selected using the interpolation-extrapolation lookup method for R0's value[22].

3. **Transient Response (R1,C1,R2,C2)** : Transient response in this model is represented by RC. The transient model is again classified based on the time constant for instance $R1 \times C1 = \tau_1$ is a one-time constant model and $R2 \times C2 = \tau_2$ is the two-time constant model; Figure 4.1(b) and Figure 4.1(c). Increasing the Time constant model will serve as a realistic model battery[22].

4.1.2 IR Model :

the IR model as shown in Figure r4.1 (a), and described by Equation 4.1 implements an ideal voltage source VOC that represents the open-circuit voltage (OCV) of the battery, and an ohmic resistance to describe the internal resistance [6]. Both resistance and open-circuit voltage VOC are functions of SOC, state of health (SOH) and temperature. I_{Batt} is the battery output current with a positive value when discharging, and a negative value when charging, V_{Batt} is the battery terminal voltage[6].

$$V_{Batt} = VOC - R_0 \times I_{Batt} \quad (4.1)$$

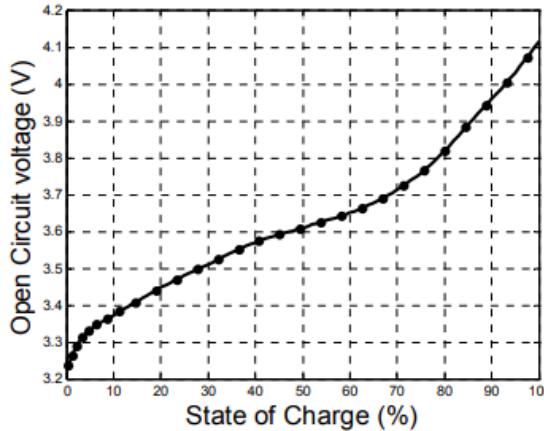


Figure 4.2: Battery OCV Vs Soc for SLPB120216216 Cell [6]

Given that the transient is not represented by the IR model Lithium-ion cell behavior is not suited for the precise SOC calculation for any dynamical operation (variable load).

4.1.3 One-Time Constant Model

A parallel RC is added by the OTC model. Network connected in series to the IR's internal resistance R0 model to approximate the lithium-ion battery's dynamic behavior. As shown in Figure 4.1 (b), it mainly consists of three parts including the voltage source V_{OC} , the ohmic resistance R0, and R_{OTC}, C_{OTC} to describe the battery transient response during charging or discharging. V_{OTC} is the voltage across C_{OTC} ; i_{OTC} is the current that flows in C_{OTC} [6] V_{OTC} is the iterative voltage of OTC model. The electric behavior of the OTC model can be expressed by Equations 4.2 and 4.3 [6] in continuous time [21]:

$$\dot{V}_{OTC} = \frac{-1}{R_{OTC} \times C_{OTC}} V_{OTC} + \frac{1}{C_{OTC}} i_{Batt} \quad (4.2)$$

$$V_{Batt} = V_{OC} - \frac{1}{C_{OTC}} V_{OTC} - R_0 \times i_{Batt} \quad (4.3)$$

The equation 4.4 and ?? (where: T_s sampling period, T_s and τ_{OTC} time constant.) represents the discrete time voltages of the one-time constant model, They are very much helpful for the advanced algorithms to calculate the SoC such as Kalman, Extended Kalman etc.

$$V_{OTC,k+1} = e^{\frac{-T_s}{\tau_{otc}}} V_{OTC,k} + R_{OTC} \left(1 - e^{\frac{-T_s}{\tau_{otc}}} \right) i_{Batt,k} \quad (4.4)$$

$$V_{Batt,k} = V_{OC}(SOC_k) - V_{OTC,k} - R_0 \times i_{Batt} \quad (4.5)$$

4.1.4 Two-Time Constant Model

Model TTC, It has been discovered that the battery exhibits a significant variation between the short- and long-term transient behavior based on observation of the battery

output voltage when the battery output current is zero (no load). Therefore, the OTC model cannot adequately describe the dynamic properties.

An additional RC network is connected in series with the OTC circuit to create the TTC circuit model, which increases the flexibility of the OTC model. As shown in Figure 4.1 (c), the TTC circuit is composed of four parts: voltage source V_{OC} , ohmic resistance R_O , T_{TTC1} and C_{TTC1} to describe the short term characteristics, R_{TTC2} and C_{TTC2} to describe the long term characteristics. v_{TTC1} and v_{TTC2} are the voltages across C_{TTC1} and C_{TTC2} respectively[6]. i_{TTC1} and i_{TTC2} are the outflows currents of C_{TTC1} and C_{TTC2} respectively [21].

Equations 4.6, 4.7, and 4.8 can be used to represent the electrical behavior of the TTC circuit in continuous time.

$$V_{TTC1} = \frac{-1}{R_{TTC1} \times C_{TTC1}} V_{TTC1} + \frac{1}{C_{TTC1}} i_{Batt} \quad (4.6)$$

$$V_{TTC2} = \frac{-1}{R_{TTC2} \times C_{TTC2}} V_{TTC2} + \frac{1}{C_{TTC2}} i_{Batt} \quad (4.7)$$

$$V_{Batt} = V_{OC} - V_{TTC1} - V_{TTC2} - R_0 \times i_{Batt} \quad (4.8)$$

The TTC model equations' description in discrete time is given by Equations 4.9, 4.10 and 4.11:

$$V_{TTC1,k+1} = e^{\frac{-T_s}{\tau_{TTC1}}} V_{TTC1,k} + R_{TTC1} \left(1 - e^{\frac{-T_s}{\tau_{TTC1}}}\right) i_{Batt,k} \quad (4.9)$$

$$V_{TTC2,k+1} = e^{\frac{-T_s}{\tau_{TTC2}}} V_{TTC2,k} + R_{TTC2} \left(1 - e^{\frac{-T_s}{\tau_{TTC2}}}\right) i_{Batt,k} \quad (4.10)$$

$$V_{Batt,k} = V_{OC}(SOC_k) - V_{TTC1,k} - V_{TTC2,k} - R_0 \times i_{Batt} \quad (4.11)$$

4.1.5 Estimation of the Model Parameters

This section demonstrates the process for estimating model parameters based on battery readings. First, the effects of temperature and aging are disregarded. At a constant temperature of 25°C, the experimental parameter identification of the battery was carried out using recently manufactured, unused cells. Figure 4.3 shows the typical Battery Charging and discharging behavior for the large current pulse. A continuation of this work will take into account the effects of temperature and aging.

4.1.5.a Charging and Discharging :

Figure 2 displays the voltage and current output characteristic curves of a battery during charging and discharging. Following is a description of the various curve subintervals:

- **Subinterval $S_0(t < t_0)$** : In this subinterval the battery the output current can be

assumed to zero over a sufficient time, though the output voltage can reach the open circuit voltage value $V_{OC}(SOC_0)$, and while the output current is zero the SOC value is constant [6],[21].

- **Subinterval $S_1(t_0 \leq t \leq t_1)$** : In this subinterval the battery is discharged with a constant current $I_{discharge} > 0$, first a steep decrease in the battery output voltage can be seen due to the internal resistance R_0 , and then it continues to decrease exponentially controlled by the OCV (as the SOC is decreasing)[6].
- **Subinterval $S_2(t_1 \leq t \leq t_2)$** : In this subinterval the battery output current $i_{Batt} = 0$, so the battery output voltage at first will have a steep increase due to R_0 , and then it shows an exponential increase until it reaches $V_{OC}(SOC_1)$.
- **Subinterval $S_3(t_2 \leq t \leq t_3)$** : In this subinterval the battery is charged with a constant current $I_{charge} < 0$; at first a steep increase in the battery output voltage can be seen due to internal resistance R_0 , and then it continues to increase exponentially controlled by the OCV (as the SOC is increasing)[6].
- **Subinterval $S_4(t_3 \leq t \leq t_4)$** : In this time subinterval the battery output current $i_{Batt} = 0$, so the battery output voltage at first will have a steep decrease due to R_0 , and then it has an exponential decrease until it reaches $V_{OC}(SOC_2)$ [6].

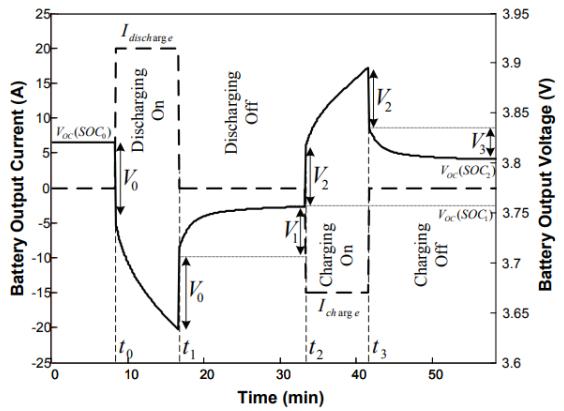


Figure 4.3: Characteristic waveforms for battery output voltage and current during charging and discharging of lithium-ion cells.

4.1.5.a.1 Ohmic Resistance : The voltage drop across R_0 at the first time instant when charging (V_2) respectively discharging (V_0) can be taken to calculate R_0 [23], according to Equation 4.12:

$$R_0 = \begin{cases} \frac{V_0}{I_{discharge}}, & : \text{for discharge.} \\ \frac{-V_2}{I_{discharge}}, & : \text{for charge.} \end{cases} \quad (4.12)$$

4.1.5.a.2 Estimation of the OTC Model Parameters : in this step battery output voltage measurements during the subintervals S2 and S4 are used, as in these subintervals OCV is constant[23], and the battery output voltage is just driven by the dynamic characteristics of the battery. The output voltage v_{Batt} during S2 and S4 can be calculated according to the OTC model by setting i_{Batt} to zero in Equations 4.2 and 4.3, then solving the differential equation as shown in Equation 4.13 [6]:

$$\begin{cases} S_2 : V_{Batt}(t) = V_{OC}(SOC_1) - v_{OTC}(t1)e^{\frac{-t}{\tau_{OTC}}}, & \text{where, } \tau_{OTC} = R_{OTC} \times C_{OTC}. \\ S_4 : V_{Batt}(t) = V_{OC}(SOC_2) - v_{OTC}(t3)e^{\frac{-t}{\tau_{OTC}}} \end{cases} \quad (4.13)$$

Estimating the values is necessary for the identification of OTC model parameters $V_{OC}(SOC_1), V_{OC}(SOC_2), v_{OTC}(t1), v_{OTC}(t3), \tau_{OTC}$ in Equations 4.13. A nonlinear least squares approach is used (also known as nonlinear data fitting) to find the values that best suit the relationship between the measurements and the nonlinear function, in this case, an exponential function, to estimate these parameters $f(t) = A + Be^{-\alpha t}$.

The vector of coefficients A, B, and α is the result of the nonlinear least squares algorithm. Through Equations 4.20 to 4.17, these coefficients will be used to calculate the OTC model parameters:

$$\begin{cases} S_2 : V_{OC}(SOC_1) = A, v_{OTC}(t1) = B, & \text{where, } \tau_{OTC} = \frac{1}{\alpha}. \\ S_4 : V_{OC}(SOC_2) = A, v_{OTC}(t2) = B, \end{cases} \quad (4.14)$$

$$\begin{cases} T_{Charge} = t1 - t0 \\ T_{Discharge} = t3 - t2 \end{cases} \quad (4.15)$$

$$\begin{cases} S_2 : R_{OTC} = \frac{v_{OTC}(t1)}{\left(1 - e^{\frac{-T_{Discharge}}{\tau_{OTC}}}\right) I_{Discharge}} \\ S_4 : R_{OTC} = \frac{v_{OTC}(t3)}{\left(1 - e^{\frac{-T_{Charge}}{\tau_{OTC}}}\right) I_{Charge}} \end{cases} \quad (4.16)$$

$$C_{OTC} = \frac{\tau_{OTC}}{R_{OTC}} \quad (4.17)$$

4.1.5.a.3 Estimation of the TTC Model Parameters : By considering the two RC networks in place of the OTC model's single RC network, the TTC model parameters can be calculated in the same manner as for the OTC model. Equations 4.18 can be used to define the output voltage of the TTC model for the subintervals S2 and S4. The experiments carried out on the LIPO Battery and the typical parameters of the Battery

are shown in table 4.1.

$$\begin{cases} S_2 : V_{Batt}(t) = V_{OC}(SOC_1) - v_{TTC1}(t1)e^{\frac{-t}{\tau_{TTC1}}} - v_{TTC2}(t1)e^{\frac{-t}{\tau_{TTC2}}}, & \tau_{TTC1} = R_{TTC1} \times C_{TTC1}. \\ S_4 : V_{Batt}(t) = V_{OC}(SOC_2) - v_{TTC1}(t3)e^{\frac{-t}{\tau_{TTC1}}} - v_{TTC2}(t3)e^{\frac{-t}{\tau_{TTC2}}}, & \tau_{TTC2} = R_{TTC2} \times C_{TTC2}. \end{cases} \quad (4.18)$$

	Typical Capacity	53 Ah
	Nominal Voltage	3.7
Charge Condition	Max. Current Voltage	53A 4.2V \pm 0.03V
Discharge Condition	Max. Current Peak Current Cut-off Voltage	159A 290A 3.0V

Table 4.1: SLPB120216216 Cell Data

Estimating the values is required for the TTC model's identification, $V_{OC}(SOC_1)$, $V_{OC}(SOC_2)$, $v_{TTC1}(t1)$, $v_{TTC1}(t3)$, $v_{TTC2}(t1)$, $v_{TTC2}(t3)$, τ_{TTC1} and τ_{TTC2} in Equations 4.18. In this case an exponential function with two-time constants $f(t) = A + Be^{-\alpha t} + Ce^{-\beta t}$ is used.

The vector of coefficients A, B, C, α , and β is the result of the nonlinear least squares algorithm. Through Equations 4.20 to 4.23, these coefficients will be utilized to calculate all the TTC model's parameters.

$$\begin{cases} S_2 : V_{OC}(SOC_1) = AS_4 : V_{OC}(SOC_2) = A \end{cases} \quad (4.19)$$

$$\begin{cases} S_2 : v_{TTC1}(t1) = B, v_{TTC2}(t1) = C, & :\tau_{TTC1} = \frac{1}{\alpha}. \\ S_4 : v_{TTC1}(t3) = B, v_{TTC2}(t3) = C, & :\tau_{TTC2} = \frac{1}{\beta}. \end{cases} \quad (4.20)$$

$$\begin{cases} S_2 : R_{TTC1} = \frac{v_{TTC1}(t1)}{\left(1 - e^{\frac{-T_{Discharge}}{\tau_{TTC1}}}\right) I_{Discharge}} \\ S_4 : R_{TTC1} = \frac{v_{TTC1}(t3)}{\left(1 - e^{\frac{-T_{Charge}}{\tau_{TTC1}}}\right) I_{Charge}} \end{cases} \quad (4.21)$$

$$\begin{cases} S_2 : R_{TTC2} = \frac{v_{TTC2}(t1)}{\left(1 - e^{\frac{-T_{Discharge}}{\tau_{TTC2}}}\right) I_{Discharge}} \\ S_4 : R_{TTC2} = \frac{v_{TTC2}(t3)}{\left(1 - e^{\frac{-T_{Charge}}{\tau_{TTC2}}}\right) I_{Charge}} \end{cases} \quad (4.22)$$

$$\begin{cases} C_{TTC1} = \frac{\tau_{TTC1}}{R_{TTC1}} \\ C_{TTC2} = \frac{\tau_{TTC2}}{R_{TTC2}} \end{cases} \quad (4.23)$$

4.1.6 Experimental and Computational Results of SLPB120216216

Cells made of lithium polymer by the producer Kokam were employed for the modeling and experimental experiments. Table 4.1 shows several significant cell data. A battery test bench was established to determine the model parameters. Using short and long interruptions, a rectangular-shaped current signal must be applied to the battery on this test bench. It is also necessary to measure the voltage of the battery output. While the OTC and TTC model parameters must be determined during extended pauses, the battery's ohmic resistance R0 can be measured during small interruptions of the current signal.

4.2 Battery Emulation

Part I of the chapter 4 described extensively the LIPO Battery Modeling and equivalent circuit analysis. The *Part II* of the chapter gives more extravagance to the Battery model implemented in real-time. *Part II* will also talk about different instrumentation and configurations. I have used python environment to implement the system, the reason behind choosing python as a coding environment is, python is a high-level used and most compatible with different instruments. The basis for implementing the battery model is the data that is collected for the SLPB120216216 by Ahmad RAHMOUN, Helmuth BIECHL. Gratitude to *Ahmad RAHMOUN and Helmuth BIECHL* for their paper[6] "*Modelling of Li-ion batteries using equivalent circuit diagrams*" this paper became the bedrock for this module implementation. Following the upcoming sections is the continuation of the *Part I* battery modeling with the coding environment.

4.2.1 Fundamental Instruments For Battery Emulation

Figure 4.5 shows the architecture of the Battery modeling and the emulation, for the external view the architecture looks very clumsy and dusky, but I have followed the modular approach in this architecture to extend the model to a one-time constant or two-time constant even three. The proposed architecture can handle multiple current sourcing, sinking, and measuring instruments without disturbing the overall system. Before diving into the architecture and modular approach, it is good to understand what kind of instruments can be used. And their specifications for the BMS applications. The following section can give brief information on the instruments and their configurations.

4.2.1.a Chroma :

The 87001 16CH Battery Cell Simulator can simulate the cell to perform charge and discharge behavior for BMS testing. It can simulate up to 480 battery cells in series with voltage and current measurement functions. It can receive IPC's commands in real-time, store the measured values temporarily and return them to the IPC [24]. Chroma has two communication one through the ethernet and CAN bus, for facilitating the modular and easy communication I preferred ethernet for this particular project, we can also use the can bus when we test the emulator with the real-time vehicle setup. Figure 6.12(a) shows the 16CH chroma which I have used in the lab.

4.2.1.a.1 Sepcifications of the Chroma :

- This simulator has built a DC Power Supply with $1\Phi 110\text{--}220V \pm 10\% VLN$ input power.
- Each unit has 16 channels output that can set parameters, start and end time respectively.
- The channel can be a constant voltage source with a constant current function.
- Maximum 30 sets of 87001 simulators can be connected in series for use and can simulate the battery cell voltage of a 480-cell battery pack (2000V/4.2V) in series.
- High-precision output and measurement that are used in laboratories for testing product specifications and characteristics.
- No display panel and operation buttons but using LED lights to indicate the standalone unit status.
- Each channel has 2 current ranges (2 Current: (-5A +5A, -0.5A +0.5A)).
- The operating interface uses the internet to give commands, control output measurement and read data via an external PC. The communication interface is Ethernet with SCPI protocol specification.
- Channels can be connected in series/parallel across a standalone unit with up to two batteries connected in parallel.
- Noise < 60db (output terminal 5V/5A/16CH)
- **Auto Range Select**
 - The CC automatically switches to the proper range according to the set current.

- The CV automatically switches to the mapping range according to the upper limit current.

6.12(a)

- **Current Range Select**

- When 5A is in use, performing CC(Constant Current) charge for 500uA may have a bigger error.
- When 500mA is in use, performing CC charge for 5A will prompt a warning and stop execution.
- **Data Transmission :** The data transmission interval is 10ms * paralleled unit no. The minimum data transmission interval is $\Delta 10\text{ms}$ for one unit and $\Delta 20\text{ms}$ for two units, and so forth.

4.2.1.a.2 Output Wiring of the Chroma :

- The figure 6.12(b) is the parallel connection diagram of two simulators [24]. (Same for serial connection.)
- The 87001 is a 4-wire measurement. The SENSE wire and BMS connection point should be as close as possible to the BMS input terminal to avoid voltage differences due to line losses.

4.2.1.a.3 Configuring the Chroma: For Programing the Chroma I took the help of the pyvisa library, which can use to interface with instruments using different protocols. The first setup is the NI (National Instrument) driver in PC to identify the instrument (install NI Max application in PC), through the NI driver, pyvisa can communicate through the VISA virtual port. The piece of code shows how to configure the visa port for the chroma(or any battery emulator commands that are more generalized) [24].

```

1 #VISA commands for the Chroma
2 set_visa_attribute(pyvisa.constants.VI_ATTR_MAX_QUEUE_LENGTH, 50)
3 #Time Out Value
4 set_visa_attribute(pyvisa.constants.VI_ATTR_TMO_VALUE, 2000)
5 set_visa_attribute(pyvisa.constants.VI_ATTR_TERMCHAR_EN,
6                     pyvisa.constants.VI_TRUE)
7 set_visa_attribute(pyvisa.constants.VI_ATTR_TERMCHAR, 0xA)
8 set_visa_attribute(pyvisa.constants.VI_ATTR_SEND_END_EN,
9                     pyvisa.constants.VI_TRUE)
10
11 set_visa_attribute(pyvisa.constants.VI_ATTR_SUPPRESS_END_EN,
12                     pyvisa.constants.VI_TRUE)
13 set_visa_attribute(pyvisa.constants.VI_ATTR_FILE_APPEND_EN,
```

```

14                     pyvisa.constants.VI_FALSE)
15     set_visa_attribute(pyvisa.constants.VI_ATTR_IO_PROT, 1)
16     set_visa_attribute(pyvisa.constants.VI_ATTR_TCPIP_NODELAY,
17                         pyvisa.constants.VI_TRUE)
18     set_visa_attribute(pyvisa.constants.VI_ATTR_TCPIP_KEEPALIVE,
19                         pyvisa.constants.VI_TRUE)

```

Listing 4.1: VISA parameters set for Chroma

The following code explores the basic programming of the chroma for BMS application:

```

1      #Basic Program for Chroma to configure the cells
2      chroma.query('*IDN?\n') # identify the instrument
3      #Query the output sampling time
4      chroma.query('SIM:CONF:SAMP:TIME?\n')
5
6      #number of BMS(each Chroma is One BMS) are parallel
7      chroma.write(f'SYST:SLAVE:PARA {self.noOfBMS}\n')
8      chroma.write(f'SYST:SLAVE:SCAN {self.noOfBMS}\n')
9
10     #Chroma Status commands
11     chroma.query('SYST:FRAME:STATE? 0\n')
12     chroma.query('SYST:FRAME:CHAN:STATE? 1\n')
13     chroma.query('SYST:FRAME:CHAN:NUMB? 0\n')
14     chroma.write('SIM:CONF:CHAN:ACT 65535\n')
15     chroma.write('SIM:CONF:CLE\n')
16
17     ''' BMS configurations '''
18     #Number of the BMS 1
19     chroma.write(f'SIM:CONF:BMS:NUMB {noOfBMS}\n')
20     #No cells use in the BMS testing #1 BMS , #2 Cells
21     chroma.write(f'SIM:CONF:CELL:NUMB {noOfBMS},{noOfBMSCells}\n')
22     #BMS 1, CellStart 1, Cellend 2,
23     # Cell parallel to the channel1 , # Current Range 2 - 5.0 A
24     chroma.write(f'SIM:CONF:CELL:PARA {noOfBMS},{noOfBMS},
25     {noOfBMSTestingCells},{parallelBMSSchannel},{cellCurrent_5A}\n')
26
27     ''' Output Parameters Set '''
28
29     ''' # BMS start 1 ,# BMS end 1 ,#set the start cell 1,
30     # set the end cell 1, # set the cell voltage 4.0 ,
31     # set the Current of the cell 0.5A '''
32
33     chroma.write(f'SIM:PROG:CELL {noOfBMS},{noOfBMS},{cellNo},
34     {cellNo},{cellVoltage},{cellCurrent5A}\n')
35
36     # Switch on all the cells immediately
37     chroma.write('SIM:OUTP:IMM\n')

```

```

38
39     '''### check if there is any error
40     in the Chroma while setting the voltages
41     ### if there is no error enable
42     all the cells outputs'''
43
44     time.sleep(10)
45     # Check the configuration Error
46     self.chroma.query('SYST:ERR?\n')
47
48     # Switch on all the cells
49     self.chroma.write('SIM:OUTP ON \n')
50     time.sleep(1) # give some time to switch on the emulator

```

Listing 4.2: Basic BMS Program for Chroma

The above-attached code is just a basic code for the BMS application which can give a better idea about the basic chroma(Battery emulator) for more SCPI commands of the chroma follow the user manual[24] and for the detailed class-based skeleton follow [here](#).

4.2.1.a.4 Response Time of the Chroma : During battery, balancing it is essential to capture the battery voltage, in reality, this is not the problem because we might be dealing with the actual batteries which do not need voltage updates to the batteries. When we deal with any instruments (battery emulators) it is essential to update the battery (Cell) voltages and battery currents. In this particular project, chroma is used as the battery emulator. Chroma is being communicated through a python script to update its parameters via ethernet. The fundamental response time of the chroma for every request is 10ms, that being said for our application few 100ms time duration is good enough for calculating the batteries SoC. Perhaps I made some demonstration of the chroma response time and the number of packets, figure 4.6 shows the round robbin delay of 8 cells current and voltage fetch from chroma. The results are quite adequate, over 10k packet request chroma has missed one or two chances of delaying 500ms, which still satisfies a few million packets.

4.2.1.b Load/Charger :

In the setup4.5 load or charger is used across the series cells (battery pack) which can only supply current or sink current from the pack. For this particular architecture, I have preferred e Keysight N6705 DC Power Analyze as a load or charger. All the controls have been passed through the power analyzer module through the script.

4.2.1.b.1 Keysight N6705 DC Power Analyzer : The Keysight N6705 Figure 6.11(a) DC Power Analyzer is a multipurpose power system that combines the

capabilities of an oscilloscope, a data logger, and a DC voltage source with numerous outputs [25].

The Keysight N6705 has up to four programmable outputs as a multiple-output DC source. The power levels of the available power modules range from 20 W to 500 W, with different voltage and current combinations, and they offer a wide range of performance capabilities. Additionally, each output can generate arbitrary (Arb) waveforms, allowing you to program. Standardized voltage and current waveforms, or create your own. With Keysight N678xA SMUs (Source/Measure Units) have a multi-quadrant power mesh with distinct voltage and sources of current priority [25].

The Keysight N6705's Meter View shows the average output voltage and current as a measurement system. Scope View, which you can modify using the vertical and horizontal sliders, displays waveforms. The Data Logger View records average and peak voltage and current measurements over a long period and plots the data [25].

The setup allows configuring the DC power supply as a charger or load, by setting the current direction. The following program shows the typical program for load/chargers:

```

1
2     #find the resource
3     rm = pyvisa.ResourceManager()
4     #open the instrument by the id
5     loadCh = rm.open_resource('USB0::0x0957::0x0F07::
6                               :MY50000622::INSTR')
7     #Identify Keysight N6705's
8     loadCh.query('*IDN?\n')
9
10    '''Configure Power analyzer channels 1 and 3 in
11    2 quadrants to sink or source current; that presumes
12    Load or Charger'''
13    loadCh.write('EMUL PS2Q,(@1,3)')
14
15    # Enable current priority for channels 1 and 3
16    loadCh.write('FUNC CURR,(@1,3)')
17
18    # Set currnet range for 1 and 3 channel 1Amp
19    loadCh.write('SOUR:CURR:RANG 1.02,(@1,3)')
20    loadCh.write('CURR 1,(@1,3)')
21
22    #Set Voltage limt for 28V
23    loadCh.write('VOLT:LIM 28,(@1,3)')
24
25    # Switch on Channel 1 and channel 3
26    loadCh.write('OUTP ON,(@1,3)')

```

Listing 4.3: Load/Charger Configuration for Keysight N6705's

The above program is just an example of programming channel 1 and channel 3,

we can couple the power supply channels for programming and trigger at the same time (*OUTP : COUP : CHAN 1,2 ; Couple channel 1 and 2*). For more details and programming examples, refer to the keysight N6705B datasheet [25].

4.2.1.c Meter View :

The proposed architecture 4.5 encounters a meter view, which meter view allows the collaboration of various measuring instruments which can be directly controlled. A meter view in the architecture is directly controlled by the power analyzer module. Measurements include DC/DC converter input/output current measurements, and battery pack current measurements. The current measurement setup in the system is very much critical, hence we can measure the shunt voltage, and we can calculate the current flow (if shunt resistance is known). Measurement view is so much modular that we can have as many measuring instruments in the setup, and we log the data without disturbing the setup. In the architecture, keysight 34470A DMM 6.11(b) has been employed for shunt voltage measurements (Battery Pack Current, DC/DC input/output current; Fig 2.9). The following sections will give more detailed information about the multimeter and configuration.

4.2.1.c.1 Digital Multimeters 34460A : The only completely drop-in, SCPI-compatible alternative to the 34401A DMM in the market is the Digital Multimeters 34461A [26]. Although some other DMMs claim to be 34401A SCPI compatible, they only support a limited number of SCPI commands. The same design team that produced the 34401A also produced the Truevolt DMMs. When developing the Truevolt family of DMMs, the team kept 34401A measures, dependability, and familiarity in mind. Consequently, people may use it without having to spend hours learning how. The following basic programming for DMM gives more insights into communication and configuration for measurement setup :

```

1 rm = visa.ResourceManager()
2   ''' usb_id='USB0::0x2A8D::0x1301::MY57216238::INSTR' VISA id of DMM
3 Open VISA port
4
5 mul_34461A = rm.open_resource(usb_id)
6
7 #Identify DMM
8 mul_34461A.query('*IDN?')
9 #Rest DMM
10 mul_34461A.write('*RST')
11 #Check for Error
12 mul_34461A.query('SYST:ERR?')
13 # set NPLC to speed up the measurements
14 mul_34461A.write('VOLT:DC:NPLC 0.02')
```

```

15     ''' Configure DMM for Voltage measurements '''
16     mul_34461A.write(':FUNC "VOLT:DC"')
17
18     if range in range_list:
19         range_auto = ':VOLT:DC:RANG:AUTO '
20         range_val = ';:VOLT:DC:RANG '
21         res_com = ';:VOLT:DC:RES '
22
23         if range == -1:
24             range_auto_cmd = 'ON'
25             range_val = ''
26             range_val_str = ''
27             res_com = ''
28             res_val_str = ''
29         else:
30             range_auto_cmd = 'OFF'
31             range_val_str = str(range)
32             if range == 0.1 or range == 1:
33                 res = 1e-6
34             elif range == 10:
35                 res = 1e-5
36             elif range == 100:
37                 res = 1e-4
38             else:
39                 res = 1e-3
40             res_val_str = str(res)
41
42         com = range_auto + range_auto_cmd + range_val +
43         range_val_str + res_com + res_val_str
44
45         #wite the Command
46         mul_34461A.write(com)
47         mul_34461A.write('VOLT:IMP:AUTO ON')
48         array = []
49         while count>0:
50             if count > 4:
51                 cnt = 4
52             else:
53                 cnt = count
54             array.append(self.read_value(cnt))
55             count -= 4
56         return(sum(array)/len(array))
57     else:
58         return('ERR: Wrong range')
59
60     # Fetch the voltage
61     def Volt(self):

```

```
62     return float(mul_34461A.query('READ?'))
```

Listing 4.4: DMM Keysight 34401A's Measuring/Configuration

4.2.2 Battery Modeling :

The above sections have described the hardware and instrument setup in the Battery Emulation architecture 4.5. After understanding the background and programming setup for instruments it is easy to understand the Battery modeling algorithms. The following sections can discretize the Battery emulation architecture and explain the algorithms.

Algorithm 1: Battery Modeling Algorithm

Data: $BattModel = \langle Q_{tot}, dt, SOC_0, V_{batt}, V_{oc}, SoC, i_{batt}, BattModelParams(SoC) \rangle$

input : Q_{tot}, dt, SOC_0

output: $V_{batt}, V_{OTC(k+1)}, SOC$

- 1 Initialization
- 2 $Q_{tot} \leftarrow$ Total Batt Capacity $\mathcal{N}(0.1 - 100)$ Ah
- 3 $SOC_0 \leftarrow$ Initial SoC ($SoC_{(k)}$) $\mathcal{N}(0 - 1)$
- 4 $dt \leftarrow$ Measurement Sampling time $\mathcal{N}(0 - 1000)$ mS
- 5 $i_{batt} \leftarrow 0$; initial battery current $i_{batt(k)}$
- 6 $V_{OC(k)} = BattModelParams.VOC(SoC_{(k)})$ BatteryOpen ckt Voltage $f(SoC_0)$
- 7 **for** $k \leftarrow 0$ **to** $iters$ **do**
- 8 $R_{0(k)} = BattModelParams(SoC_{(k)})$
- 9 $C_{OTC(k)} = BattModelParams.COTC(SoC_{(k)})$
- 10 $R_{OTC(k)} = BattModelParams.ROTC(SoC_{(k)})$ Battery OTC Dynamic Components $f(SoC)$
- 11 $V_{OC(k)} = BattModelParams.VOC(SoC_{(k)})$ BatteryOpen ckt Voltage $f(SoC)$
- 12 $V_{batt(k)} = V_{OC(k)} - V_{OTC(k)} - R_{0(k)} \times i_{batt(k)}$
- 13 $V_{OTC(k+1)} = V_{OTC(k)} \times exp^{\frac{-dt}{C_{OTC(k)} * R_{OTC(k)}}} + R_{OTC(k)} \times (1 - exp^{\frac{-dt}{C_{OTC(k)} * R_{OTC(k)}}}) \times i_{batt(k)}$
- 14 $SoC(k+1) = SoC(k) - i_{batt(k)} \times \frac{dt}{Q_{tot} * 3600}$ Coloumb SOC
- 15 $i_{batt(k+1)} \leftarrow i_{battNew}$ the latest Battery current measurement
- 16 **end**
- 17 **return** $V_{batt(k)}, SoC_{(k)}, V_{OTC(k+1)}$

The section shows the basic battery modeling algorithm, the explanation is as follows:

$$SoC(k+1) = SoC(k) \pm dt \times \frac{i_{batt}(k)}{Q_{tot}} \quad (4.24)$$

- *Batt* module name which will take $< Q_{tot}, dt, SOC_0, i_{batt}, BattModelParams(SoC) >$ inputs and produces $V_{batt}, V_{OC}, SoC >$ as the outputs
- Initialization of the algorithm parameters
 - $< Q_{tot}$ is the total capacity of the battery and dt measurement time used to calculate the battery SoC for instance by the coulomb count eq :4.24
 - SOC_0 initial SoC which can help to extract the open circuit voltage(V_{OC}) of the battery at first instance, when $i_{Batt} = 0$ the V_{OC} is same as V_{Batt}
 - Open circuit voltage(V_{OC}) is the function of the SoC, the V_{OC} can directly extract from the Battery Voltage/SoC curve which will be provided by the battery manufacturer
 - *BattModelParams(SoC)* module take SoC as input provide the Battery modeling parameters $V_{OC}, R_0, C_{OTC}, R_{OTC}$ by interpolating SoC with the manufacturer provided battery component lookup tables
- Iterate the for (k) loop from 0 to N -1
- For every $SoC(k)$ *BattModelParams(SoC_(k))* will provide k^{th} updated batter parameters $V_{OC(k)}, R_{0(k)}, C_{OTC(k)}, R_{OTC(k)}$
- Battery voltage is calculated by the equation 4.5 ; initial $V_{OTC} = 0, \therefore i_{batt} = 0$
- The updated onetime constant voltage of the battery $V_{OTC(k+1)}$ is calculated by the equation 4.4
- Update the $SOC(k + 1)$ by any SoC calculating algorithms for instance Coulomb count 4.24 or Kalman etc
- The battery current i_{batt} updated with the latest current acquisition made in dt delay
- *Batt* module will return updated $V_{batt(k)}, SoC_{(k+1)}, V_{OTC(k+1)}$ battery voltages and SOC

4.2.3 Battery Pack Modeling :

The battery pack module will instantiate the *BattModel 1*, a module created in algorithm 2 which will manage several batteries depending on the user's requirements(setting the updated battery voltages, calculating SoC, measuring batteries current). The

algorithm describes the implementation of the battery pack for 8 batteries, we can extend even further just by changing the initial SoC array for the module.

Algorithm 2: Battery Pack Modeling Algorithm

Data: $BattPack = < Q_{tot}, dt, N_{Batts}, SOC_0[], V_{batt}[], V_{oc}[], SOC[], i_{batt}[], BattModel(), Chroma(V_{Batt})[] >$

input : $Q_{tot}, dt, SOC_0[]$

output: $V_{batt}[], SOC[]$

- 1 Initialization
- 2 $Q_{tot} \leftarrow$ Total Batt Capacity $\mathcal{N}(0.1 \sim 100)$ Ah
- 3 $SOC_0[] \leftarrow$ Initial SoC ($SOC_{(k)}[]$) $\mathcal{N}[1 \dots 8] (0 \sim 1)$
- 4 $N_{Batts} = \text{len}(SOC_0[])$ No of Cells in BATT Pack
- 5 $dt \leftarrow$ Measurement Sampling time $\mathcal{N}(0 \sim 1000)$ mS
- 6 $i_{batt}[] \leftarrow = 0$; initial battery current $i_{batt(k)}$ $[1 \dots N_{Batts}]$
- 7 $Batt = []$ Store $BattModel()$ instances
- 8 Initialize Chroma Channels
- 9 $Chroma(V_{Cell} = \text{default}(4V), N_{Batts})$
- 10 Initialize N_{Batts} Battery Model instances
- 11 with SOC_0
- 12 **for** $i \leftarrow 0$ to $N_{Batts} - 1$ **do**
- 13 | $Batt[i] = BattModel(SOC_0[i], Q_{tot}, dt)$
- 14 **end**
- 15 **for** $k \leftarrow 0$ to N_{Batts} **do**
- 16 | $i_{batt}[k] \leftarrow Chroma.Currents[k]$
- 17 | $[V_{batt}[k], V_{oc}[k]] = Batt[k].battVoltage(i_{batt}[k])$
- 18 | $SOC[k] = Batt[k].CoulombSOC()$
- 19 | $Chroma.VoltageSet(cellNo = k, V_{Cell} = V_{OC}[k])$
- 20 **end**
- 21 **return** $V_{batt}[], SOC[]$

- The battery pack module will operate everything on batch-wise like Soc, current, and voltage as arrays ($SOC_0[], V_{batt}[], V_{oc}[], SOC[], i_{batt}[]$).
- Initialize $Q_{tot}, dt, SOC_0[]$ is the initial soc of the batteries which can be declared as an array the length $N_{Batt} = \text{len}(SOC_0[])$ of the array determines the number of batteries used in the battery pack.
- $i_{batt}[] = 0$ array initialized to zero because there is no current flow at t=0, and declare $Batt[] = \text{len}([], N_{Batt})$ empty array of N_{Batt} size to store the

BatteryModel module instance, each instance will operate individually as a battery.

- Initialize and configure chroma for N_{Batt} channels in series with an initial voltage of 4v and a maximum current of 5A $Chroma(V_{Cell} = default(4V), N_{Batts})$.
- Collect the N_{Batt} Battery Model instance in the Batt array; each Battery Model module will take initial parameters SoC_0, Q_{tot} and dt as inputs.
- Iterate for (k) loop 0 to $N_{Batt} - 1$ to emulate each battery from $Batt[k]$ instances
 - Measure $i_{batt}[k]$ of k^{th} battery from chroma; $Chroma.Currents[k]$ can provide the current flowing in the k^{th} of the chroma
 - k^{th} battery model instance function $Batt[k].battVoltage(i_{batt}[k])$ newly calculated battery voltage and $SoC(k)$ corresponding open circuit voltage V_{OC}
 - $SoC[k] = Batt[k].CoulombSOC()$ will calculate the updated SoC by the newly acquired $i_{batt}(k)$
 - Set the k^{th} battery/channel voltage of the chroma to newly estimated V_{OC}
- The loop will return N_{Batt} batteries updated $SOC[]$ and $V_{batt}[]$

4.2.4 Power Analyzer Modeling

Algorithm 3: Power Analyzer Modeling Algorithm

Data: $PowerAnalyzer = < BattPack(), LoadCharger(), MeterView(), DataCollection(), dt, SOC[], V_{Batt}[] >$

input : $BatteryPack(), LoadCharger(), MeterView()$

output: $SOC[], V_{Batt}[]$

- 1 Initialization all the instruments with VISA USB id
- 2 $dt \leftarrow$ Measurement Sampling time $\mathcal{N}(0 \sim 1000)$ mS
- 3 $battPack = BattPack(); loadCharger = LoadCharger();$
 $meterView = MeterView()$
- 4 $BattLowV = 2.5; Volts; BattHighV = 4.2; Volts$
- 5 $DCDCShunt = 3e^{-3}; \Omega; PackShunt = 500e^{-6}; \Omega$
- 6 $SOC[] = [], V_{Batt}[] = []$
- 7 Tigger DC/DC Converter
- 8 $meterView.Digilent.TriggerDCDC()$
- 9 **while** $TRUE$ **do**
- 10 Battery Safety Area
- 11 **if** $\min(V_{Batt}[]) != BattLowVoltage | \max(V_{Batt}[]) != BattHighVoltage$
- 12 **then**
- 13 $BattPack() N_{Batts} = 8$ data as single array
- 14 $[SOC[], V_{Batt}[]] = BattPack()$
- 15 $DCDCoutI = meterView.DCDCoutShuntV() / DCDCShunt$
- 16 $DCDCinI = meterView.DCDCinShuntV() / DCDCShunt$
- 17 $ChargingI = meterView.PackTopShuntV() / PackShunt$
- 18 $DataCollection(SOC[], V_{Batt}[], DCDCoutI, DCDCinI, ChargingI)$
- 19 **end**
- 20 **else**
- 21 break the Loop
- 22 $Clearall();$
- 23 $break;$
- 24 **end**
- 25 $Delay(dt)$
- 26 **end**

Power Analyzer will integrate the complete setup 4.5, which includes meter-views,

battery packs, and data collection. The loop in the power analyzer will continuously run until the batteries enter the safety of operation. The loop will be iterated by delaying every dt for calculating soc and measuring the battery parameters (chroma). The PowerAnalyzer module will parallelly execute the DataCollection Module to log the DC/DC Converter input/output current, Battery Voltages, and SoC of the batteries. In the algorithm, I have collected shunt voltages instead of collecting directly current because in the system the shunt resistance values are known, and also measuring current needs to break the circuit loops or needed expense current probes.

4.3 Discussion of The Battery Modeling Results

The results from the power analyzer have been satisfactory and the robustness of the power analyzer architecture allows for the simulation of various BMS tests, such as low battery voltage, high battery voltage protection, and soc estimation. Batteries can be imbalanced for testing different battery balancing algorithms in the battery pack module by passing different initial SoC values. In the practical sense, low and high battery voltage testing takes tons of time with batteries. Achieving fast charging and discharging with the batteries needs a high sink/source current, which could be a limitation in many instruments. Thanks to the PowerAnalyzer, it allows emulating fast charging and discharging of batteries by adding some bias current(only added in the script) with the actual current that is flowing in the battery emulator. The actual battery emulator does not know anything it is not smart enough to realize what is going on with the current flowing in the system. On contrary, the script can emulate this behavior and set a new terminal voltage to each channel of the battery emulator, every time the PowerAnalyzer sample the current flowing in the battery emulator.

The following code, snippet illustrates the biased current simulation. “currents = self.batEmulator.BateryEmulatorCellCurrent” will fetch the actual current that is flowing in the battery emulator; for the “currents” array the “ibattBias” biased current is added and calculated as new open circuit voltage “batEmulator.batteryEmulatorVoltageSet(cellNo = i, cellVoltage = VOC)”, and SoC is the updated, updated soc can help to determine the new open circuit voltage(VOC) and VOC set to the battery emulator as terminal voltage(each channel respectively).

```

1  def batVoltageSOC(self):
2      batVoltSOC =dict()
3      currents = self.batEmulator.BateryEmulatorCellCurrent
4
5      biasedCurrent = []
6      # print(f'Current that flowinf in Chroma {currents}')
7

```

```

8     #add the sudo bias current
9
10    for i in range(0,len(self.SOC0)):
11        biasedCurrent.append(currents[i]+self.ibattBias)
12
13    for i in range(0,len(self.SOC0)):
14        [batVlot,VOC] = self.Batt[i].battVoltage(biasedCurrent[i])
15        batVoltSOC[batVlot] = self.Batt[i].CoulombSOC
16        self.batEmulator.batteryEmulatorVoltageSet(cellNo=i,
17                                         cellVoltage=VOC)
18
19    return batVoltSOC

```

Listing 4.5: Emulating Sudo BiasCurrent in the PowerAnalyzer

The results in 4.7 will enrich the battery modeling and power analyzer implementation, the data shown in the figure 4.7 will collect for one single battery with a one-time constant model. The data has been collected for one single battery from full charge to discharge, soc is from 5% to 95%, and vice versa. The obtained results of battery voltage Vs SoC must match with the Voltage Soc curve provided by the manufacturer. The charging voltage and soc 4.7(a) (discharging 4.7(b)) of the battery impressively match the results provided by the manufacturer in the voltage SoC graph 4.2. Undoubtedly the battery modeling 4.7 results match the OCV curve of the battery 4.7(a) and 4.7(b), yet it is very important to consider the symmetry of the OCV curve during charging and discharging Figure 4.7(c) and 4.7(d). The charging and discharging of curves of the battery are symmetry about 47% of the SoC, which is a good sign for an estimate of the battery soc both at charging and discharging. Figure 4.7(c) and 4.7(d) plotted battery voltage and SoC vs cycles, several consecutive sampling times between the measurements are cycles. The sampling dt time in this project has used multiples of 100mS. Nevertheless, dt is the independent choice for the user which again depends on the application.

The target of the battery modeling is to build the battery pack with sophisticated control over it for BMS applications. Results in Figure 4.8 achieved such a target, I have implemented for 8 batteries (The Figures show only 3 battery results, to avoid clumsiness in the graphs). The battery pack results are pretty much the same as results collected for a single battery Figures 4.8(a) and 4.8(d) show results for 8 batteries simulated with the same SOC assigned for all batteries. Thanks to the power analyzer, which will allow several battery tests for instance keep different socs and perform battery balancing, battery low and high voltage cut off. Figures 4.8(e) and 4.8(f) shows one such example of keeping different socs charging the batteries.

4.4 Summary of Chapter 4

Part I of the chapter 4 described the mathematical modeling of the battery with One-time and two-time constant equivalent circuit components. An extended subsection of Part I helped to estimate the OTC and TTC model parameters with the SOC curve which became the fundamental base for the battery pack power analyzer design. Part I also briefed about the discrete-time implementation of the OTC and TTC model for the battery. The discrete-time OTC and TTC model equations are useful for estimating the battery soc with advanced algorithms like Kalman, extended Kalman, and Columb-Extended Kalman. The most satisfactory conclusion in Part I can be seen in Part II, implementing battery models with the script and emulating with lab instruments. Nonetheless, for a more analytical and mathematical understanding of batteries, I diverted read attention toward the reference papers mentioned in the Bibliography. Part II talks about the practical implementation of Part I in terms of script and different instruments. Starting subsection of Part II walks through several instruments' specifications and configurations used in this project. This chapter is indeed a bit lengthy and diversified. Because battery modeling and implementation got to go together which is the reason I took extra liberty to extend this chapter more descriptive. I got less opportunity to describe the script but I have pushed everything to GitHub and referenced the links in miscellaneous.

To sum up the results came out from this chapter are convincing, and this can be still pursued further to develop a sophisticated graphical interface for the application. In the battery modeling, I have used the Columb counting approach for estimating the battery SOC, this can be still dragged into higher algorithms and can also increase the robustness of the model by adding more and more battery time constant models.

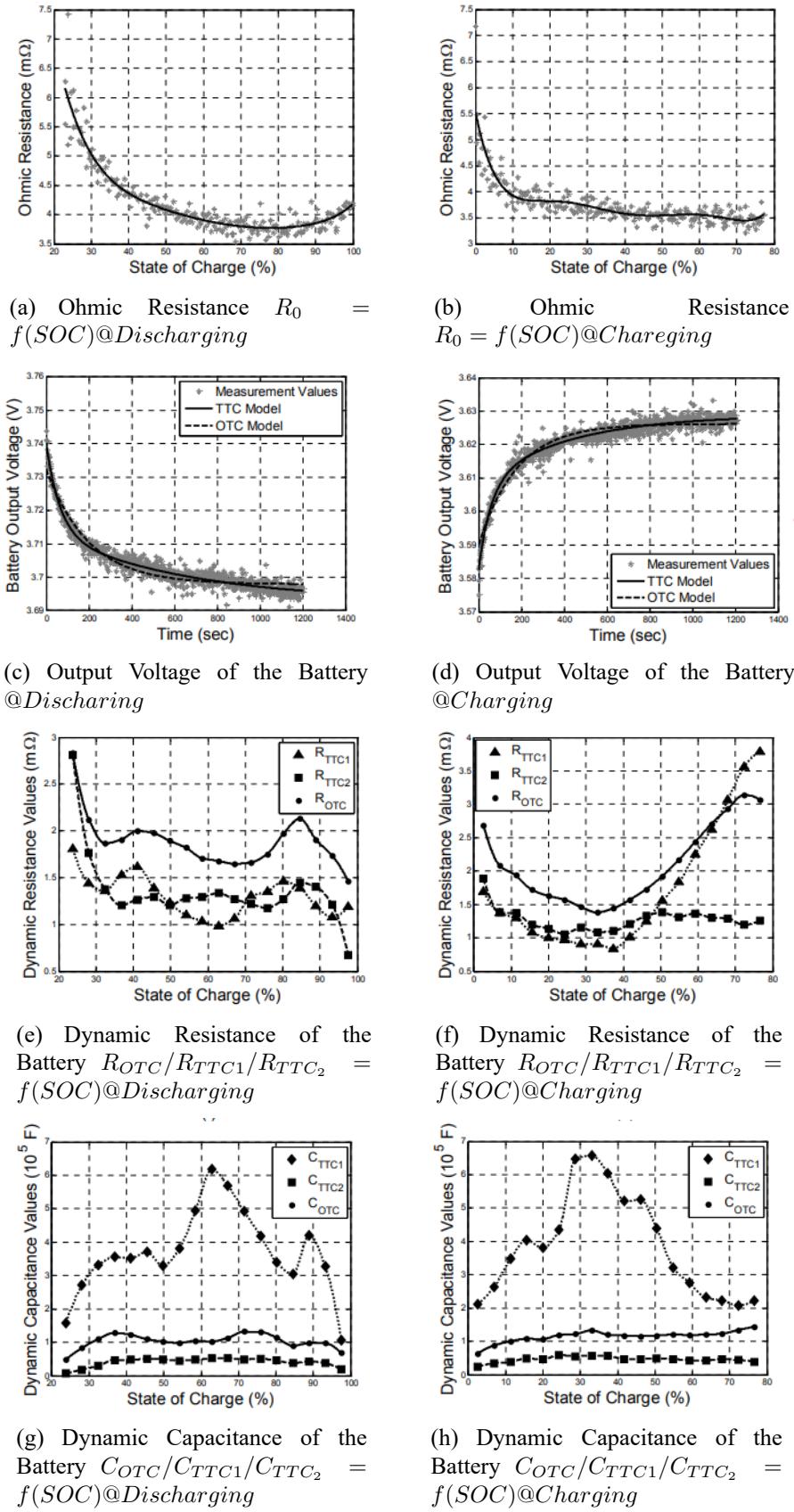


Figure 4.4: LIPo Battery SLPB120216216 Simulated Results [6]

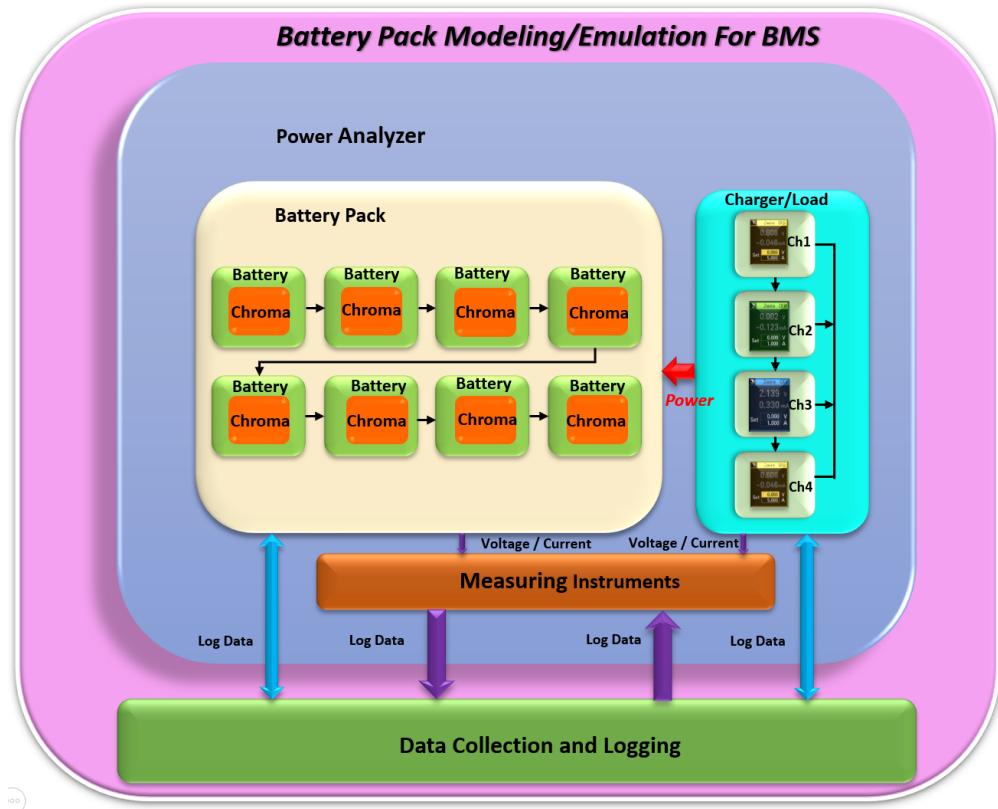


Figure 4.5: Architecture of the Battery Pack Modeling/Emulation For BMS

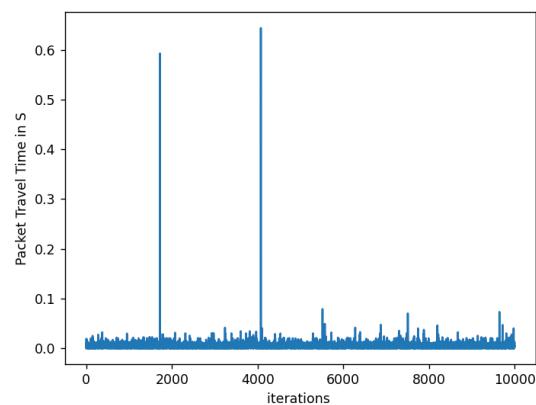


Figure 4.6: Chroma Response Time for Voltage and Current Request

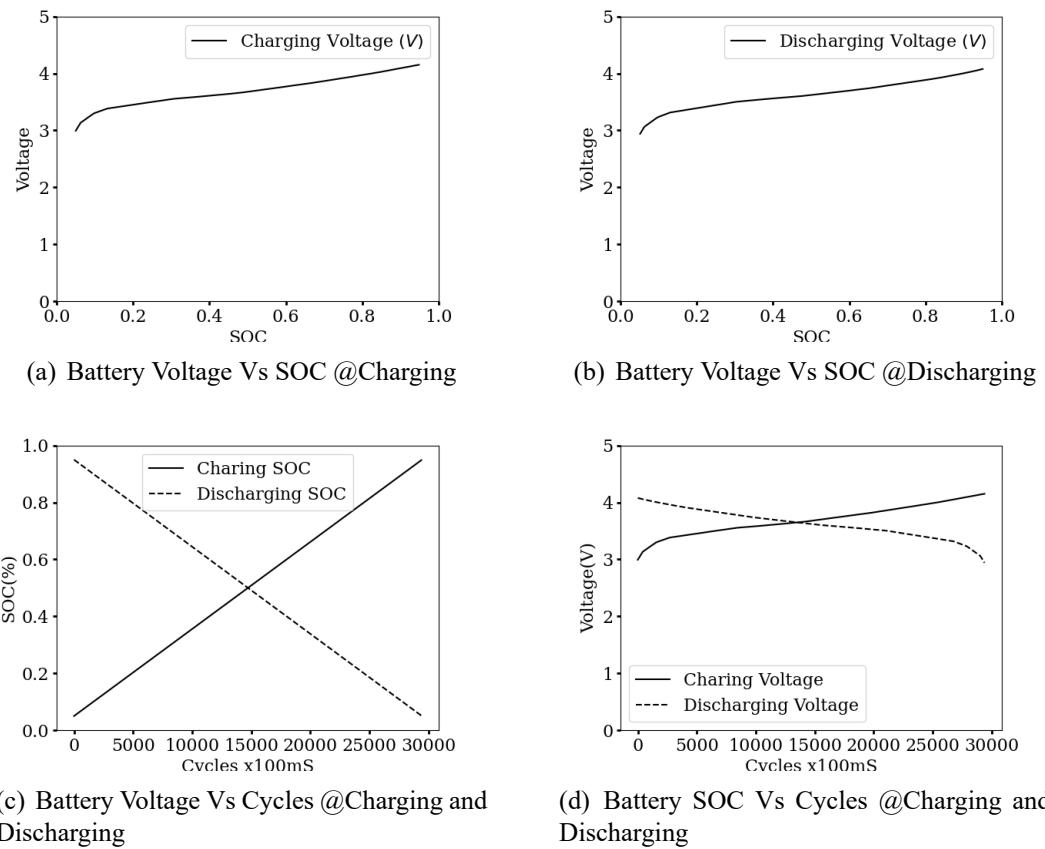


Figure 4.7: Single Battery Modeling Characteristics with PowerAnalyzer

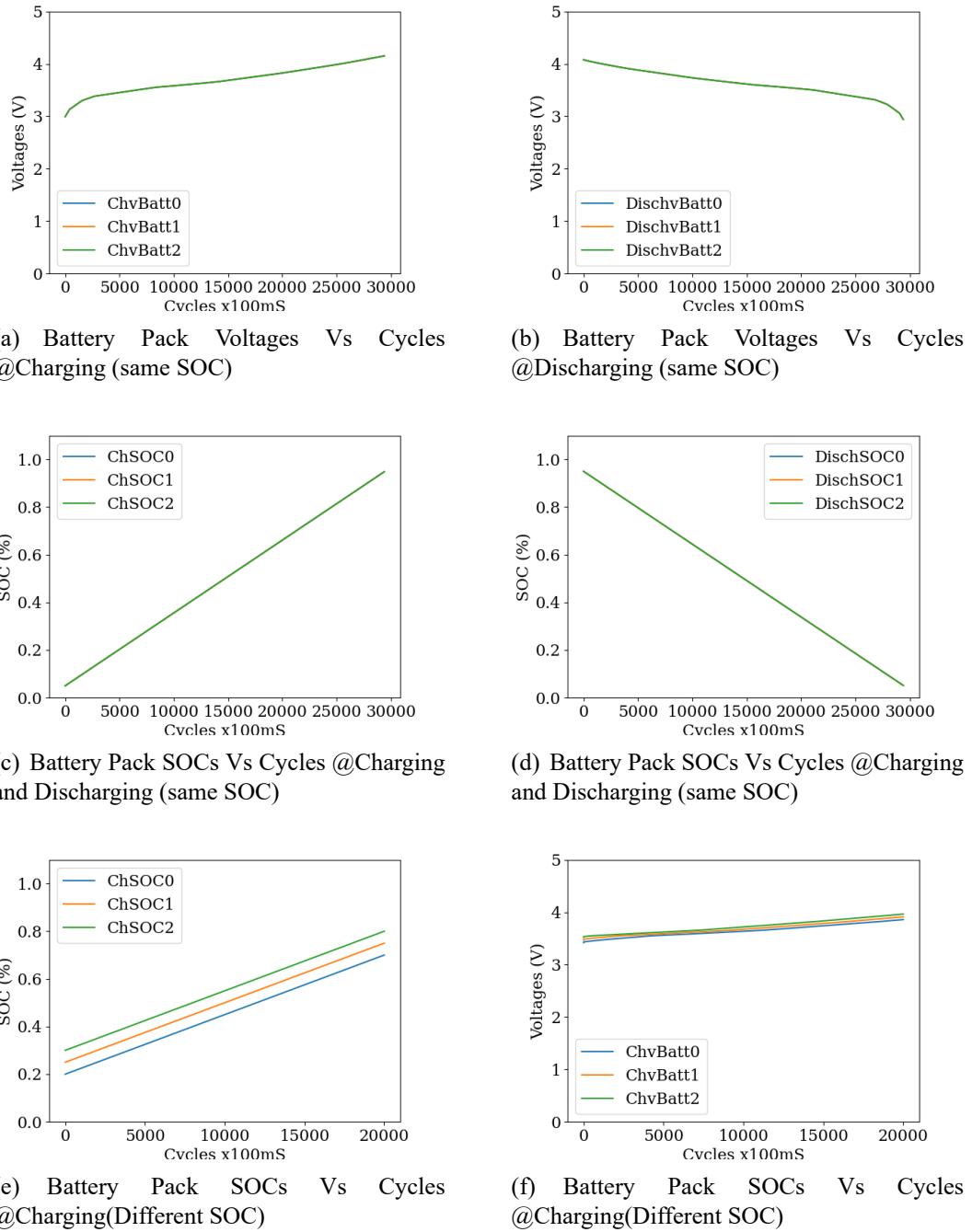


Figure 4.8: Battery Pack Modeling Characteristics with PowerAnalyzer(3 Cells)

Chapter 5

Battery SOC Estimation Algorithms

5.1 Kalman Filter

In essence, a Kalman filter is a system of recursive equations that implements a predictor-corrector type estimator. It creates an ideal guess of the system state based on the input control and output measurements; as a result, it is typically employed when the system state cannot be directly monitored and needs to be predicted optimally from the output measurements [27]. In this section 5.1, the extended Kalman filter (EKF) for non-linear systems is explained, followed by the discrete Kalman filter for linear systems, and lastly a state space model for the Li-Ion battery is built up. To assess the reliability of the suggested method, comparisons are also made between SOC values calculated by Ampere-counting and SOC values estimated by EKF [28].

5.1.1 The Discrete Kalam Filter

This section outlines the fundamental design of a Kalman filter, which takes measurements and estimates the system state at discrete time intervals [29].

The linear difference stochastic equation 5.1 governs a discrete time-controlled process, and the problem of estimating the state vector $x_k \in \Re^m$ of this process is handled by the discrete Kalman filter.

$$x_{k+1} = A_k x_k + B_k u_k + w_k \quad (5.1)$$

where the measurement vector $y_k \in \Re^m$ is given by 5.2.

$$y_k = C_k x_k + D_k u_k + v_k \quad (5.2)$$

Equation 5.1 is referred to as a "state equation" or "process equation". This equation explains the dynamics, stability, controllability, and disturbance sensitivity of the system. The control input to the system is $u_k \in \Re^p$, and $w_k \in \Re^n$ is a random variable that represents the "process noise" [27]. The output equation of the discrete system is represented in the equation 5.2, the output state equation defines the dependency on the state vector x_k , control input u_k and $v_k \in \Re^m$, Which models the measurement noise in the system.

The matrix $A_k \in \Re^{n \times n}$ describes the system dynamics and relates the state at the previous time step $k - 1$ to the state at the current time step k when the control input u_k is zero. The matrix $B_k \in \Re^{n \times p}$ relates the control input u_k to the state x_k . The matrices $C_k \in \Re^{m \times n}$ and $D_k \in \Re^{m \times p}$ relate the measurement y_k to the state x_k and control input u_k . All these matrices can be time-varying which can be extensively described through the Extended Kalman Filter.

Given a system model, a known control input u_k , a known measurement y_k , and certain assumptions, the Kalman filter approach can provide the most accurate estimation of the unmeasured state value x_k . First, it is assumed that both w_k and v_k are mutually uncorrelated white Gaussian random processes with zero mean and known values for the covariance matrices.

$$P(w) \sim N(0, Q); P(v) \sim N(0, R) \quad (5.3)$$

Process noise covariance Q and measurement noise covariance R might change with each time step, but here we assume that they are constants [27]. The system must also be "observable," which means that it must be feasible to infer its state from its output. This criterion is met by the system we are developing.

Algorithm 4: General Discrete Kalman Filter Algorithm

```

1 Initialize
2  $A, B, C, D$ 
3  $x_0, P_0, Q, R$ 
4 while  $I$  do
5    $State1Prediction : updateInput(u_k)$ 
6    $x_{k+1/k}(x_k, u_k)$ 
7    $P_{k+1/k}(P_k)$ 
8    $State2Update : updateMeasurment(y_k)$ 
9    $KalmanGain : K_k(y_k, P_{k+1/k})$ 
10   $Updatestate :$ 
11   $x_{k+1}(K_k, y_k, x_{k+1/k})$ 
12   $P_{k+1}(K_k, P_{k+1/k})$ 
13 end

```

Algorithm 5: General Discrete Kalman Filter Algorithm

```

1 Initialize
2  $InitialEstimate : x_{0/0}$ 
3  $ErrorCovariance : P_0, Q, and R, k = 0$ 
4 while  $TRUE$  do
5    $State1Prediction : updateInput(u_k)$ 
6    $DetermineState x_{k + 1/k} = Adx_k/k + Bdu_k$   $DetermineOutput$ 
     $y_{k + 1} = Cd x_k/k + Ddu_k$   $DetermineErrorCovariance$ 
     $P_{k + 1/k} = AdP_k/kAdT + R$ 
7    $State2Correction : updateMeasurment(y_k)$ 
8    $DetermineKalmanGain$ 
     $K_{k + 1} = P_{k + 1/k}CdT[CdP_k + 1/kCdT + Q]^{-1}$ 
     $EmployCorrectiononPredictionofStates$ 
     $x_{k + 1/k + 1} = x_{k + 1/k} + K_{k + 1}[y_{k + 1} - y_{k + 1}]$ 
     $DetermineErrorCovariance P_{k + 1/k + 1} = [I - K_{k + 1}Cd]P_{k + 1/k}$ 
9 end

```

- **Initialization :** A, B, C, and D represent the system and have to be defined. Then the state vector x_0 and its associated covariance vector P_0 for $K = 0$ are initialized. Both perturbations, w and v are uncorrelated white Gaussian random processes with known value covariance matrices Q and R are initialized at this step of the algorithm.

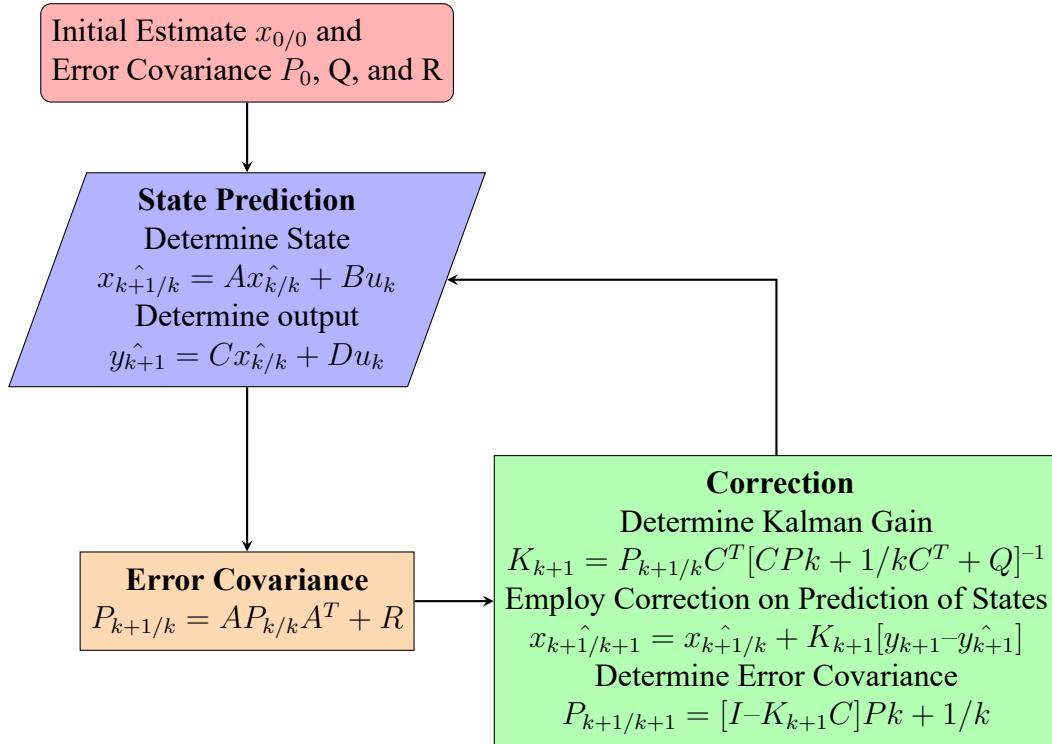


Figure 5.1: Discrete Kalman Filter Algorithm Flow Chart

- **Prediction :** For each iteration k newly acquired input data, u is injected into the system, Based on the calculated prior state x_k and $x_{k+1/k}$, the state vector is predicted along with predicted covariance $P_{k+1/k}$.

$$x_{k+1/k} = A_k x_k + B_k u_k \quad (5.4)$$

$$P_{k+1/k} = A_k P_k A_k^T + Q \quad (5.5)$$

If the system is stable then $A_k P_k A_k^T$ is diminished and reduces the uncertainty of the state estimation over time. The process noise term Q always increases the uncertainty because w_k cannot be measured. The second estimated x_{k+1} tunes up the first estimated $x_{k+1/k}$ (prior state) after measuring the system output y_k . The state and error covariance x_{k+1} and P_{k+1} are more accurate than $x_{k+1/k}$ and $P_{k+1/k}$ as they involve the information from the measurement y_k .

- **Correction and Update :** A correction factor () equal to the system output is added to the new measurement to provide fresh information.

5.1.2 Extended Kalman Filter

The extended Kalman filter is the Kalman filter for nonlinear systems. With the extended Kalman filter technique, a linearization procedure is carried out at each time step to approximate the nonlinear system with a linear time-varying system. The extended

Kalman filter for the real nonlinear system is produced by using the linear time-changing system in a Kalman filter. Similar to a Kalman filter, an extended Kalman filter assumes that the process noise and sensor noise are independent, zero-mean Gaussian noises and uses the measured input and output to get the minimum mean squared error estimate of the true state

In the battery pack system Equation 28 and 29, the system state variables are defined as $x_1(t) = SOC_0$ and $x_2(t) = V_{cs}$. The input is defined as $u(t) = i_{batt}$ and the output is $y(t) = V_{batt}$. The battery pack system Equation 28 and 29 can be rewritten as :

$$\dot{x} = f(x, u) + w \quad (5.6)$$

$$y = g(x, u) + v \quad (5.7)$$

where $x = [x_1, x_2]^T$, The functions $f(x, u)$ and $g(x, u)$ are :

$$f(x, u) = \begin{bmatrix} \frac{u}{kC_{OTC}} \\ -\frac{1}{R_{OTC}C_{OTC}}x_2 + \frac{1}{C_{OTC}}u \end{bmatrix} \quad (5.8)$$

$$g(x, u) = kx_1 + x_2 + R_0u + d \quad (5.9)$$

If the functions $f(x, u)$ and $g(x, u)$ are linearized by a first-order, Taylor series expansion, at each sample step about the current operating point, the linearized model is

$$\delta\dot{x} = A_k\delta x + B_k\delta u \quad (5.10)$$

$$\delta y = C_k\delta x + D_k\delta u \quad (5.11)$$

where ;

$$A_k = \frac{df(x, u)}{dx} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{OTC}C_{OTC}} \end{bmatrix} \quad (5.12)$$

$$B_k = \frac{df(x, u)}{du} = \begin{bmatrix} -\frac{1}{KC_{cb}} \\ -\frac{1}{C_{OTC}} \end{bmatrix} \quad (5.13)$$

$$C_k = \frac{df(x, u)}{dx} = \begin{bmatrix} K & 1 \end{bmatrix} \quad (5.14)$$

$$D_k = \frac{df(x, u)}{du} = [R_0] \quad (5.15)$$

The battery model represented by equation 5.10 and 5.13 can be discretized as

$$x_{k+1} = A_d x_k + B_d u_k \quad (5.16)$$

$$y_{k+1} = C_d x_k + D_d u_k \quad (5.17)$$

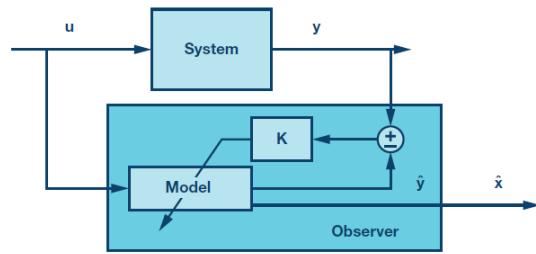


Figure 5.2: Kalman Filter Principle

where $A_d \simeq E + T_c A_k$, $B_d \simeq T_c B_k$, E is the unit matrix and T_c is the sampling period, and $C_d \simeq C_k$, $D_d \simeq D_k$.

Chapter 6

Misellaneous

6.1 Chapter 1

6.1.0.a BLUeNRG-355mc BLE module Layout :

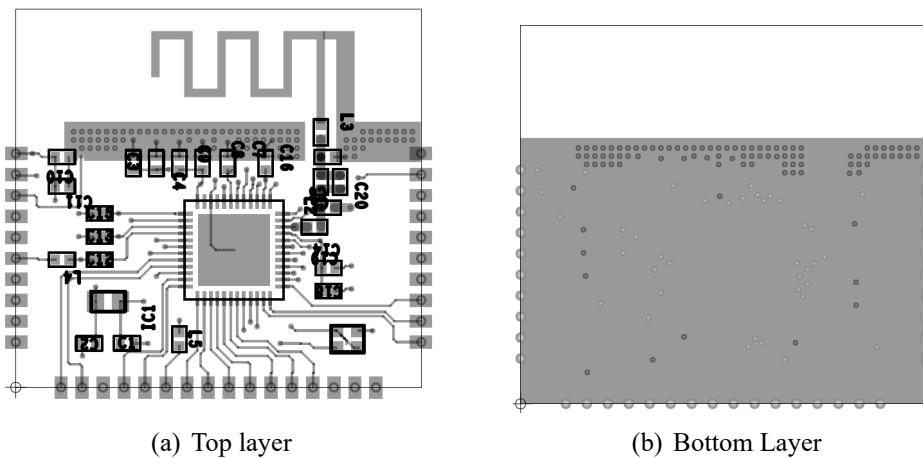


Figure 6.1: BLUeNRG-355mc BLE Module Layout

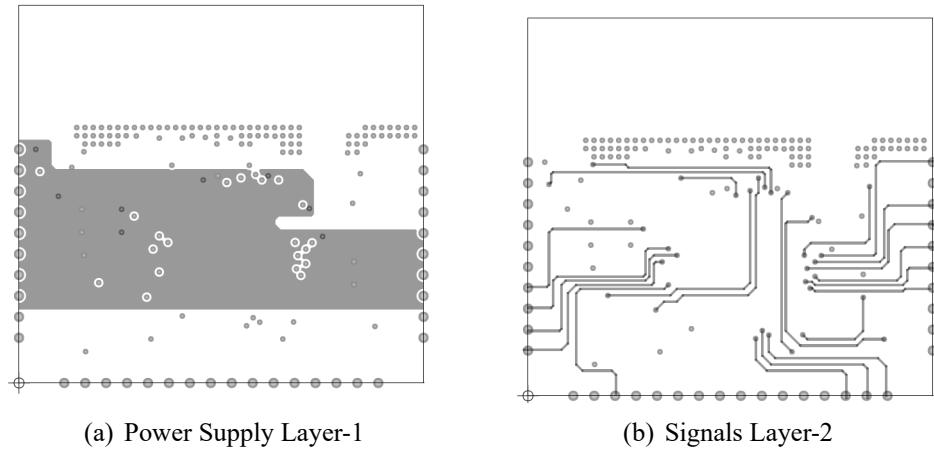


Figure 6.2: BLUeNRG-355mc BLE Module Layout

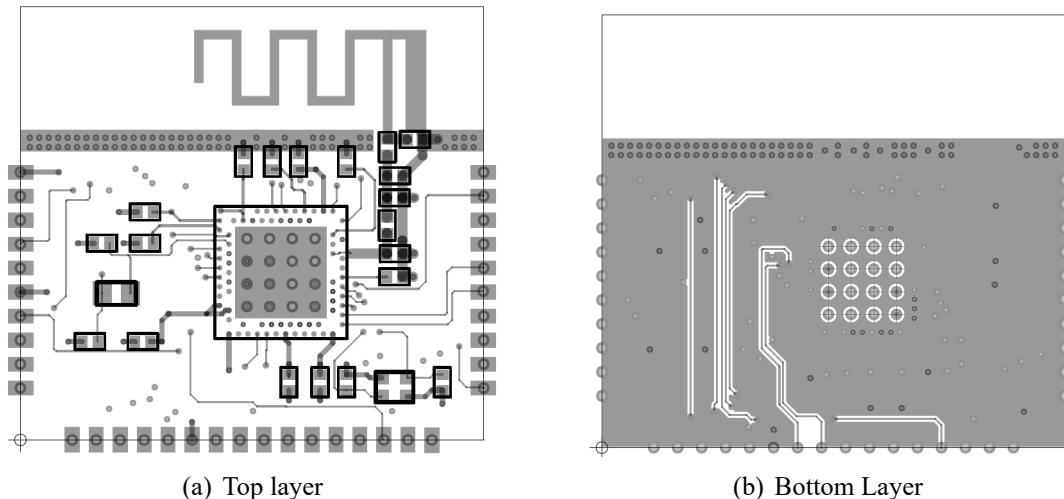
6.1.0.b Nordic nrf52840 BLE module Layout :

Figure 6.3: Nordic nrf52840 BLE module Layout

6.2 Chapter 2

6.2.0.a Design Example for the LTC4321 Gate Driver :

As Design takes the following specifications for the Figure6.8 application circuit. The application is rated for a max battery pack voltage of 24V at 5A, $C_L = 100\mu F$. UV raising=23V, UV falling = 22V, OV rising = 26V.

Sense Resistor :

$$R_{sense} = \frac{\Delta V_{sense(CB)(MIN)}}{I_{Inrush}} = \frac{(47mV)}{(2A)} = (23.5m\Omega) \quad (6.1)$$

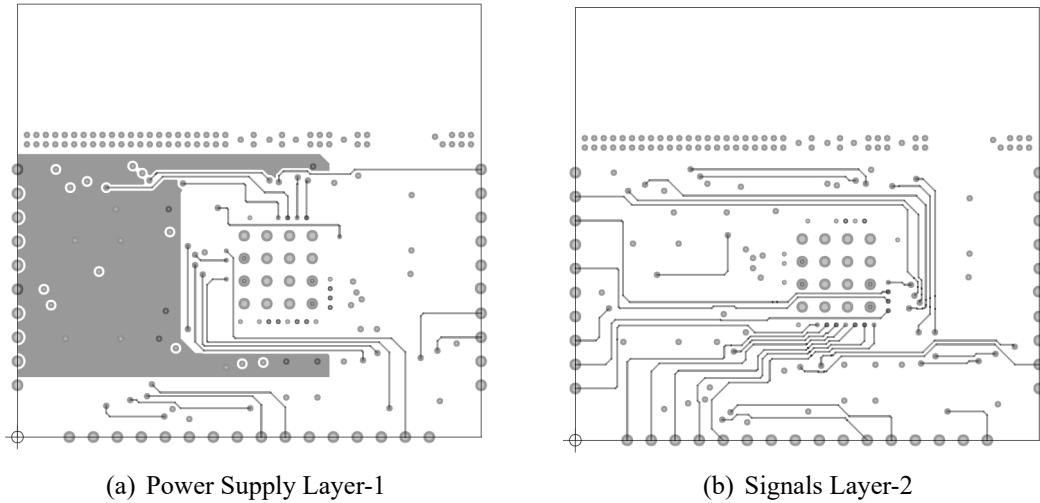


Figure 6.4: Nordic nrf52840 BLE module Layout

Use RSENSE = 22.5mΩ for margin. Worst case analog current limit:

$$I_{LIMIT(MIN)} = \frac{\Delta V_{sense(ACL)(MIN)}}{R_{sense}} = \frac{(65mV)}{(23.5m\Omega)} = (2.89A) \quad (6.2)$$

$$I_{LIMIT(MAX)} = \frac{\Delta V_{sense(ACL)(MAX)}}{R_{sense}} = \frac{(90mV)}{(23.5m\Omega)} = (4A) \quad (6.3)$$

Calculate the worst-case time it takes to charge up CL analog current limit:

$$t_{CHARGE(MAX)} = \frac{C_L \times V_{IN}}{I_{LIMIT(MIN)}} = \frac{(100\mu F \times 24V)}{(2.89A)} = (0.9ms) \quad (6.4)$$

For inrush control using analog current limit, $t_{CHARGE(MAX)}$ must be less than the circuit breaker delay (tCB) for a proper start-up [18].

The worst-case power dissipation in MOSFET M1 occurs "

$$P_{DISS} = V_{IN} \times I_{LIMIT(MAX)} = (24V \times 4A) = (96W) \quad (6.5)$$

during a severe overcurrent fault when the current is controlled by analog current limit for the duration of tCB:

$$C_T = \frac{t_{CB}}{24V} = \frac{(2mS)}{(24V)} = (82nF) \quad (6.6)$$

If a low inrush current ($< \Delta V_{SENSE(CB)}$) is preferred, refer to the Figure 6.8 application circuit which uses a gate capacitor CG to limit the inrush current. Choose IINRUSH = 0.5A which is set using C_G [18]:

$$C_G = \frac{C_l \times 10\mu A}{I_{Inrush}} = \frac{(100\mu F \times 10\mu A)}{(2.89A)} = (20nF) \quad (6.7)$$

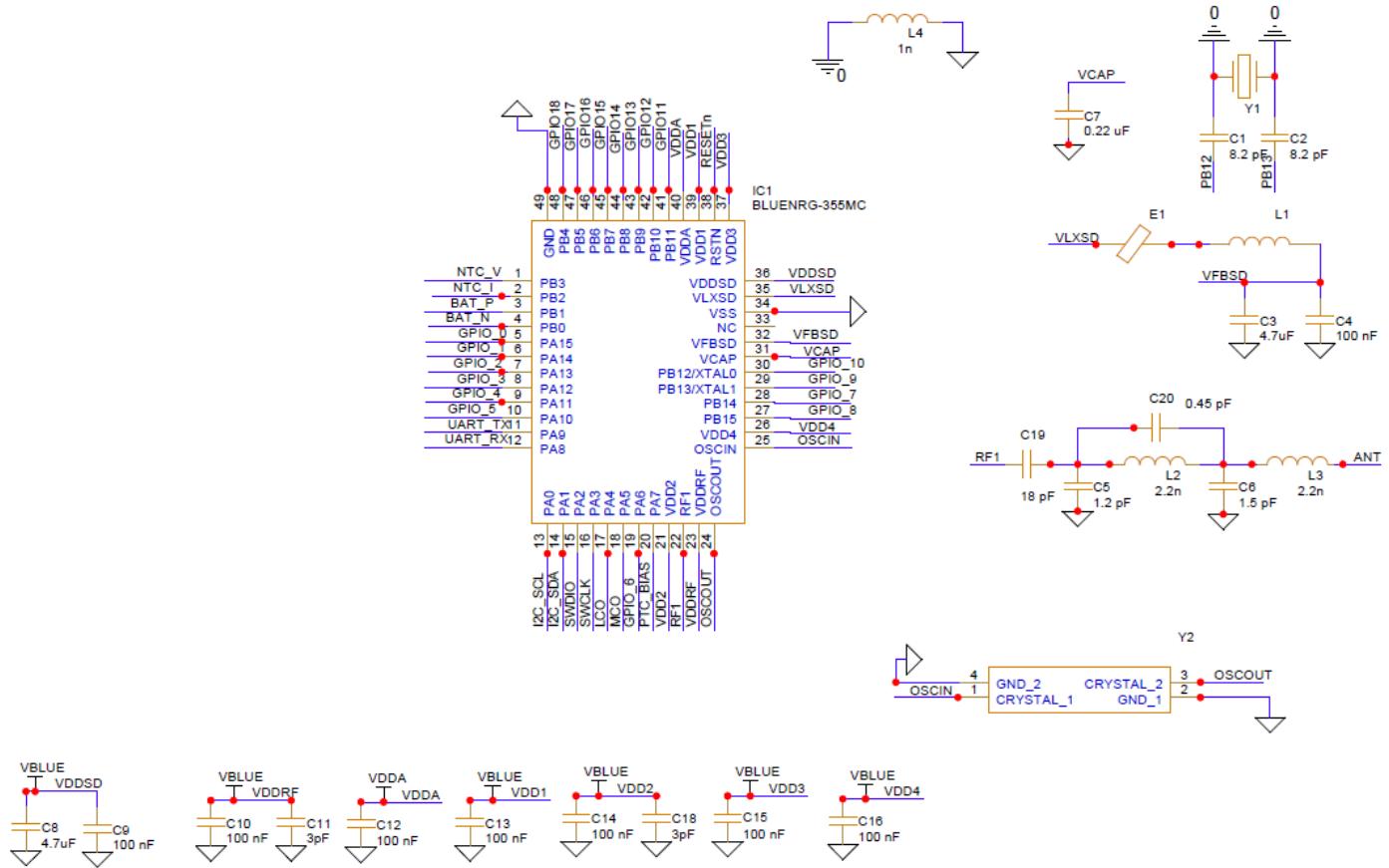


Figure 6.5: BLUeNRG-355mc BLE Complete Schematic

The time to charge up CL with 0.5A is:

$$t_{CHARGE(MAX)} = \frac{C_L \times V_{IN}}{I_{Inrush}} = \frac{(100\mu F \times 24V)}{(0.5A)} = (48ms) \quad (6.8)$$

The average power dissipation in the MOSFET M1 during this start-up is:

$$P_{DISS} = V_{IN} \times I_{LIMIT(MAX)} = (24V \times 0.5A) = (6W) \quad (6.9)$$

6.3 Chapter 4

6.3.1 Chroma SCPI Commands Example Programs

The following programming is a raw program that we can do through NI drivers.

6.3.1.1 Example 1: The following commands in example 1 simulate a BMS containing 16 independent batteries with sampling 10ms and current range to 5A. The initial voltage of the 16 batteries is 3.8V/2A and remains 0.5 second after output. When the voltage changes to 4.2V/3A and remains for 0.5 second, it reports the first 100

records of battery 1 and 2, and then turn off the output'[24].

```
*IDN?
SYSTem : FRAME : STATE? 0
SYST : FRAME? 0
SYST : FRAME : CHAN : STAT? 0
SYST : FRAME : CHAN : NUMB? 0
SYST : ERR?
SYSTem : ERRor?
SYST : FRAME : PROT : CLE
SIM : CONF : BMS : NUMB 1
SIM : CONF : BMS : NUMB?
SIM : CONF : SAMP : TIME 10
SIM : CONF : SAMP : TIME?
SIM : CONF : CELL : NUMB 1,16
SIM : CONF : CELL : NUMB? 1
SIM : CONF : CELL : PARA 1,1,16,1,2
SYSTem : ERRor?
SIM : PROG : CELL 1,1,1,16,3.8,2
SIM : OUTPON
SYSTem : ERRor?
SIM : OUTP?
*D 500
SIM : PROG : CELL 1,1,1,16,4.2,3
SYSTem : ERRor?
SIM : OUTP : IMM
SYSTem : ERRor?
*D 500
SIM : REP : CELL : REC : DATA? 1,1,1,100
SIM : REP : CELL : REC : DATA? 1,2,1,100
SIM : OUTPOFF
SYSTem : ERRor?SIM : OUTP?
```

6.3.1.2 Example 2: The following commands in example 2 simulate a BMS containing 16 independent batteries that are paralleled into 8 separate batteries with sampling 10ms and a current range of 5A. The voltage of the 8 batteries is 4.2 V/2A, and it performs measurement 1 second after output. It returns the instant voltage, current and protection status of BMS 1 8 batteries, and turns off the output after 10 seconds.

*IDN?

SYSTem : FRAME : STATE? 0

SYST : FRAME? 0

SYST : FRAME : CHAN : STAT? 0

SYST : FRAME : CHAN : NUMB? 0

SYST : ERR?

SYSTem : ERRor?

SYST : FRAME : PROT : CLE

SIM : CONF : BMS : NUMB 1

SIM : CONF : BMS : NUMB?

SIM : CONF : SAMP : TIME 10

SIM : CONF : SAMP : TIME?

SIM : CONF : CELL : NUMB 1,16

SIM : CONF : CELL : NUMB? 1

SIM : CONF : CELL : PARA 1,1,8,2,2

SIM : OUTPON

SYSTem : ERRor?

SIM : OUTP?

*D1000

SIM : MEAS : BMS : VOLT? 1

SIM : MEAS : BMS : CURR? 1

SIM : MEAS : BMS : PROT? 1

*D10000

SIM : OUTPOFF

SYSTem : ERRor?

SIM : OUTP?

6.4 Chapter 5

6.4.1

Extended Kaman Filter Implementation

```

1 class ExtendedKalmanFilter(object):
2     def __init__(self, x, A, B, P, Q, R, Hx, HJacobian):
3         self._x = x
4         self._A = A
5         self._B = B
6         self._P = P

```

```

7      self._Q = Q
8      self._R = R
9      self._Hx = Hx
10     self._HJacobian = HJacobian
11
12     def update(self, z):
13         P = self._P
14         R = self._R
15         x = self._x
16         # H Jacobian of Matrix C and D
17         H = self._HJacobian(x)
18         S = H * P * H.T + R
19         #K is the Kalman Gain
20         K = P * H.T * S.I
21         self._K = K
22         hx = self._Hx(x)
23         y = np.subtract(z, hx)
24         self._x = x + K * y
25
26         KH = K * H
27         I_KH = np.identity((KH).shape[1]) - KH
28         self._P = I_KH * P * I_KH.T + K * R * K.T
29     def predict(self, u=0):
30         self._x = self._A * self._x + self._B * u
31         self._P = self._A * self._P * self._A.T + self._Q
32     @property
33     def x(self):
34         return self._x

```

Listing 6.1: Extended Kalaman Filter Script

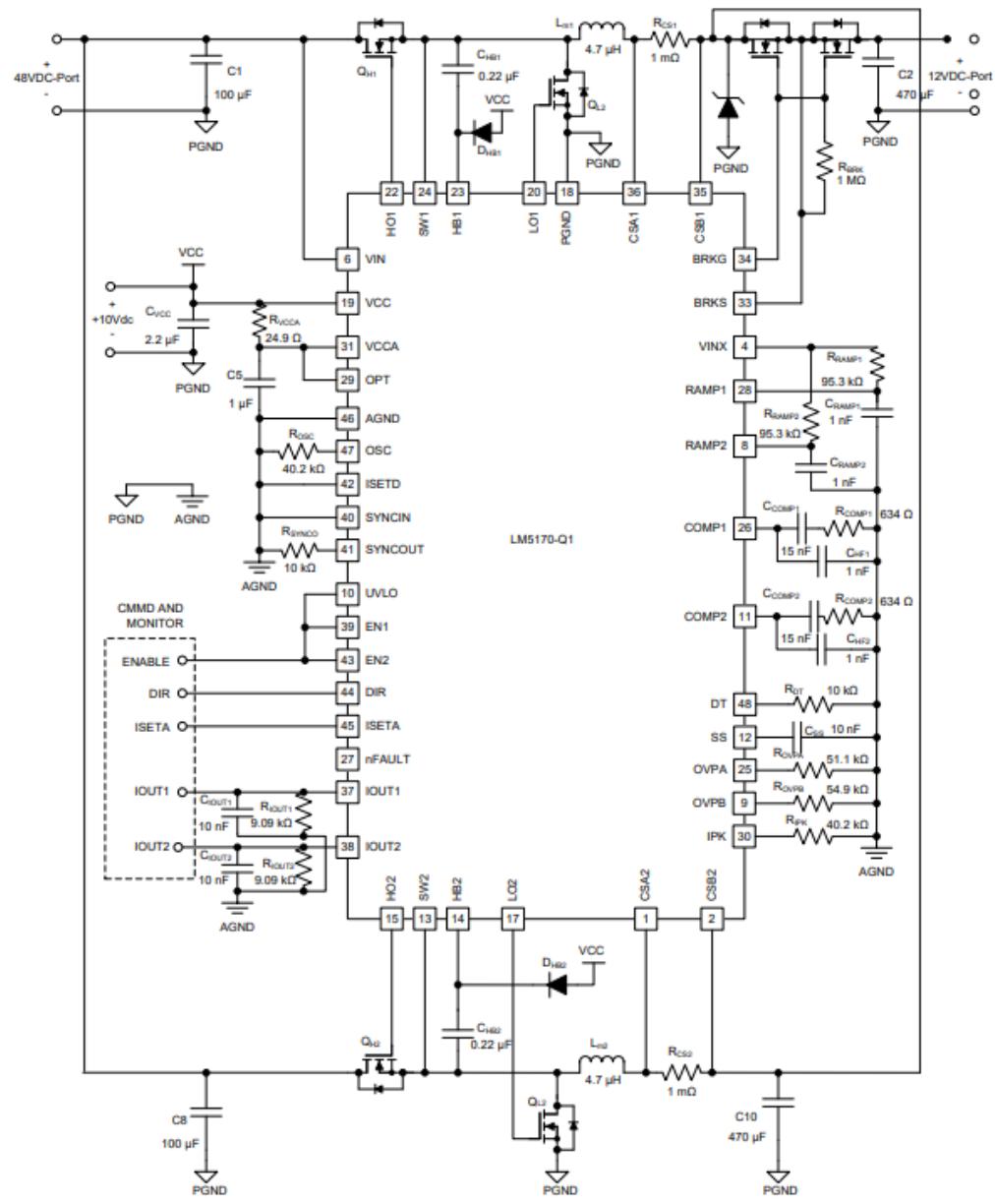
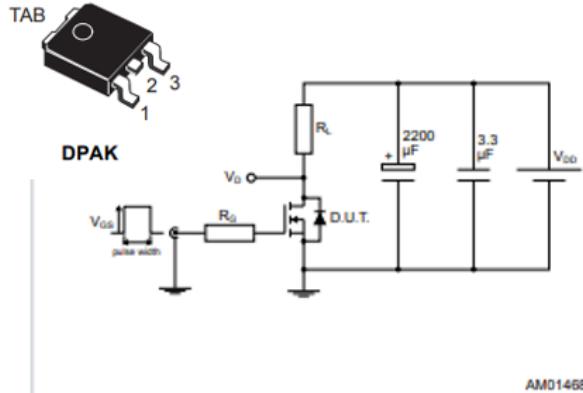
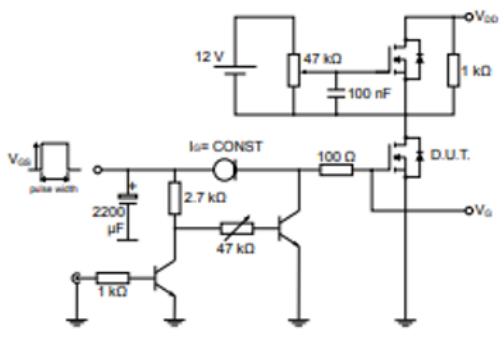
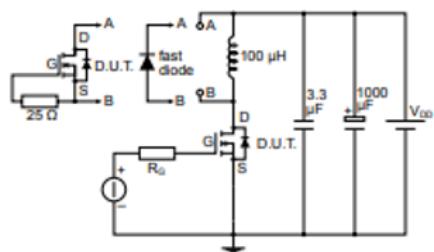
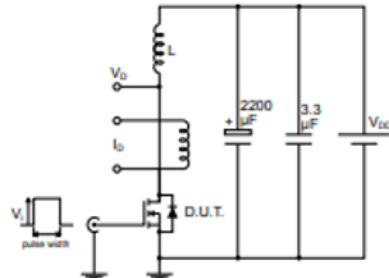
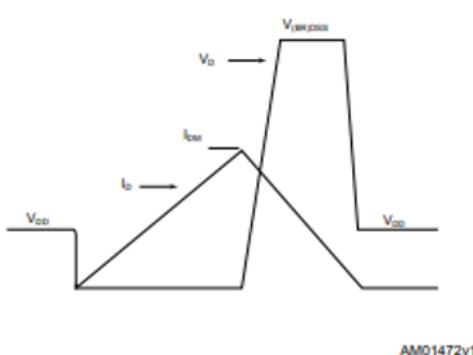
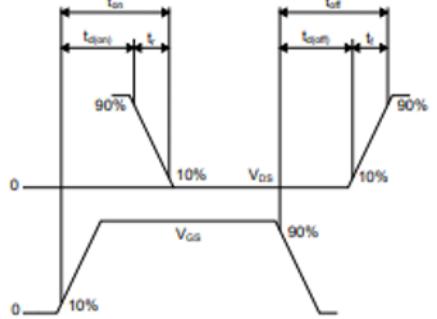


Figure 6.6: Typical Bidirectional circuit of the LM5170

Figure 11. Test circuit for resistive load switching times**Figure 12. Test circuit for gate charge behavior****Figure 13. Test circuit for inductive load switching and diode recovery times****Figure 14. Unclamped inductive load test circuit****Figure 15. Unclamped inductive waveform****Figure 16. Switching time waveform****Figure 6.7: STD20NF06L Application typical circuit and package**

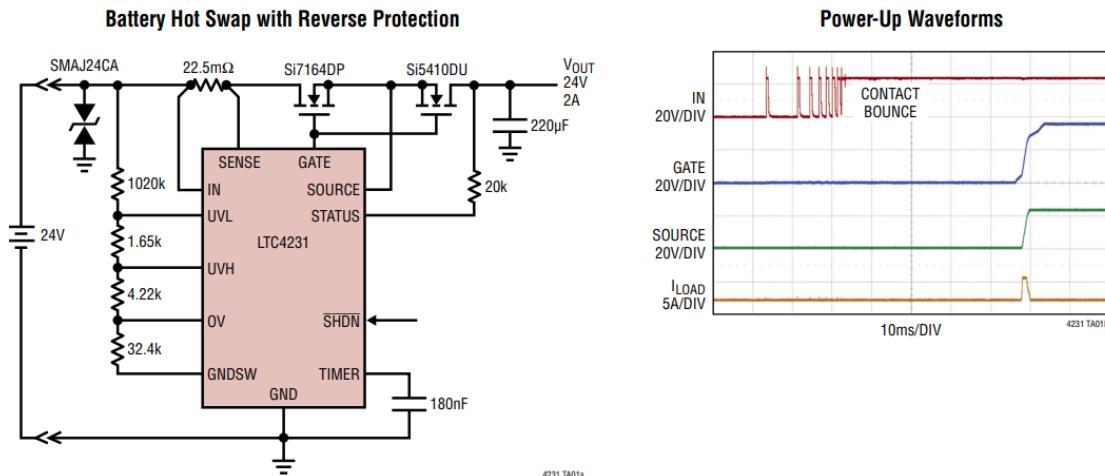


Figure 6.8: LTC4231 Application circuit and the Operational waveform

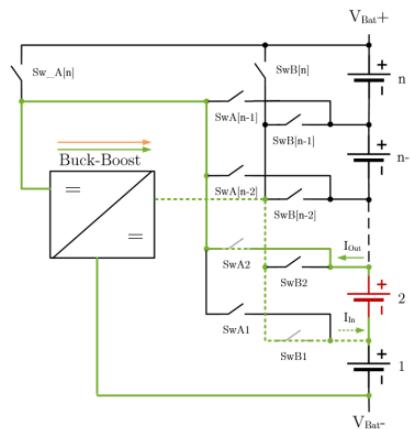


Figure 6.9: Type Ib Active Balancing Circuit

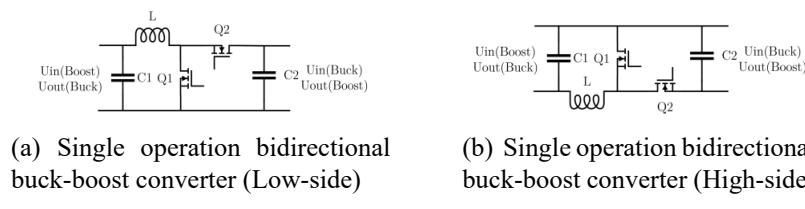


Figure 6.10: Typical Schematics of the Low side and High Side buck-boost Converter



Figure 6.11: keysight N6705 Power Supply and DMM 34460A

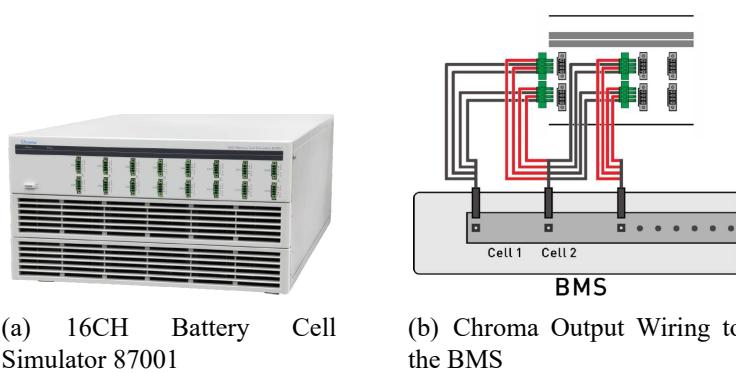


Figure 6.12: 16CH Battery Cell Simulator 87001

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