Case study: Materials selection for Power Electronics Packaging

Prepared for ME1000@IIITDM by Satish Gunturi

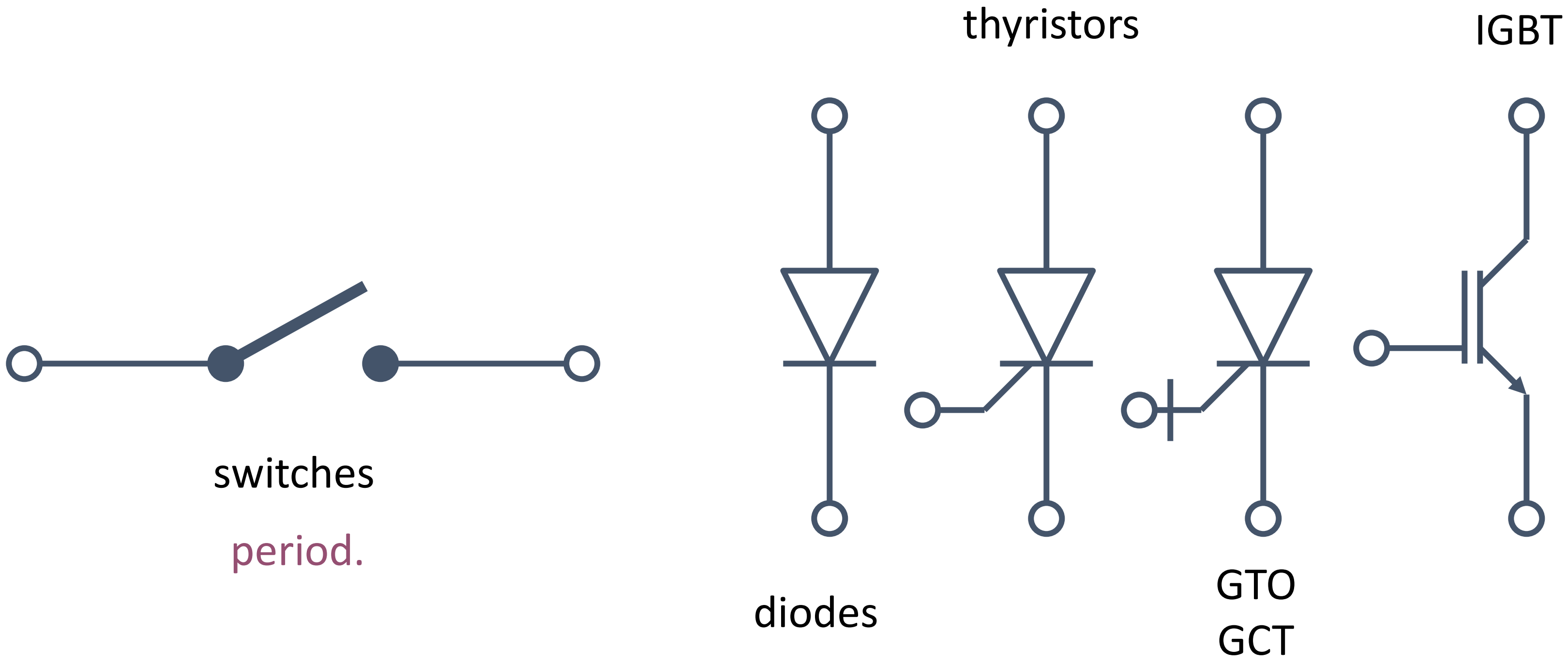
Adapted from refs:

- M. Ciappa / Microelectronics Reliability 42 (2002) 653–667
- A. Hamidi, J.H Fabian & S. Gunturi, "Packaging related failure mechanisms of high power IGBT modules" IPEC-Niigata, 2005

Power electronics products

- deal with power conversion from one from to another form using Inductors, Capacitors, Semiconductor devices (Diode, Thyristor, MOSFET, IGBT etc.).
- The power may range from mW to MW (Power Systems).
- Mainly used for energy conversion
  - DC ➔ AC
  - AC ➔ DC
  - $AC(V_1, \omega_1, \varphi_1) \rightarrow AC(V_2, \omega_2, \varphi_2)$
  - $DC(V_1) \rightarrow DC(V_2)$

Power Semiconductor products



Electronics Packaging

- An enclosure for a single element, integrated circuit or a hybrid circuit. Provides
  - hermetic or non-hermetic protection
  - Form factor
  - Serves as first level interconnection externally for the device through package terminals
- Functions of a PE package
  - Power and signal distribution
  - HV insulation
  - Heat dissipation
  - Protection

Power Semiconductors – Applications

Semiconductor Devices

Device Encapsulation

Standard- and Tailor-Made Products for...

...T&D

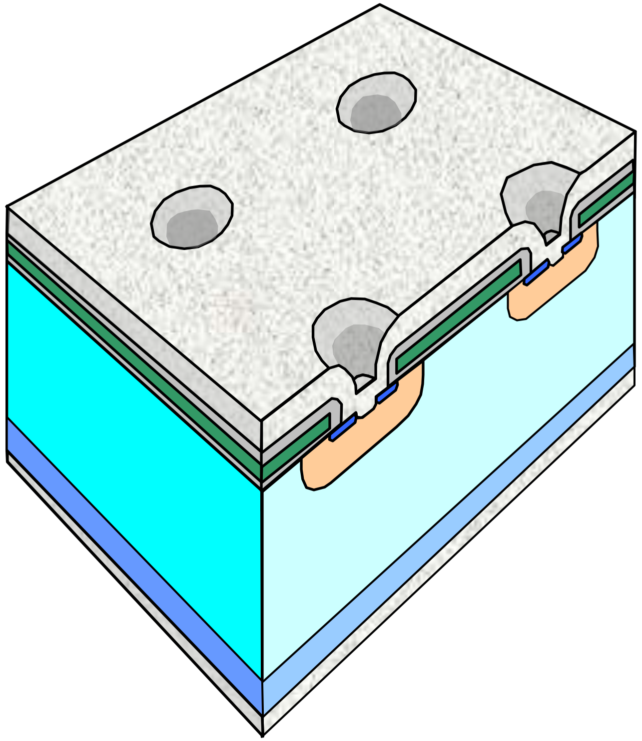
...Industry

...Transportation

Power Semiconductor Limitations

state-of-art safe-operating area of power semiconductors:
0.5 - 1 MW/cm^2

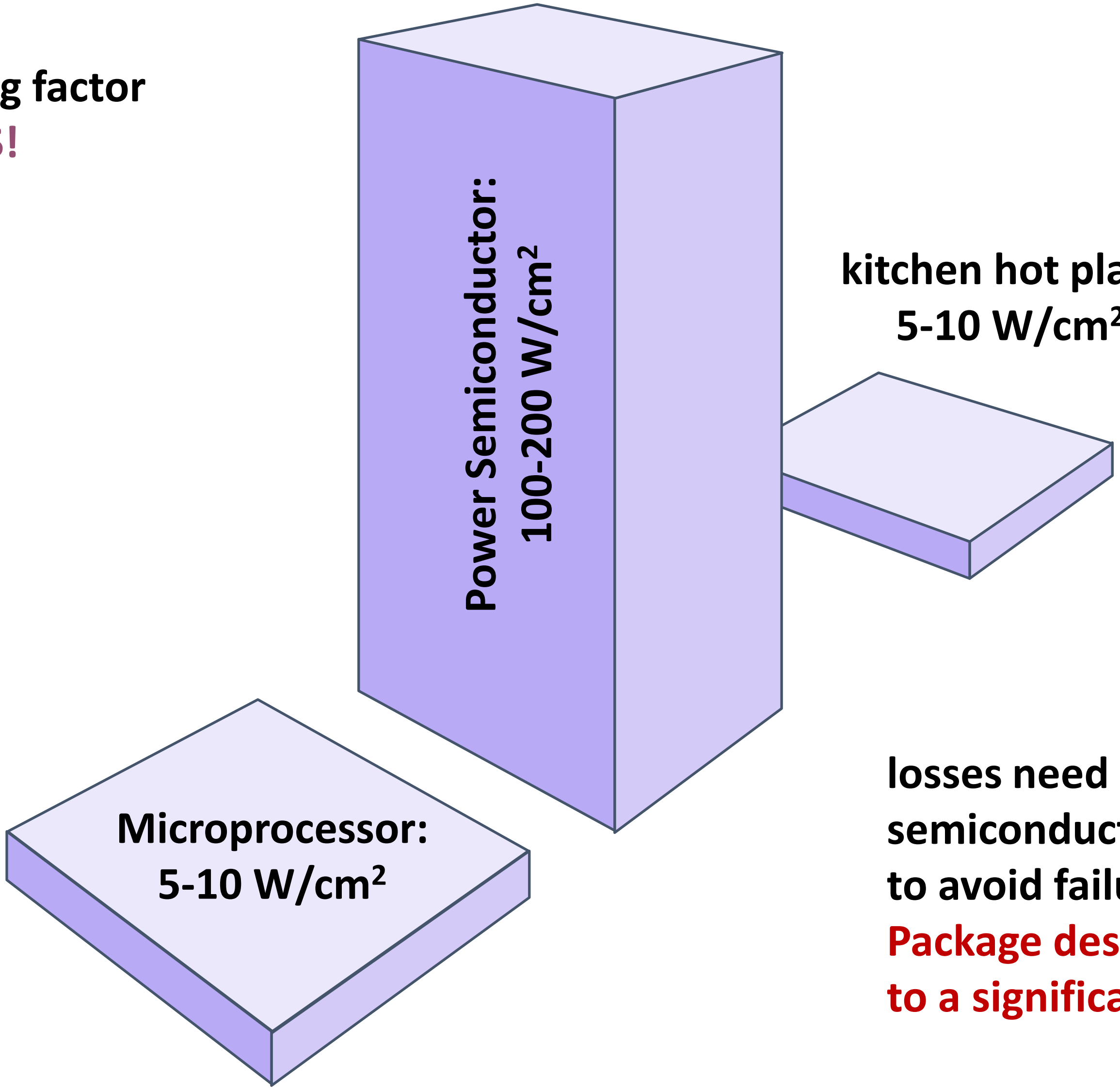
typical average operating power:
50 kW/cm^2



Semiconductor performance is not the limiting factor in power electronic systems

Power Semiconductor Limitations

The limiting factor are LOSSES!

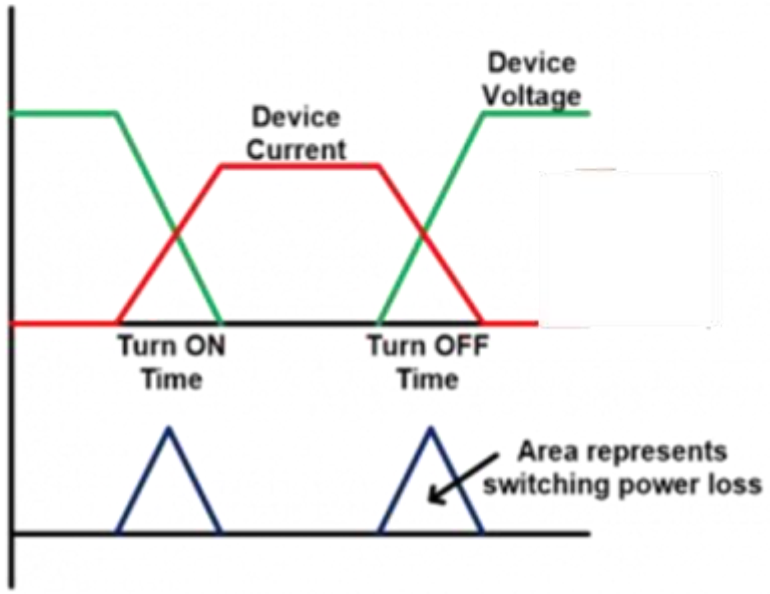


losses need COOLING to keep the semiconductor jn temp well below 125°C to avoid failures.

Package design based on thermal aspects to a significant extent

Origin of Losses in semiconductor packages

- Conduction losses - ohmic
- Blocking losses - leakage
- Switching losses

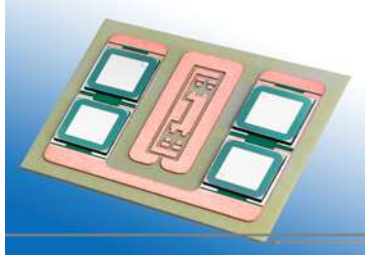


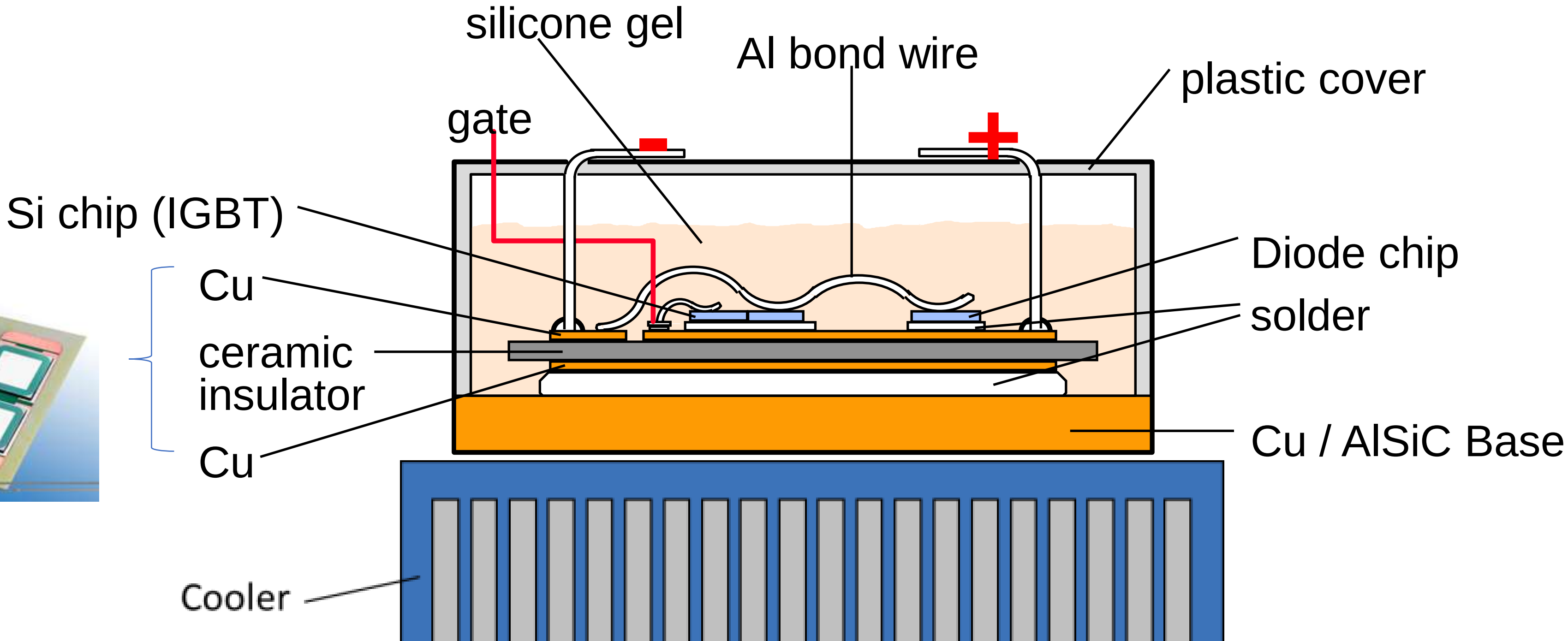
Wire Bonded Modules

Insulated module construction

Little cooling possible from topside due to poor conductivity of insulating mtls

Efficient cooling and thermal mismatch imp for performance without failures



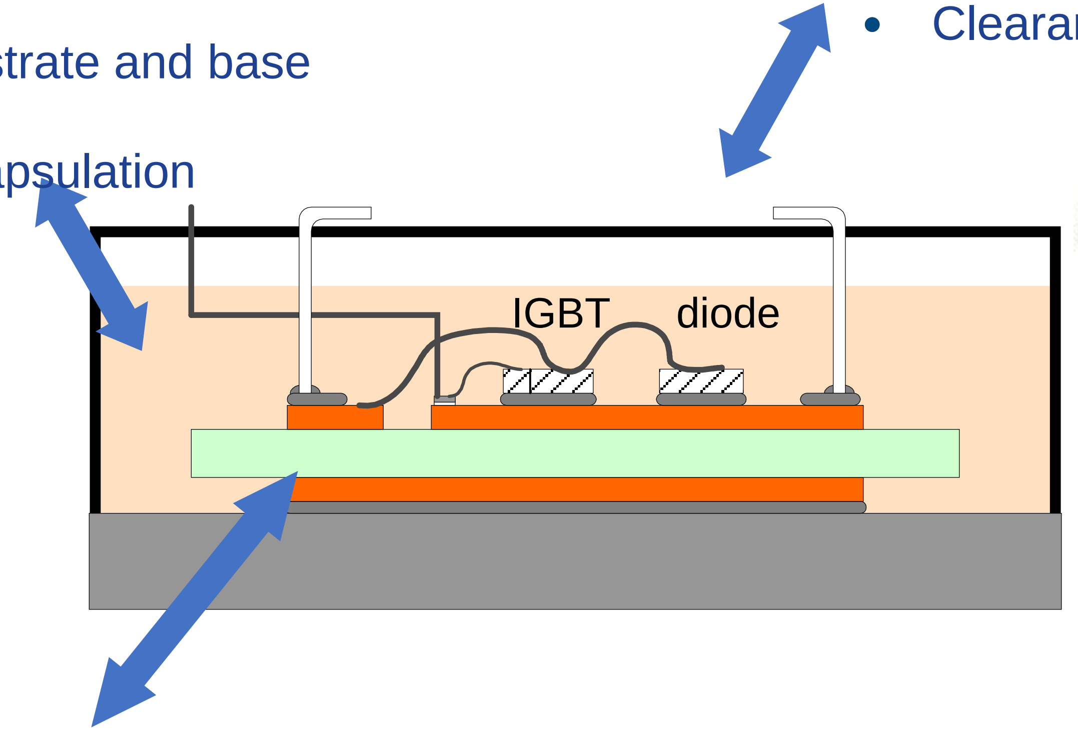


Materials for HV insulation

Voltage Insulation - Key components / characteristics

Silicone gel
- Good adhesion to substrate and base plate
- HV insulation and encapsulation

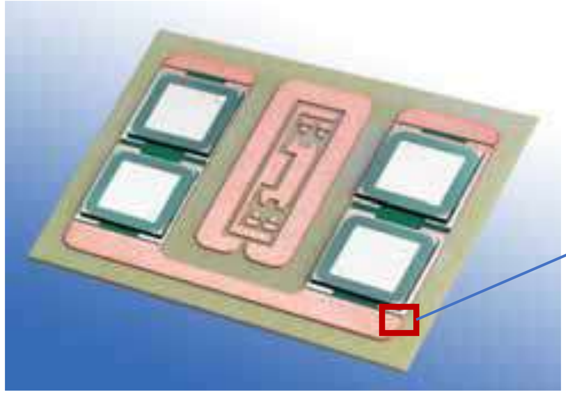
Plastic casing
- High CTI class material
- Clearance distances



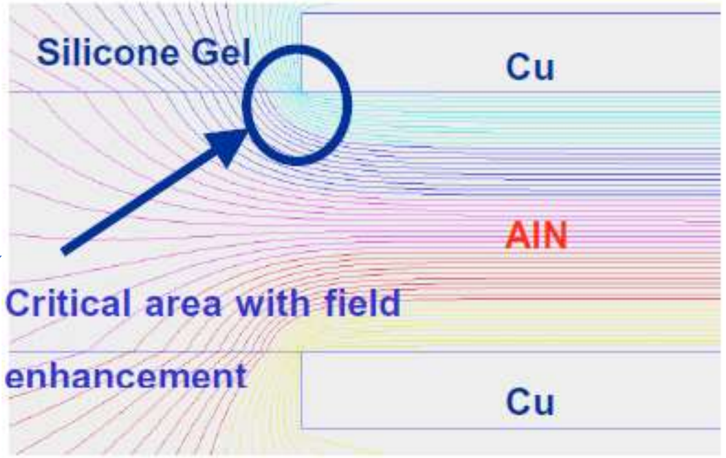
AlN ceramic substrate
- HV insulation and
- connection to heat sink (low thermal resistance required)

Hamidi et al. proc. IPEC 2005

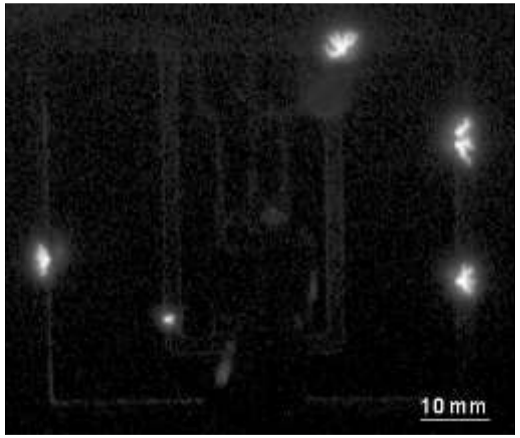
Partial discharge (PD) at AlN-Cu-Silicone triple points



AlN Substrate w Si chips / Cu overlay



Electrical field simulation



partial discharges at border of Cu layer.

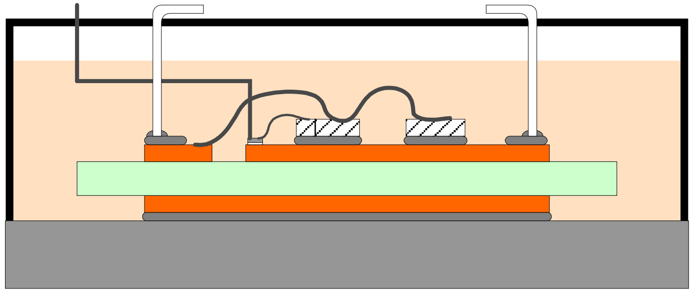
In order to minimize PD, the heel structure has to be smooth, the gel has to adhere well and no voids and bubbles should be enclosed at this critical region to avoid regions of high field concentration.

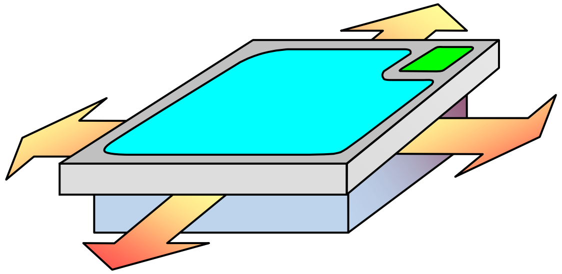
Post PD treeing in gel

Materials for Thermal conduction

Packaging Materials properties

Material	CTE [ppm/K]	E [GPa]	λ [W/mK]	Application
Si	2.6	128-185	150	current power device material
SiC	3.7	460	390	future power device material
Diamond	1-1.2	1000	2000	HV isolation, excellent thermal properties, heat spreaders for laser diodes
Al_2O_3	5.5	370	30	HV isolation, cost effective
AlN	3.1	340	190	HV isolation, good thermal properties
Mo	4.8	310	130	CTE matching material in contact with die
Al	23	70	240	heat sink and bond wire material, low cost
Cu	16	120	390	high specific heat, not suited for liquid heat sinks
Silver	19	80	420	excellent current conductor, soft material used as plating for soldering and high current contacts
AlSiC	6.5-12	230	180-220	low CTE material for heat sinks, good thermal properties, CTE tailoring possible
FR 4	13	17	0.4	circuit boards, bus bar support
$Au_{97}Si_3$	13	80	27	eutectic solder, used for dye attach
$Pb_{63}Sn_{37}$	25	30	50	eutectic soft solder
thermal grease	-	-	0.4 – 1	used to increase thermal contact between dry surfaces

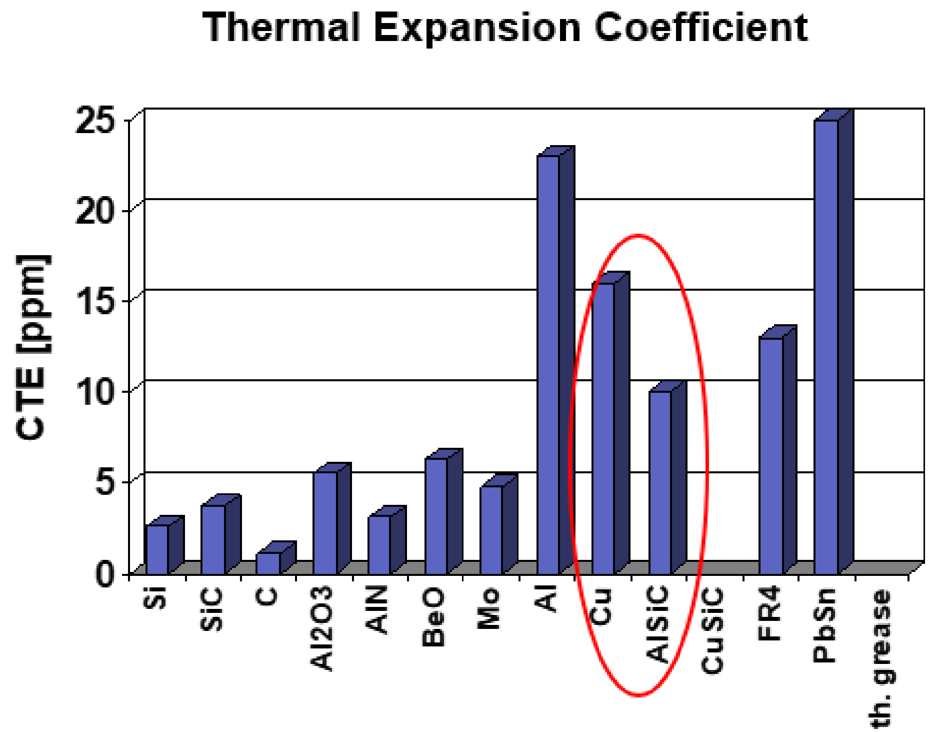


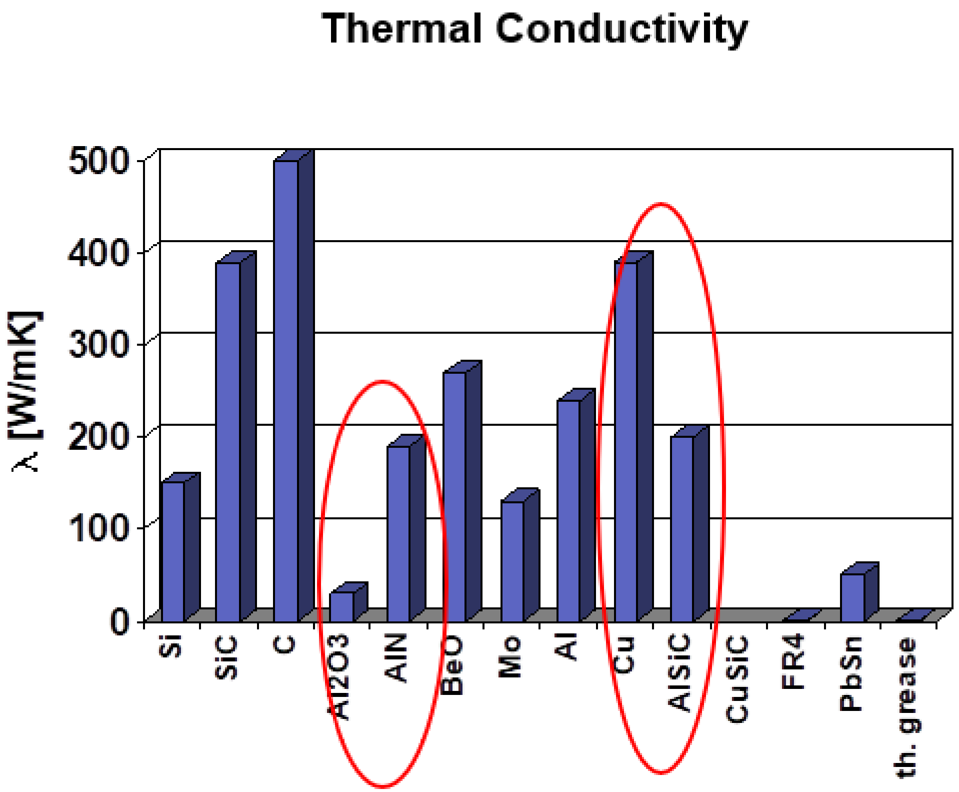


Thermal expansion mismatch

Al-SiC metal matrix composite plates and microstructure

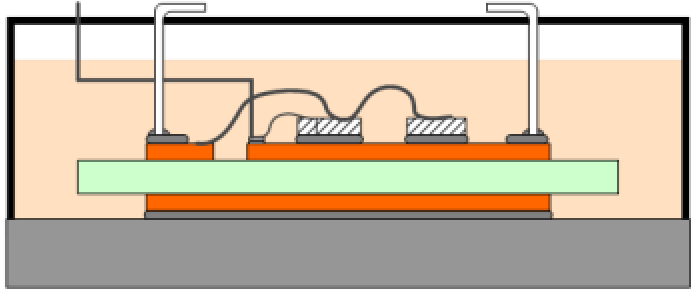
Packaging Materials Properties



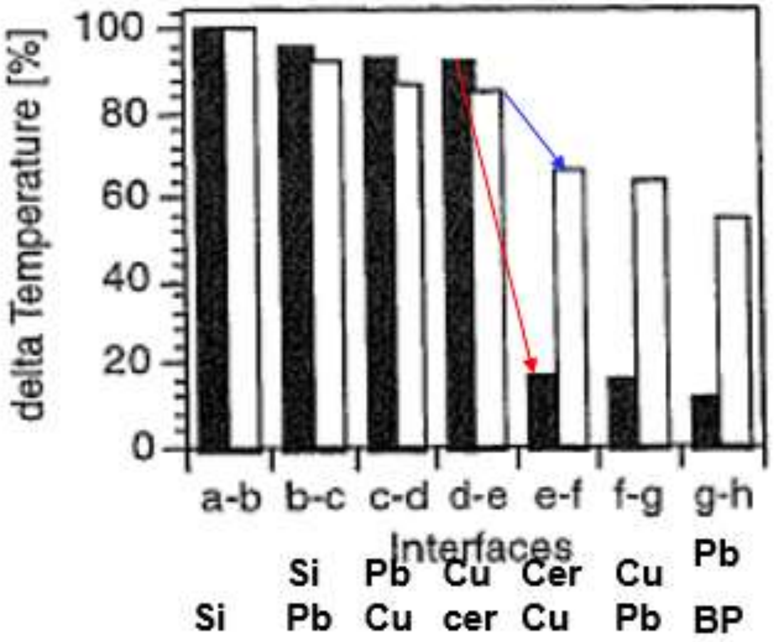


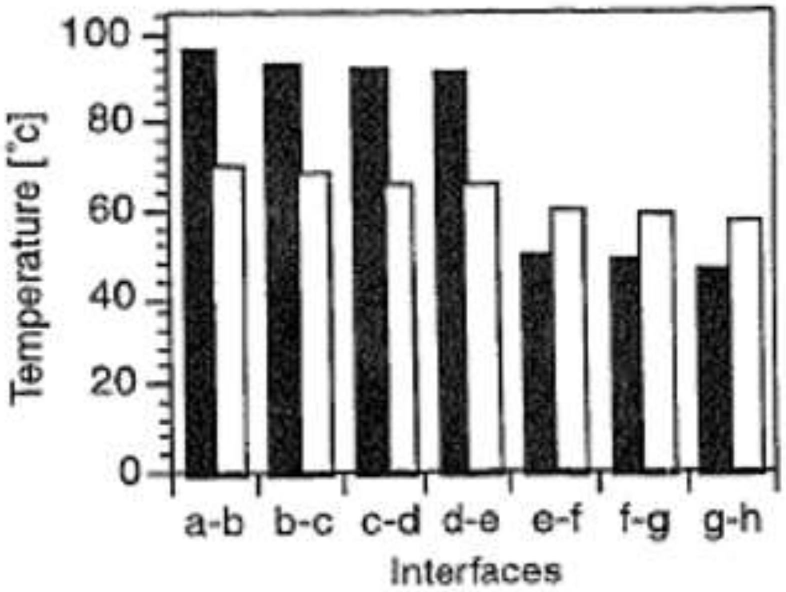
Al-SiC metal matrix composite plates and microstructure

Temperature swing in modules



M. Ciappa / Microelectronics Reliability 42 (2002) 653–667

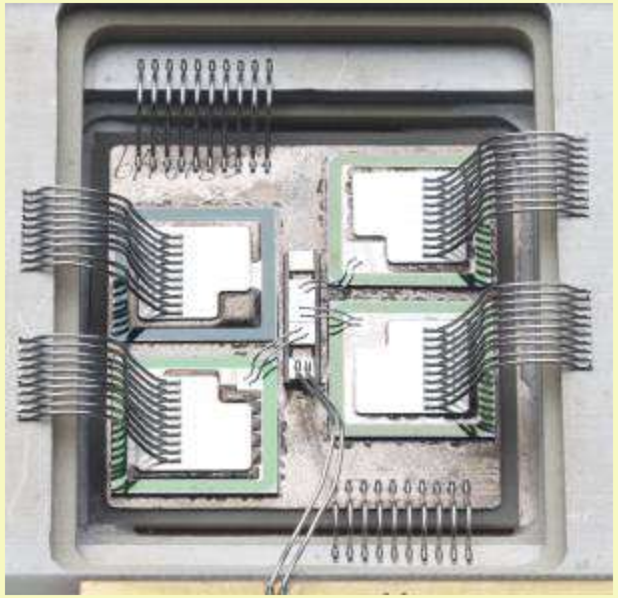




- Black bars: Ceramic insulation material Al_2O_3 (30w/mK), Cu (~400w/mK) baseplate
- White bars: Ceramic insulation material AlN (190w/mK), AlSiC (190w/mK) baseplate
- AlN and AlSiC with higher thermal conductivity reduce the thermal swing and the thermal resistance of the module ➔ lower failure probability

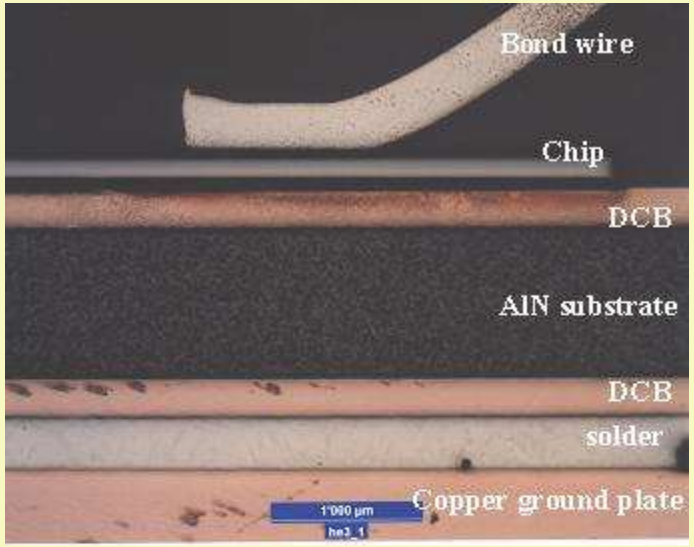
Temp effect on wire bonds and solder interconnects

Packaging of high power IGBT modules - Present Technology



Several hundreds of Al wires

Providing electrical interconnection between the large number of chips in parallel.

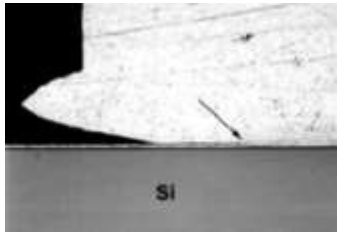


Several materials and interfaces

- AlN or Al2O3 DCB ceramics for HV insulation.
- Copper base-plate as mechanical support and heat-spreader.
- Solder layers between chips / DCB / Cu base-plate.

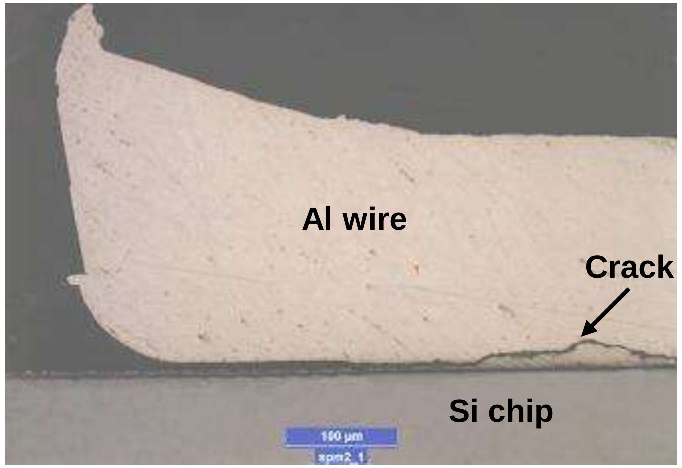
Other wire mtls used: Au, Ag, Cu based on properties & cost

Bonding by ultrasonic vibration – localized deformation causes bonding

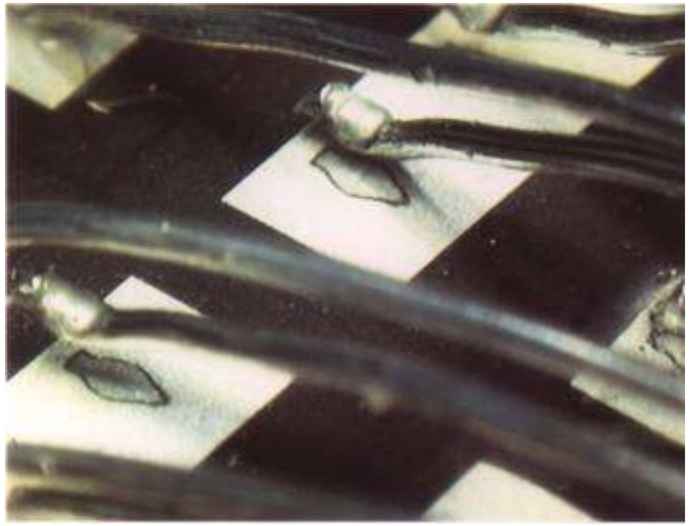


Thermo-mechanical Fatigue – Wire Bonds

- Failure Mechanism-1
  - Thermal expansion coefficient mismatch between Al (23 W/m.K) and Si (2.6 W/m.K)
  - High stress at bond interface during thermal cycling of the IGBTs.



Crack propagation in bond interface

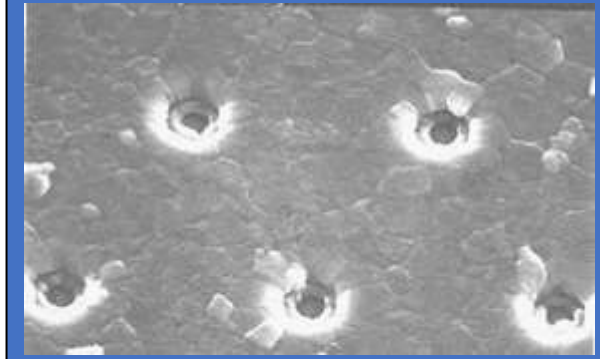


Wire lift-off

  - Appears as increase in Vce

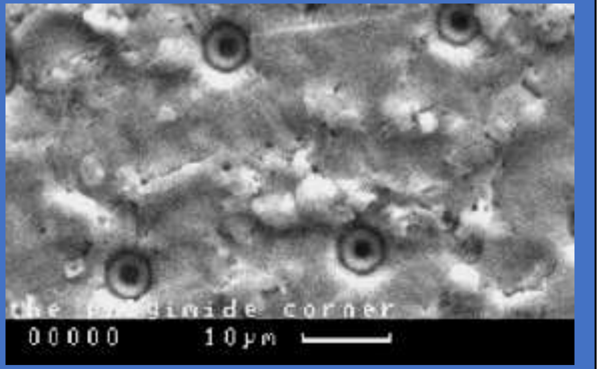
Wire Bond Lift-off Mechanism

SEM pictures of Al metallization on chip



Original surface

After thermal cycling

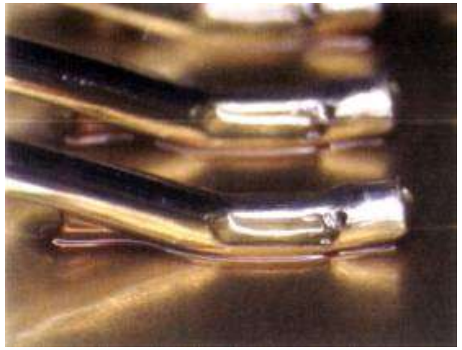


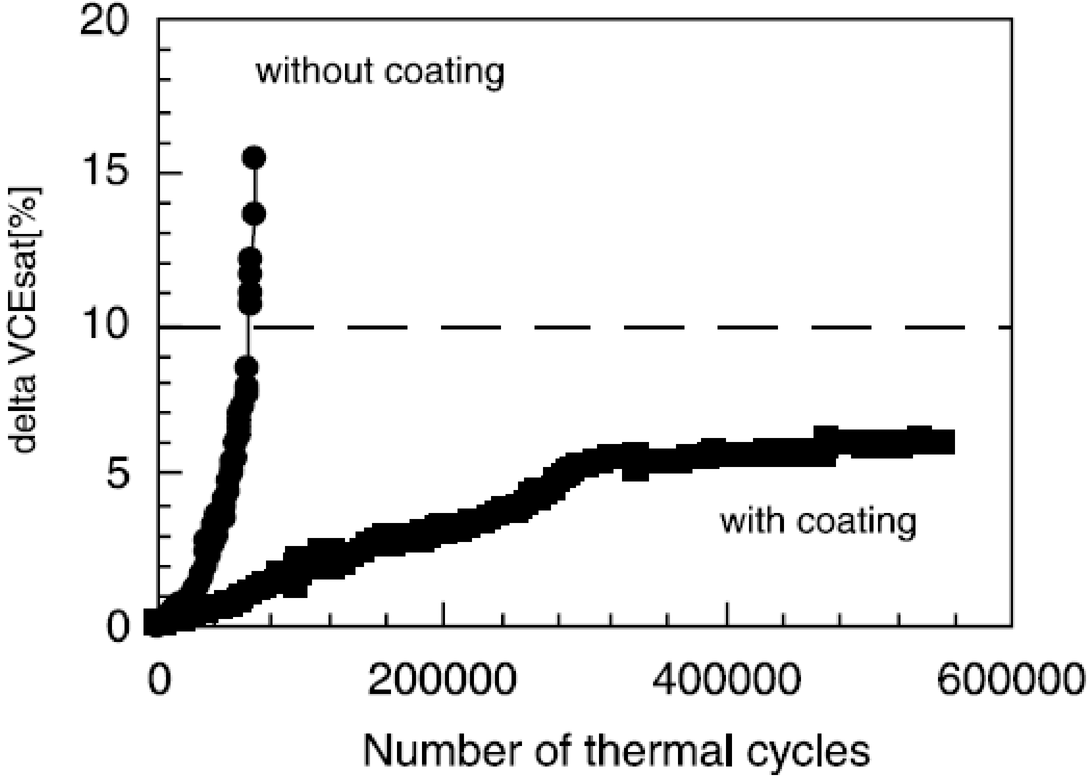
Conformal coating + thermal cycling

- Mechanism 2: Reconstruction of Al metallization due to CTE mismatch with the Si chip.
- Remedy: Conformal coatings improve wire bond lifetime by
  - inducing compressive forces on wire improving bond strength and
  - Reducing reconstruction of metallization (Al) on chip

Wire Bond Life Time Enhancement

- Conformal polymeric coatings on the wire bonds result in significantly improved life time under thermo-mechanical fatigue conditions

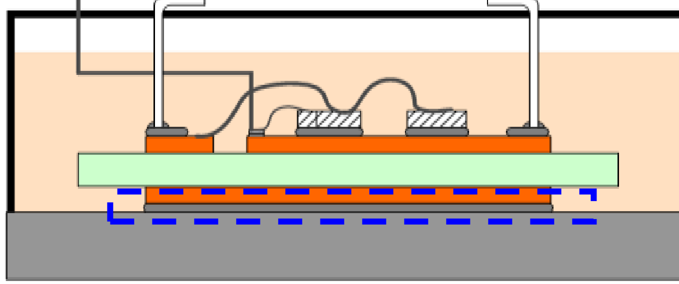




Wire bonds -summary

- Material selection: Al, Au, Ag or copper based on chip metallization and cost factors
- Process: Ultrasonic wire bonding
- Failures due to interface cracking and surface reconstruction due to CTE mismatch
    - Improve life/performance of wire bond further by application of polymer coating on wire bonds.

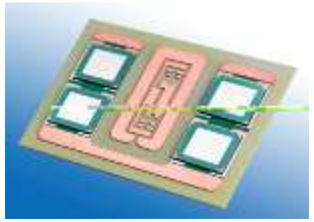
Solders

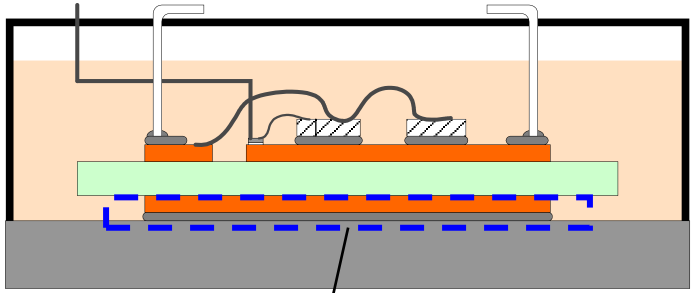


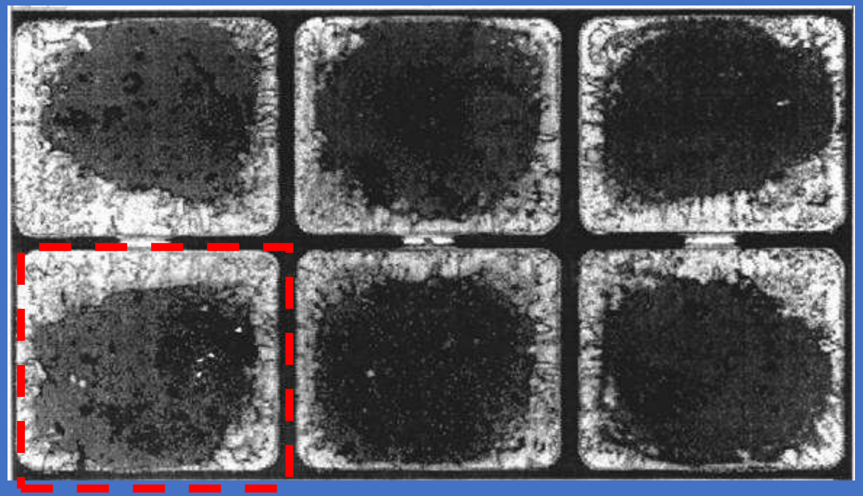
- Solders are either lead solders or lead free solders
- Soft lead solder helps to buffer strain due to expansion mismatch of components
- However cyclic stresses cause progressive delamination of solder layer.
    - As the area of delamination increases, the area of contact with the heatsink reduces ➔ higher thermal resistance and failure of chips above the delaminated area
- Remedy: Choose materials with closer CTE match

Thermo-mechanical Fatigue – Solder Joints

- Failure mechanism
  - Thermal expansion mismatch between ceramic (3.1ppm/K) and Cu baseplate (16 ppm/K).
  - Thermal cycling gives rise to stresses in solder layer leading to failure
  - Chips above debonded interface experience high thermal resistance / higher junction temp ➔degradation failures



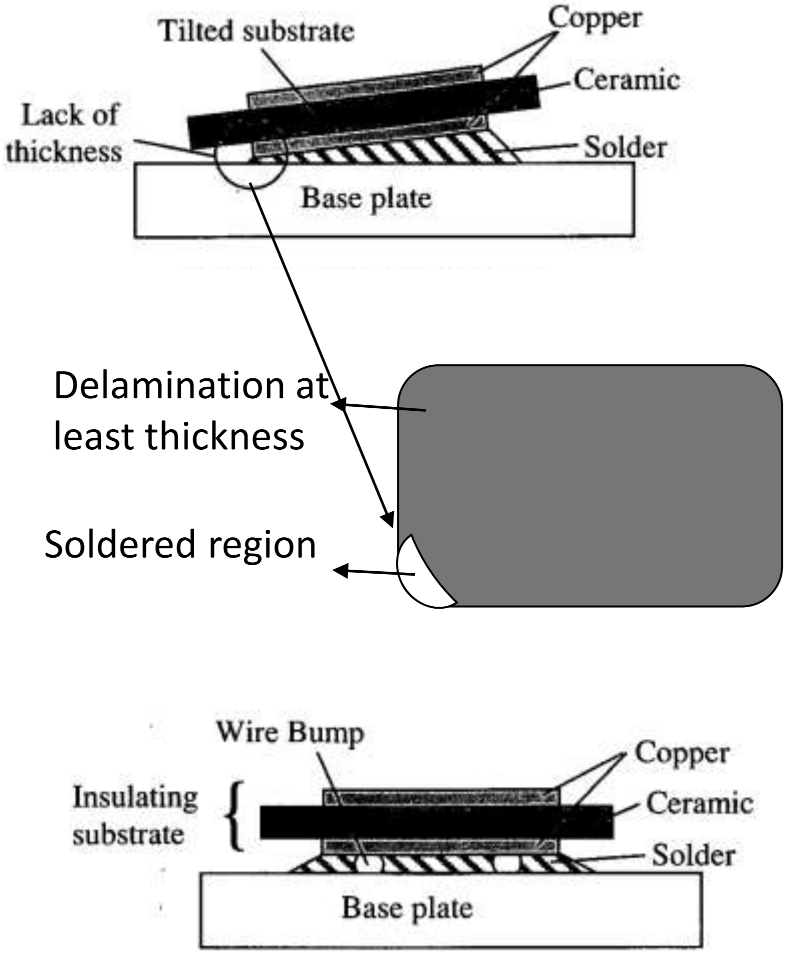


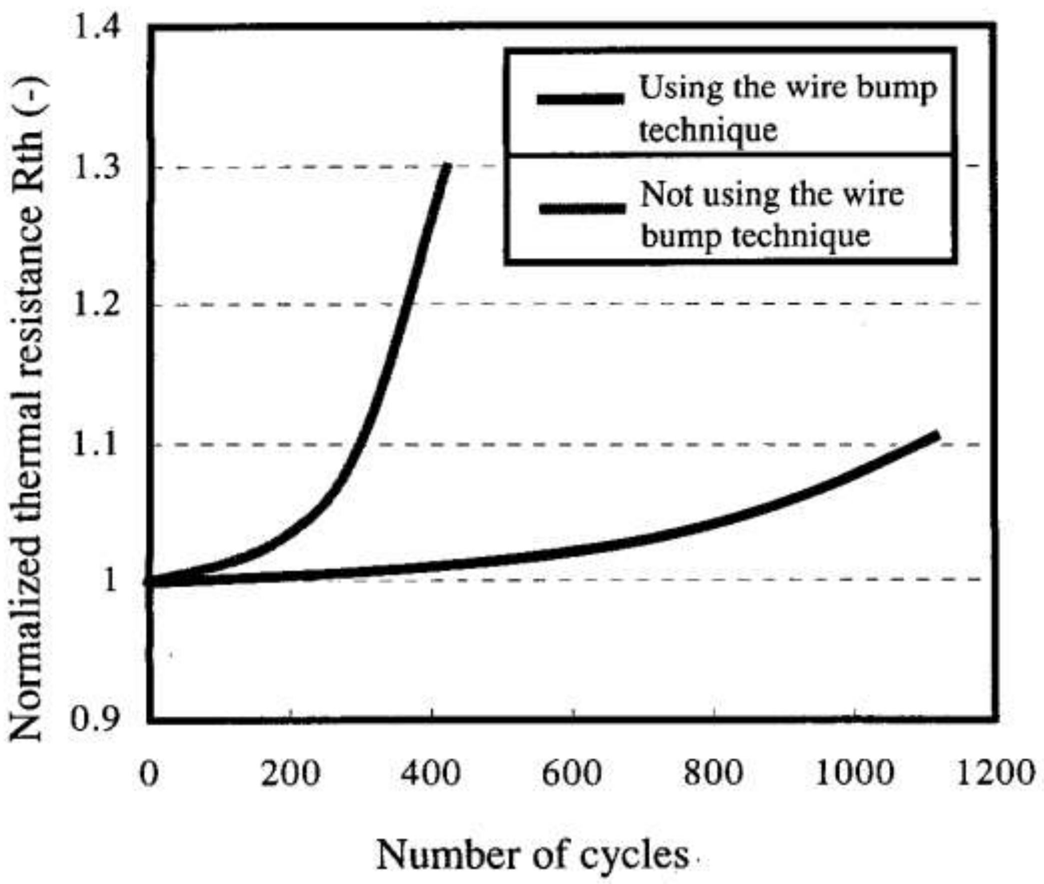


Solder interface between ceramic & Cu base plate

- AlSiC baseplate (6.5-9 ppm/K)
  - Reduces thermal expansion mismatch.
  - Enhances thermal cycling life time

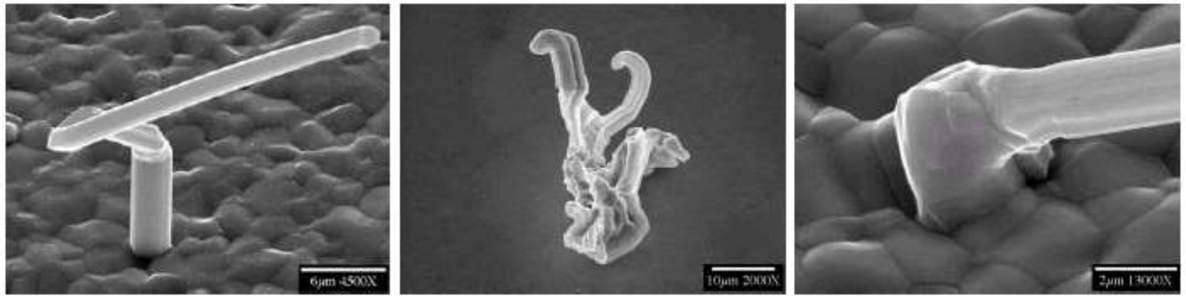
Solder tilt- effect on reliability





Hayashi K et al, ECTC2002

Issues with lead-free soldering

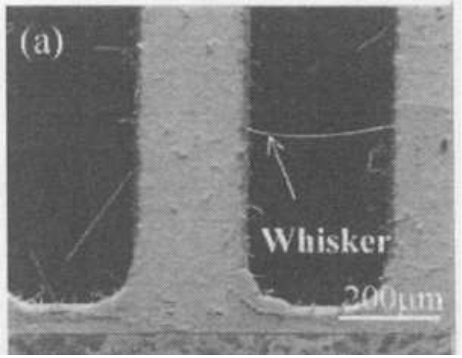


Kinked

Branched

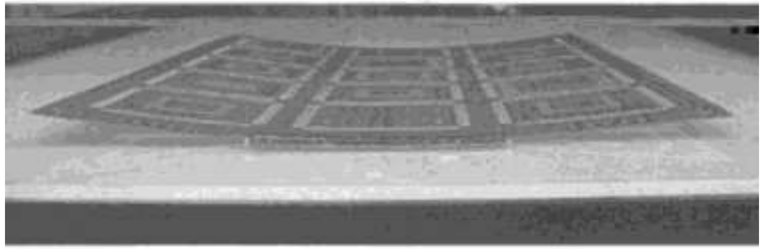
Initiating from Hillock

Tin whiskers

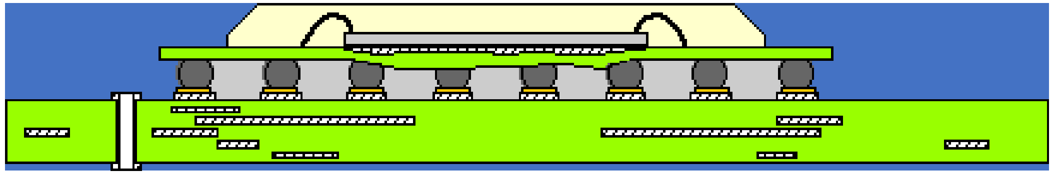


Tin whisker shorts

[Irina Boguslavsky, NEMI Sn whisker project,

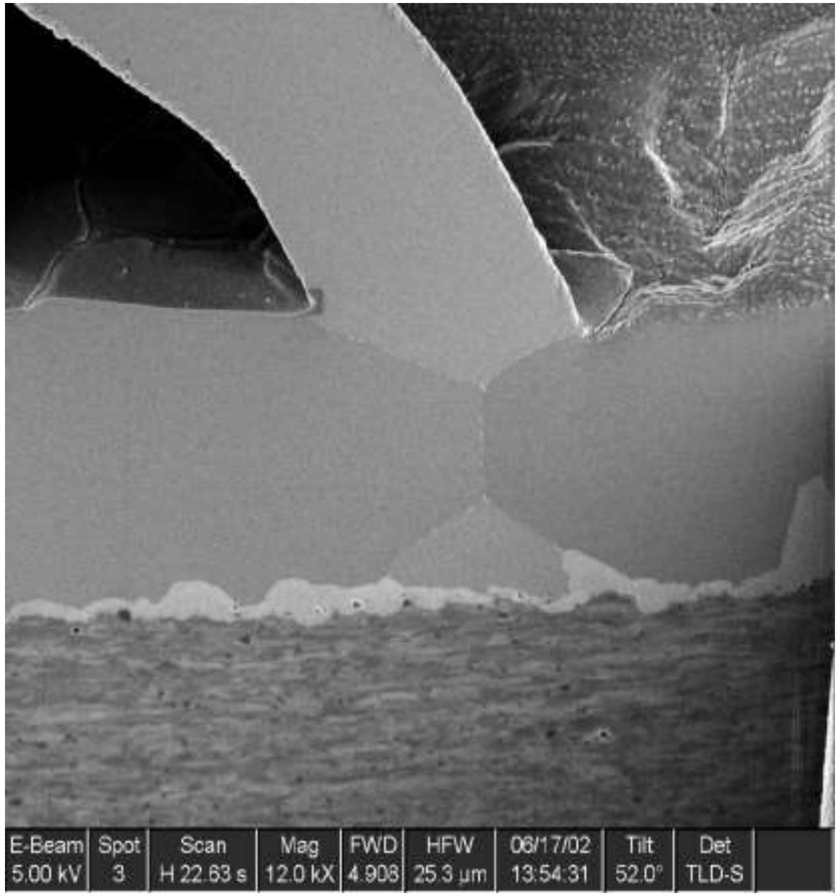


Warpage of PCBs due to higher soldering temp



Popcorning of PCBs due to absorbed moisture

Tin whisker growth & mitigation



N. Vo , Motorola

Whiskers form due to compressive force on Sn during

-Intermetallic formation

-Applied stress

Mitigation

- Diffusion barrier coatings Ni/Ti

-Avoiding compressive stress

Summary of failures and remedies by materials & design

- Insulation failures:
  - Partial discharges leading to treeing.
  - Remedy:Avoid defects in insulation – contamination, sharp features that enhance electric fields

- Wirebond failures
  - Thermal expansion mismatch ➔ thermo-mechanical fatigue ➔heal cracks in interface & ageing of chip metallisation (rough pattern) ➔ V increase
  - Remedy: conformal coatings increase life time

- Solder failures
  - Thermal cycling of Substrate solder➔ delamination of solder interfaces ➔ Rth/Tj increase
    - Remedy: Use low CTE base plates like composite AlSiC
  - Tin whisker growth in platings and solders ➔ fail by short-circuits
    - Remedy: Barrier coatings, avoid compressive stress, non-tin solders