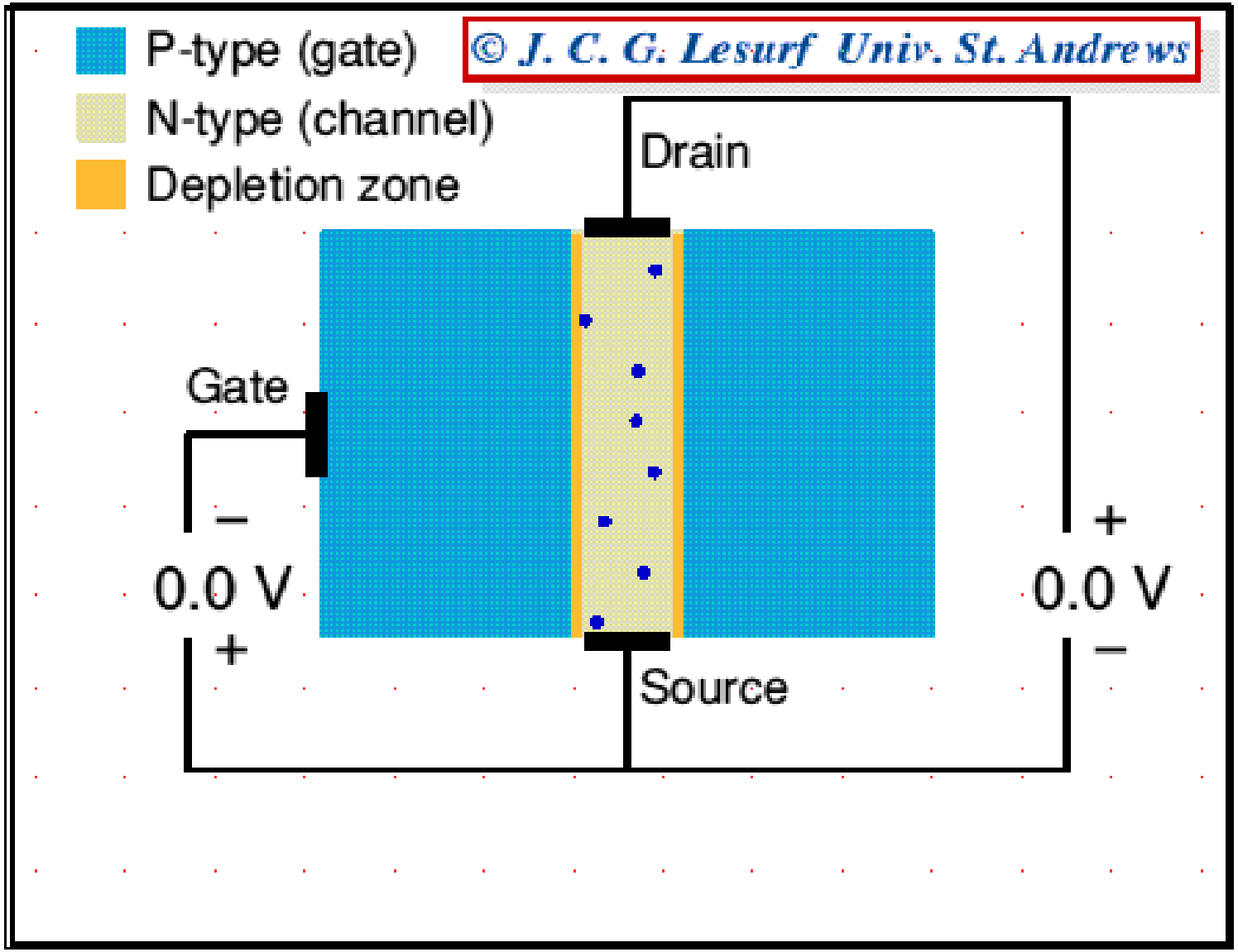
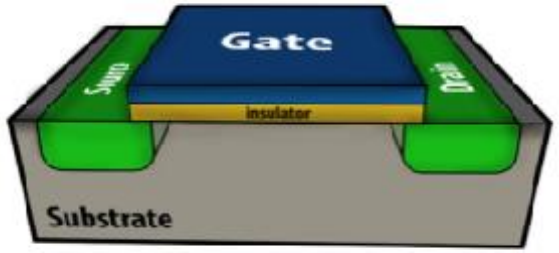
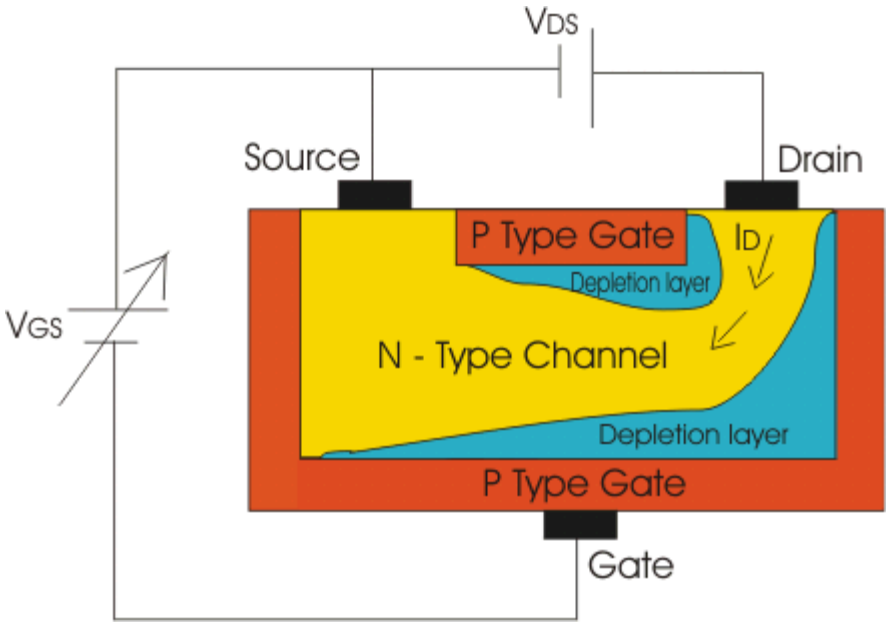
Field Effect Transistor (FET)

- A voltage applied to the metal plate modulated the conductance of the semiconductor under the metal and controlled the current between the ohmic contacts.
- The phenomenon of modulating the conductance of a semiconductor by an electric field applied perpendicular to the surface of a semiconductor is called field effect.
- This type of transistor has also been called the **unipolar transistor**, to emphasize that only one type of carrier, the majority carrier, is involved in the operation.
- **Types:**
  - JFET - Junction Field Effect Transistor
  - MESFET - MEtal-Semiconductor Field-Effect Transistor
  - MOSFET - MEtal-Oxide Semiconductor Field-Effect Transistor


P-type (gate)
N-type (channel)
Depletion zone
© J. C. G. Lesurf Univ. St. Andrews
Drain
Gate
–
0.0 V
+
+
0.0 V
–
Source


Gate
Source
Drain
Insulator
Substrate


VDS
Source
Drain
P Type Gate
ID
Depletion layer
VGS
N - Type Channel
Depletion layer
P Type Gate
Gate

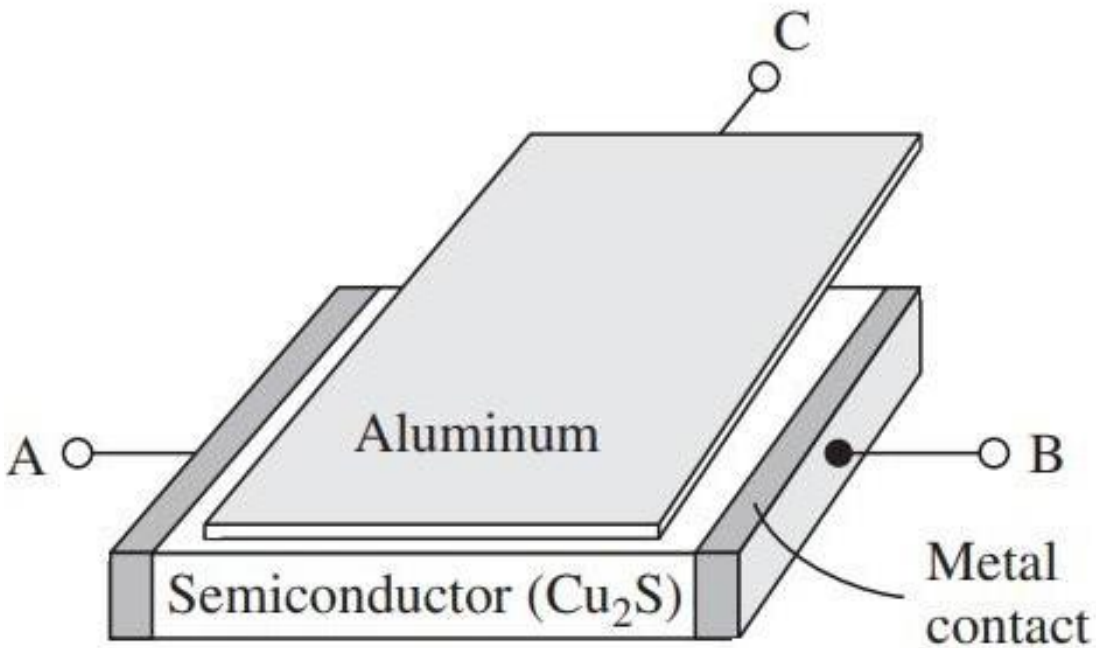


Figure 13.1 | Idealization of the Lilienfeld transistor.
(From Pierret [10].)

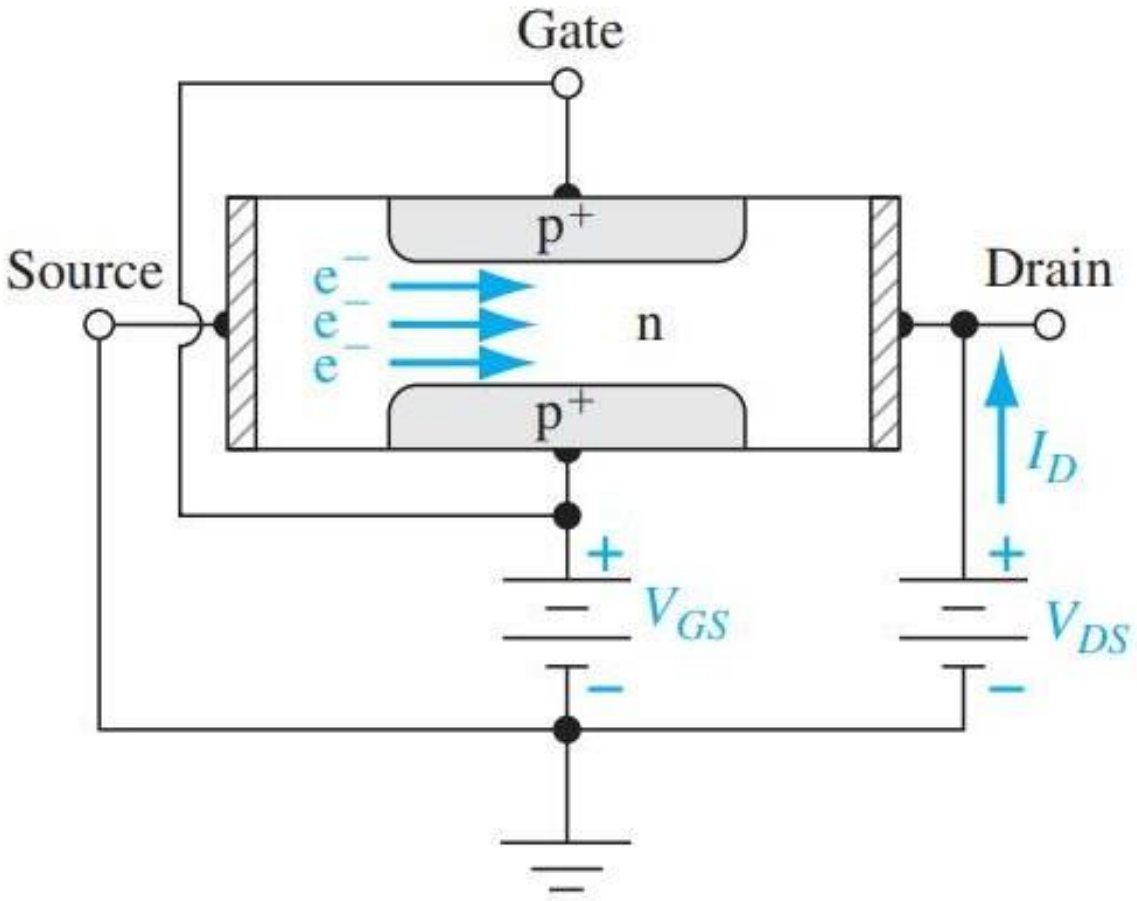
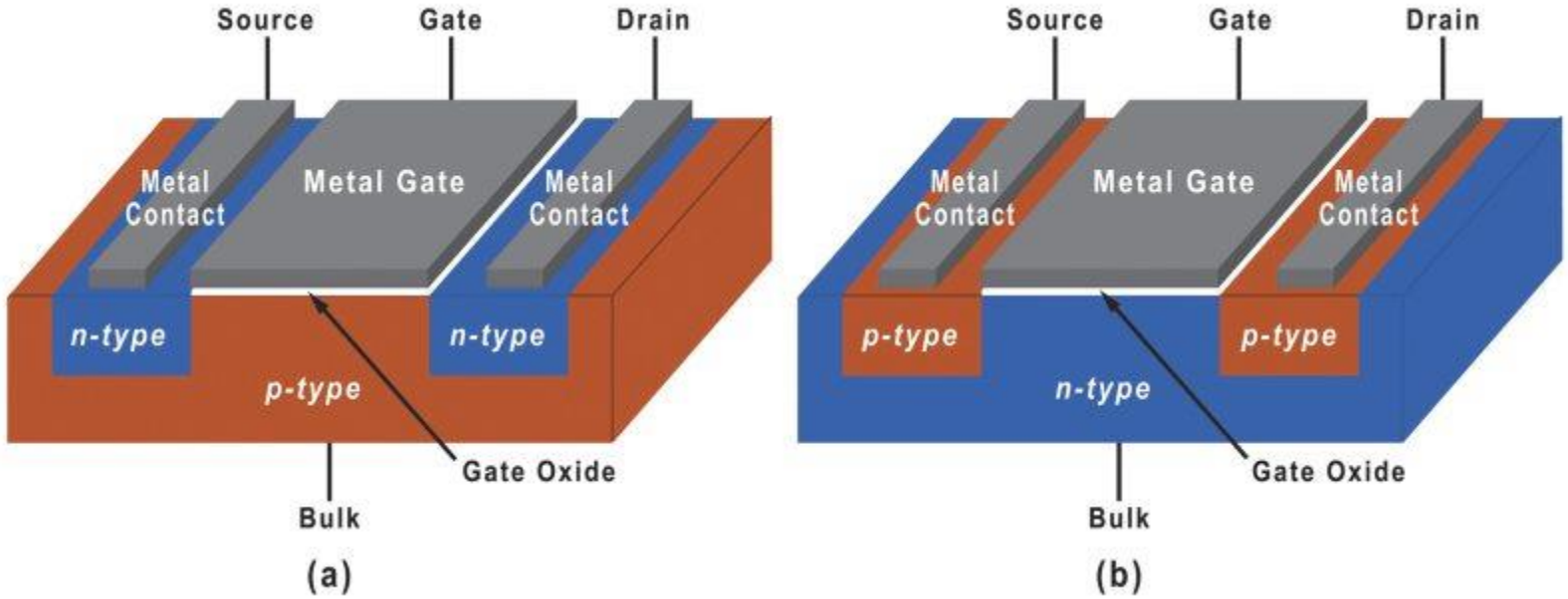
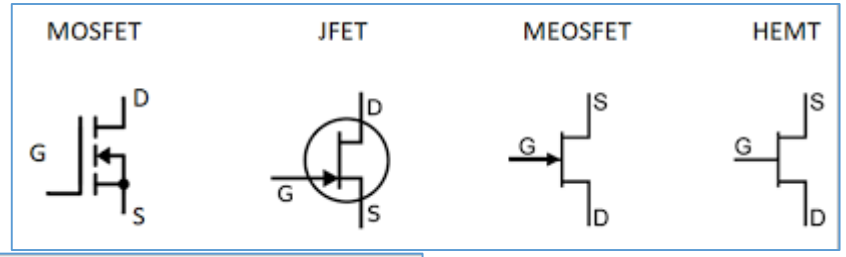
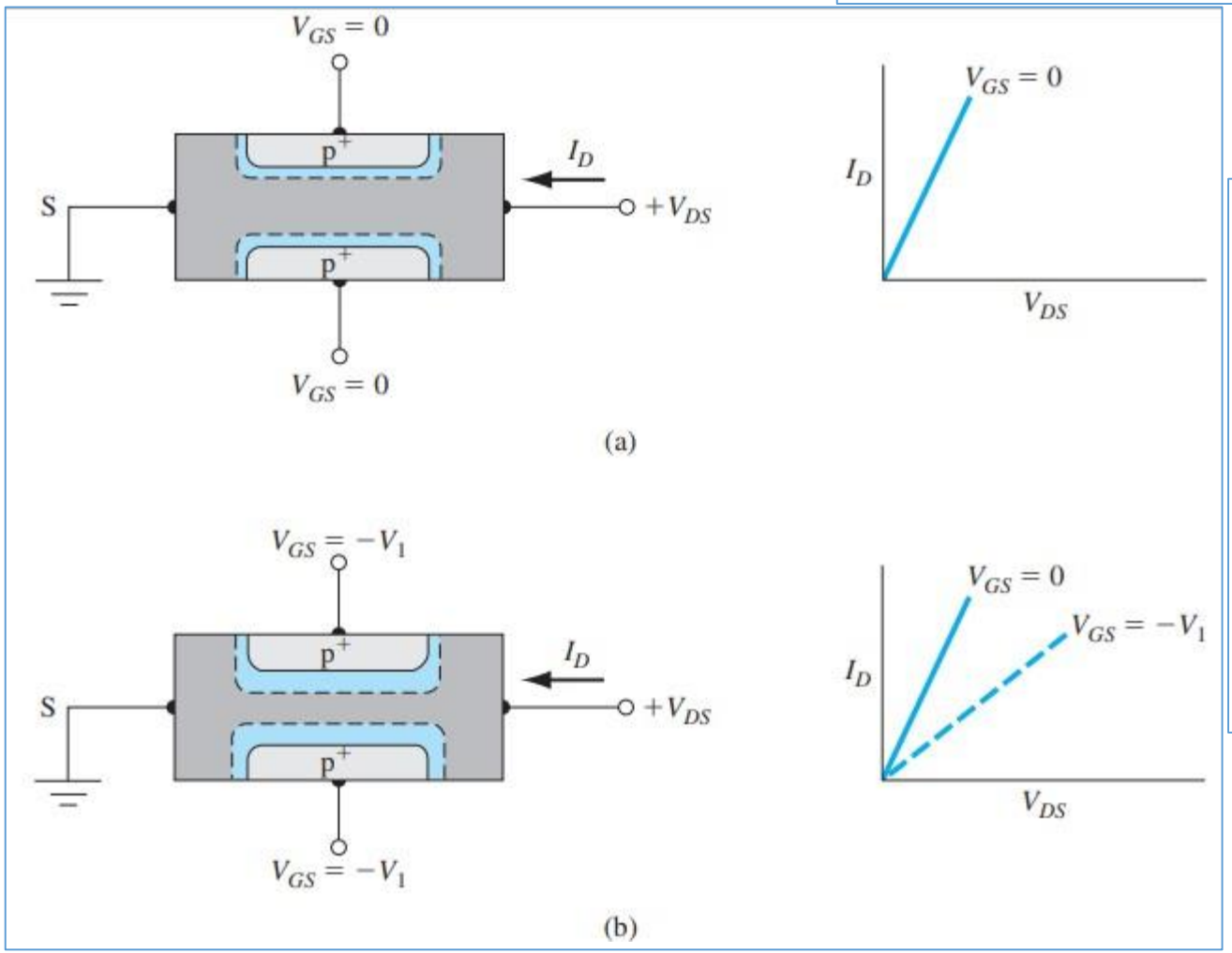


Figure 13.2 | Cross section of a symmetrical n-channel pn junction FET.


Source
Gate
Drain
Metal Contact
Metal Gate
Metal Contact
n-type
n-type
p-type
Gate Oxide
Bulk
(a)
Source
Gate
Drain
Metal Contact
Metal Gate
Metal Contact
p-type
p-type
n-type
Gate Oxide
Bulk
(b)





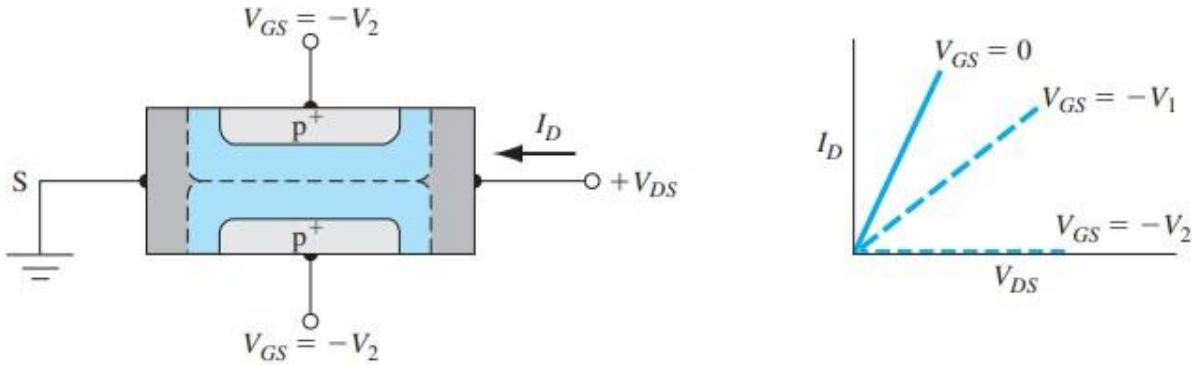
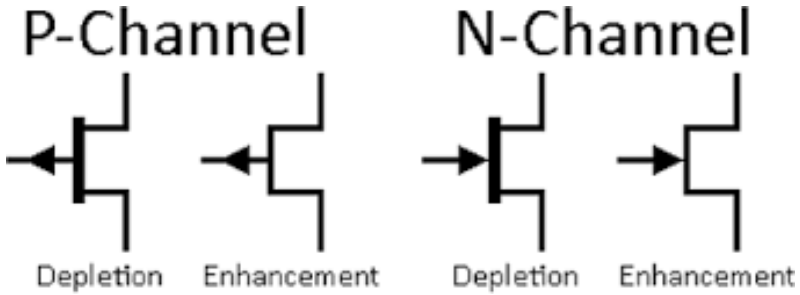


Figure 13.3 | Gate-to-channel space charge regions and *I–V* characteristics for small V_{DS} values and for (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage to achieve pinchoff.

- When we apply a voltage to the gate of a pn JFET with respect to the source and drain, we alter the channel conductance.
- If a negative voltage is applied to the gate of the n-channel pn JFET shown in Figure 13.3, the gate-to-channel pn junction becomes reverse biased.
- The space charge region now widens so the channel region becomes narrower and the resistance of the n channel increases.
- The slope of the ID versus VDS curve, for small VDS, decreases (Figure 13.3b).
- If a larger negative gate voltage is applied, the condition shown in Figure 13.3c can be achieved.
- The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as **pinchoff**. The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals.

Two modes of operation

- Depletion mode
- The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or **depletion mode device**, which means that a voltage must be applied to the gate terminal to turn the device off.
- **Enhancement mode device,** these types of transistors require a gate-source voltage to switch ON the device.



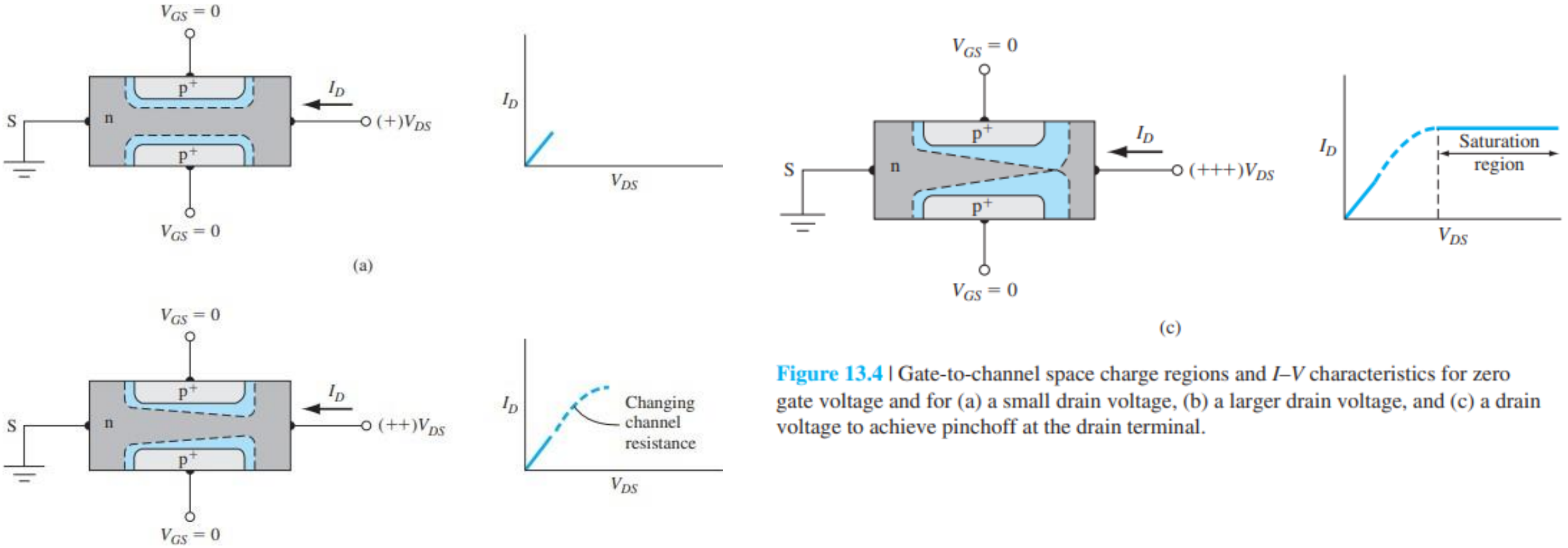


Figure 13.4 | Gate-to-channel space charge regions and *I–V* characteristics for zero gate voltage and for (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage to achieve pinchoff at the drain terminal.

- As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse biased near the drain terminal so that the **space charge region extends further into the channel**. The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases as shown in Figure 13.4b.
- The effective channel resistance now varies along the channel length and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

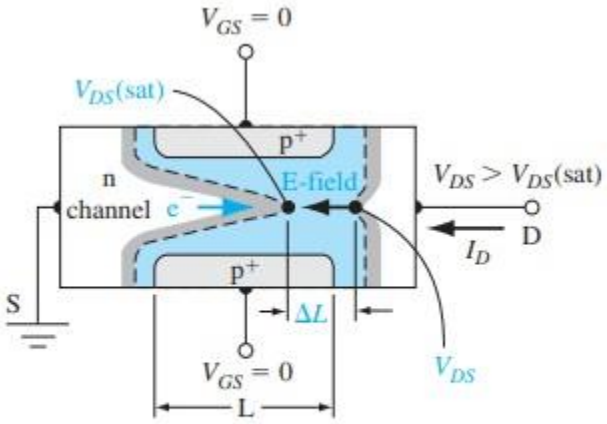


Figure 13.5 | Expanded view of the space charge region in the channel for $V_{DS} > V_{DS}(sat)$.

- The n channel and drain terminal are now separated by a space charge region which has a length L.
- The electrons move through the n channel from the source and are injected into the space charge region where, subjected to the E-field force, they are swept through into the drain contact area.

  If we assume that ΔL< L, then the electric field in the n-channel region remains unchanged from the V_{DS}(sat) case; the drain current will remain constant as V_{DS} changes.
- Once the carriers are in the drain region, the drain current will be independent of VDS; thus, the device looks like a **constant current source.**

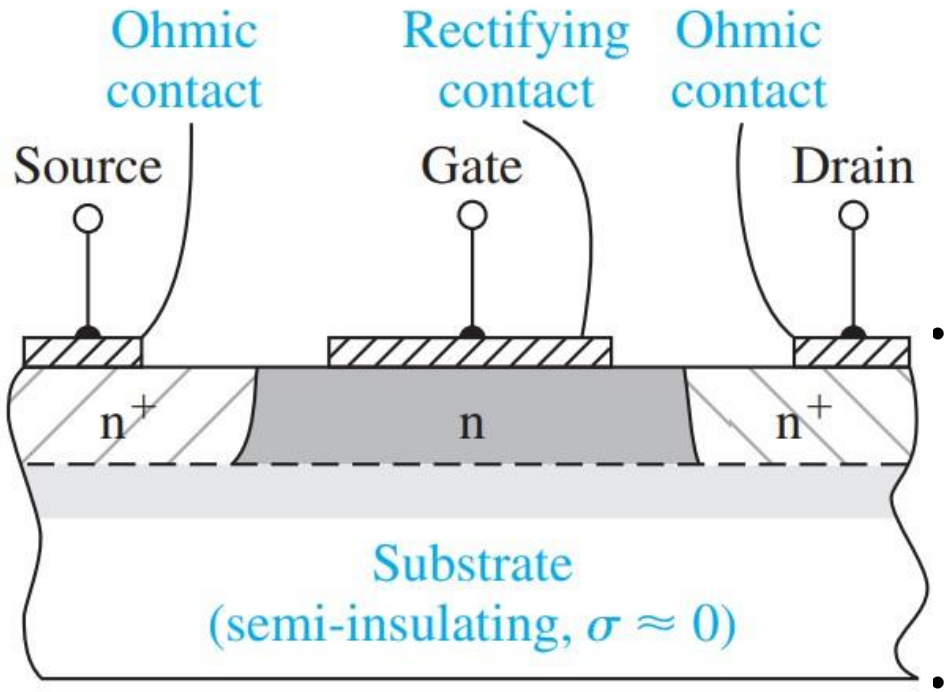
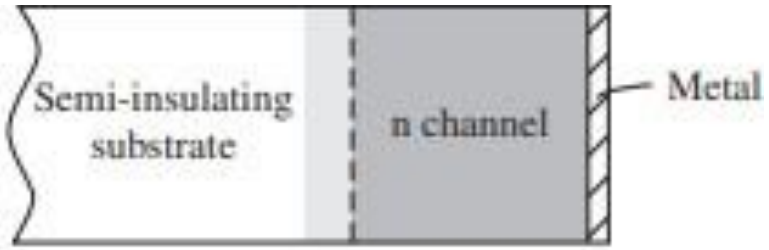


Figure 13.6 | Cross section of an n-channel MESFET with a semi-insulating substrate.

- A reverse-biased gate-to-source voltage induces a space charge region under the metal gate that modulates the channel conductance as in the case of the pn JFET.
- The space charge region will eventually reach the substrate if the applied negative gate voltage is sufficiently large. This condition, again, is known as pinchoff.
- The device shown in this figure is also a depletion mode device, since a gate voltage must be applied to pinch off the channel.

MESFET



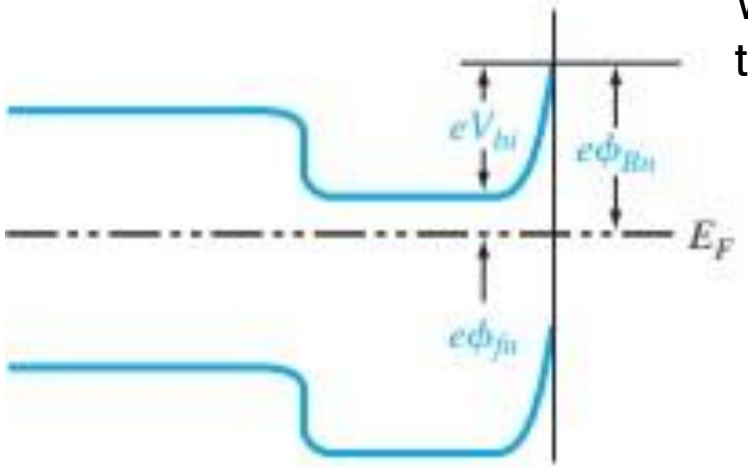
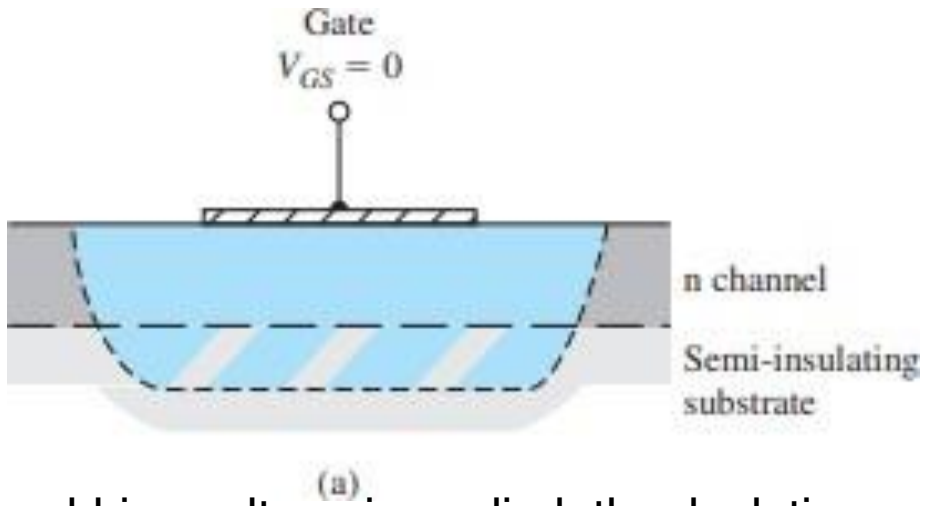


Figure 13.7 | Idealized energy-band diagram of the substrate–channel–metal in the n-channel MESFET.



When a slightly forward-bias voltage is applied, the depletion region just extends through the channel—a condition known as threshold

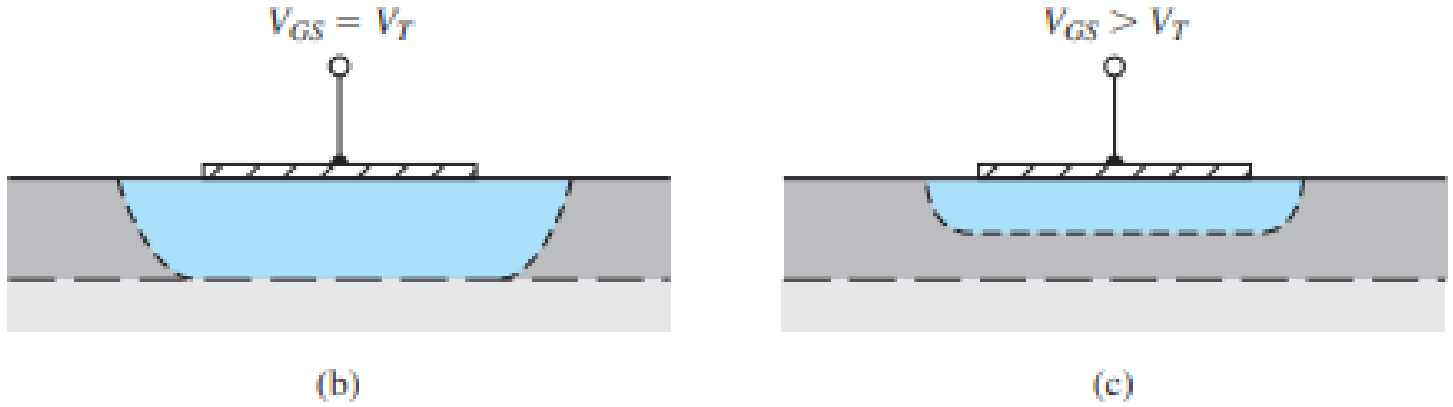


Figure 13.8 | Channel space charge region of an enhancement mode MESFET for (a) $V_{GS} = 0$, (b) $V_{GS} = V_T$, and (c) $V_{GS} > V_T$.

- When a slightly forward-bias voltage is applied, the depletion region just extends through the channel—a condition known as threshold,
- The threshold voltage is the gate-to-source voltage that must be applied to create the pinchoff condition.
- The threshold voltage for this n-channel MESFET is positive, in contrast to the negative voltage for the n-channel depletion mode device.
- If a larger forward bias is applied, the channel region opens as shown in Figure 13.8c.
- The applied forward-bias gate voltage is limited to a few tenths of a volt before there is signifi cant gate current. This device is known as an **n-channel enhancement mode MESFET.**

h. Assume the drain-to-source voltage is zero. If we assume the abrupt depletion approximation, then the space charge width is given by

$$h = \left[\frac{2\epsilon_s(V_{bi} - V_{GS})}{eN_d}\right]^{1/2} \tag{13.1}$$

where V_{GS} is the gate-to-source voltage and V_{bi} is the built-in potential barrier. For a reverse-biased p^+n junction, V_{GS} must be a negative voltage.

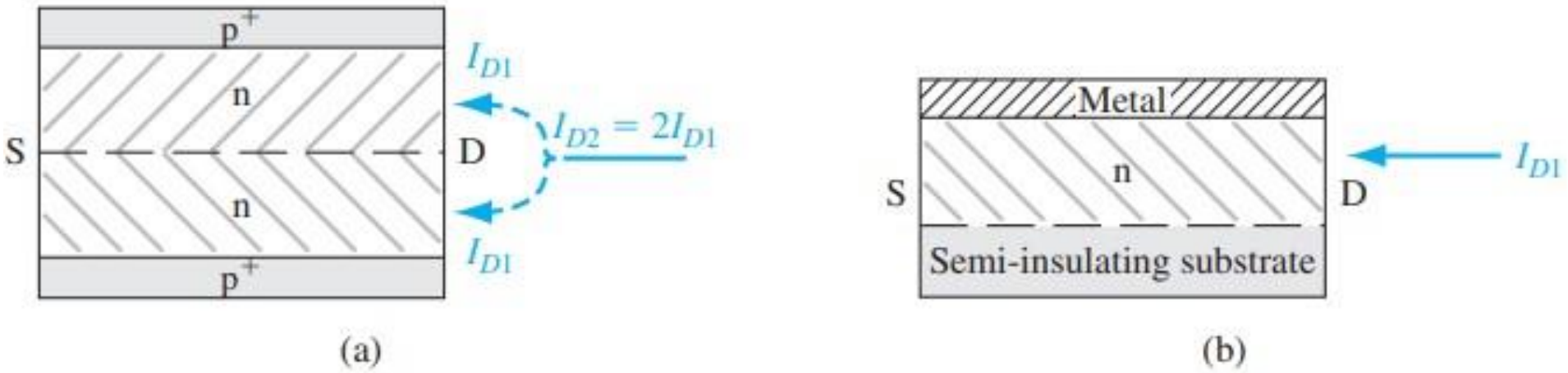


Figure 13.9 | Drain currents of (a) a symmetrical, two-sided pn JFET, and (b) a one-sided MESFET.

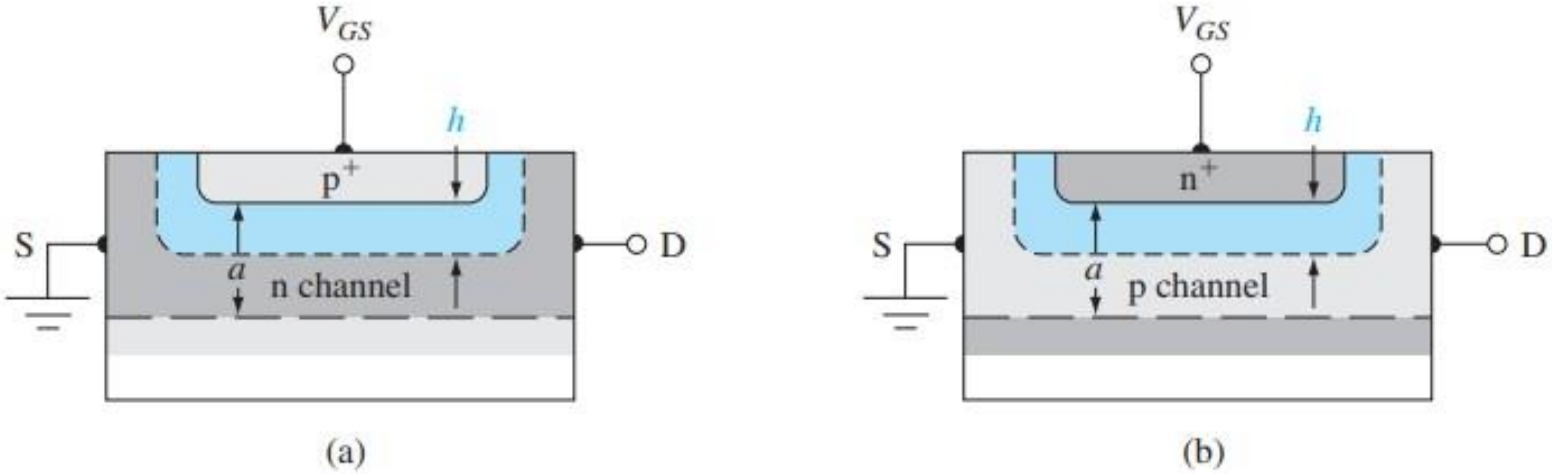


Figure 13.10 | Geometries of simplified (a) n-channel and (b) p-channel pn JFETs.

At pinchoff, $h = a$ and the total potential across the p^+n junction is called the *internal pinchoff voltage*, denoted by V_{p0}. We now have

$$a = \left[\frac{2\epsilon_s V_{p0}}{eN_d}\right]^{1/2} \tag{13.2}$$

or

$$V_{p0} = \frac{ea^2 N_d}{2\epsilon_s} \tag{13.3}$$

Note that the internal pinchoff voltage is defined as a positive quantity.

The internal pinchoff voltage V_{p0} is not the gate-to-source voltage to achieve pinchoff. The gate-to-source voltage that must be applied to achieve pinchoff is described as the *pinchoff voltage* and is also variously called the *turn-off voltage* or *threshold voltage*. The pinchoff voltage is denoted by V_p and is defined from Equations (13.1) and (13.2) as

$$V_{bi} - V_p = V_{p0} \qquad \text{or} \qquad \boxed{V_p = V_{bi} - V_{p0}} \tag{13.4}$$

The gate-to-source voltage to achieve pinchoff in an n-channel depletion mode JFET is negative; thus, $V_{p0} > V_{bi}$.

Objective: Calculate the internal pinchoff voltage and pinchoff voltage of an n-channel JFET.

Assume that the p^+n junction of a uniformly doped silicon n-channel JFET at $T = 300$ K has doping concentrations of $N_a = 10^{18}$ cm^{-3} and $N_d = 10^{16}$ cm^{-3}. Assume that the metallurgical channel thickness, a, is $0.75\ \mu\text{m} = 0.75 \times 10^{-4}$ cm.

■ Solution

The internal pinchoff voltage is given by Equation (13.3), so we have

$$V_{p0} = \frac{ea^2 N_d}{2\epsilon_s} = \frac{(1.6 \times 10^{-19})(0.75 \times 10^{-4})^2(10^{16})}{2(11.7)(8.85 \times 10^{-14})} = 4.35 \text{ V}$$

The built-in potential barrier is

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259)\ln\left[\frac{(10^{18})(10^{16})}{(1.5 \times 10^{10})^2}\right] = 0.814 \text{ V}$$

The pinchoff voltage, from Equation (13.4), is then found as

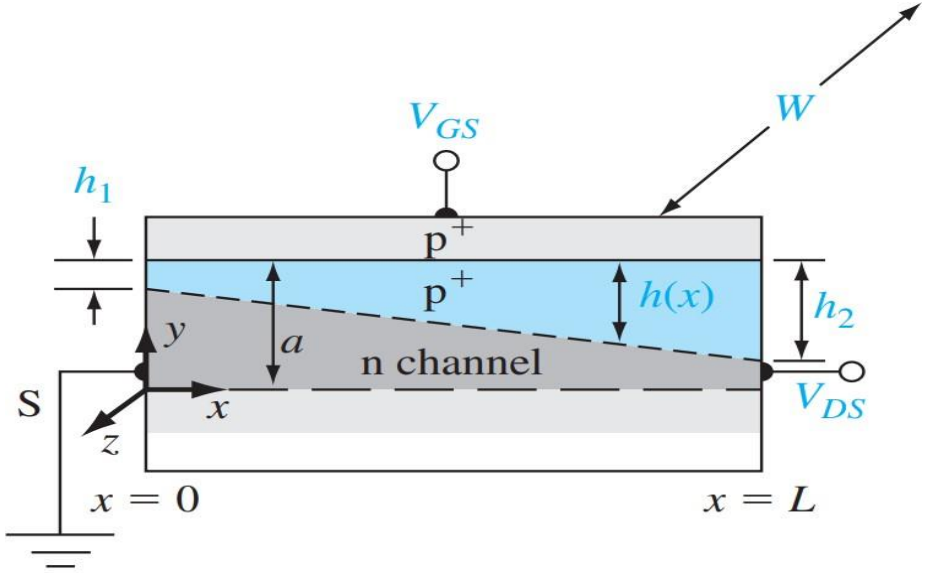
$$V_p = V_{bi} - V_{p0} = 0.814 - 4.35 = -3.54 \text{ V}$$

Comment

The pinchoff voltage, or gate-to-source voltage to achieve pinchoff, for the n-channel depletion mode device is a negative quantity as we have said.

A silicon n-channel JFET at $T = 300$ K has a gate doping concentration of $N_a = 10^{18}$ cm^{-3} and a channel doping concentration of $N_d = 2 \times 10^{16}$ cm^{-3}. Determine the metallurgical channel thickness, a, such that the pinchoff voltage is $V_p = -2.50$ V.

Ans. $a = 0.464\ \mu$m



- What is the value of V_{GS}?
- When will pinch off occur?
- What is the mode of operation of this n-channel pn JFET?

Figure 13.11 | Simplified geometry of an n-channel pn JFET.

n-channel device. The depletion width h_1 at the source end is a function of V_{bi} and V_{GS} but is not a function of drain voltage. The depletion width at the drain terminal is given by

$$h_2 = \left[\frac{2\epsilon_s(V_{bi} + V_{DS} - V_{GS})}{eN_d}\right]^{1/2} \tag{13.9}$$

Again, we must keep in mind that V_{GS} is a negative quantity for the n-channel device.

Pinchoff at the drain terminal occurs when $h_2 = a$. At this point we reach what is known as the saturation condition; thus, we can write that $V_{DS} = V_{DS}(\text{sat})$. Then

$$a = \left[\frac{2\epsilon_s(V_{bi} + V_{DS}(\text{sat}) - V_{GS})}{eN_d}\right]^{1/2} \tag{13.10}$$

This can be rewritten as

$$V_{bi} + V_{DS}(\text{sat}) - V_{GS} = \frac{ea^2N_d}{2\epsilon_s} = V_{p0} \tag{13.11}$$

or

$$V_{DS}(\text{sat}) = V_{p0} - (V_{bi} - V_{GS}) \tag{13.12}$$

- The **drain-to-source saturation voltage decreases** with increasing reverse biased gate-to-source voltage.

Ideal DC Current-Voltage Relationship—Depletion Mode JFET

to the *I–V* characteristics when the JFET is biased in the saturation region. This equation is used extensively in JFET applications and is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{13.14}$$

where I_{DSS} is the saturation current when $V_{GS} = 0$. At the end of this section, we compare the approximation given by Equation (13.14) and the ideal current–voltage equation that we have derived.

Diode	BJT	FET
$I = I_0\left(e^{\frac{qV}{kT}} - 1\right)$	$i_C = I_S \exp\left(\frac{v_{BE}}{V_t}\right)$	$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

The transconductance is the transistor gain of the JFET; it indicates the amount of control the gate voltage has on the drain current. The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{13.37}$$

Using the current–voltage approximation given by Equation (13.14), we can also write the transconductance as

$$g_{ms} = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{13.41b}$$

Since V_p is negative for the n-channel JFET, g_{ms} is positive.

N-channel Enhancement mode JFET

- The design of enhancement mode JFETs implies the use of **narrow channel thicknesses and low channel doping concentrations** to achieve this condition.

For the n-channel MESFET, the threshold voltage is defined from Equation (13.4) as

$$V_{bi} - V_T = V_{p0} \quad \text{or} \quad \boxed{V_T = V_{bi} - V_{p0}} \tag{13.42}$$

For an n-channel depletion mode JFET, $V_T < 0$, and for the enhancement mode device, $V_T > 0$. We can see from Equation (13.42) that $V_{bi} > V_{p0}$ for an enhancement mode n-channel JFET.

$$I_{D1}(\text{sat}) = k_n(V_{GS} - V_T)^2 \tag{13.47}$$

where

$$k_n = \frac{\mu_n \epsilon_s W}{2aL} \tag{13.48}$$

The factor k_n is called a *conduction parameter*. The form of Equation (13.47) is the same as for a MOSFET.

The transconductance of the enhancement mode device operating in the saturation region can also be derived. Using Equation (13.47), we can write

$$g_{ms} = \frac{\partial I_{D1}(\text{sat})}{\partial V_{GS}} = 2k_n(V_{GS} - V_T) \tag{13.49}$$

The transconductance increases as V_{GS} increases for the enhancement mode device as it did for the depletion mode device.

Non ideal effects

- Channel-length modulation
- Velocity saturation
- Subthreshold current

Heterojunctions

- The FETs fabricated from these heterojunctions are termed high electron mobility transistor (HEMT).
- Other names include modulation-doped field-effect transistor (MODFET), selectively doped hetero junction field-effect transistor (SDHT), and two-dimensional electron gas field effect transistor (TEGFET).

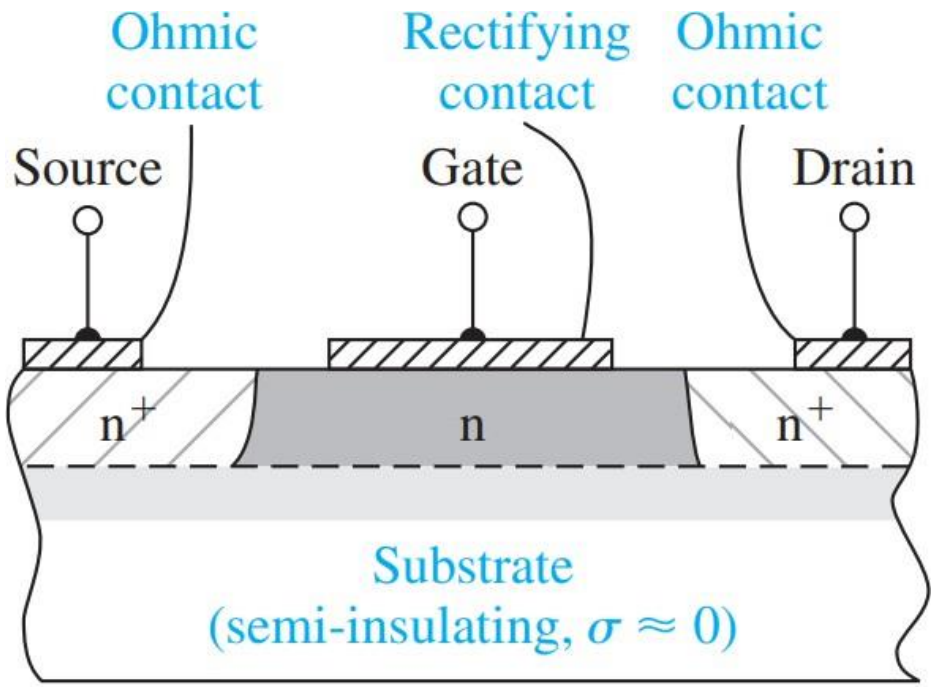


Figure 13.6 | Cross section of an n-channel MESFET with a semi-insulating substrate.

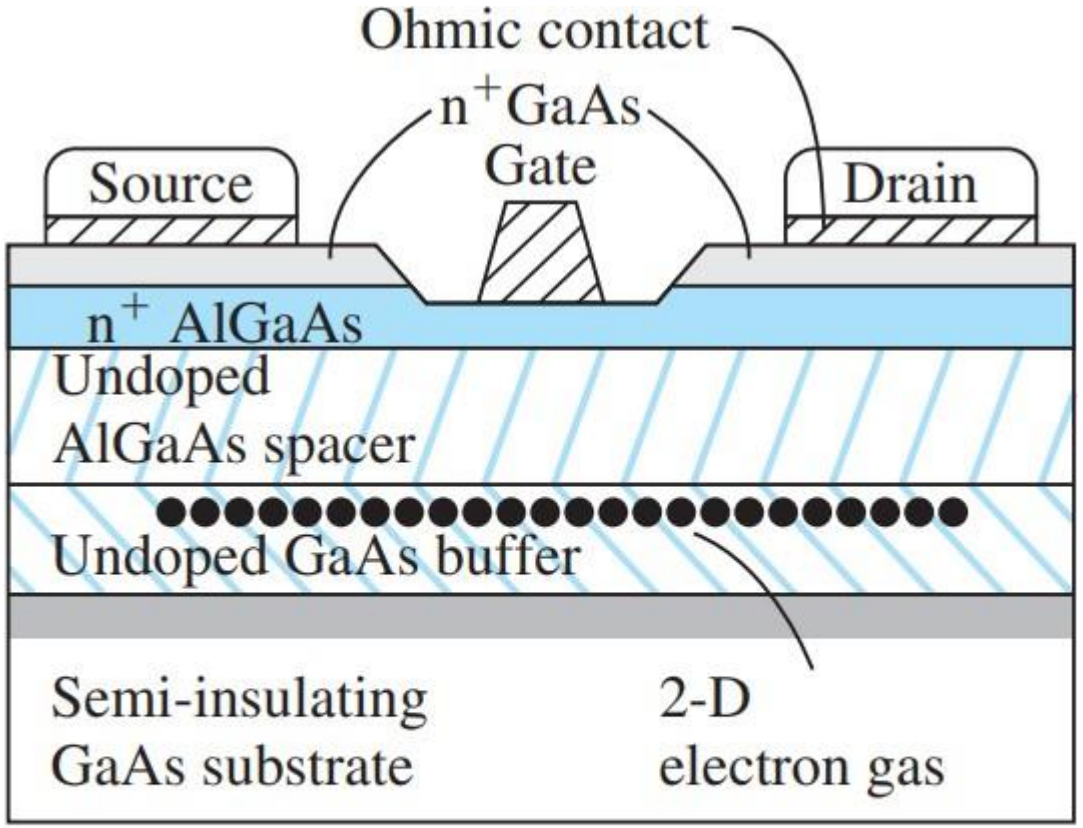


Figure 13.26 | A "normal" AlGaAs–GaAs HEMT.

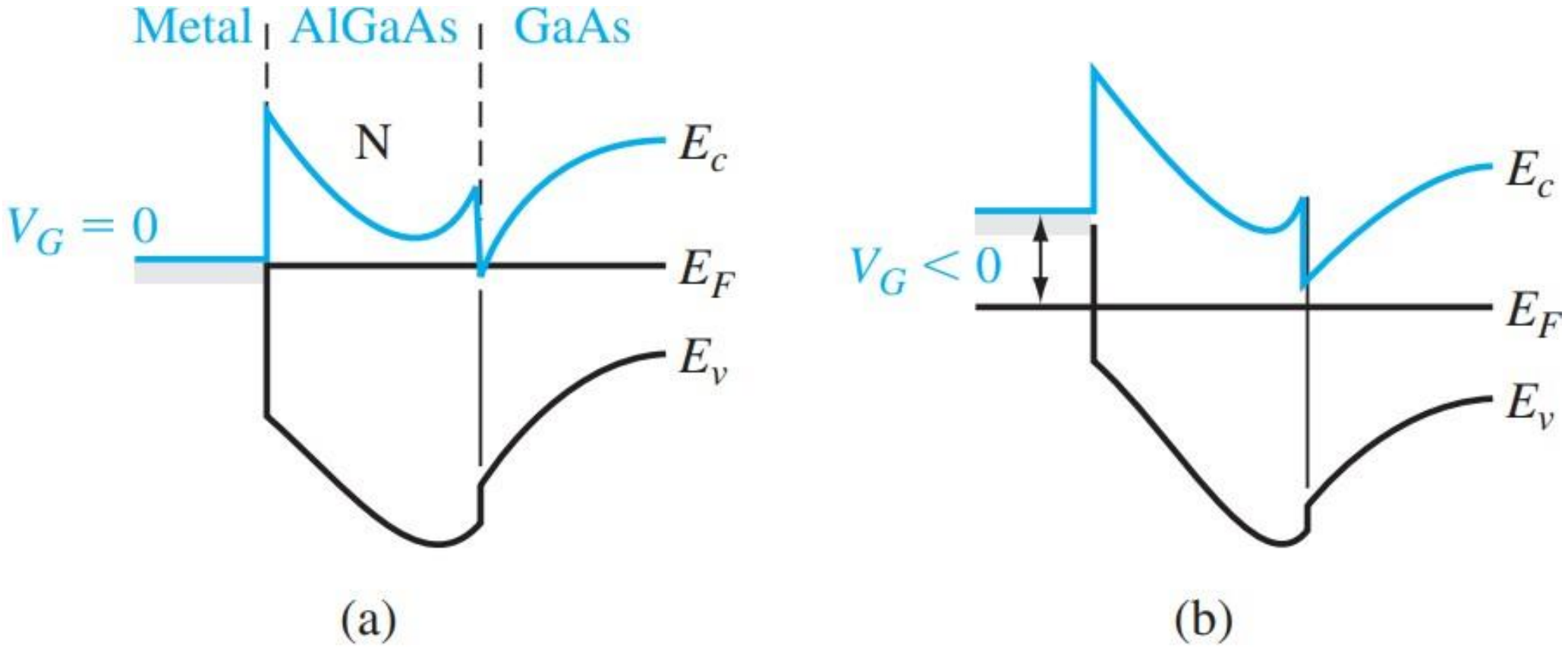
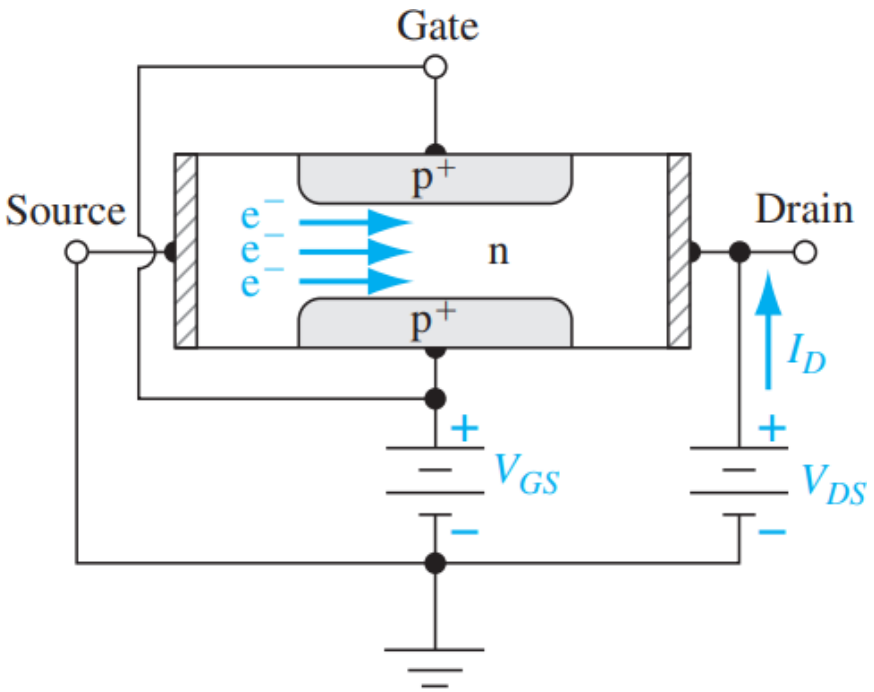
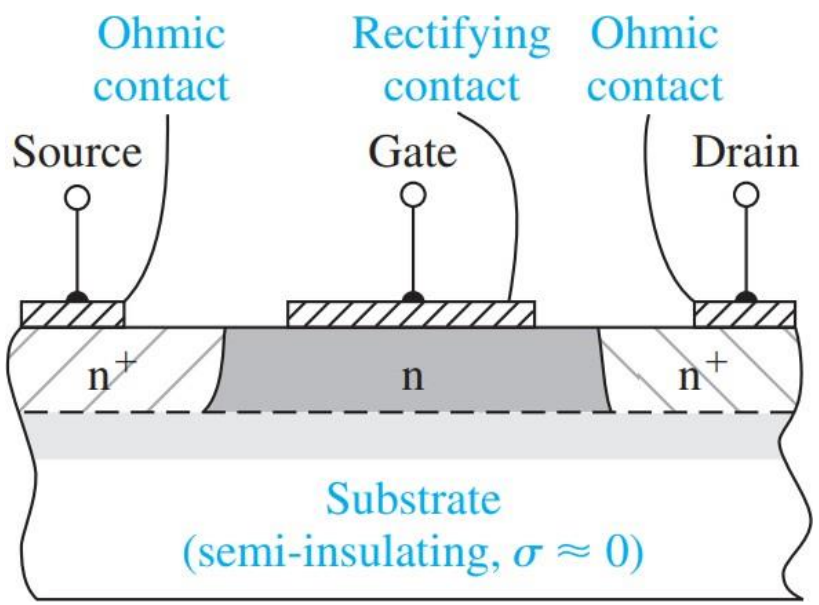


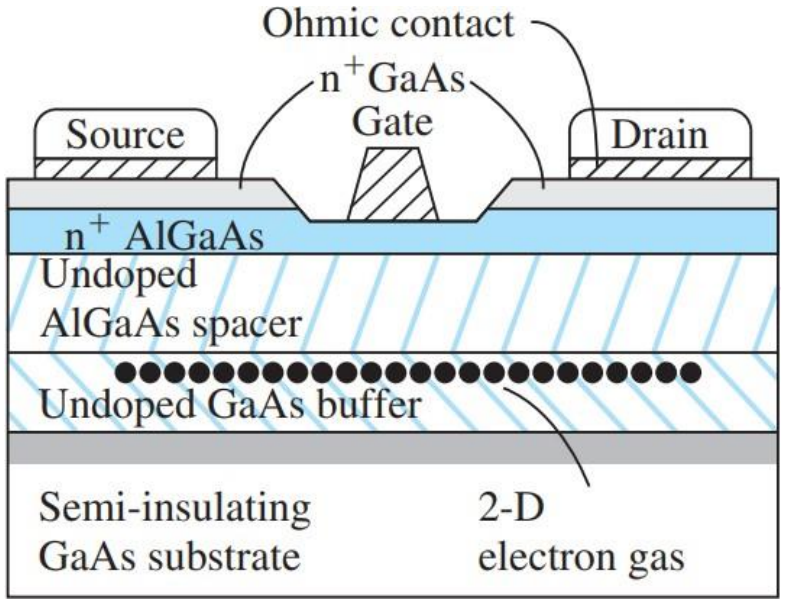
Figure 13.28 | Energy-band diagram of a normal HEMT (a) with zero gate bias and (b) with a negative gate bias.



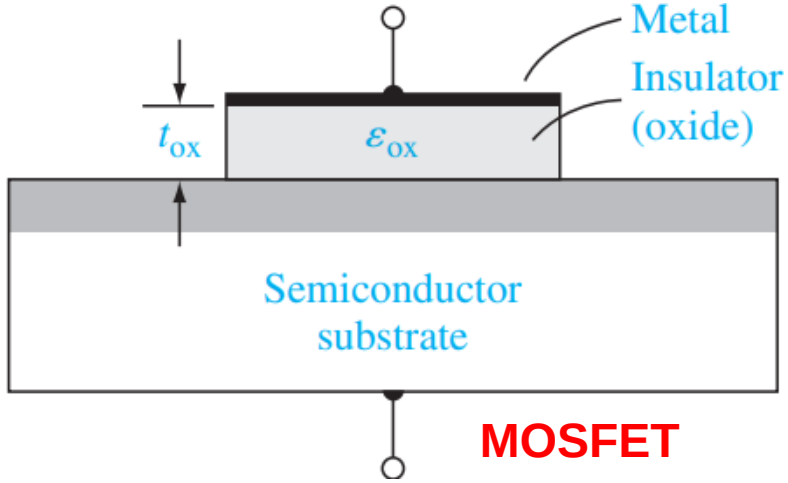
JFET



MESFET

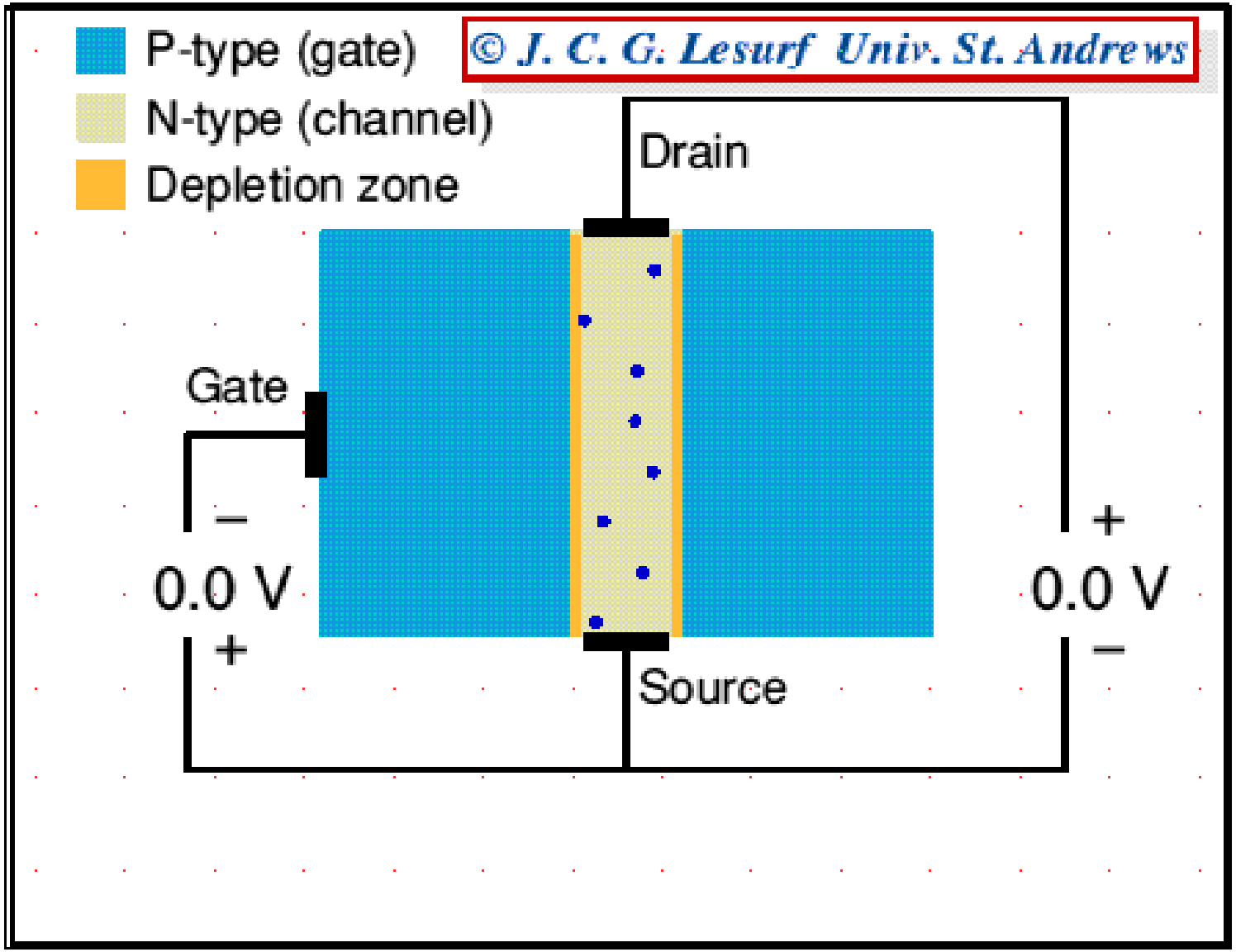


HEMT

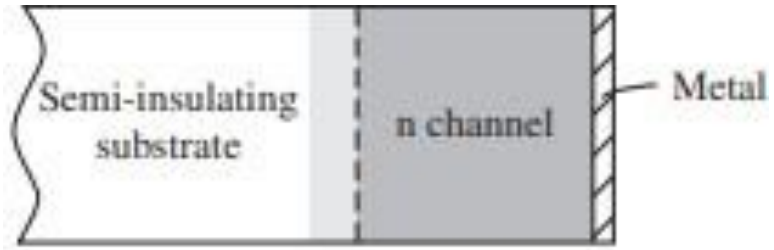


MOSFET

Working of JFET



MESFET



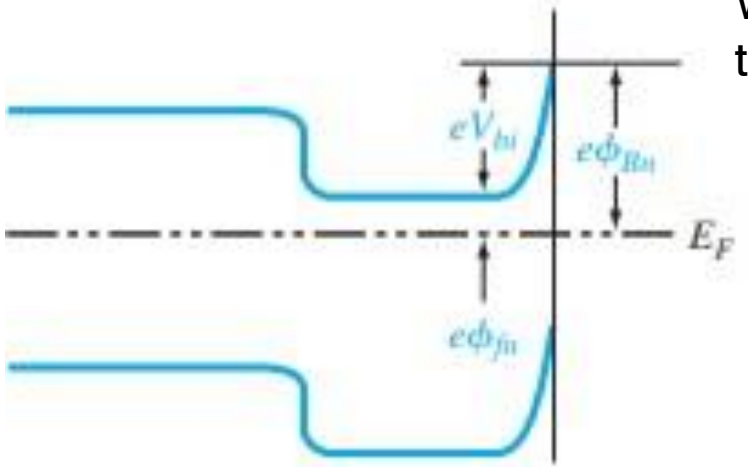
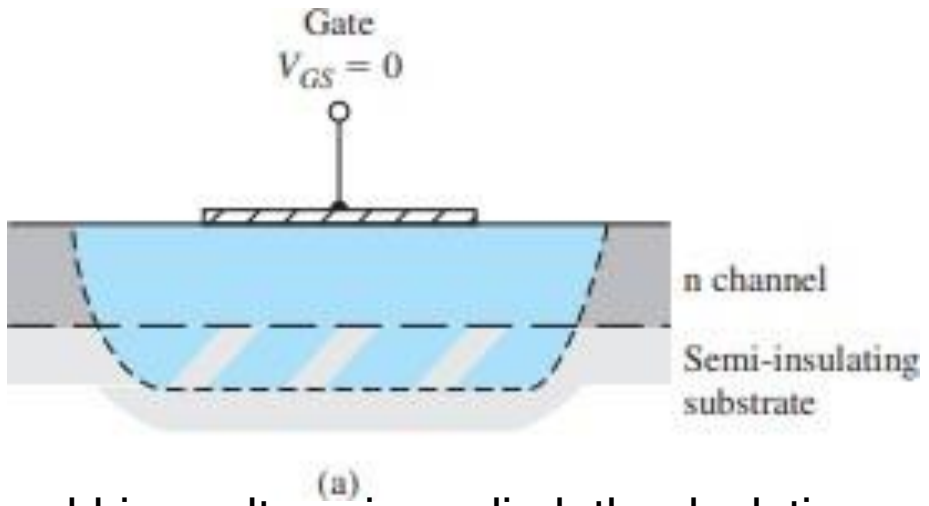


Figure 13.7 | Idealized energy-band diagram of the substrate–channel–metal in the n-channel MESFET.



When a slightly forward-bias voltage is applied, the depletion region just extends through the channel—a condition known as threshold

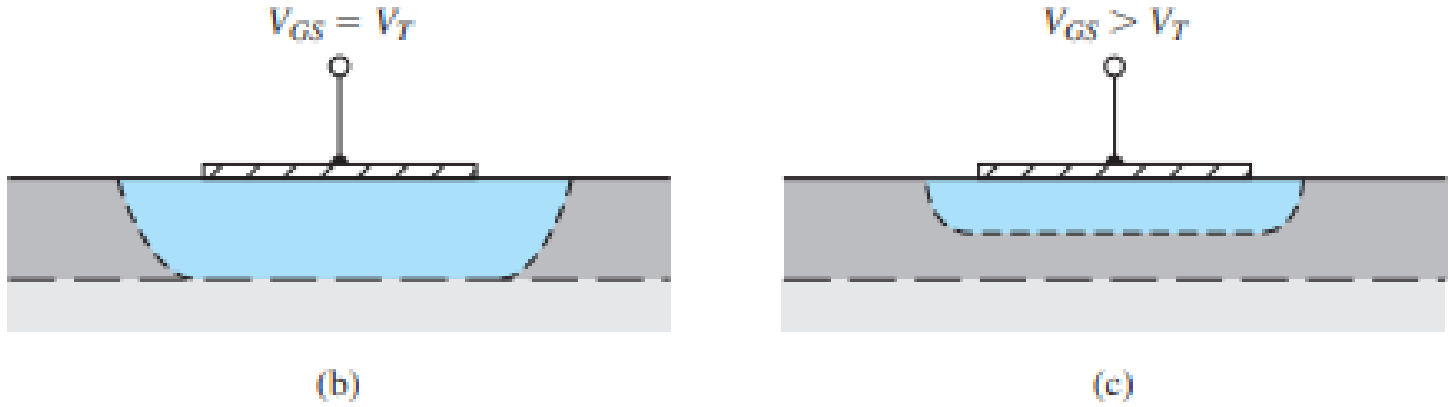


Figure 13.8 | Channel space charge region of an enhancement mode MESFET for (a) $V_{GS} = 0$, (b) $V_{GS} = V_T$, and (c) $V_{GS} > V_T$.

Working of HEMT

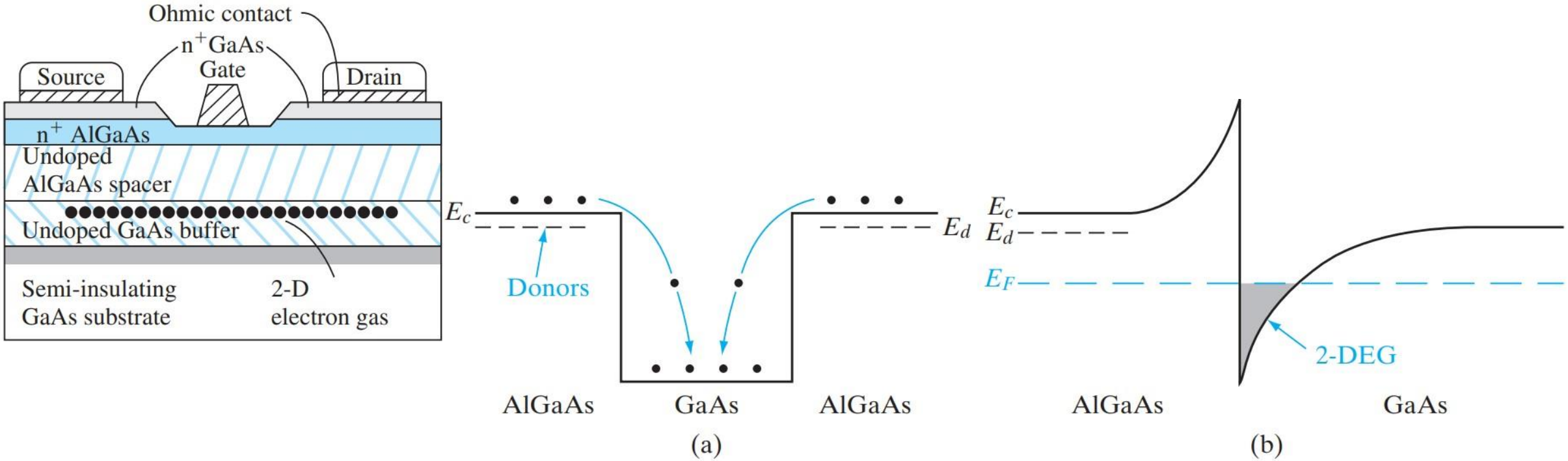


Figure 6–8
(a) Simplified view of modulation doping, showing only the conduction band. Electrons in the donor-doped AlGaAs fall into the GaAs potential well and become trapped. As a result, the undoped GaAs becomes n type, without the scattering by ionized donors which is typical of bulk n-type material.
(b) Use of a single AlGaAs/GaAs heterojunction to trap electrons in the undoped GaAs. The thin sheet of charge due to free electrons at the interface forms a two-dimensional electron gas (2-DEG), which can be exploited in HEMT devices.

MOSFET

- Metal oxide semiconductor structure is called MOS capacitor.
- Energy band in the semiconductor near the oxide-semiconductor interface bend as a voltage is applied across MOS capacitor.
- Position of CB and VB w.r.t fermi level at the oxide-semiconductor interface is a function of MOS capacitor voltage so that the **characteristics of semiconductor surface can be inverted from p-type to n-type or from n-type to p-type**.
- Operation of MOSFET depends
  - Inversion and inversion charge density created at interface
  - Threshold voltage – applied gate voltage to create the inversion layer charge
  - **The current in a MOSFET is due to the flow of charge in the inversion layer or channel region adjacent to the oxide–semiconductor interface.**

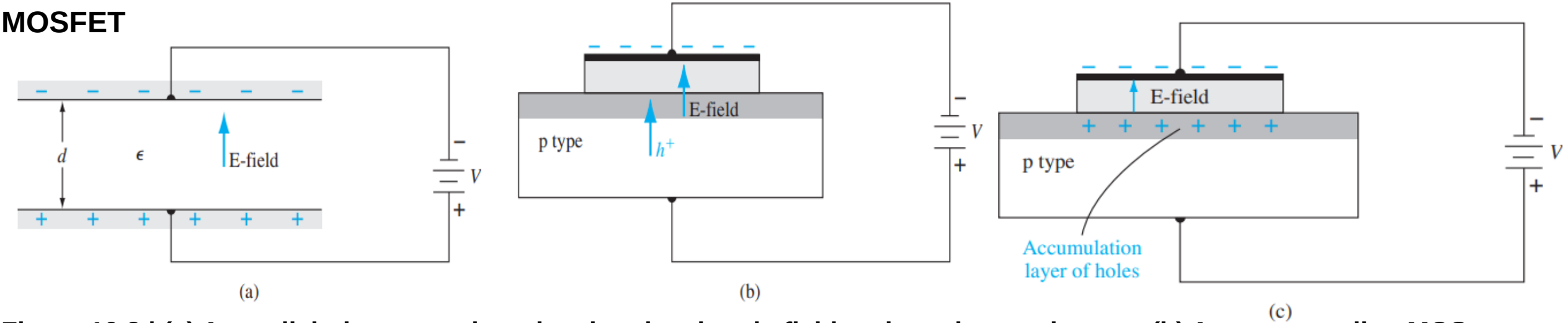


Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow. (c) The MOS capacitor with an accumulation layer of holes.

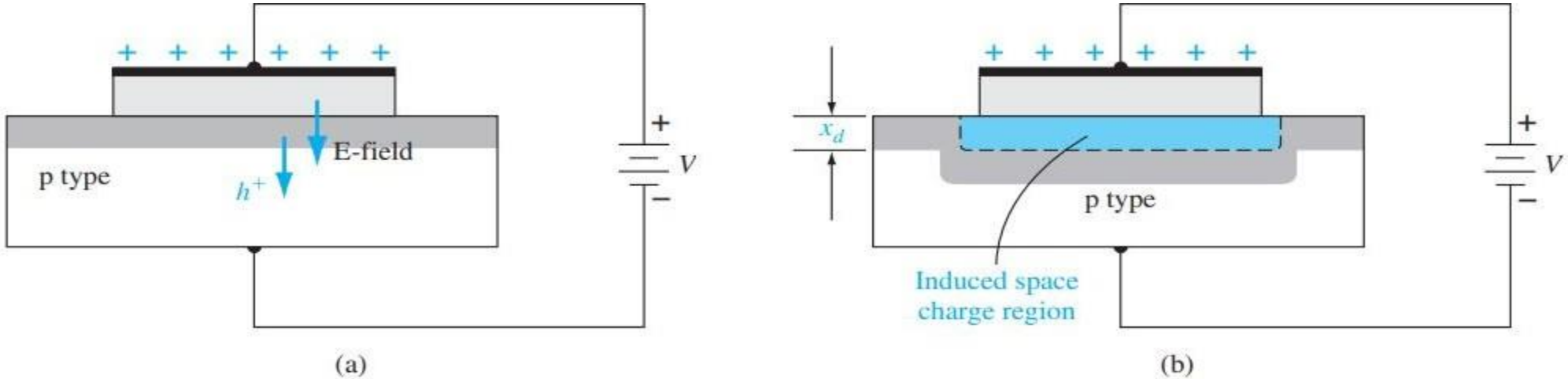


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

- The top metal gate is at a negative voltage with respect to the semiconductor substrate.
- From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure.
- If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide- semiconductor interface.
- An accumulation layer of holes at the oxide-semiconductor junction corresponds to the positive charge on the bottom “plate” of the MOS capacitor.

- The same MOS capacitor in which the polarity of the applied voltage is reversed.
- A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction as shown.
- If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a force away from the oxide-semiconductor interface.
- As the holes are pushed away from (the interface, a negative space charge region is created because of the fixed ionized acceptor atoms.
- The negative charge in the induced depletion region corresponds to the negative charge on the bottom “plate” of the MOS capacitor
- The energy bands in the semiconductor are flat indicating no net charge exists in the semiconductor. This condition is known as flat band.

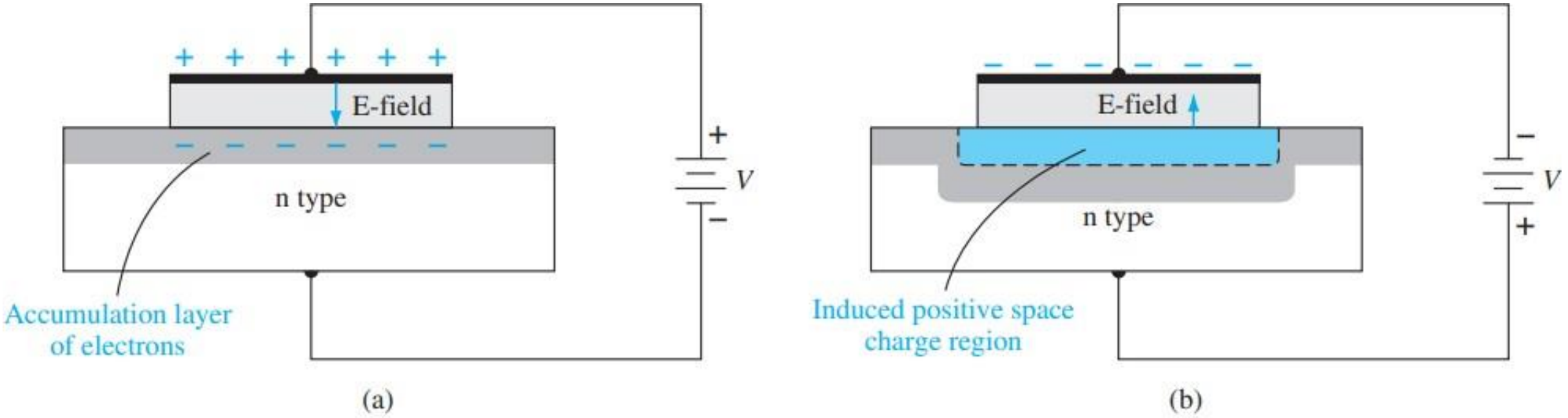
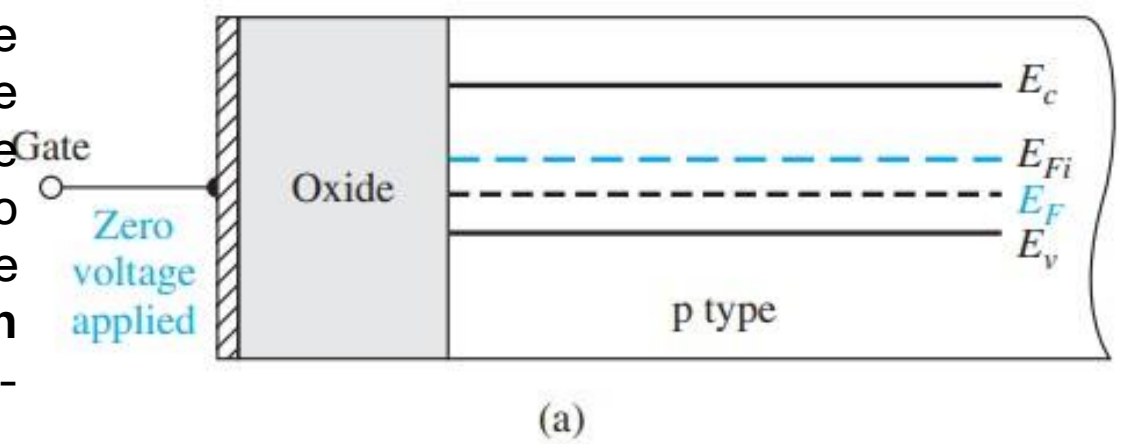


Figure 10.6 | The MOS capacitor with an n-type substrate for (a) a positive gate bias and (b) a moderate negative gate bias.

By applying a sufficiently large **positive gate voltage**, we have inverted the surface of the semiconductor from a p-type to an n-type semiconductor. We have created an **inversion layer** of electrons at the oxide-semiconductor interface.



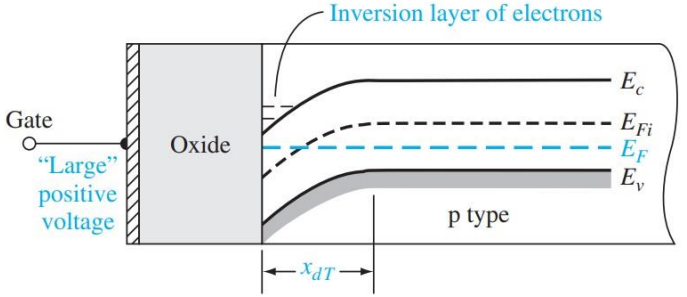
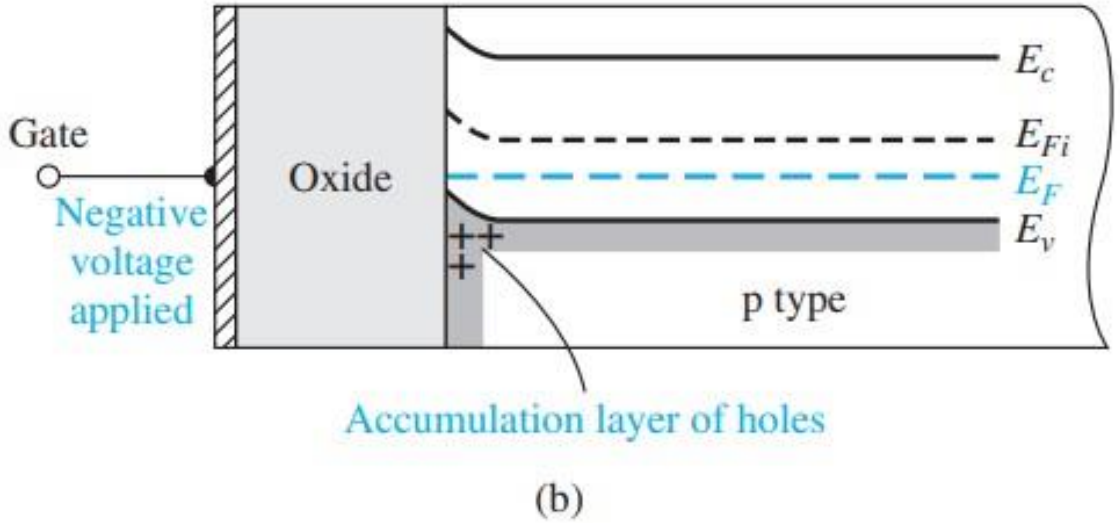


Figure 10.5 | The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.



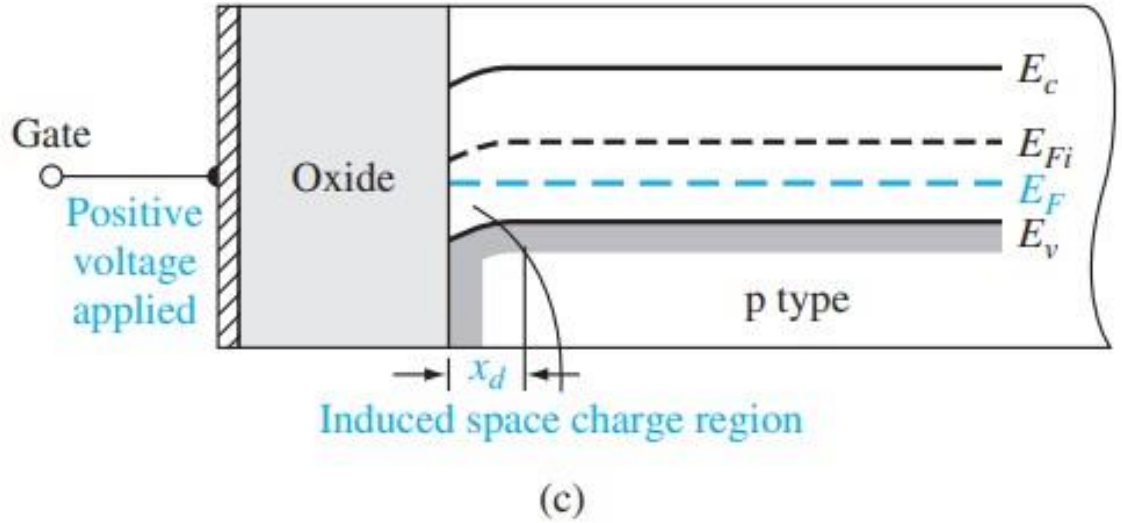
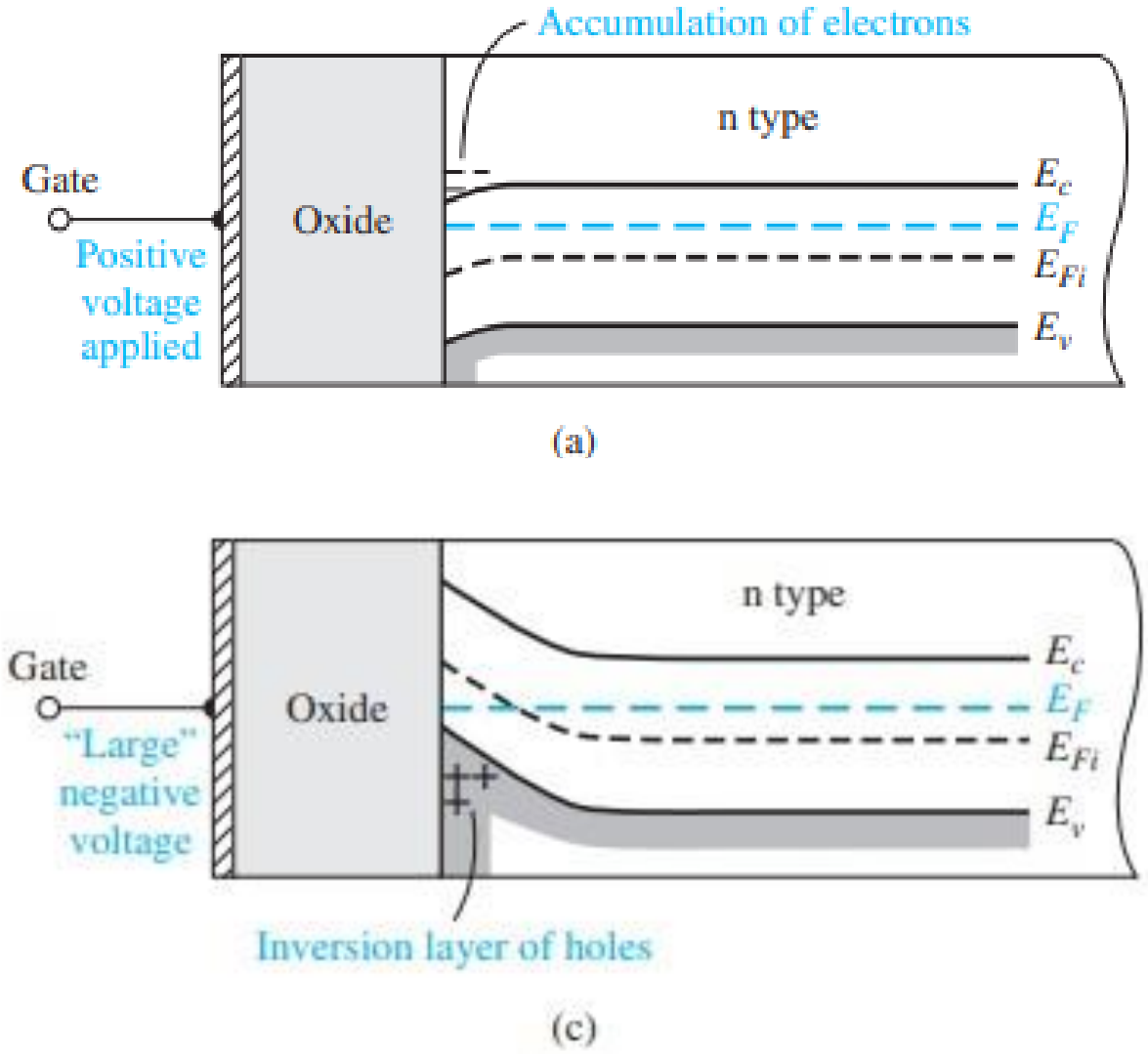


Figure 10.4 | The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the *ideal* case, (b) a negative gate bias, and (c) a moderate positive gate bias.



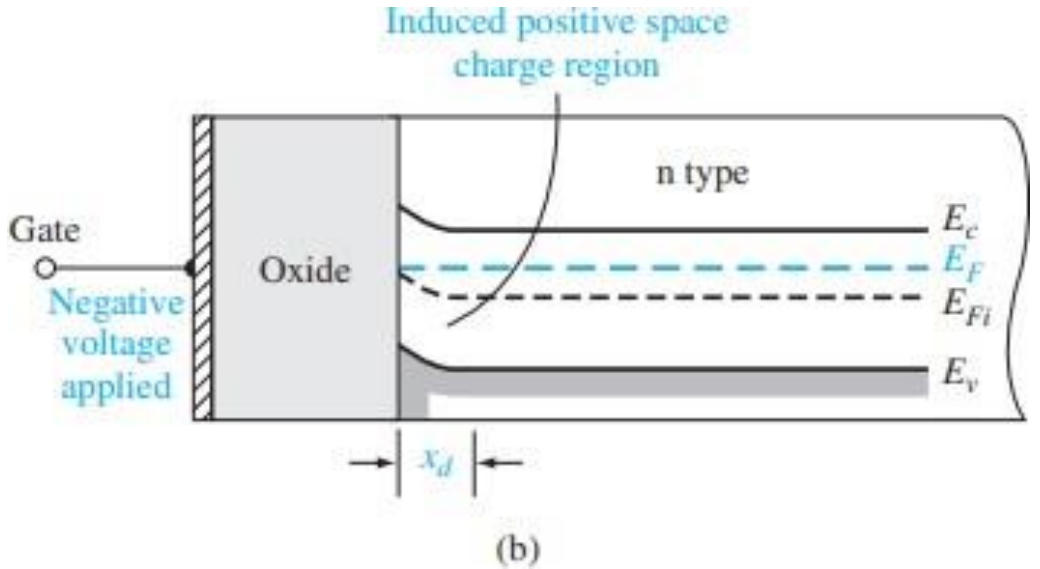


Figure 10.7 | The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias, (b) a moderate negative bias, and (c) a "large" negative gate bias.

The maximum space charge width, x_{dT}, at this inversion transition point can be calculated from Equation (10.5) by setting $\phi_s = 2\phi_{fp}$. Then

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2} \tag{10.6}$$

- The flat-band voltage is defined as the applied gate voltage such that there is no band bending in the semiconductor and, as a result, zero net space charge in this region.

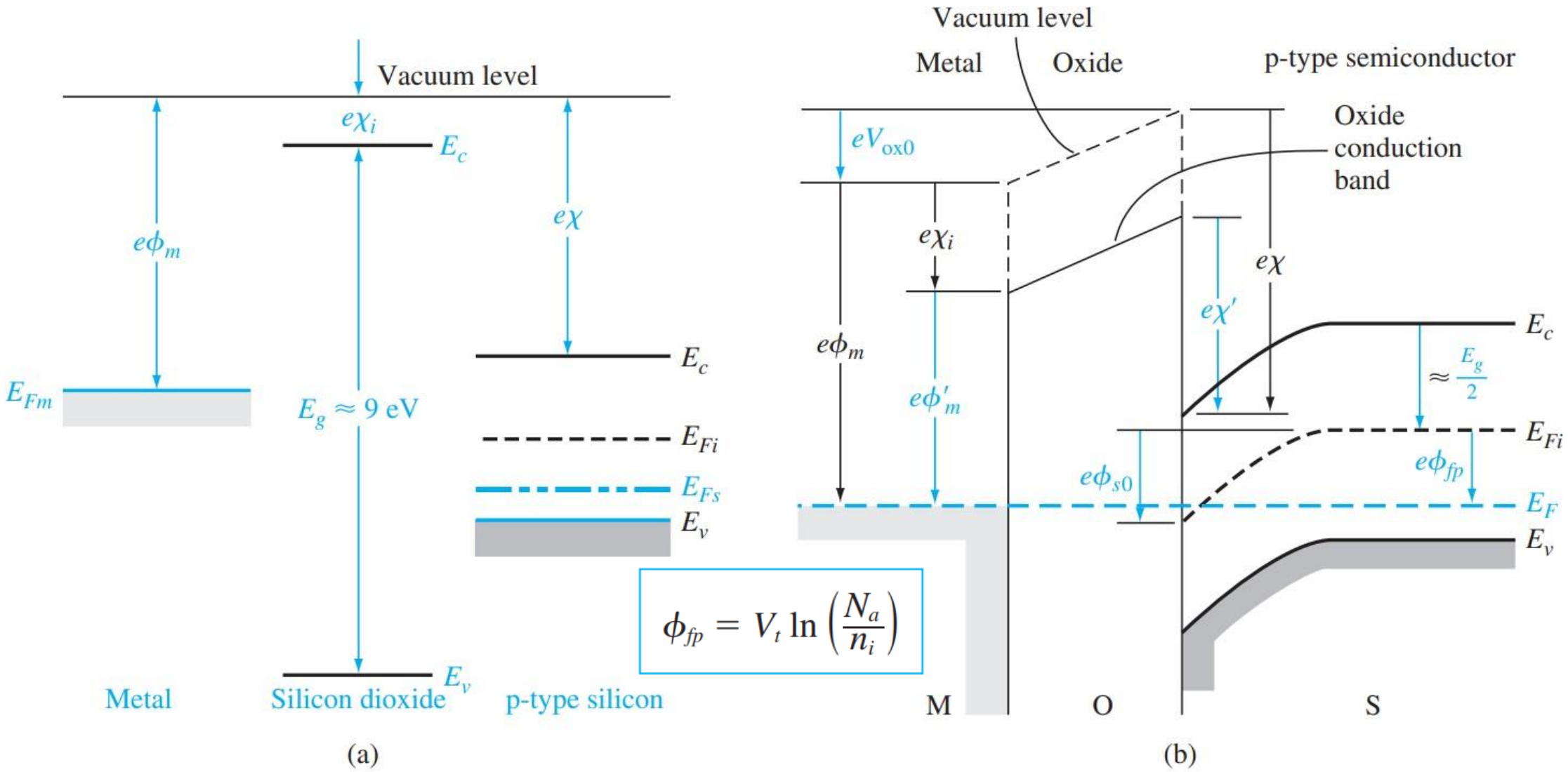
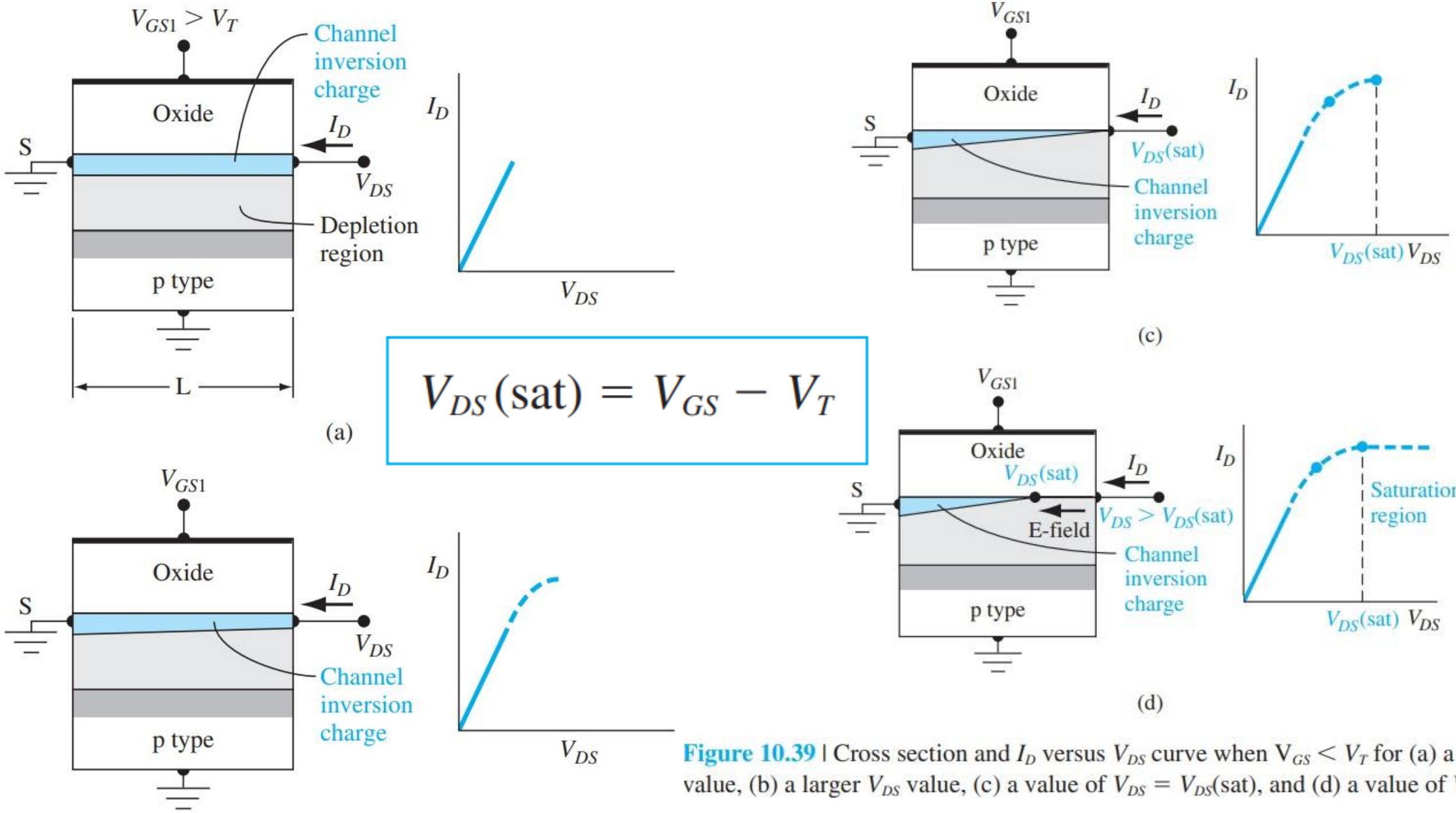


Figure 10.13 | (a) Energy levels in a MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact.



$$V_{DS}(\text{sat}) = V_{GS} - V_T$$

Figure 10.39 | Cross section and I_D versus V_{DS} curve when $V_{GS} < V_T$ for (a) a small V_{DS} value, (b) a larger V_{DS} value, (c) a value of $V_{DS} = V_{DS}(\text{sat})$, and (d) a value of $V_{DS} > V_{DS}(\text{sat})$.

- The inversion layer charge is a function of the gate voltage.
- Thus, the basic MOS transistor action is the **modulation of the channel conductance by the gate voltage**.
- The channel conductance, in turn, determines the drain current.
- As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases.
- The incremental conductance of the channel at the drain decreases, which then means that the slope of the I_D versus V_{DS} curve will decrease.
- When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_T, the induced inversion charge density is zero at the drain terminal.

Problems

1. Consider an oxide-to-p-type silicon junction at T =300 K. The impurity doping concentration in the silicon is Na = 2 *10^{15} cm^{-3} . Calculate the maximum space charge width. Does the space charge width increase or decrease as the p-type doping concentration decreases?
2. The parameters of an n-channel silicon MOSFET are μ_n= 650 cm^2 /V-s, t_{ox} = 8 nm = 80 Å, W/L = 12, and V_T = 0.40 V. If the transistor is biased in the saturation region, find the drain current for (a) V_{GS} = 0.8 V, (b) V_{GS} = 1.2 V, and (c) V_{GS} = 1.6 V.
3. An n-channel silicon MOSFET has the following parameters: W = 6 µm, L = 1.5 µm, and t_{ox} = 8 nm = 80 Å. When the transistor is biased in the saturation region, the drain current is $I_{D(sat)}$ = 0.132 mA at VGS = 1.0 V and $I_{D(sat)}$ =0.295 mA at V_{GS} = 1.25 V. Determine the electron mobility and the threshold voltage.
4. Calculate the theoretical punch-through voltage assuming the abrupt junction approximation. Consider an n-channel MOSFET with source and drain doping concentrations of N_d = 10^{19} cm^{-3} and a channel region doping of N_a = 10^{16} cm^{-3}. Assume a channel length of L = 1.2 µm, and assume the source and body are at ground potential.
5. Calculate C_{ox}, Φ_{fp} and x_{dT}. Consider an n-channel MOSFET with N_a = 3 *10^{16} cm^{-3} , L = 1.0 µm and t_{ox} = 20 nm = 200 Å.