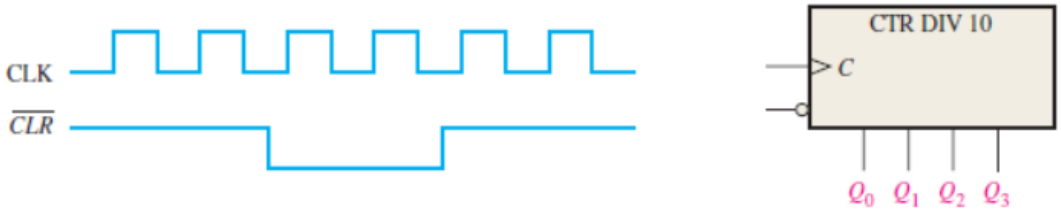
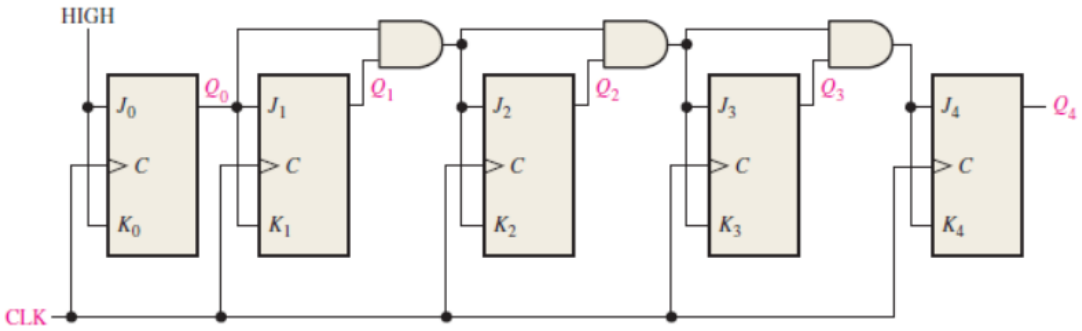
1. Draw the timing diagram for a 3-bit up/down counter for the following sequence.
0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0

2. For a mod10 counter, the waveforms are applied to the clock and clear inputs as indicated. Determine the waveforms for each of the counter outputs (Q_0, Q_1, Q_2, and Q_3). The clear is synchronous, and the counter is initially in the binary 1000 state.



3. Design a mod 13 asynchronous counter. Assume positive edge triggering. Draw its timing diagram

4. Draw the timing diagram for the counter shown below



5. Design a counter with the following **repeated** binary sequence: 1,3,5,7,9,11,13. (Use state table to determine the inputs for the flip flops)

6. Design a mod10 counter that uses excess 3 weighted code for decimal digits.