CED18I056

Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram

End Semester Examination

Digital and Analogue Circuits Design (COM206T)

Total Marks: 50 **Date: 19/11/2019** **Time: 3 hours**

1. A flip-flop has a 3ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably? **(3)**

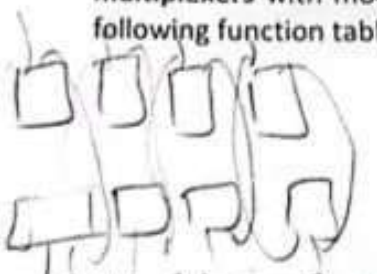
2. An M-N flip-flop works as follows:
   If MN = 00, the next state of the flip-flop is 0.
   If MN = 01, the next state of the flip-flop is the same as the present state.
   If MN = 10, the next state of the flip-flop is the complement of the present state.
   If MN = 11, the next state of the flip-flop is 1.
   (a) Complete the following table (use don't-cares when possible):

	Present State	Next State	M	N
00 / 01 reset/reset	0	0	0	X
11 / 10 set/toggle	0	1	1	X
00 / 10 reset/toggle	1	0	X	0
01 / 11 noop/set	1	1	X	1

   (b) Using this table and Karnaugh maps, derive and minimize the input equations for a counter composed of three M-N flip-flops which counts in the following sequence: **ABC = 000, 001, 011, 111, 101, 100, (repeat) 000, . . .**

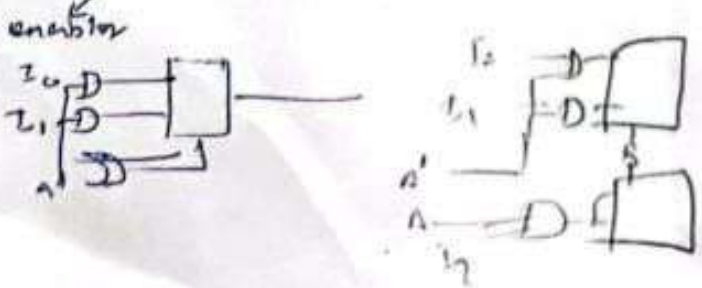
   (c) Draw a logic diagram for the above mentioned counter. **(7)**

4. Draw the logic (Block) diagram of a **four-bit register** with **four *D* flip-flops** and **four 4 × 1 multiplexers** with mode selection inputs s_1 and s_0. The register operates according to the following function table. **(5)**



S_1	S_0	Register Operation
0	0	No Change
0	1	Compliment the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data.

5. Show how two 2-to-1 multiplexers (with no added gates) could be connected to form a 3-to-1 MUX (Block diagram). Input selection should be as follows:
   If **AB = 00**, select I_0
   If **AB = 01**, select I_1
   If **AB = 1X** (B is a don't-care), select I_2. **(3)**



6. Find the complement of F = wx + yz; then show that FF' = 0 and F + F' = 1. (2)

7. Realize a **full adder** using a **3-to-8 line decoder** and **two NOR gates**. (2)

8. Design a combinational circuit that generates the **9's complement** of a **BCD** digit. (5)

9. Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign.
   (a) 10011 – 10001
   (b) 100010 – 100011 (4)

10. What is the largest binary number that can be expressed with 14 bits? What are the equivalent decimal and hexadecimal numbers? (2)

11. The state of a 12-bit register is **100010010111**. What is its content, if it represents
    (a) Three decimal digits in BCD?
    (b) Three decimal digits in the excess-3 code? (2)

12. A sequential circuit has three flip-flops A, B, C; one input *x*-in; and one output *y*-out. The state diagram is shown in Fig.1. The circuit is to be designed by treating the in the design. (5)

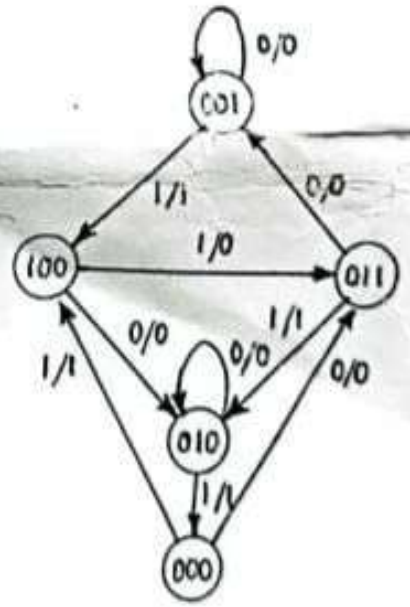


Fig. 1

13. Design a sequence detector that detects **three or more consecutive 1's** in a string of bits coming through the input lines. (5)

14. Represent the unsigned decimal numbers 842 and 537 in BCD, and form their sum. (2)

15. Draw a circuit for four bit Binary to Grey code conversion. (3)