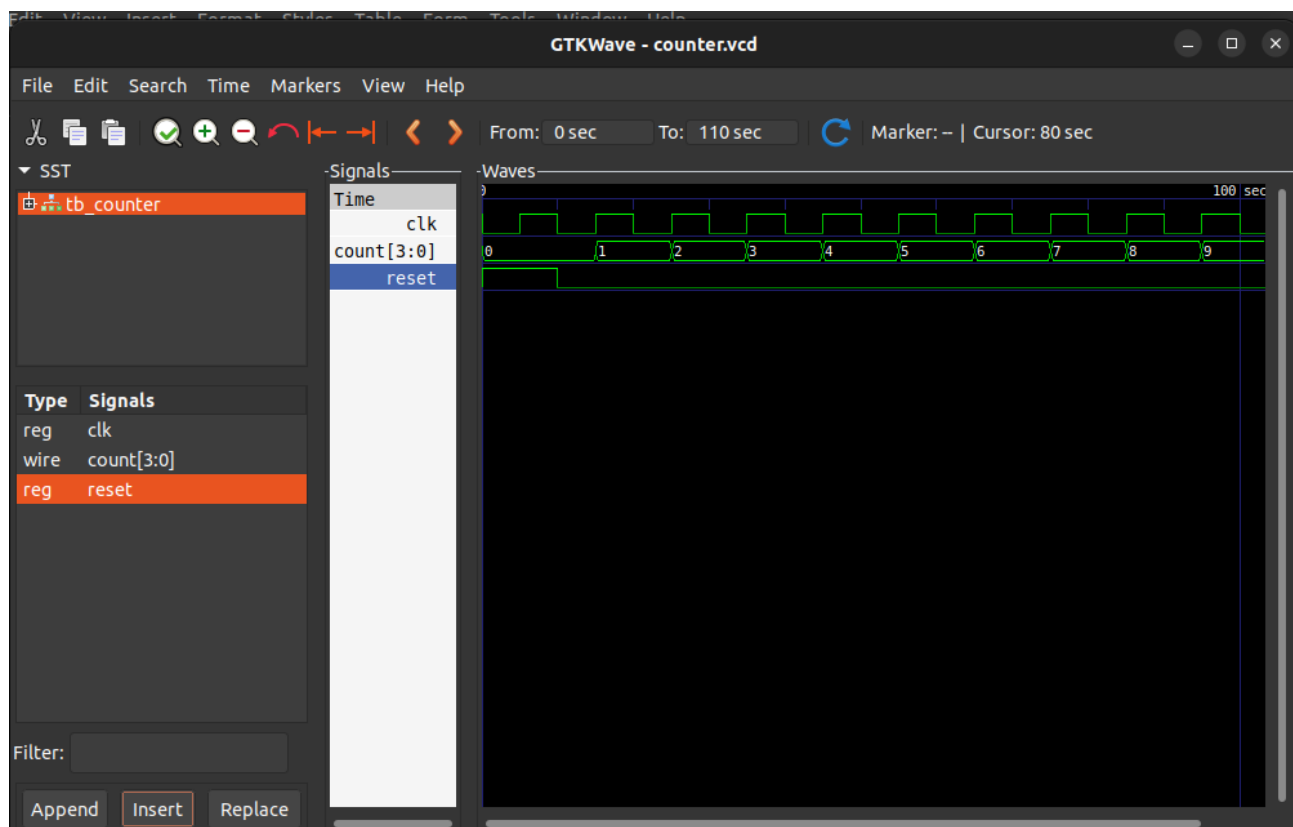


Q1)

```
l209@l209-Veriton-S2680G:~/Documents/CS23I1027$ iverilog counter.v tb_counter.v
-o counter
l209@l209-Veriton-S2680G:~/Documents/CS23I1027$ vvp counter
VCD info: dumpfile counter.vcd opened for output.
Time = 0 | reset = 1 | count = 0
Time = 10 | reset = 0 | count = 0
Time = 15 | reset = 0 | count = 1
Time = 25 | reset = 0 | count = 2
Time = 35 | reset = 0 | count = 3
Time = 45 | reset = 0 | count = 4
Time = 55 | reset = 0 | count = 5
Time = 65 | reset = 0 | count = 6
Time = 75 | reset = 0 | count = 7
Time = 85 | reset = 0 | count = 8
Time = 95 | reset = 0 | count = 9
Time = 105 | reset = 0 | count = 0
l209@l209-Veriton-S2680G:~/Documents/CS23I1027$ gtkwave counter.vcd
Gtk-Message: 16:28:16.719: Failed to load module "canberra-gtk-module"

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[0] start time.
[110] end time.
GTKWAVE | Reloading waveform...
[0] start time.
[110] end time.
GTKWAVE | ...waveform reloaded
```

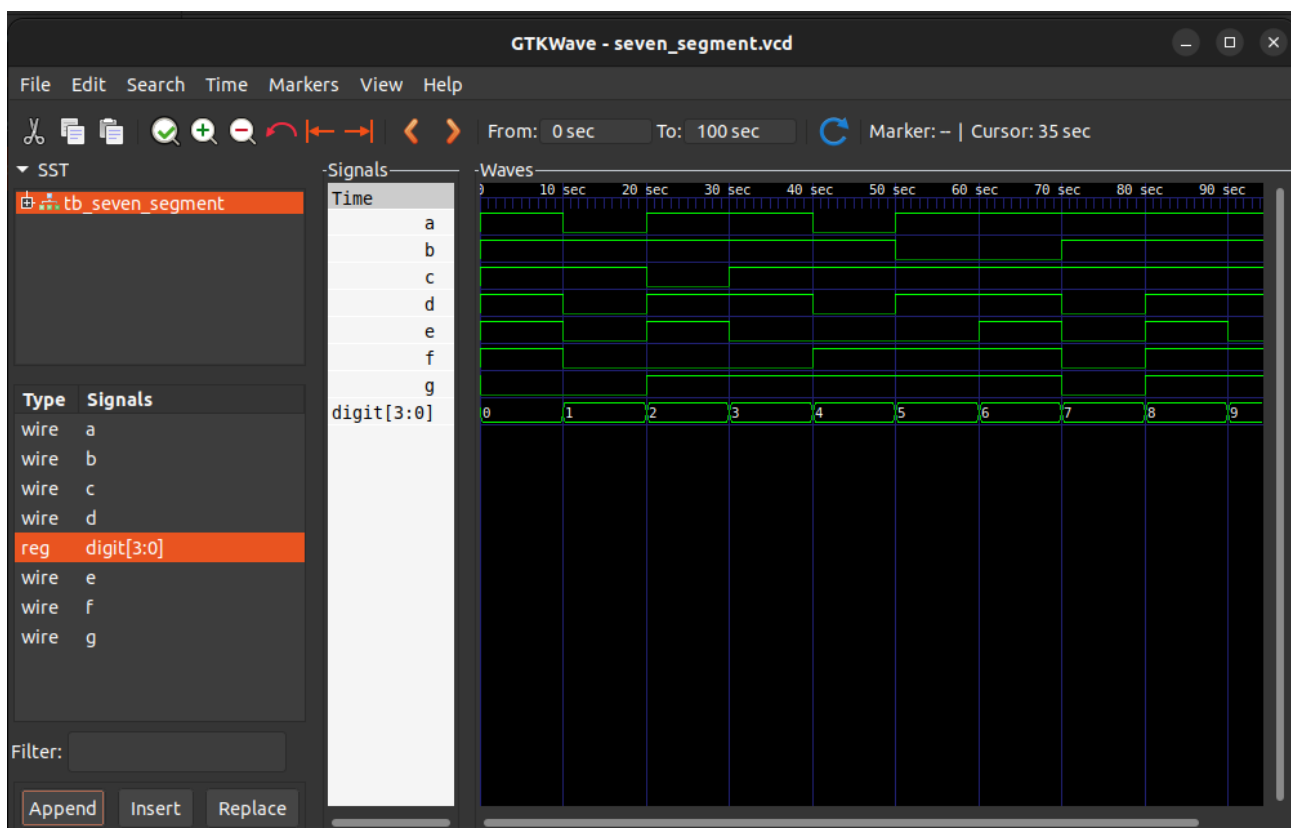


Q2)

```
l209@l209-Veriton-S2680G:~/Documents/CS23I1027/Q2$ iverilog seven_segment.v tb_s
even_segment.v -o seven_segment
tb_seven_segment.v:15: error: Unable to bind wire/reg/memory 'tb_counter' in 'tb
_seven_segment'
1 error(s) during elaboration.
l209@l209-Veriton-S2680G:~/Documents/CS23I1027/Q2$ iverilog seven_segment.v tb_s
even_segment.v -o seven_segment
l209@l209-Veriton-S2680G:~/Documents/CS23I1027/Q2$ vvp seven_segment
VCD info: dumpfile seven_segment.vcd opened for output.
Time = 0 | digit = 0 | a = 1 | b = 1 | c = 1 | d = 1 | e = 1 | f = 1 | g = 0
Time = 10 | digit = 1 | a = 0 | b = 1 | c = 1 | d = 0 | e = 0 | f = 0 | g = 0
Time = 20 | digit = 2 | a = 1 | b = 1 | c = 0 | d = 1 | e = 1 | f = 0 | g = 1
Time = 30 | digit = 3 | a = 1 | b = 1 | c = 1 | d = 1 | e = 0 | f = 0 | g = 1
Time = 40 | digit = 4 | a = 0 | b = 1 | c = 1 | d = 0 | e = 0 | f = 1 | g = 1
Time = 50 | digit = 5 | a = 1 | b = 0 | c = 1 | d = 1 | e = 0 | f = 1 | g = 1
Time = 60 | digit = 6 | a = 1 | b = 0 | c = 1 | d = 1 | e = 1 | f = 1 | g = 1
Time = 70 | digit = 7 | a = 1 | b = 1 | c = 1 | d = 0 | e = 0 | f = 0 | g = 0
Time = 80 | digit = 8 | a = 1 | b = 1 | c = 1 | d = 1 | e = 1 | f = 1 | g = 1
Time = 90 | digit = 9 | a = 1 | b = 1 | c = 1 | d = 1 | e = 0 | f = 1 | g = 1
l209@l209-Veriton-S2680G:~/Documents/CS23I1027/Q2$ gtkwave seven_segment.vcd
Gtk-Message: 16:36:52.707: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

[0] start time.
[100] end time.
```



Q3)

```
l209@l209-Veriton-S2680G:~/Documents/CS23I1027/Q2_1$ iverilog ss_counter.v tb_ss_counter.v -o ss_counter
vvp ss_counter
VCD info: dumpfile counter.vcd opened for output.
Time = 0 | reset = 1 | count = 0 | segments = 1111110
Time = 10 | reset = 0 | count = 0 | segments = 1111110
Time = 15 | reset = 0 | count = 1 | segments = 0110000
Time = 25 | reset = 0 | count = 2 | segments = 1101101
Time = 35 | reset = 0 | count = 3 | segments = 1111001
Time = 45 | reset = 0 | count = 4 | segments = 0110011
Time = 55 | reset = 0 | count = 5 | segments = 1011011
Time = 65 | reset = 0 | count = 6 | segments = 1011111
Time = 75 | reset = 0 | count = 7 | segments = 1110000
Time = 85 | reset = 0 | count = 8 | segments = 1111111
Time = 95 | reset = 0 | count = 9 | segments = 1111011
Time = 105 | reset = 0 | count = 0 | segments = 1111110
```

