```
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q1$ iverilog half_adder.v tb_half_add
er.v -o file
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q1$ vvp file
VCD info: dumpfile half_adder.vcd opened for output.
Time = 0 | A = 0 | B = 0 | sum = 0 | carry = 0
Time = 10 | A = 0 | B = 1 | sum = 1 | carry = 0
Time = 20 | A = 1 | B = 0 | sum = 1 | carry = 0
Time = 30 | A = 1 | B = 1 | sum = 0 | carry = 1
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q1$ cd ../Q2
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q2$ iverilog full_adder.v tb_full_add
er.v -o file
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q2$ vvp file
VCD info: dumpfile full_adder.vcd opened for output.
Time = 0 | A = 0 | B = 0 | C = 0 | sum = 0 | carry = 0
Time = 10 | A = 0 | B = 0 | C = 1 | sum = 1 | carry = 0
Time = 20 | A = 0 | B = 1 | C = 0 | sum = 1 | carry = 0
Time = 30 | A = 0 | B = 1 | C = 1 | sum = 0 | carry = 1
Time = 40 | A = 1 | B = 0 | C = 0 | sum = 1 | carry = 0
Time = 50 | A = 1 | B = 0 | C = 1 | sum = 0 | carry = 1
Time = 60 | A = 1 | B = 1 | C = 0 | sum = 0 | carry = 1
Time = 70 | A = 1 | B = 1 | C = 1 | sum = 1 | carry = 1
l509@cse:~/Documents/CS23I1027/Lab2Verilog/Q2$
```