Computer Organization and Architecture

CS 2007

Instructor: Dr. Krishnakumar Gnanambikai

Human Computers

Katherine Johnson

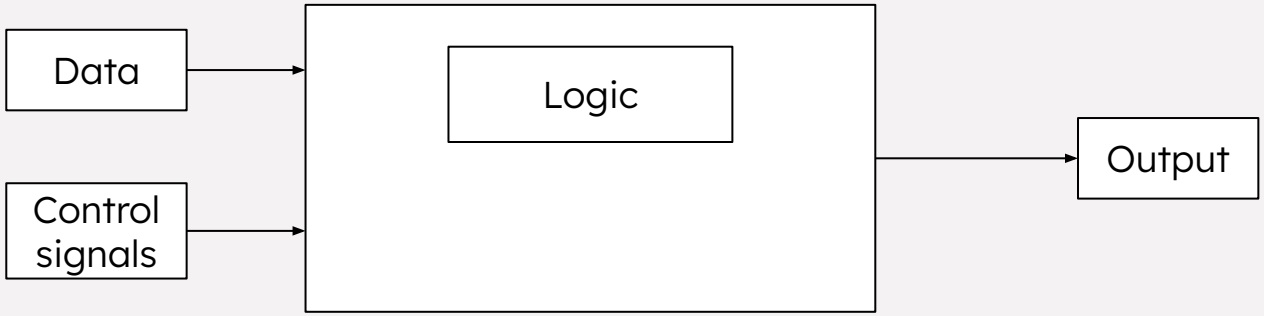
One of the human computers at NASA.

Calculated the flight trajectories for a number of historic missions, including the Apollo 11 flight to the Moon in 1969.

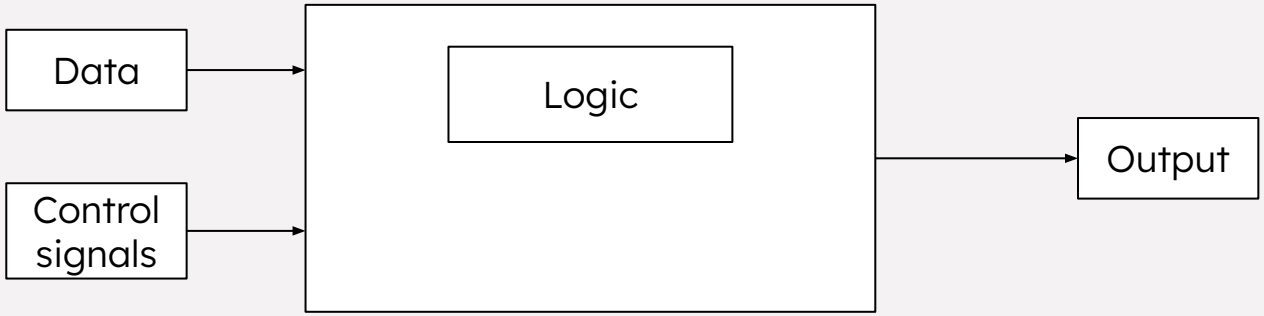
Digital Computers

Digital Computers

Structure of a computer

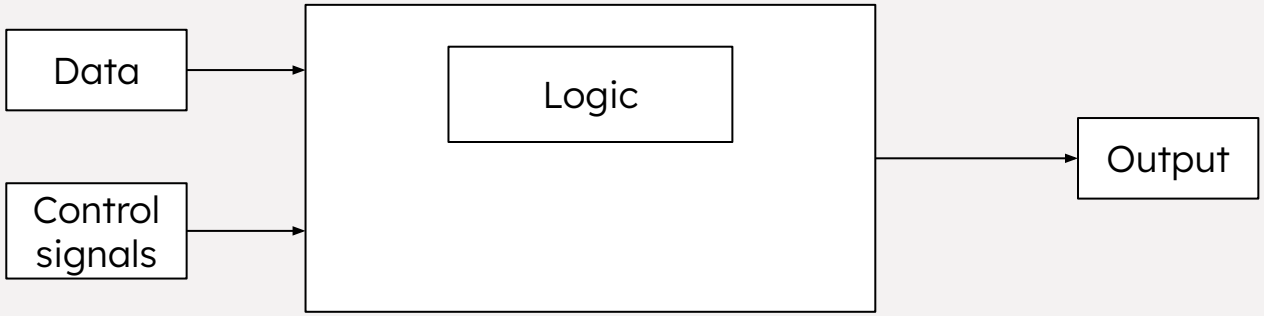


Structure of a computer



Will a computer change its **state** on producing the output?

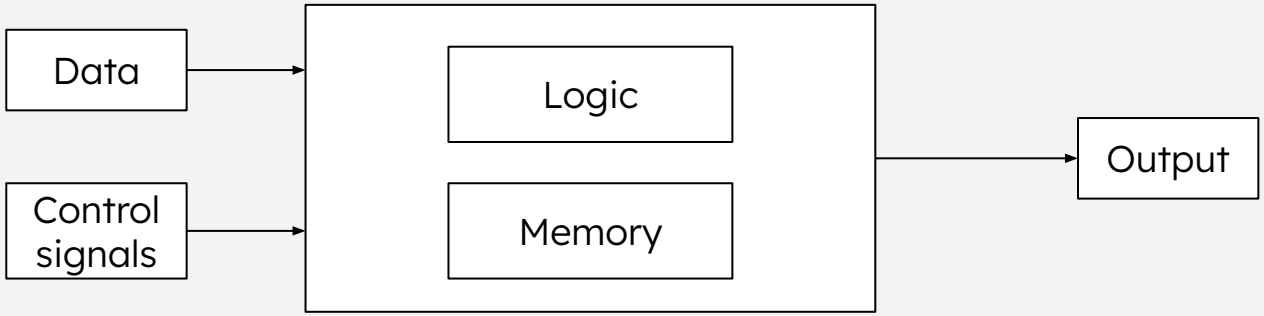
Structure of a computer



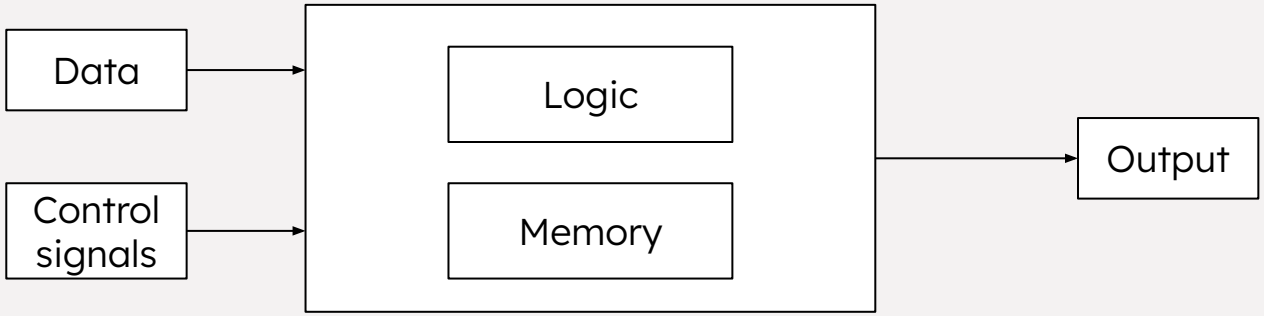
Will a computer change its **state** on producing the output?

Will output of a computer depend on its previous computations?

Structure of a computer



Structure of a computer



- Registers
- Cache memories
- Main memory

Question

P1

```
int a;
int main()
{

     a = 10;
     return 0;

}
```

P2

```
int a;
int main()
{

     printf("%d\n", a);
     return 0;

}
```

P1 executes first and then P2. What will be the output of P2?

Functions of a computer

- Multi-user
- Programmability
- Secure
- Fast
- Reliable
- Energy-efficient

Course Name	Computer Organization and Architecture	Course Code	CS2007			
Offered by Department	Computer Science and Engineering	Structure(LTP C)	3	1	0	4
To be offered for	B.Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	The course aims to introduce various aspects of computer organization such as Instruction format, Instruction codes, Addressing Modes, processor design and hierarchical memory design, Input and Output Interface design using Programmed Controlled and Interrupt Control way					
Learning Outcomes	• Understand the organization of a Computer system and ISAs • Apply the knowledge of combinational and sequential logical circuits to design computer architecture. • Understand the input / output and Memory related concepts. • Analyse the performance of different scalar Computers • Develop the Pipelining Concept for a given set of Instructions • Distinguish the performance of pipelining and non-pipelining environment in a processor					
Course Contents (with approximate breakup of hours for lecture/ tutorial/practice)	• Introduction: function and structure of a computer, functional components of a computer, performance of a computer system. Instruction set architectures – CISC and RISC architectures. (5L,1T) • Instructions: Language of the Computer, Operations of the Computer Hardware, Operands of the Computer Hardware, Representing Instructions in the Computer, Logical Operations Instructions for Making Decisions, addressing Modes, Parallelism & Instructions. (5L,1T) • Arithmetic Design: – Carry look ahead adder, Wallace tree multiplier, Floating–point adder/sub tractor, Division. (5L,2T) • The Processor: Logic Design Conventions, Building a Data path, A Simple Implementation Scheme (3L,1T) • An Overview of Pipelining, Pipelined Data path and Control, Data Hazards: Forwarding versus Stalling, Control Hazards, Exceptions and Parallelism via Instructions. (7L,2T) • Memory Hierarchy: Introduction, Memory Technologies (SRAM, DRAM), The Basics of Caches, Measuring and Improving Cache Performance, Dependable Memory, Virtual Machines, Virtual Memory, A Common Framework for Memory Hierarchy, using a Finite State Machine to Control a Simple Cache, Parallelism and Memory Hierarchies: Cache Coherence, Parallelism and Memory Hierarchy: Redundant Arrays of Inexpensive Disks and • Implementing Cache Controllers. (9L,2T) • Input/output Unit: access of I/O devices, I/O ports, I/O control mechanisms – Program Controlled I/O. Interrupt controlled I/O and DMA controlled I/O; I/O interfaces – Serial port, parallel port, USB port, SCSI bus, PCI bus; I/O peripherals – Keyboard, display, secondary storage devices. (8L,2T)					
Essential Reading	1. Patterson and Hennessy, "Computer Organization and Design," Morgan Kaufmann, 5 th Edition, ISBN-13 : 978-8131222744, 2013. 2. C. Hamacher, Z. Vranesic, and S. Zaky, "Computer Organization," Tata McGraw Hill, 5 th Edition, ISBN-9789339212131, 2002.					
Supplementary Reading	1. J. P. Hayes, "Computer Architecture and Organization," Tata McGraw Hill,ISBN-13 : 978-1259028564, 2017. 2. M. J. Murdocca, V. P. Heuring, "Computer Architecture and Organization - An Integrated Approach," John Wiley & Sons Inc., ISBN-13:978-0471733881, 2007. 3. A. S. Tanenbaum, "Structured Computer Organization," Prentice Hall, 5th Edition, ISBN-13 : 978-0132916523, 2006.					

Course Structure

Course Project - 20%

Mid Sem Exam - 30%

End Sem Exam - 50%