

1. Simplify the following function, and implement it with a two-level NAND gate circuit.

$$F = (A' + C' + D')(A' + C')(C' + D')$$

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$$F' = (A' + C' + D')' + (A' + C')' + (C' + D')'$$

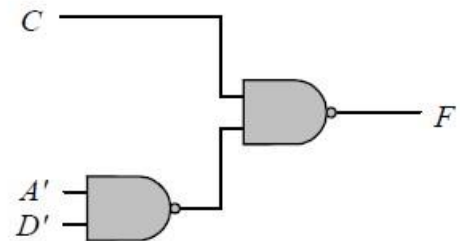
$$F' = ACD + AC + CD$$

		CD					
		00	01	11	10	C	
AB	00	m_0 1	m_1 1	m_3 0	m_2 1	B	D
	01	m_4 1	m_5 1	m_7 0	m_6 1		
	11	m_{12} 1	m_{13} 1	m_{15} 0	m_{14} 0		
	10	m_8 1	m_9 1	m_{11} 0	m_{10} 0		
A							

$$F = C' + A'D'$$

$$F = (C(A + D))'$$

$$F = (C(A'D'))'$$



2. Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is not divisible by 3.

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

		yz					
		00	01	11	10	y	
x	0	m_0 0	m_1 1	m_3 0	m_2 1	x	z
	1	m_4 1	m_5 1	m_7 1	m_6 0		

$$F = x' + xy' + xz + y'z$$

