EC1001
Digital Circuits

(Batch: EC23B1, EC23I1 & EC23I2)

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY,
DESIGN AND MANUFACTURING,
KANCHEEPURAM

Dr. Kalpana Settu

Assistant Professor

ECE, IIITDM Kancheepuram

Schedule

- Monday: 11 – 11: 50 am
- Tuesday: 8 – 8: 50 am
- Wednesday: 1 – 1: 50 pm
- Thursday: 9 – 9: 50 am

Course Information

- Digital Circuits– **Core Course**
- A digital system is an interconnection of digital modules. To understand the operation of each digital module, it is necessary to have a basic knowledge of digital circuits and their logical function.
- This course will equip the students with an ability to understand the basics of digital electronics.

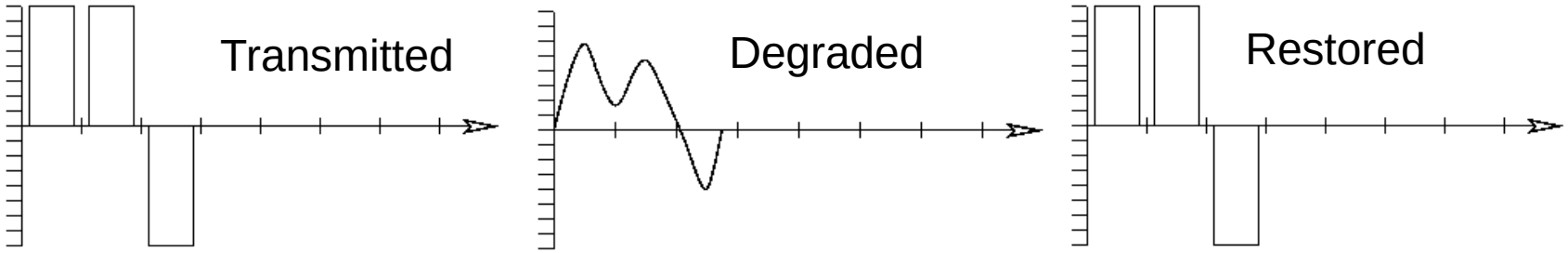
What are Analog & Digital Systems?

- An analog system varies continuously over a specified range
- A digital system assumes only discrete values

Why Use Digital Systems?

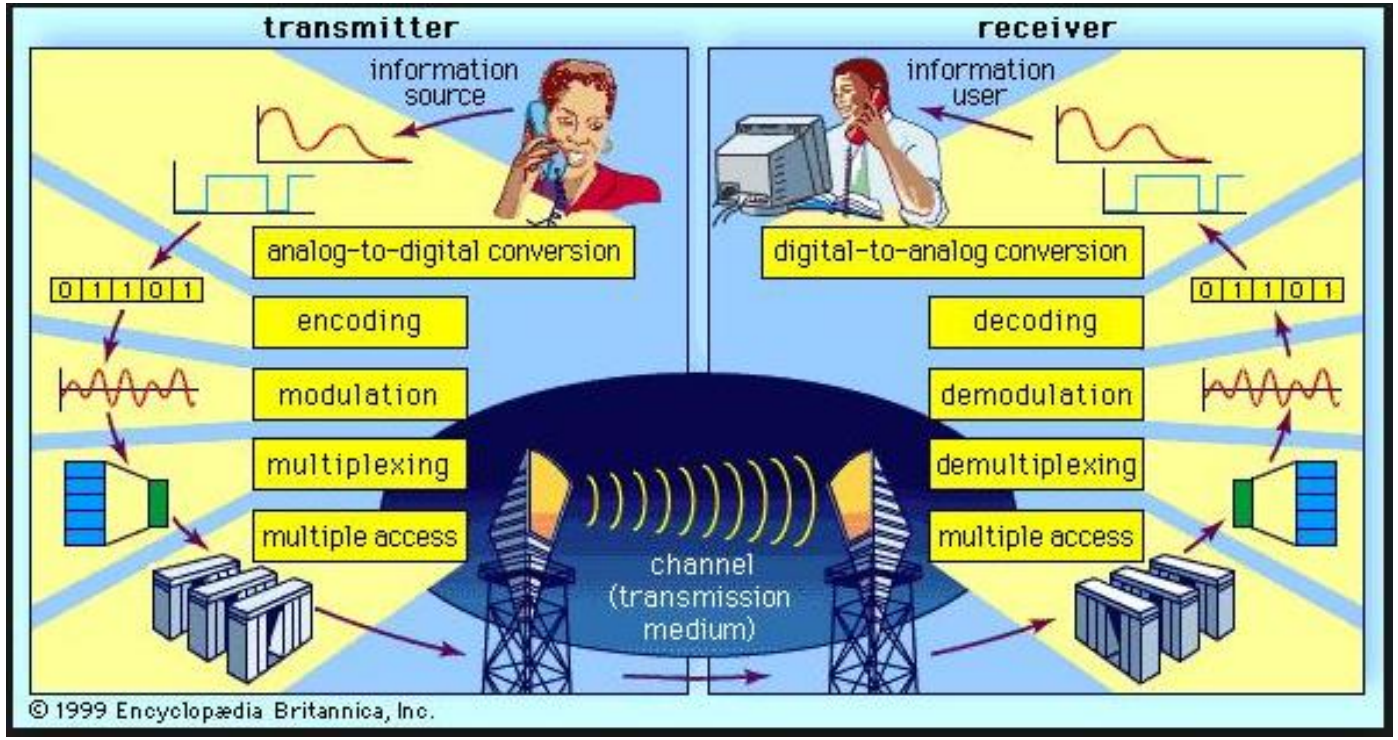
- A digital system is used for machine computing → Binary (0,1) computing in a PC
- A digital signal can be restored more easily

Ex: Transmit the number 6. In binary, it is 110.



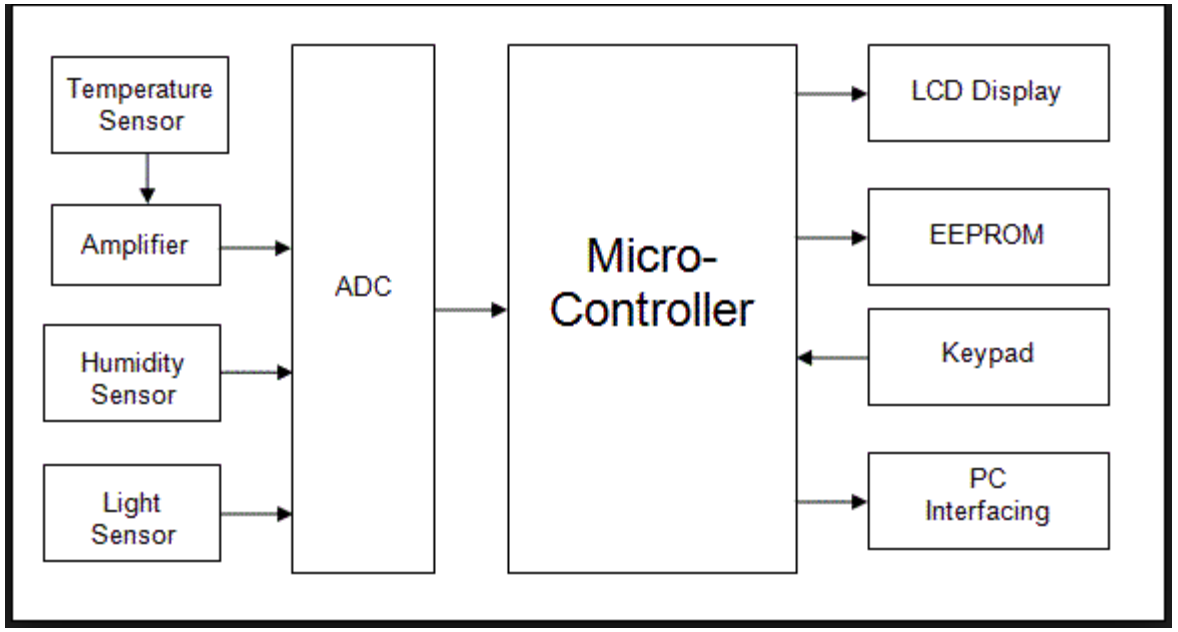
Digital Systems

- Ex: Telecommunication



Digital Systems

- Ex: Weather Monitoring



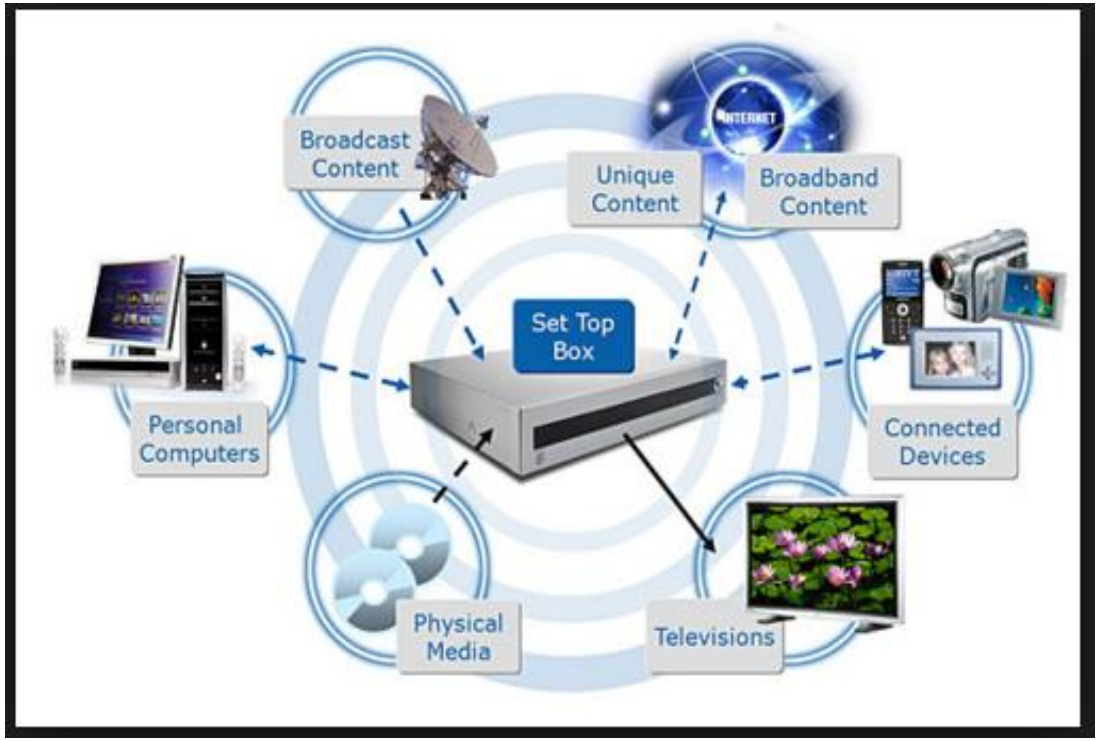
Digital Systems

- Ex: Medical Technology

Wearable Devices

Digital Systems

- Digital systems have such a prominent role in everyday life that we refer to the present technological period as the digital age.



Course Content

- **Introduction to Digital Systems**: Introduction to Digital Logic, Data Representations, Number systems, Code conversion (L5+T1)
- **Boolean Algebra & Logic**: Laws and theorems of Boolean Algebra, Truth Table and algebraic form, Boolean Logic Minimization, Design using MSI Components, K Maps, QM method, SOP, POS; NAND and NOR implementations, Digital Circuit Characterization (L7+T2)
- **Combinational Circuit Design**: Design Procedure, Multiplexer, Decoder, Encoder, Comparator, Seven-segment display, Parity generator, Design of large circuits. (L8+T2)
- **Sequential Circuit Design**: Asynchronous and Synchronous Design, Flip Flops & Latches, Design of sequential modules – SR, D, T and J-K Flip-flops, applications, Clock generation, Registers and Counters. (L10 +T3)
- **State Machine Design**: Moore and Mealy Machines, State Table and Diagram, State machine Design Approach, Digital Implementation of State Machine. (L8+T3)
- **Introduction to HDL and Design Examples** : (L3+T1)

Text Book

Textbook:

- M Morris Mano and Michael D. Ciletti**, "Digital Design with an Introduction to the Verilog HDL, VHDL & System Verilog",** 6th Edition, Pearson, ISBN: 978-9353062019, 2018.

References:

- Digital Fundamentals by Thomas L. Floyd
- C. H. Roth, Jr., Fundamentals of Logic Design, 7th Edition, Cengage Learning, ISBN: 9781133628477, 2013.
- S. Brown and Z. Vranesic, Fundamentals of Digital Logic with VHDL Design, 3rd Edition, ISBN: 9780077221430, 2008.

What will we learn from this course?

- Binary Numbers
- Boolean Algebra
- Gate Level Minimization
- Combination Logic
- Synchronous Sequential Logic
- Registers and Counters
- Introduction to HDL

What will we learn from this course?

- Chapter 1: Binary Numbers
  - presents the various binary systems suitable for representing information in digital systems.
- Chapter 2: Boolean Algebra and Logic Gates
  - introduces the basic postulates of Boolean algebra and shows the correlation between Boolean expressions and their corresponding logic diagrams.
- Chapter 3: Gate Level Minimization
  - covers the map method for simplifying Boolean expressions and digital circuits.

What will we learn from this course?

- Chapter 4: Combinational Logic
  - outlines the formal procedures for the analysis and design of combinational circuits. (adders, subtractors, decoders, encoders, and multiplexers)
- Chapter 5: Synchronous Sequential Logic
  - outlines the formal procedures for analyzing and designing clocked sequential circuits. (Flip-Flop, Latches)
  - state equation, state table, and state diagram, Moore and Mealy Machines
- Chapter 6: Registers and Counters
  - deals with registers, shift registers, and counters

Grading

- Assignments/Weekly Quiz: 25%
- Mid Semester Exam: 25%
- End Semester Exam: 50%

Attendance

- IIITDM Kancheepuram is a residential Institute and students are expected to maintain 100% attendance in all the courses that they have registered. A minimum of 85% attendance is required in each course to appear for the end semester examination. Students failing in the attendance criterion will be awarded **W grade** in the respective course and have to repeat the course when it is offered next time.
- Attendance is absolutely mandatory on the examination dates. No makeup exams will be given.

Contact

- Instructor

Dr. Kalpana Settu

Office: Laboratory Block 219C

E-mail: skalpana@iiitdm.ac.in