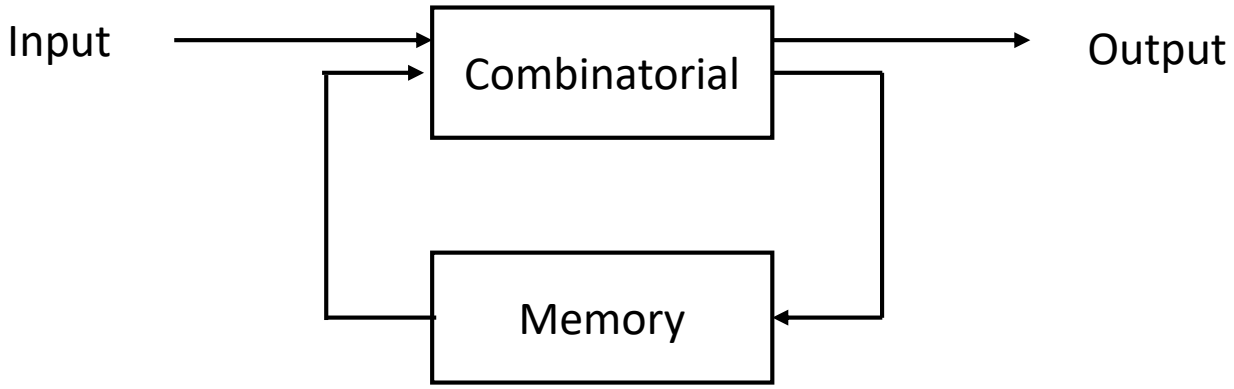
Digital System Design

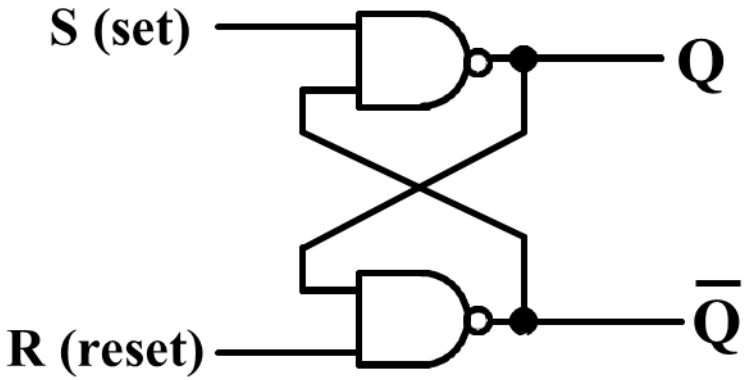
Notes on Important Sequential Circuits

Sequential Circuit



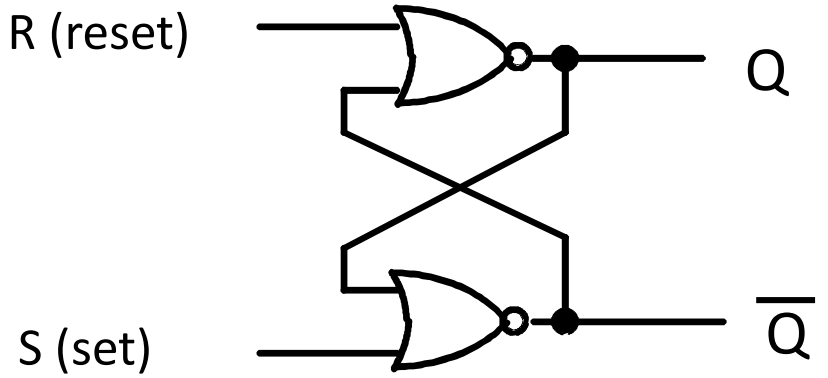
S-R Latch (NAND Gate)

S	R	Q	State
0	0	1	Invalid (Indeterminate)
0	1	1	Set (S)
1	0	0	Reset (S)
1	1	0	Existing values



R-S Latch (NOR gate)

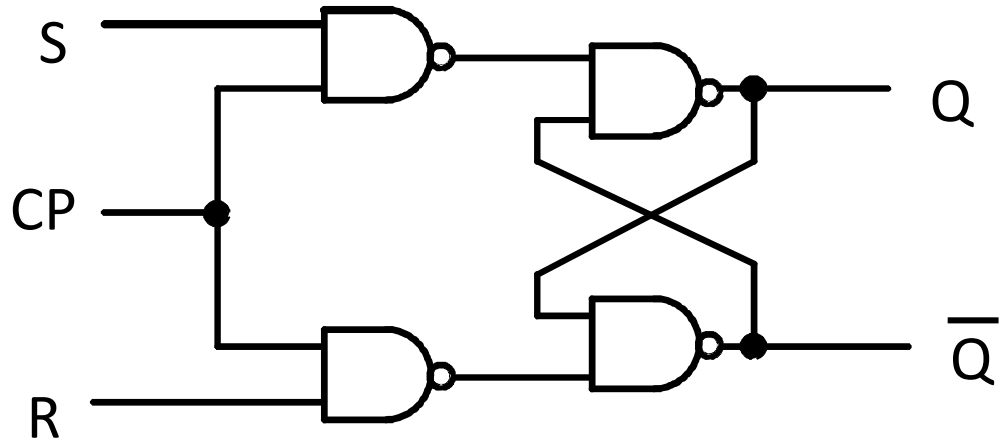
R	S	Q	State
0	1	1	Set (S)
0	0	1	Existing
1	0	0	Reset (R)
1	1	1	Invalid (Indeterminate)



S R Flip-flop

Characteristic Table

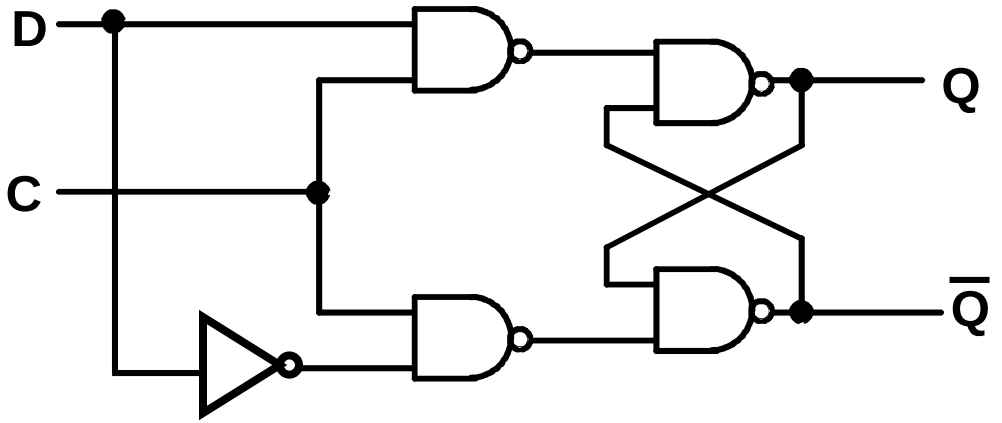
Q	**S**	**R**	**Q (t+1)**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	In
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	In



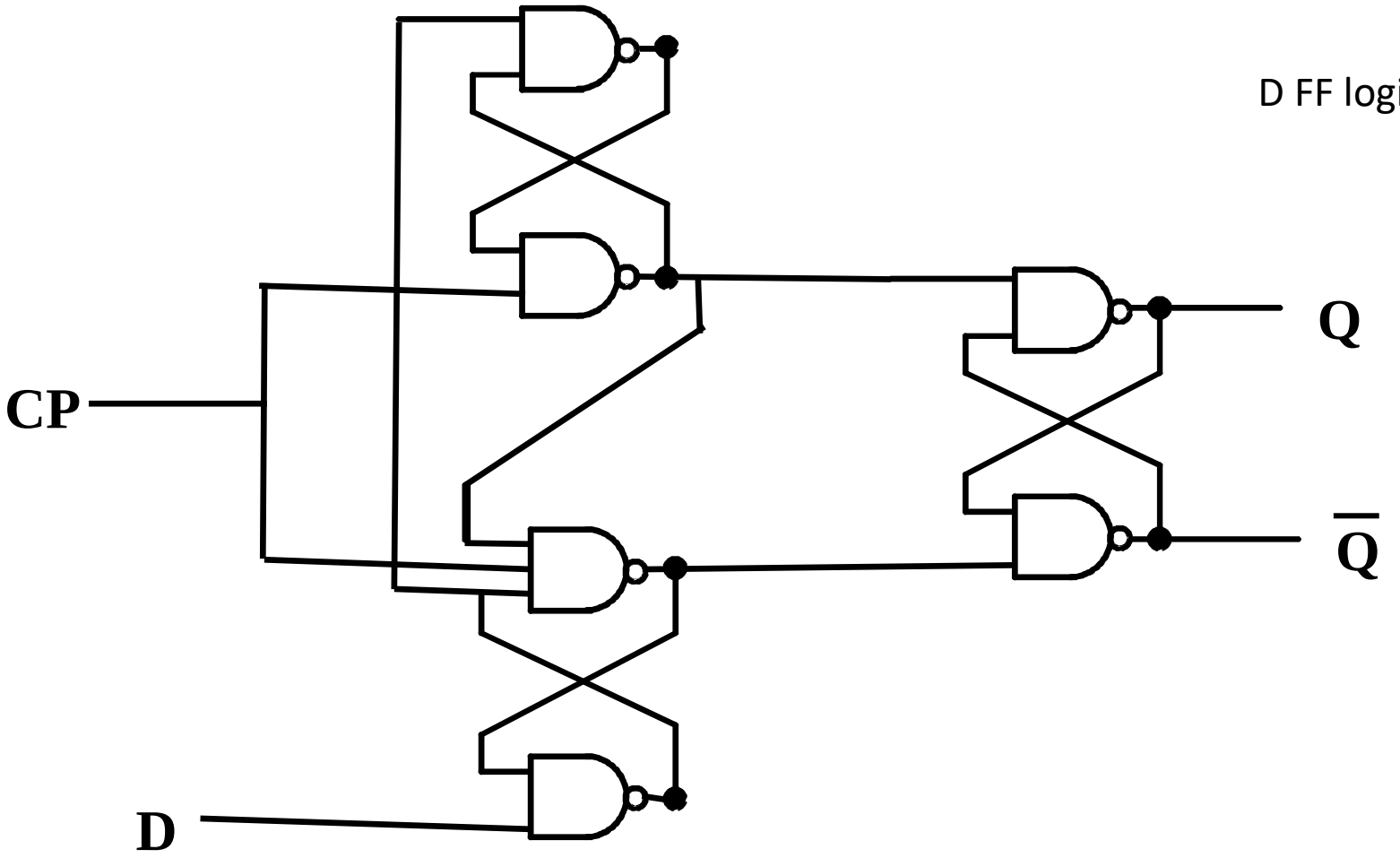
D Flip-flop

Characteristic Table

Q	D	Q (t+1)
0	0	0
0	1	1
1	0	0
1	1	1



Edge triggered D Flip-Flop



D FF logic with edge trigger

Edge triggered D Flip-Flop

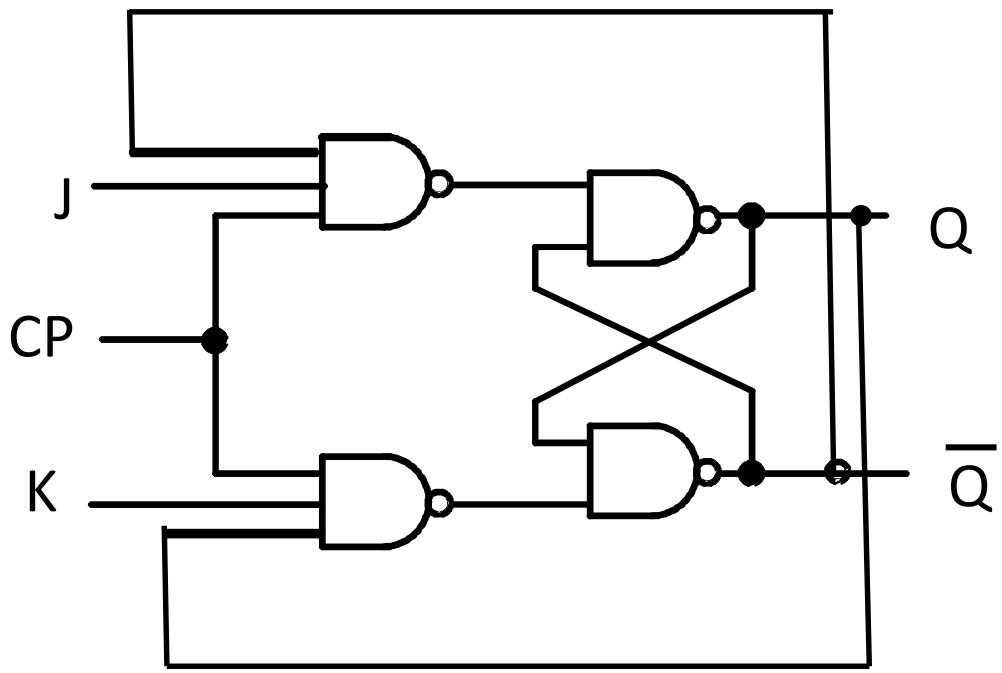
Setup Time – The time in which D Input must be maintained as a constant value prior to the application of the pulse.

Hold Time – The time for which D Input must not change after the application of positive-going transition of the pulse.

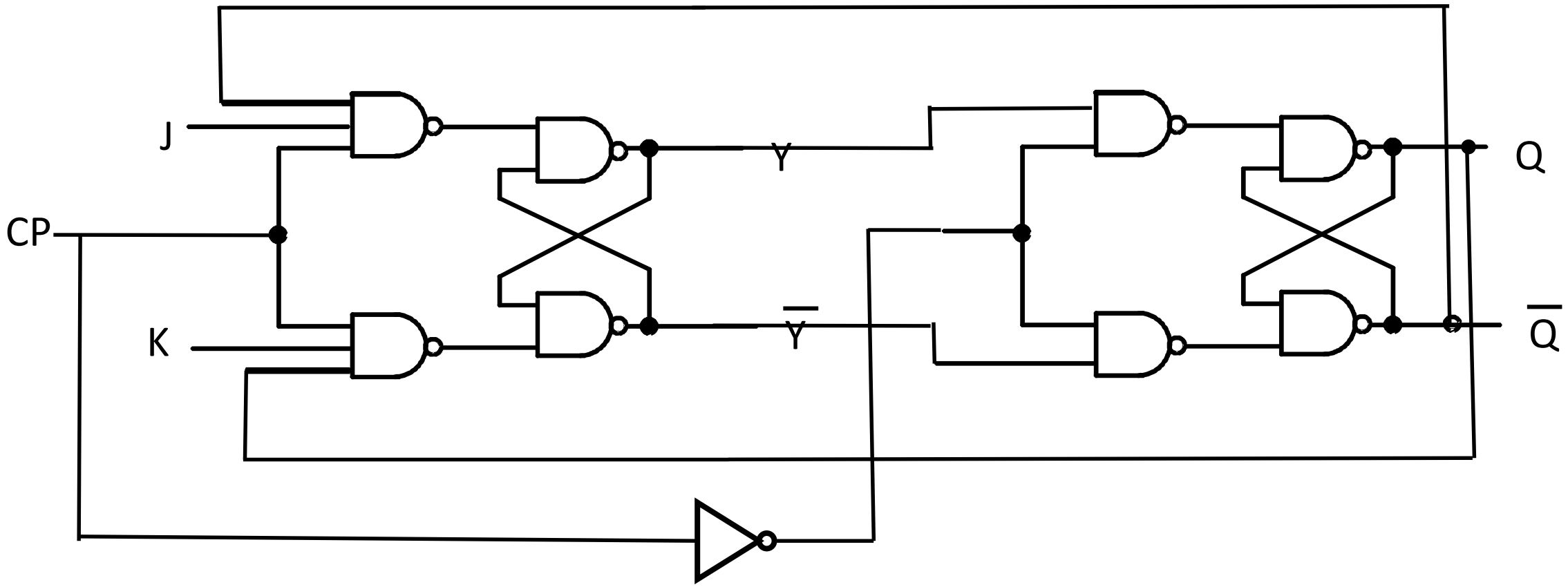
JK Flip-flop

Characteristic Table

Q	J	K	Q (t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



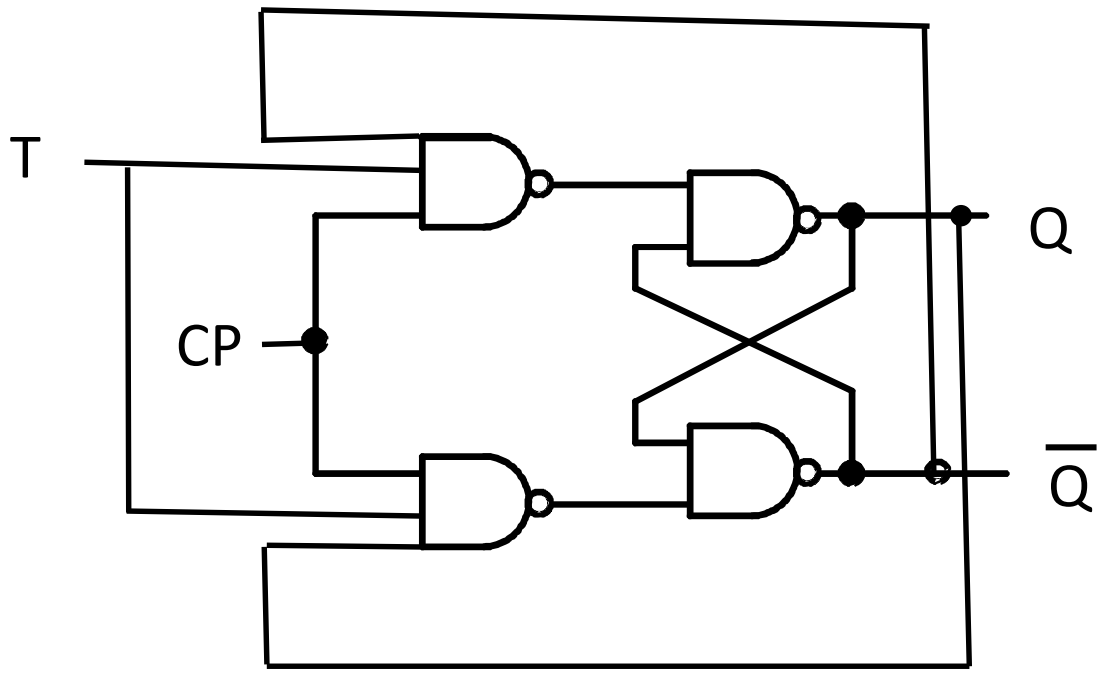
Master Slave J K Flip-flop



T Flip-flop

Characteristic Table

Q	T	Q (t+1)
0	0	0
0	1	1
1	0	1
1	1	0



Excitation Tables

T Flip-flop

Q	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

D Flip-flop

Q	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

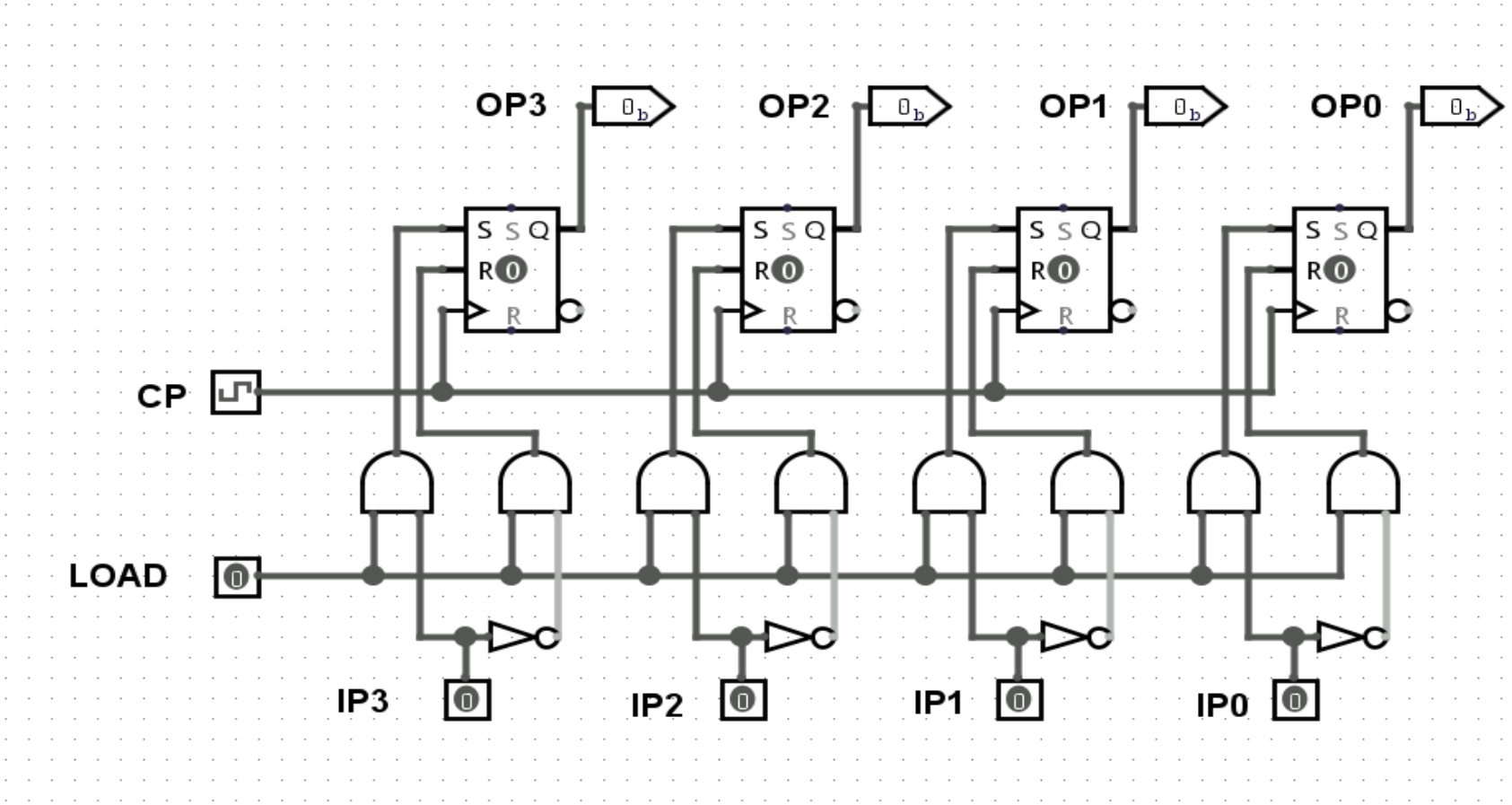
SR Flip-flop

Q	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

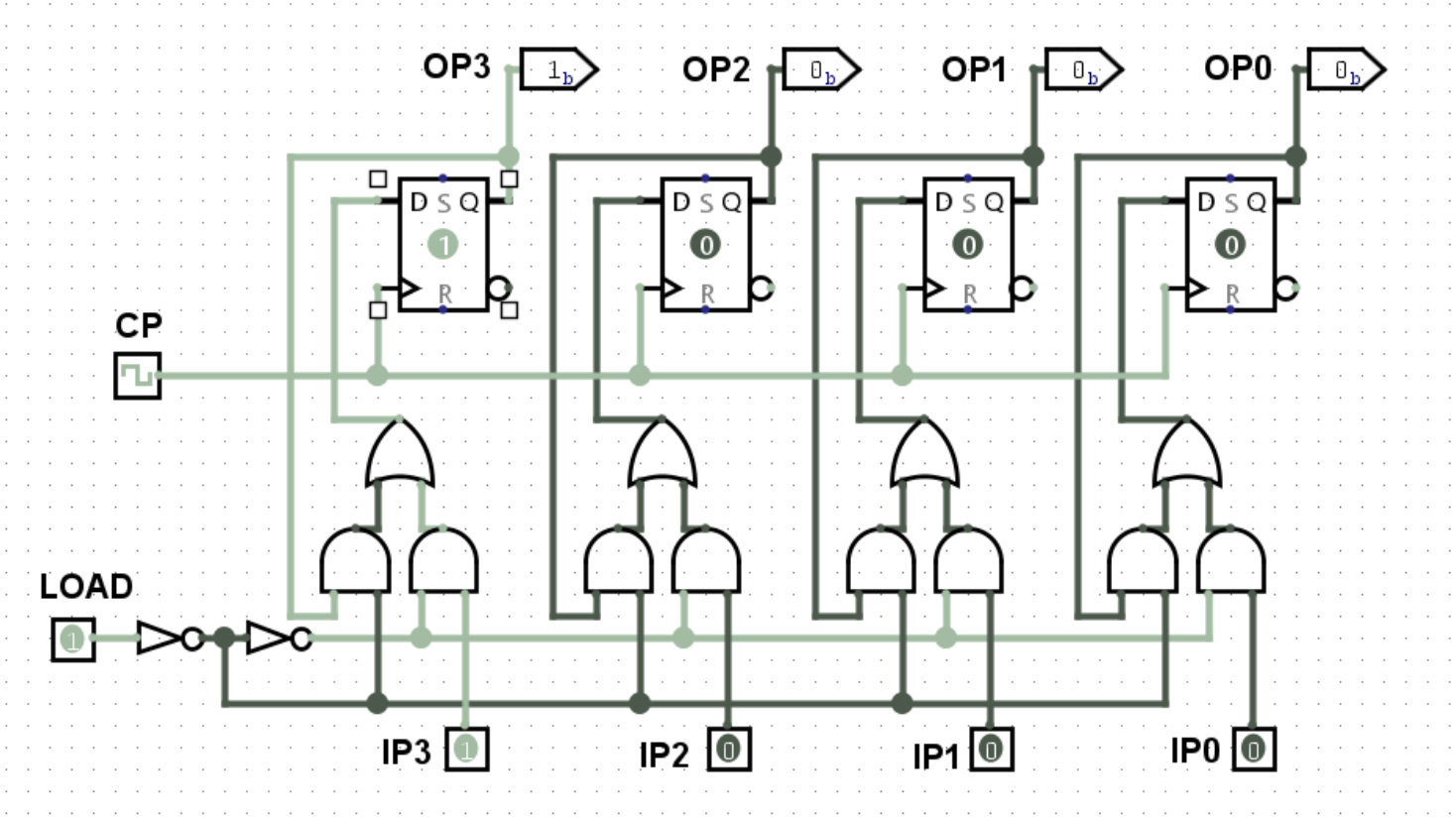
JK Flip-flop

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

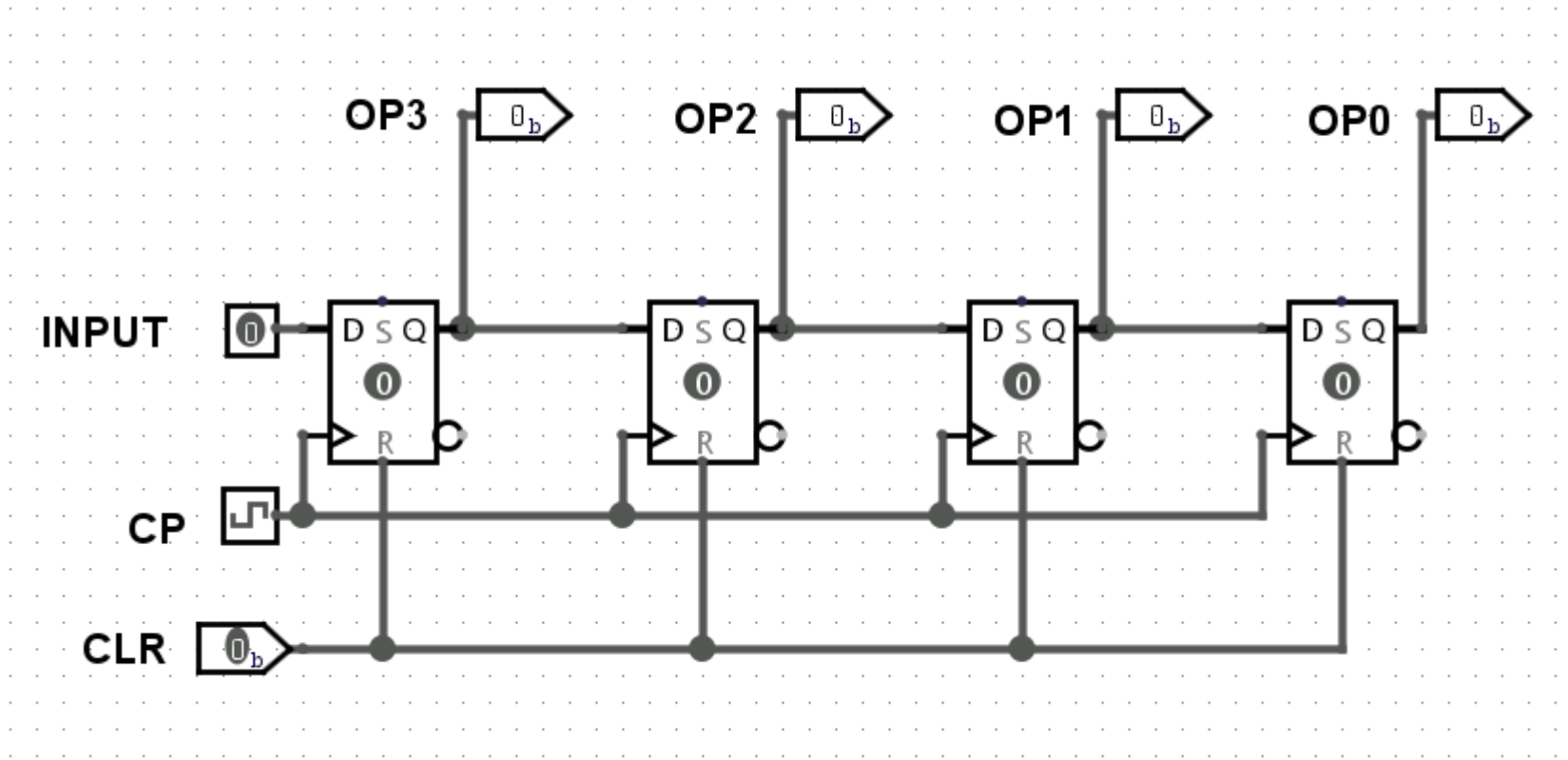
4-bit register with parallel load (SR-FF)



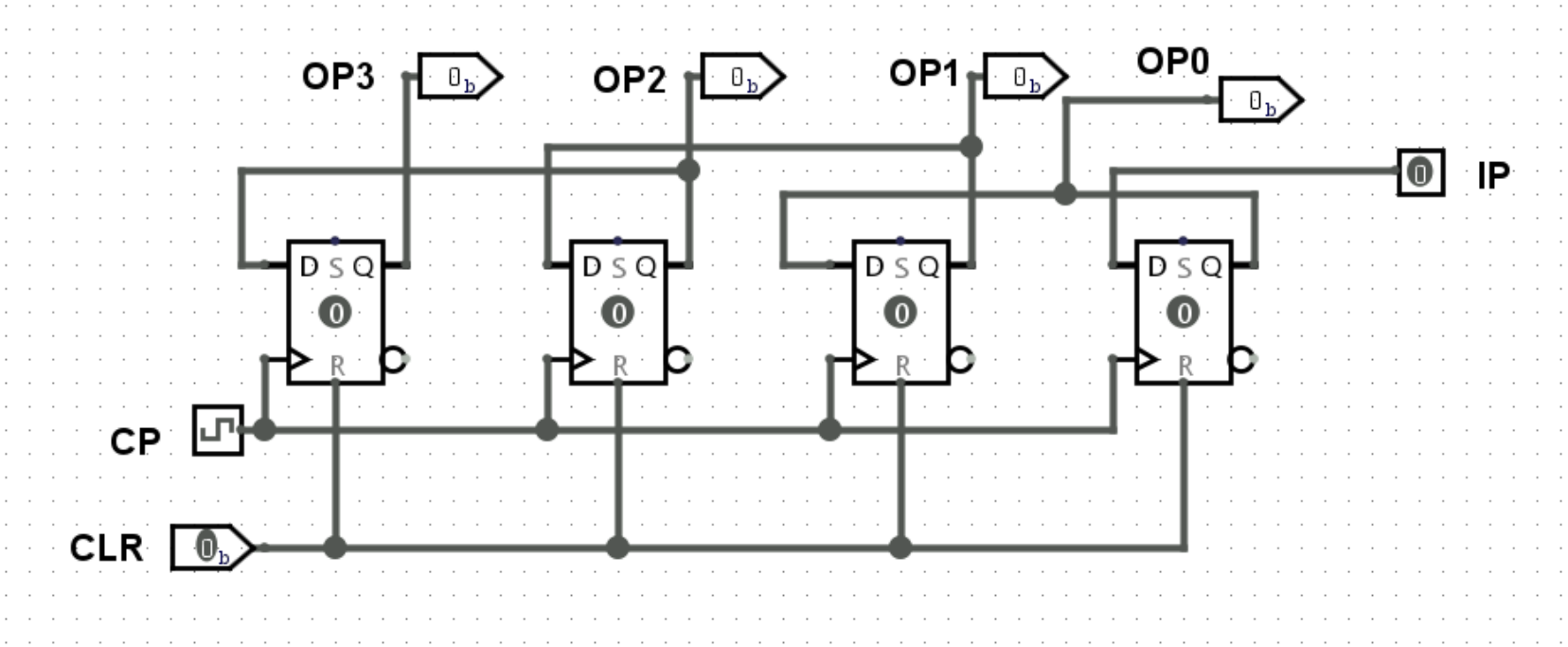
4-bit Register with Parallel load (D-FF)



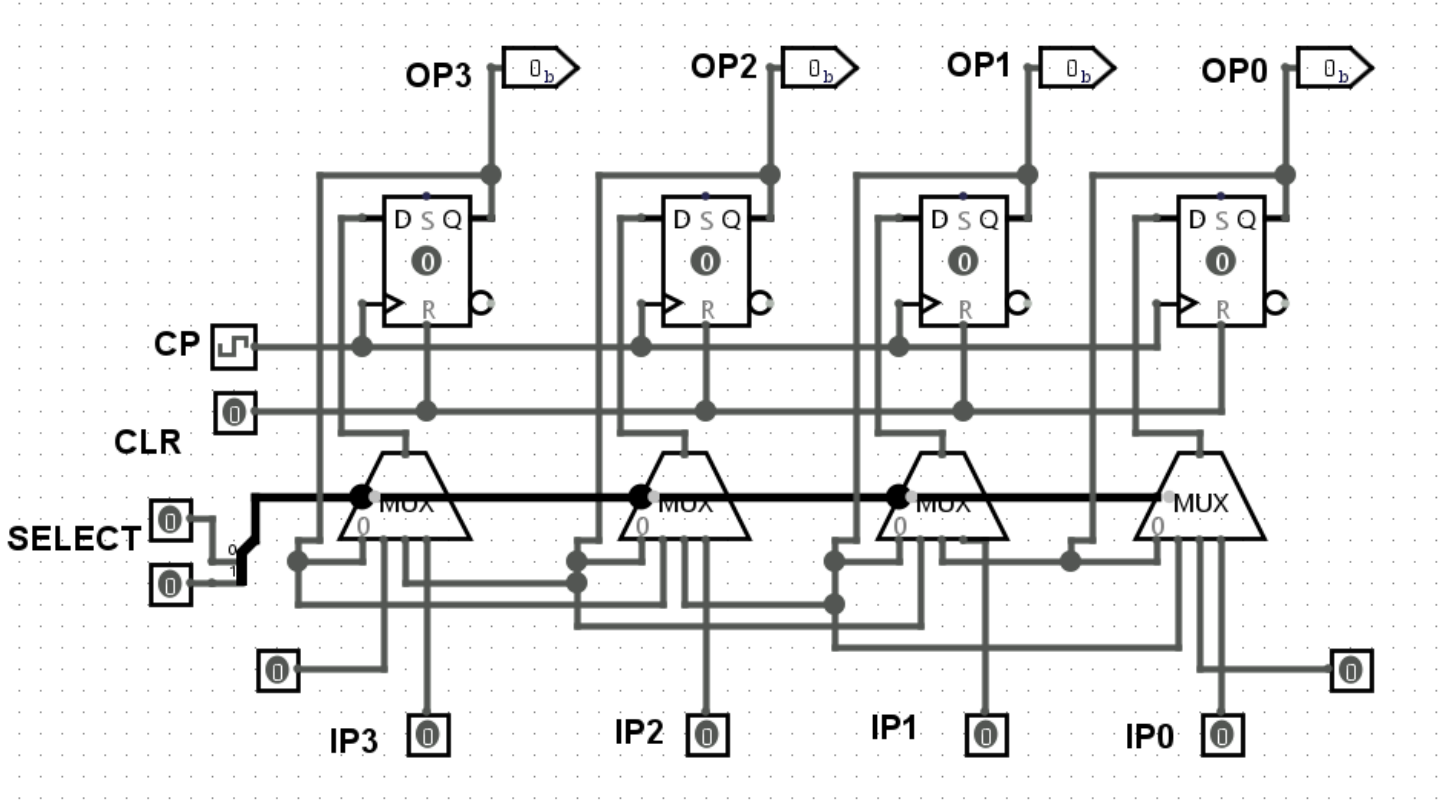
4-bit Shift Register (Left to Right)



4-bit Shift Register (Right to Left)

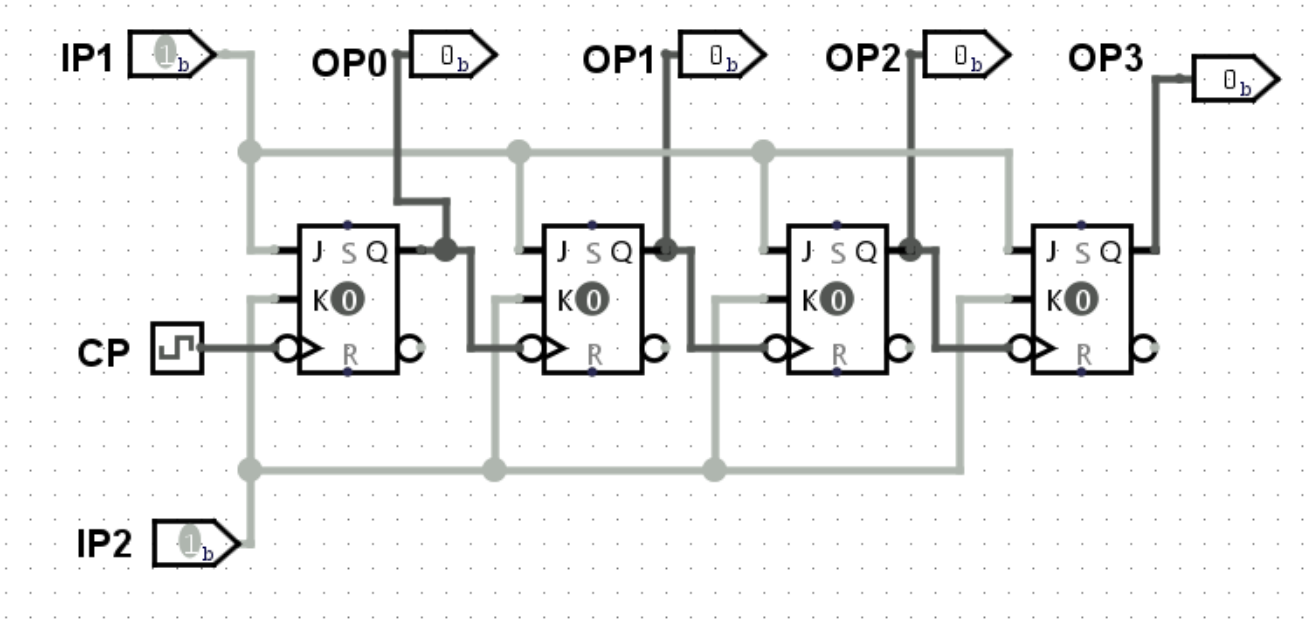


4-bit Universal Register



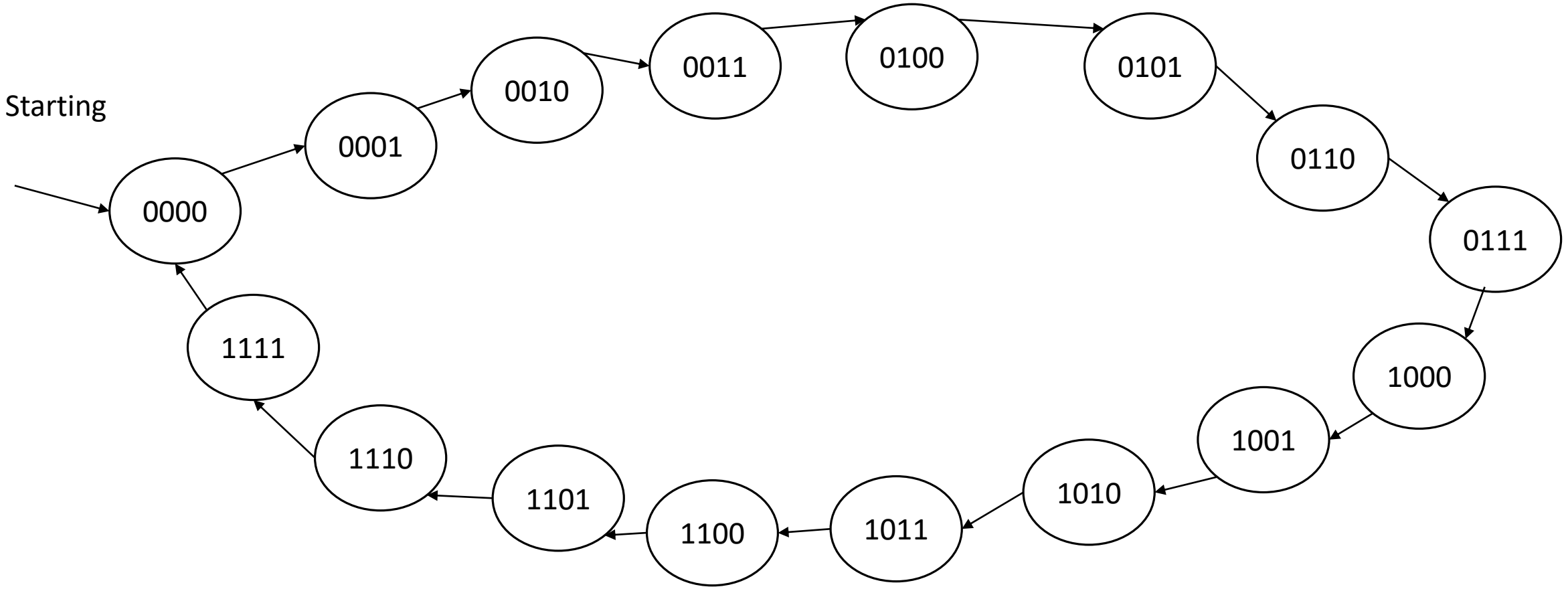
Select	Operation
00	Retain
01	Left to Right Shift
10	Right to left Shift
11	Parallel Load

Asynchronous – Ripple Counter (4 bit)

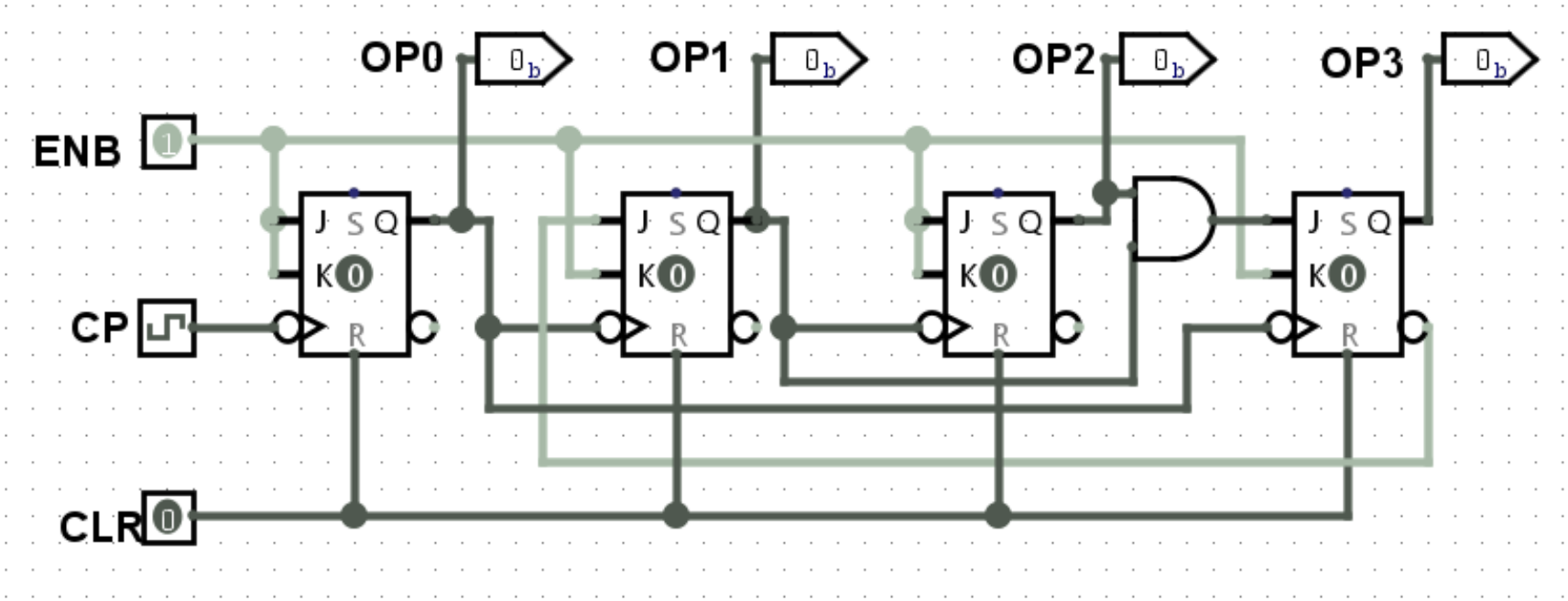


Note: JK FF should be negative-edge triggered

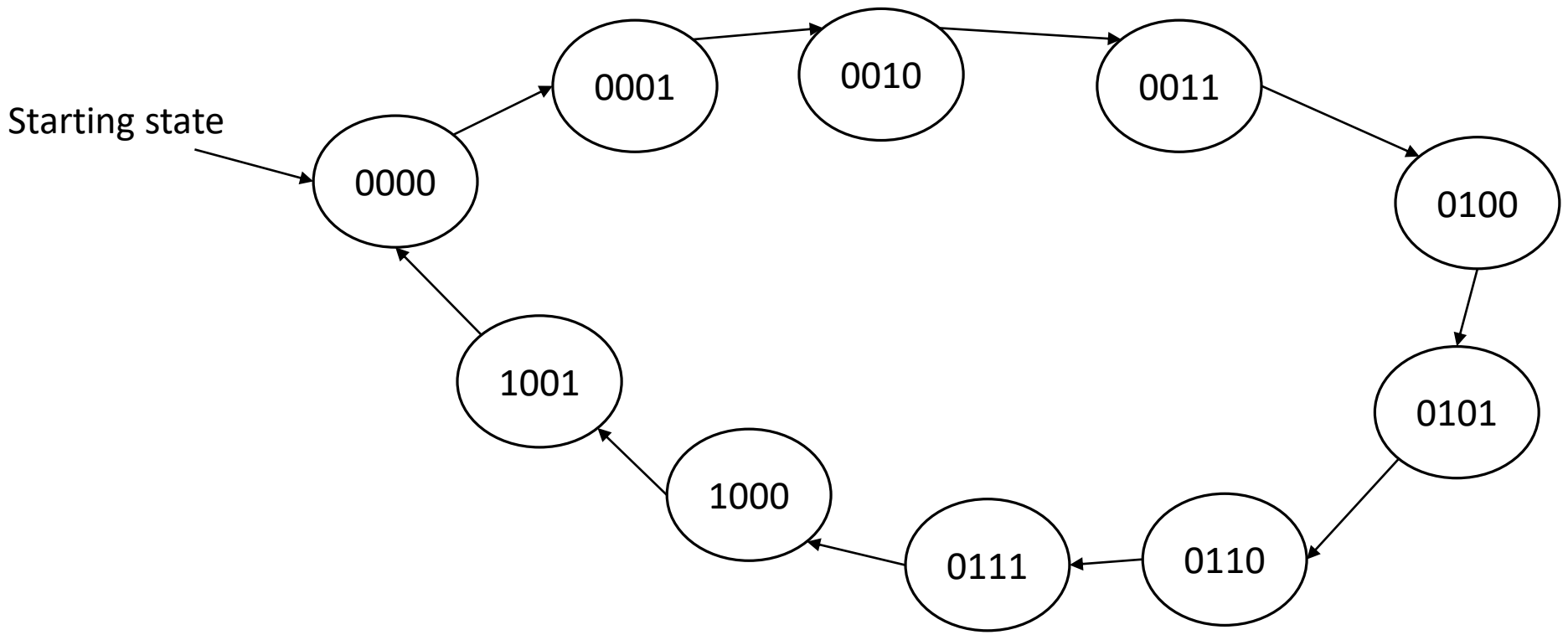
Asynchronous – Ripple (4 bit)



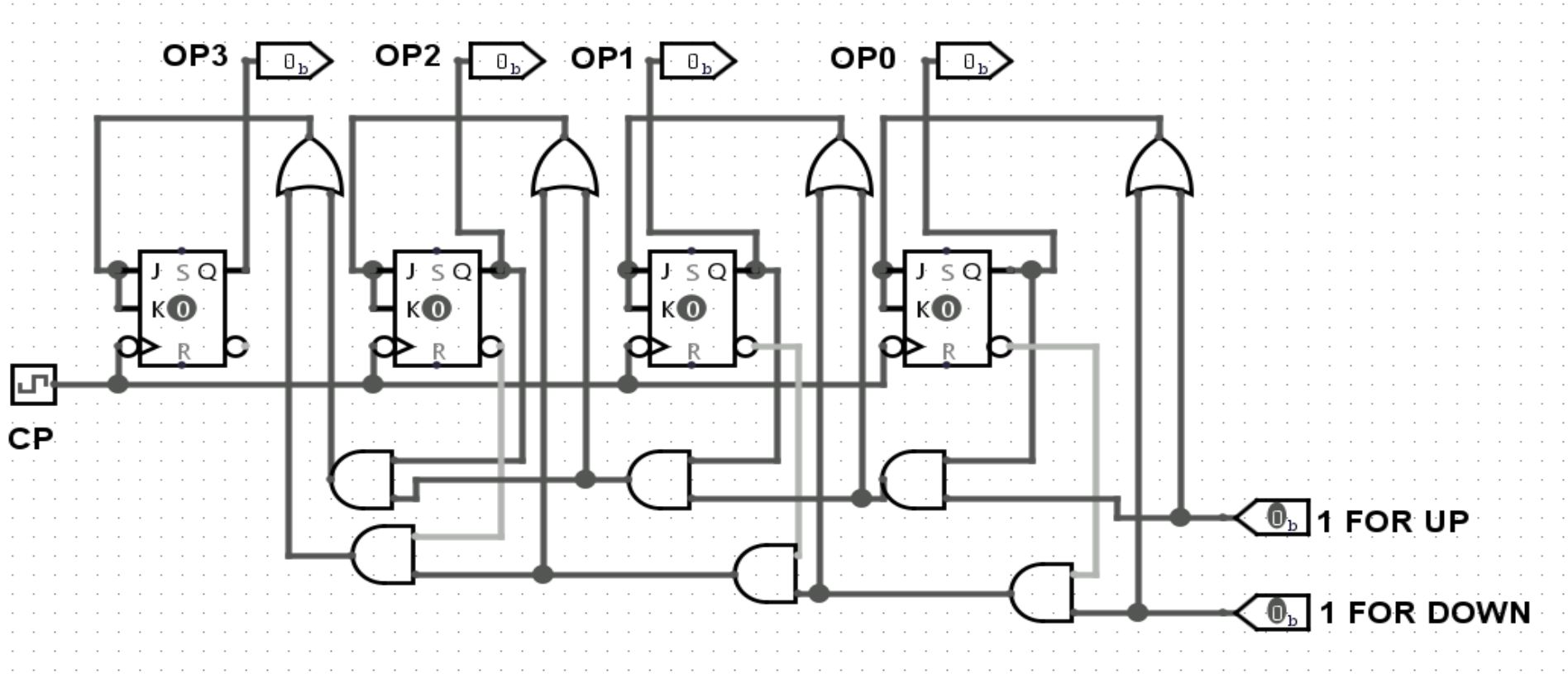
Asynchronous – BCD Counter (4 bit)



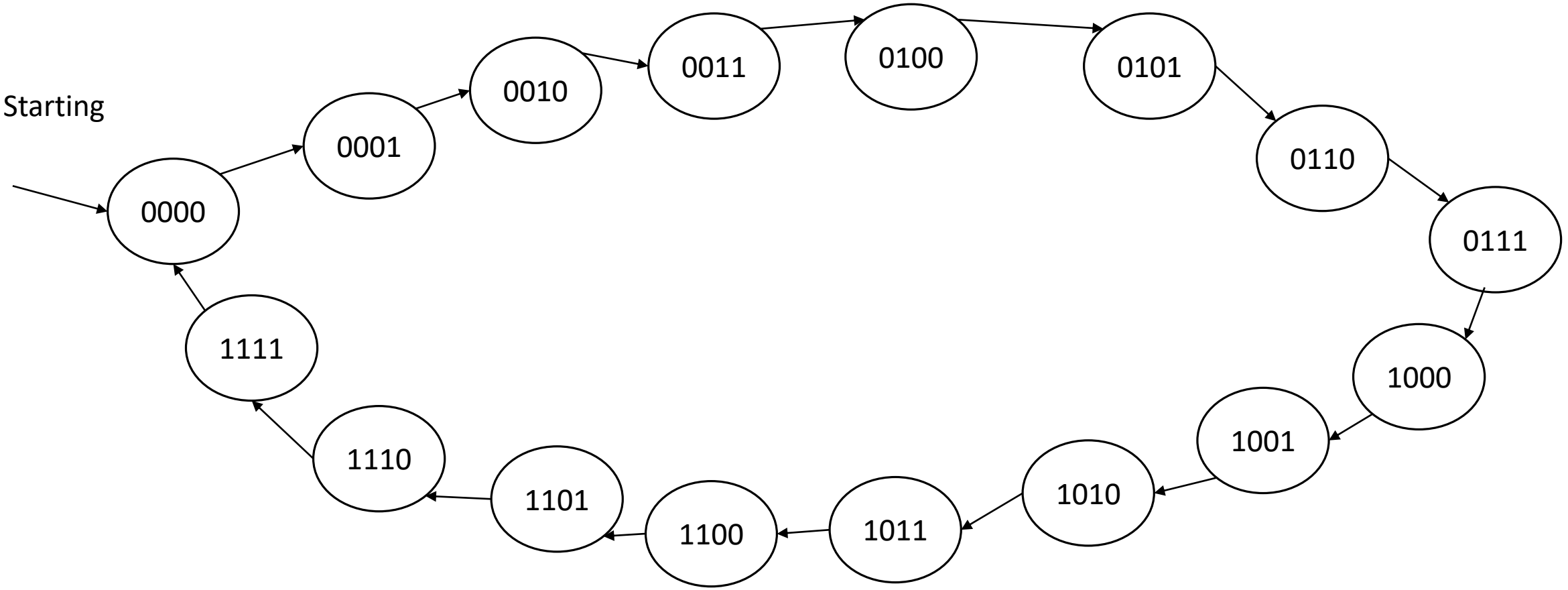
Asynchronous – BCD Counter (4 bit)



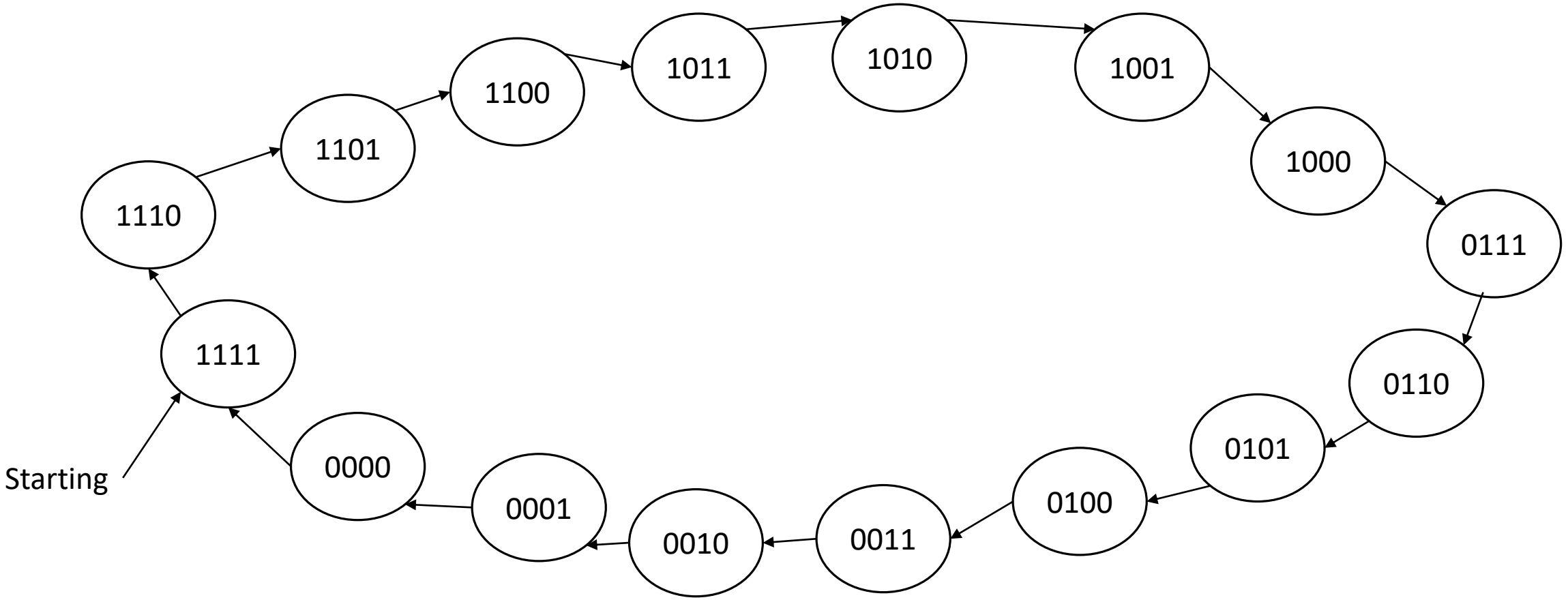
Synchronous – Up/Down Counter (4 bit)



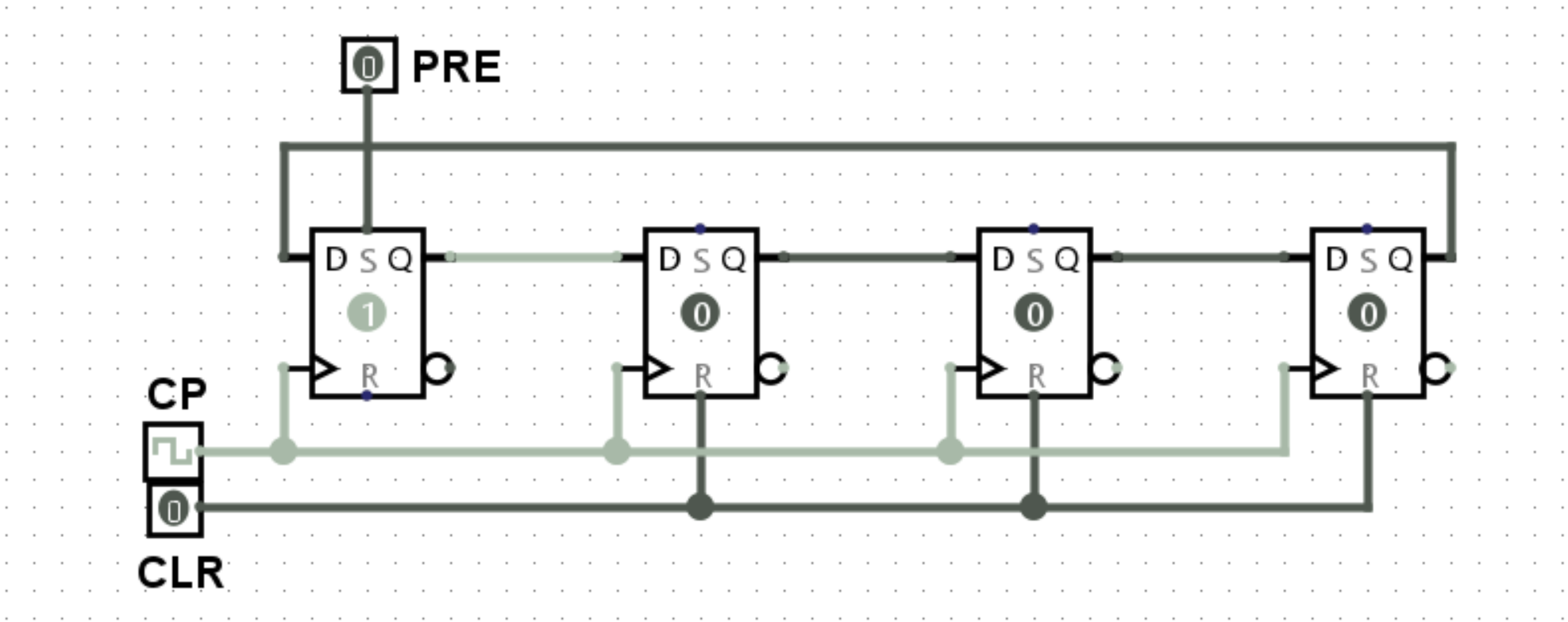
4-bit Up Counter



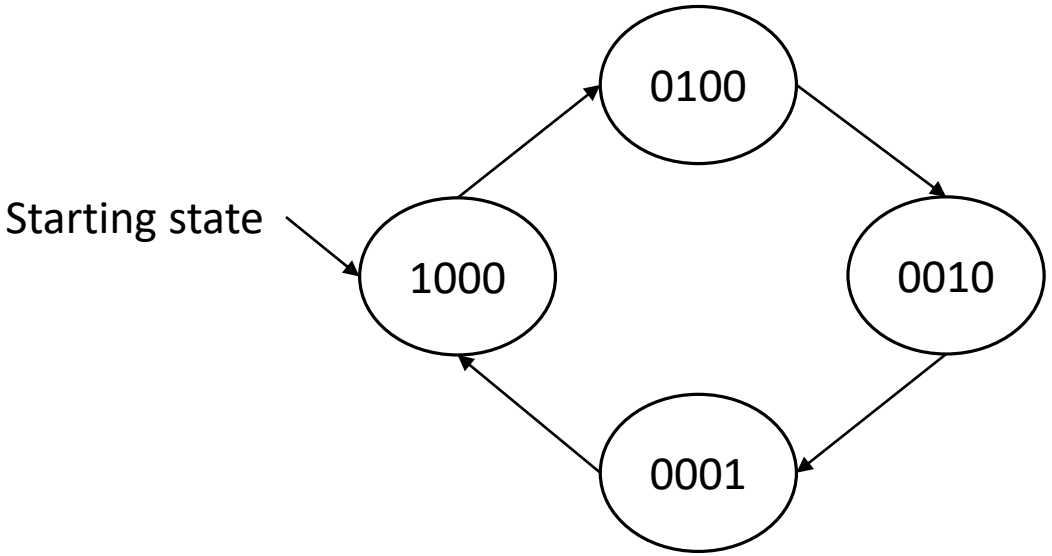
4-bit Down Counter



4-bit Ring Counter

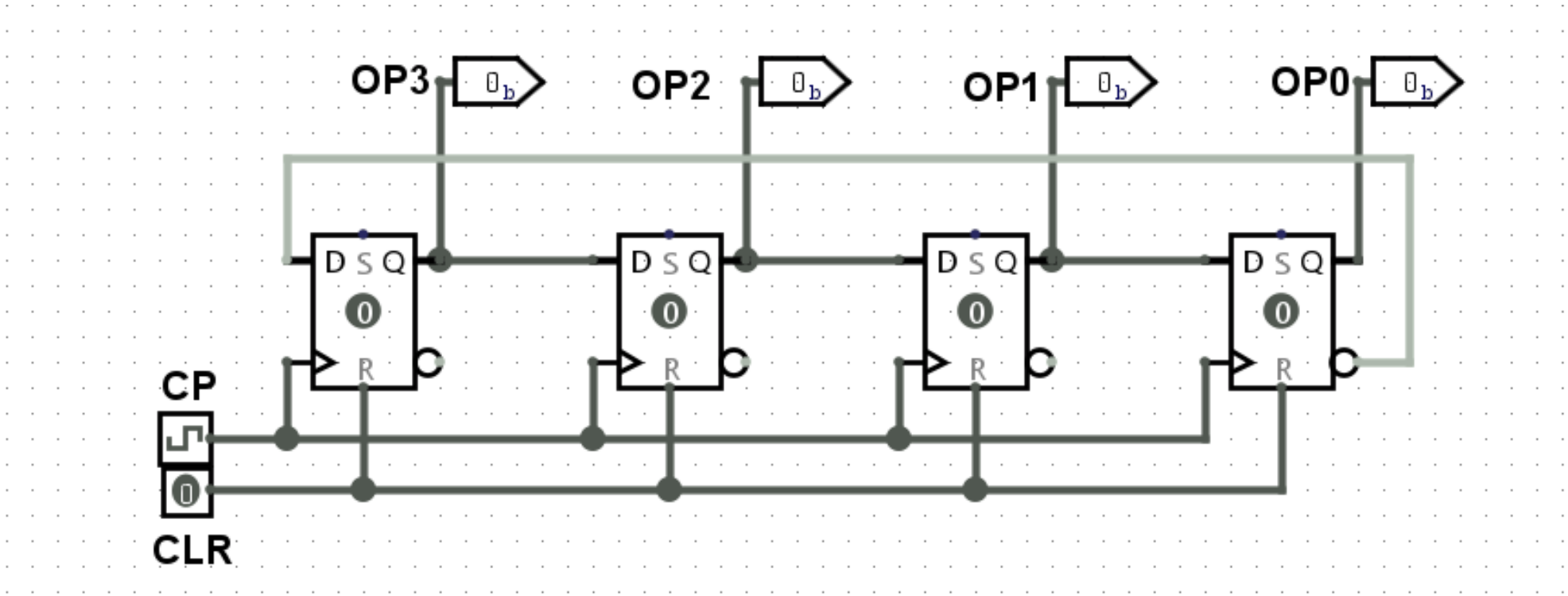


4-bit Ring Counter



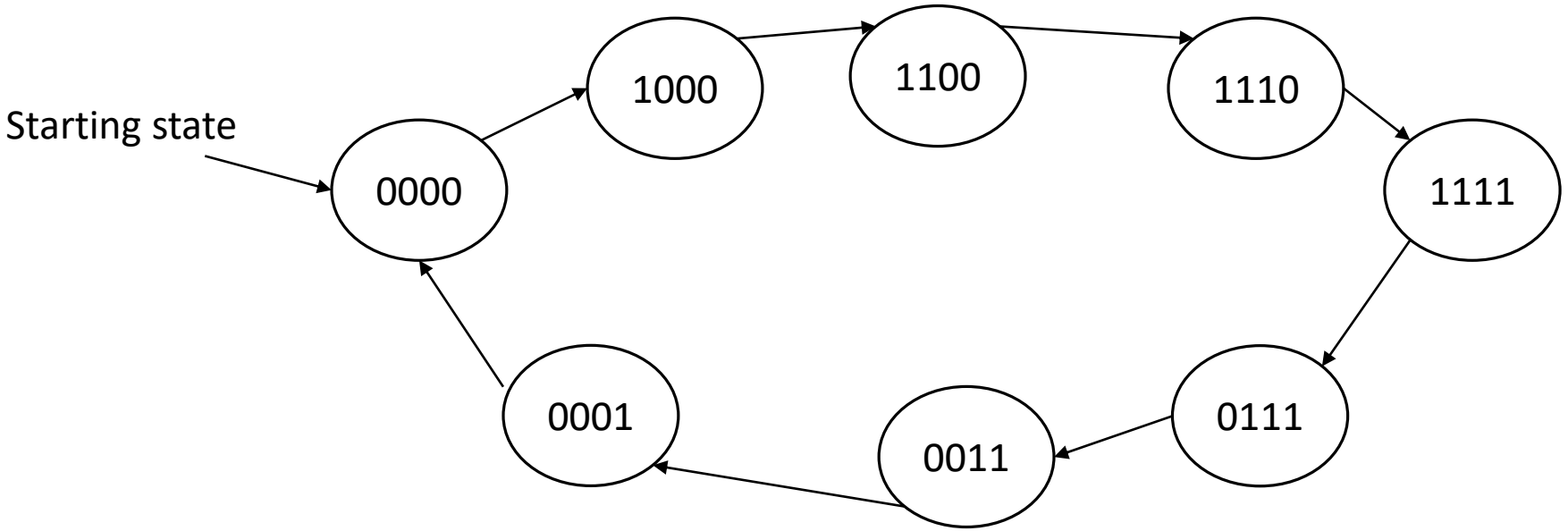
Number of states = Number of Flip-flops

4-bit Johnson Counter



Number of states = 2 * Number of Flip-flops

4-bit Johnson Counter



Number of states = 2 * Number of Flip-flops

Reference

Mano, M. Morris. *Digital logic and computer design*. Pearson Education India, 2017.