# Smart Locking System IC Design

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06-MARCH-2022

#### I. ABSTRACT

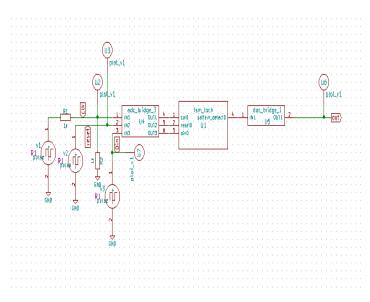
Abstract—This paper presents a design and implementation of a Smart Lock using Finite State Machine (FSM) as a digital block and some analog circuitry built around it. The mixed-mode simulation is also being done for the proposed system.

### Keywords—Finite State Machine (FSM), Clock Generator etc.

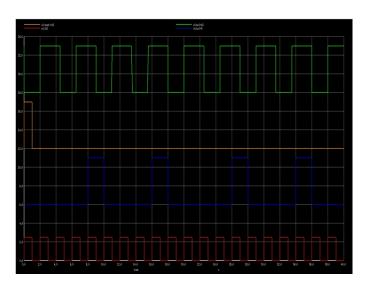
#### II. REFERENCE CIRCUIT DETAILS

The following paper focuses on the design of a smart lock. The design comprises of both analog as well as digital circuits. Finite state machine (FSM) is being used as a heart of this design. FSM here will act as sequence detector and will have a pre-loadesd pattern inside it for its output to go high. Only when the user gives correct input to our smart locking system (which matches with the preloaded sequence in the FSM) the lock will open otherwise it will remain closed. There will be a clock generating circuitry (analog in nature) which will provide clock to the FSM. The output of the FSM can be sceen as the LED glowing at the output side. The mixed-mode simulation of the proposed system will also be done and analyzed usingeSim (a free/libre and open source EDA tool for circuit design, simulation, analysis and PCB design. It is an integrated tool built using free/libre and open source software such as KiCad, Ngspice, Verilator, makerchip-app, sandpiper-saas and GHDL.

## III. REFERENCE CIRCUIT



#### IV. REFERENCE CIRCUIT WAVEFORM



V. REFERENCES

[1] https://www.circuitstoday.com/simple-electroniccombination-lock-using-ic-ls-7220