Analysis on Resistive Random Access Memory (RRAM) 1S1R Array

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I. Introduction

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Increasing dependence of the functionality and performance of computing system on the characteristics of the memory subsystem calls for further study on various memory technologies. Conventional memory technologies, such as SRAM, DRAM and FLASH, suffer from the formidable device scaling challenges, which makes researchers pay more attention to the emerging memories. Resistive Ramdom Access Memory (RRAM) is considered as one of the promising emerging memory candidates due to its simple structure, low switching voltage ($< 3V$), fast switching speed ($< 10ns$), excellent scalability ($< 10nm$) and good compatibility with the current CMOS technology.

However, a purely passive RRAM array suffers from intrinsic drawbacks such as parasitic leakage paths in un-selected cells and series resistance of the interconnects. They only limit the signal swing, which annihilates the advantage of the high density of the crossbar/3D structures by adding large sensing circuits and lowering the memory-array efficiency, but also reduce the maximum allowable array size. To resolve these issues, selection devices like diodes or transistors in series with the memory cell has been investigated. Among all those selection devices, two-terminal selection device (selector) are more attractive due to larger cell size ($> 8F^2$) of three-terminal transistors in series with RRAMs (1T1R) Array. Thus, in this project, we focus on diode type of two-terminal selection device RRAM (1S1R) Array, exploring the characteristics of diodes influences on 1S1R array programming performance.

We hope to estimate the array performance from selector characteristics before fabrication and simulation which will waste painful time and cost if the selector is not a good choice for that RRAM. Despite the popularity of applying machine learning in different fields, few researchers, either in machine learning or semiconductor domains, have used machine learning algorithms to predict devices effects in circuit/system. Here, we presented a new methodology to use features extracted from the diodes' characteristics to predict 1S1R array performances, saving the time and cost. Crossbar 1S1R arrays (Fig. 1) are analyzed to give an insight for 3D RRAM array (Fig. 2).

*The present work benefited from inputs of Yilong Geng, Shahar Kvatinsky, Prof. Shimeng Yu and Prof. H. -S. Philip Wong, who provided valuable comments and assistance to the undertaking of the project.

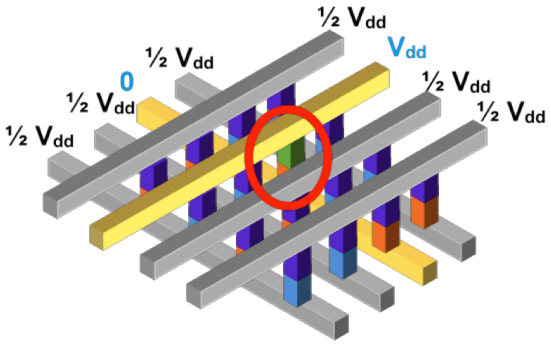

Fig.1, Crossbar array schematic under 12 bias scheme, in which one selected 1S1R cell is circled

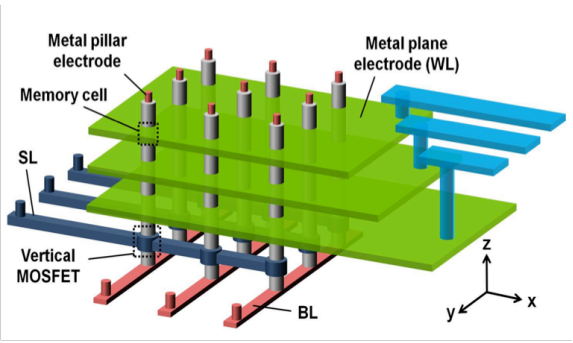

Fig.2, 3D array schematic

II. Methodology

II.A Features

A typical characteristics of diode selectors is shown in Fig. 3(a). We extract features of the curves from numeric modeling equation (1) of selector characteristics.

$$I = I_S \times e^{(V-V_S)/S_S} - I_R \times e^{(V-V_R)/S_R} \tag{1}$$

where I_S, IR is the saturation current, V_S, V_R is the dependence factor of current on voltage, and S_S, S_R is the dependence factor of current on voltage.
The equation is derived from normal diode equation (2). A diode selector work like two reversed-direction diodes in parallel shown as Fig.3(b). We can change I_S, V_S, S_S, I_R, V_R, and S_R to generate various of diode selector characteristics (Fig. 4).

$$I = I_b \times \left(e^{V/S} - 1\right) \tag{2}$$

We take I_S, V_S, S_S for the RRAM SET progress (Fig. 5) as the methodology demonstration, which we can adopt similarly on I_R, V_R, and S_R of the RESET part. (We call programming RRAM to low resistance state (LRS) as SET process, and to high resistance state (HRS) as RESET process). The ranges of features that we use to generate random feature values are shown in Table 1.

Table 1: *Ranges of Features on SET progress*

Feature	I_S	V_S	S_S
Range	$(10^{-10}, 10^{-3})$	$(0, 3)$	$(0, 5)$

II.B Targets

Using a RRAM compact model and different selector characteristics, we generate HSPICE circuit netlists of 1S1R crossbar array to simulate the minimum programming voltage of one 1S1R cell, and 1S1R array worst case write margin and write margin (Fig. 6). Those three numbers are key parameters we care in memory systems, which are our targets.

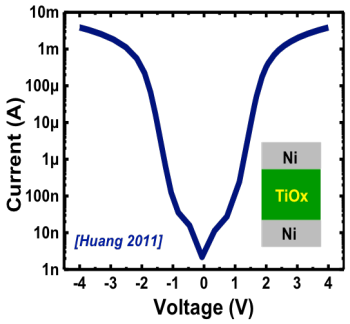

Fig.3(a), Diode selector experimental characteristics

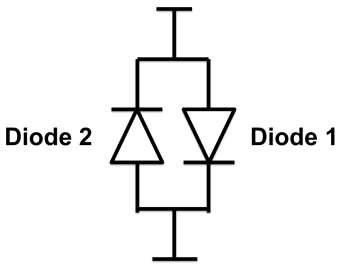

Fig.3(b), Circuit schematic of diode selector switching mechanism

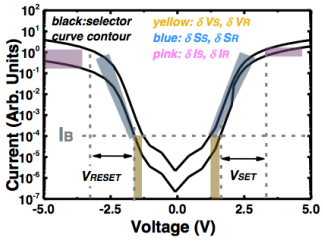

Fig.4, Various random generated selector characteristics range

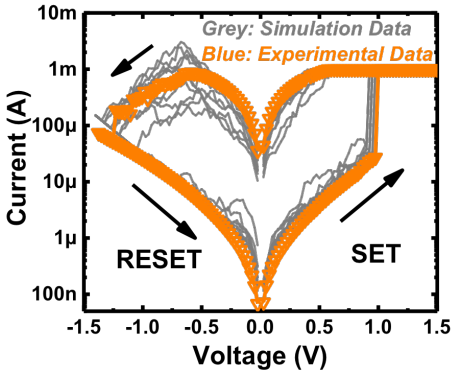

Fig.5, SET and RESET processes of RRAM

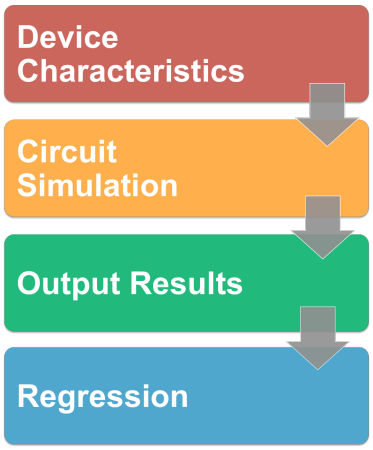

Fig.6, Simulation and Analysis Flow

II.C Processing

We simulate one 1S1R cell for Vmin and 4x4 (16 bits) 1S1R array for write margin and energy with 1000 random generated diode selectors. For each target, we randomly choose 800 samples as the training set and the remained 200 samples as the testing set.

Different regression algorithms, 'Linear', 'Near Neighbor', 'Support Vector Regression' and 'Decision Tree', are used to find out better regression methods on each data pattern.

III. Results and Discussion

We optimize different algorithms to give the smallest error. For example in 'Ada Boost', the least testing error is achieved at parameter n-estimators (the number of decision trees) = 90 and learning-rate (boosting parameter) = 1 (Fig. 7).

Among various algorithms, 'Ada Boost' gives best regression error (Table 2).

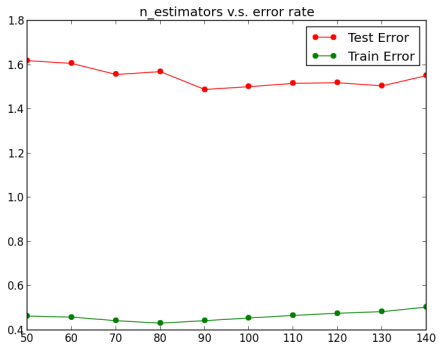

Fig.7(a), training error and testing error of 'Ada Boost' by changing parameter, n-estimator

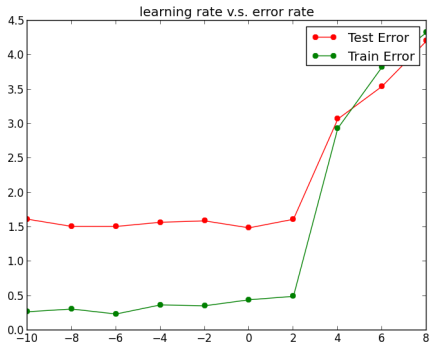

Fig.7(b), training error and testing error of 'Ada Boost' by changing parameter, learning-rate

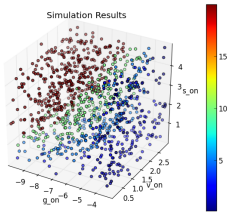

Fig.8, Vmin (V) simulation results from various selector characteristics

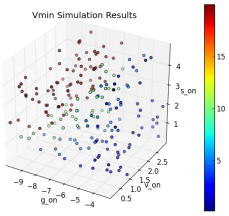

Fig.9(a), Simulation of Vmin from 'Ada Boost'

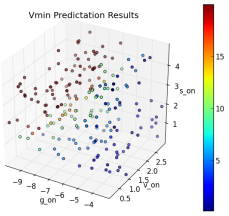

Fig.9(b), Prediction of Vmin from 'Ada Boost'

Table 2: *Different Regression Algorithms Error Analysis*

Vmin	Linear	Nearest Neighbor	Decision Tree	**Ada Boost**	SVR-rbf	SVR-linear	SVR-poly
Testing Error	3.79	4.58	2.28	**1.49**	1.77	3.78	3.17
Training Error	3.89	4.50	0.60	**0.44**	1.51	3.94	3.27

It is reasonable that 'Decision Tree' and 'Ada Boost' (a series of 'Decision Tree') provide better regression, which are piece-wise constant functions, matching the data pattern in (Fig. 8).

For 200 samples of the testing set, simulation result and prediction result from 'Ada Boost' are shown in Fig. 9. We can see 'Ada Boost' gives a good prediction on the minimum programming voltage (Vmin).

Similarly, we can use the approach to analyze data of 1S1R array write margin and write energy ($4x4$ bits array as an example in Fig. 10). Better regression algorithms can be achieved.

IV. Summary and Future Work

A methodology to predict 1S1R array performance is provided. We extract key parameters (I_S, V_S, S_S, I_R, V_R, and S_R) of diodes selector as features. Various of selector characteristics are adopted into HSPICE simulation in which the target parameters (Vmin, Write Margin and Write Energy) are measured. The experiment proves that using machine learning algorithms (like 'Ada Boost'

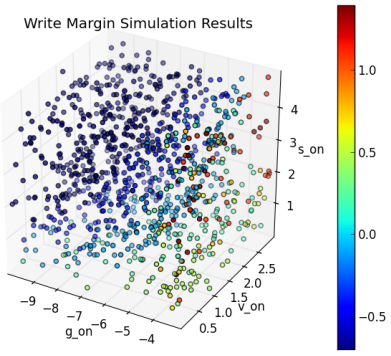

Fig.10(a), Simulation results of Write Margin, (WriteMargin > 0 ACCESSED, < 0 FAILED)

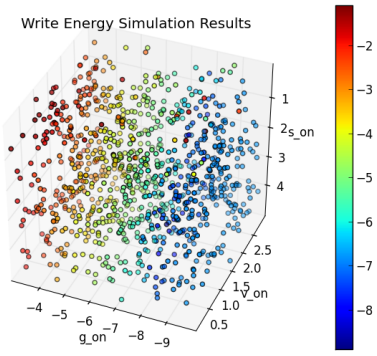

Fig.10(b), Simulation results of Write Energy, energy shown in log scale

or 'Nearest Neighbor'), we can successfully predict 1S1R array performance without fabrication and simulation.

The long-term goal of regression analysis is to predict larger array simulation by using smaller array simulation results since fabrication cost will increase exponentially along with array size and simulation will also take extremely long time. As example, with 800 samples from smaller arrays, we can use one machine learning algorithm to predict larger array (1024x1024) of 1000 selector curves within $1min$ much smaller than $2 \times 1000 = 2000\ hours \approx 83\ days$

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