Practical 3

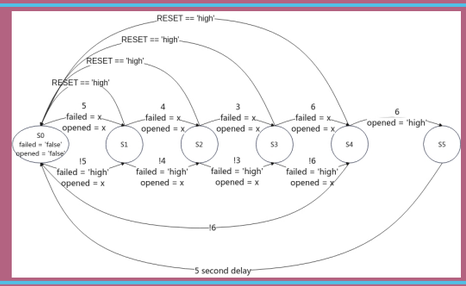
Functionality

English

A User interface that is capable of analysing a set count of numerical inputs. When all the numbers are input, the sequence is checked against an expected sequence, and if it passes - an output pin is enabled. Otherwise, an error is indicated, and the sequence resets.

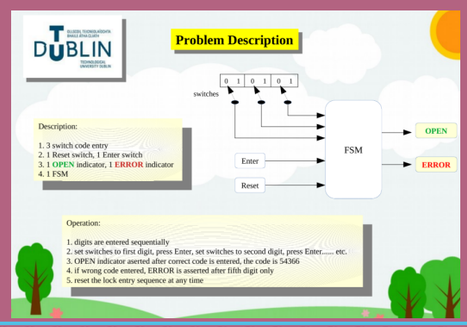
Diagrams

State Diagram



FSM Diagram

Reference



State Transition Diagram

		Inputs						Signal	Output
Description	Current State	b2	b1	b0	RESET	ENTER	Next State	failed	unlocked
RESET	ANY	x	x	x	1	RISE UP	S0	Set to 0	Set to 0
INPUT DIGIT 1 PASS	S0	1	0	1	0	RISE UP	S1		
INPUT DIGIT 1 FAIL	S0	!1	!0	!1	0	RISE UP	S1	Set to 1	
INPUT DIGIT 2 PASS	S1	1	0	0	0	RISE UP	S2		
INPUT DIGIT 2 FAIL	S1	!1	!0	!0	0	RISE UP	S2	Set to 1	
INPUT DIGIT 3 PASS	S2	0	1	1	0	RISE UP	S3		
INPUT DIGIT 3 FAIL	S2	!0	!1	!1	0	RISE UP	S3	Set to 1	
INPUT DIGIT 4 PASS	S3	1	1	0	0	RISE UP	S4		
INPUT DIGIT 4 FAIL	S3	!1	!1	!0	0	RISE UP	S4	Set to 1	
INPUT DIGIT 5 PASS	S4	1	1	0	0	RISE UP	S5		Set to 1
INPUT DIGIT 5 FAIL	S4	!1	!1	!1	0	RISE UP	S0		
RESET IN 5 SECONDS	S5	x	x	x	0	x	S0		Set to 0

Circuit Components

- D flip-flop
  - State count — 3 bits — ripple counter — mod 6 — 6 States
  - Boolean Failed — 1 bit — true/false

Encoded State Transition Diagram

Todo

Derive Logic expressions

Draw the circuit diagram

Write the VHDL for the components to be used (if not lib)

Write the VHDL code (structural style) for the FSm

Test/verify the operation (simulator)

Document

Generate presentation/report