Car Parking Management System

(Bi-Directional Counter using Laser Detection System)

Course Information: Digital Logic Design, Course Code: CE-221
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ABSTRACT

Car parking spaces often lack a real-time tracking mechanism to monitor the number of vehicles parked and the available slots. This results in inefficiencies such as over-parking, confusion, and wasted time. To address this, our system automates the counting process and provides immediate feedback using a buzzer and LED indicators when parking space is full.

Our project aimed to solve the problem of exhausting the car parking space in car parking facilities around us by digitally integrating a laser system with a counter circuit, we created a system to store/indicate the number of cars parked in a particular parking facility and how many more cars can be parked until the sensor goes off indicating the facility has reached its limit. This project involves designing and implementing a 4-bit digital counter system using a 74193 synchronous counter, combinational logic, and a 7-segment display. The circuit also integrates a buzzer and an LED indicator to signal specific logic conditions. The project addresses the problem of real-time counting and alert mechanisms in digital circuits, achieving this through a systematic methodology that includes logic circuit design, simulation, and testing.

Utilizing Proteus 8.13 Pro for simulation, the system demonstrates accurate counting, seamless logic transitions, and conditional alerts. Results align with the expected behavior, showcasing the design's reliability and practical applicability in digital systems.

PROJECT CODE OF CONDUCT:

It is certified that the work presented/proposed in this proposal will be performed by the group comprising of four members from FCSE, Computer Science major batch 33. The work is performed with the best of knowledge attained in the course CE-221 and CE-221L, while satisfying all the adequate requirements and would be submitted in due course of allotted time.

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INTRODUCTION

BACKGROUND

With increasing demand for parking spaces, there is a pressing need for real-time parking management systems. Manual counting and monitoring are inefficient and prone to errors, leading to over-parking and confusion. Digital systems provide a reliable and automated solution to these challenges.

OBJECTIVE

The goal of this project is to design a digital parking management system that can count vehicles entering and exiting a parking lot, display available slots, and alert when the lot reaches full capacity.

SCOPE

This project focuses on the development and simulation of a 4-bit digital counter system using combinational and sequential logic. It covers the design, simulation, and partial hardware implementation of the parking management system.

OVERVIEW

Addressing the issue of **exhausting car parking space** in parking facilities by digitally integrating a **laser detection system** with a counter circuit. The system is designed to track the number of cars parked in a facility, display the available parking slots, and trigger an alert when the facility reaches its maximum capacity. This project demonstrates a practical application of digital electronics by combining sequential and combinational logic to achieve real-time tracking and alerting. This report outlines the problem statement, design requirements, methodology, simulation results, and discussions on the challenges and outcomes.

METHODOLOGY

PROBLEM STATEMENT:

Car parking spaces often lack a real-time tracking mechanism to monitor the number of vehicles parked and the available slots. This results in inefficiencies such as over-parking, confusion, and wasted time. To address this, our system automates the counting process and provides immediate feedback using a buzzer and LED indicators when parking space is full.

DESIGN REQUIREMENTS:

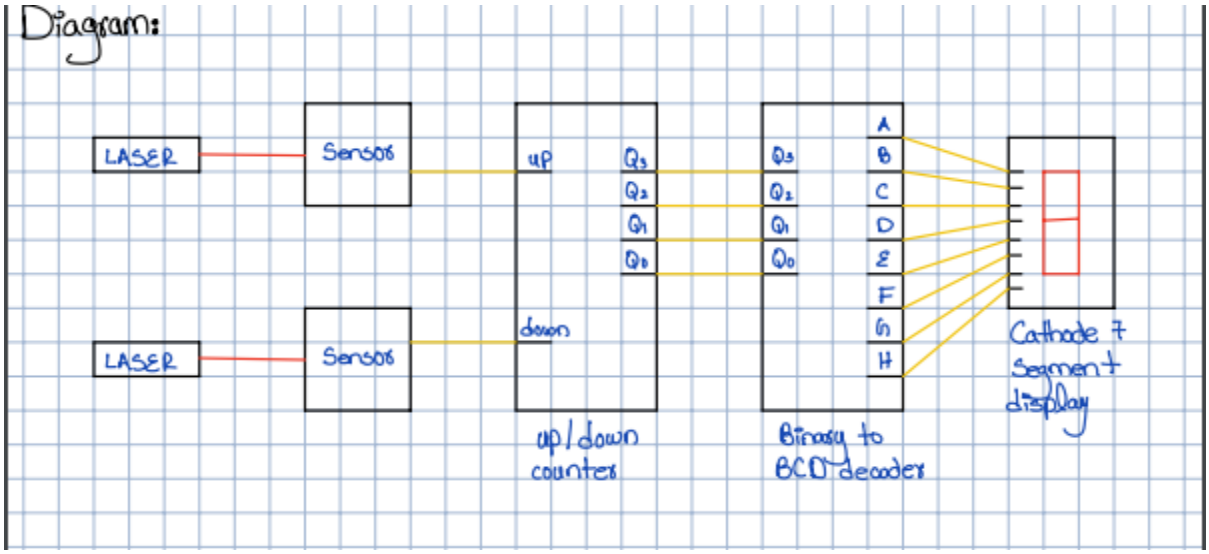
- **ICs Used:**
  - 74193: 4-bit binary synchronous counter
  - 7448: BCD to 7-segment decoder
  - 7404: NOT gate
  - 7411: AND gate
  - 7408: AND gate
  - 7432: OR gate
- **Output Devices:**
  - 7-segment display
  - LED (Red)
  - Buzzer
- **Power Supply:** 5V DC

DESIGN APPROACH:

- **Logic Design:**
  - The 74193 counter is used to increment or decrement based on inputs.
  - Outputs from the counter (Q0-Q3) are fed to the 7448 decoders for 7-segment display visualization.

- Specific logic conditions (e.g., maximum count) are handled using combinational gates (AND, OR, NOT).
- The LED lights up, and the buzzer activates under specific logic conditions defined by the combinational circuit i.e. after the threshold of ____ is reached which indicates the logic of the car parking facility reaching its maximum capacity.

- **Basic Logic Diagram**



- **Truth Tables and K-Maps:**

UP-COUNTER:

Up Counter

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	0	0	0	0	0	0	0	0

K-Maps:

D_3

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	0	X	X

$D_3 = Q_2Q_1Q_0 + Q_3\overline{Q_0}$

D_2

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	1
01	1	1	0	1
11	X	X	X	X
10	1	0	X	X

$D_2 = Q_1\overline{Q_0} + \overline{Q_1}Q_2 + Q_3\overline{Q_0}$

D_1

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

$D_1 = \overline{Q_3}\overline{Q_1}Q_0 + Q_1\overline{Q_0}$

D_0

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$D_0 = \overline{Q_0}$

DOWN-COUNTER:

Down Counter

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	D_3	D_2	D_1	D_0
0	0	0	0	1	0	0	1	1	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0	0	0	1	0
0	1	0	0	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	0	0	1	0	0
0	1	1	0	0	1	0	1	0	1	0	1
0	1	1	1	0	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	0	1	1	1
1	0	0	1	1	0	0	0	1	0	0	0

K-Maps:

D_3

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	X	X	X	X
10	0	1	X	X

$D_3 = \overline{Q}_3\overline{Q}_2\overline{Q}_1\overline{Q}_0 + Q_3Q_0$

D_2

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	0	X	X

$D_2 = Q_3Q_1 + Q_2Q_0 + Q_2Q_1$

D_1

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

$D_1 = Q_3\overline{Q}_0 + Q_1Q_0 + Q_2\overline{Q}_1\overline{Q}_0$

D_0

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$D_0 = \overline{Q}_0$

TOOLS AND TECHNOLOGIES:

Software:

Proteus 8.13 Pro for circuit simulation

Hardware:

Note: LEDS and Buzzer were components added to make the system responsive.

Table 1: Required components and specifications.

Component	Specification
Laser Sensors	Laser diode module (650nm, 5mW) with photodetectors (LDRs or phototransistors).
Logic Gates	ICs like 7408 (AND), 7432 (OR), 7404 (NOT).
Decoder	7448 IC
Up/Down Counter	74193 or similar 4-bit binary up/down counter IC.
Display Driver IC	7447 or 7448 BCD to 7-segment display driver.
7-Segment Display	Common anode or common cathode 7-segment display.
Resistors	For current limiting and pull-up purposes (e.g., 330Ω for display, 10kΩ for pull-up).
Capacitors	Decoupling capacitors (0.1µF) and noise filtering capacitors for sensor circuits.
Power Supply	Regulated 5V DC power source (battery or adapter).
Breadboard/PCB	For prototyping and assembling the circuit.
Cables/Connectors	Jumper wires and connectors for circuit assembly.
Time IC	x2 555 Time IC

IMPLEMENTATION

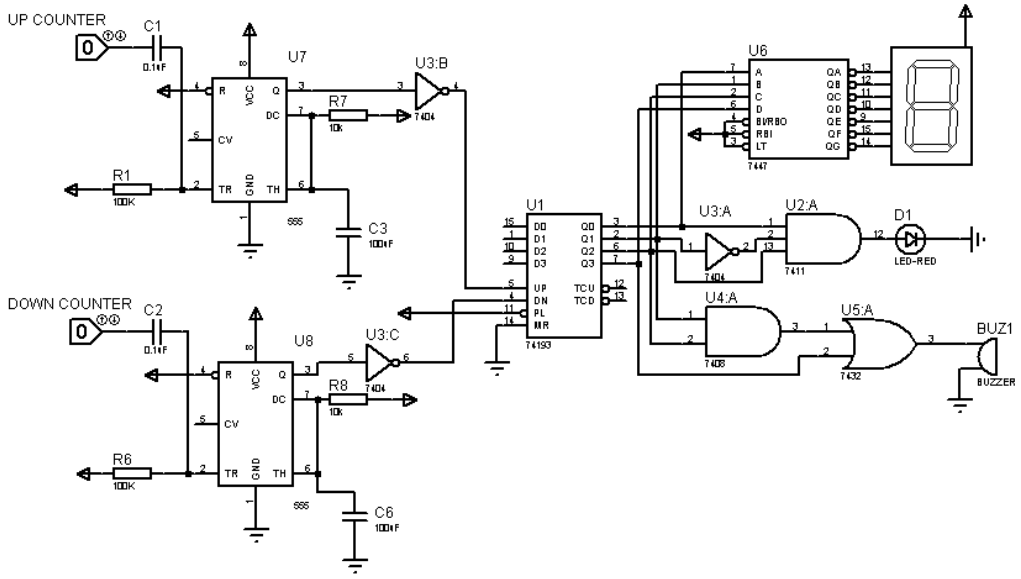
Simulation:

In our simulation, we have designed a digital counter system using a 4-bit binary up/down counter (74193), logic gates, a 7-segment display decoder (7447), and a combination of input switches, LEDs, and a buzzer. The 74193 IC acts as the main counter, with inputs for up and down counting controlled by two 555 timers configured as input pulse generators. The output from the counter (Q0-Q3) is connected to the 7447 decoders, which translates the binary output into signals suitable for driving a 7-segment display, allowing us to visualize the current count. Additional logic gates (7404, 7408, 7411, and 7432) are used to manage conditional outputs: one for lighting an LED when specific conditions are met and another to activate a buzzer, signaling a special event such as an overflow or a predefined count. The interconnections between these components create a fully functional and robust counting and signaling system.

The circuit was simulated in Proteus 8.13 Pro to verify the logic functionality.

- Key results include:
    - Accurate increment/decrement of the 7-segment display
    - Activation of LED and buzzer at predefined logic conditions
    - Accurate detection of object passing by sensor to increment/decrement counter Logic.
    - Accurately setting an upper bound limit to the counter IC to activate the LED and Buzzer Logic accordingly.

Note: It is to note that the Light Detection Sensor implementation has been done directly at hardware and not at the Proteus Simulation to avoid Fatal and Logical errors in the software-based Implementation.



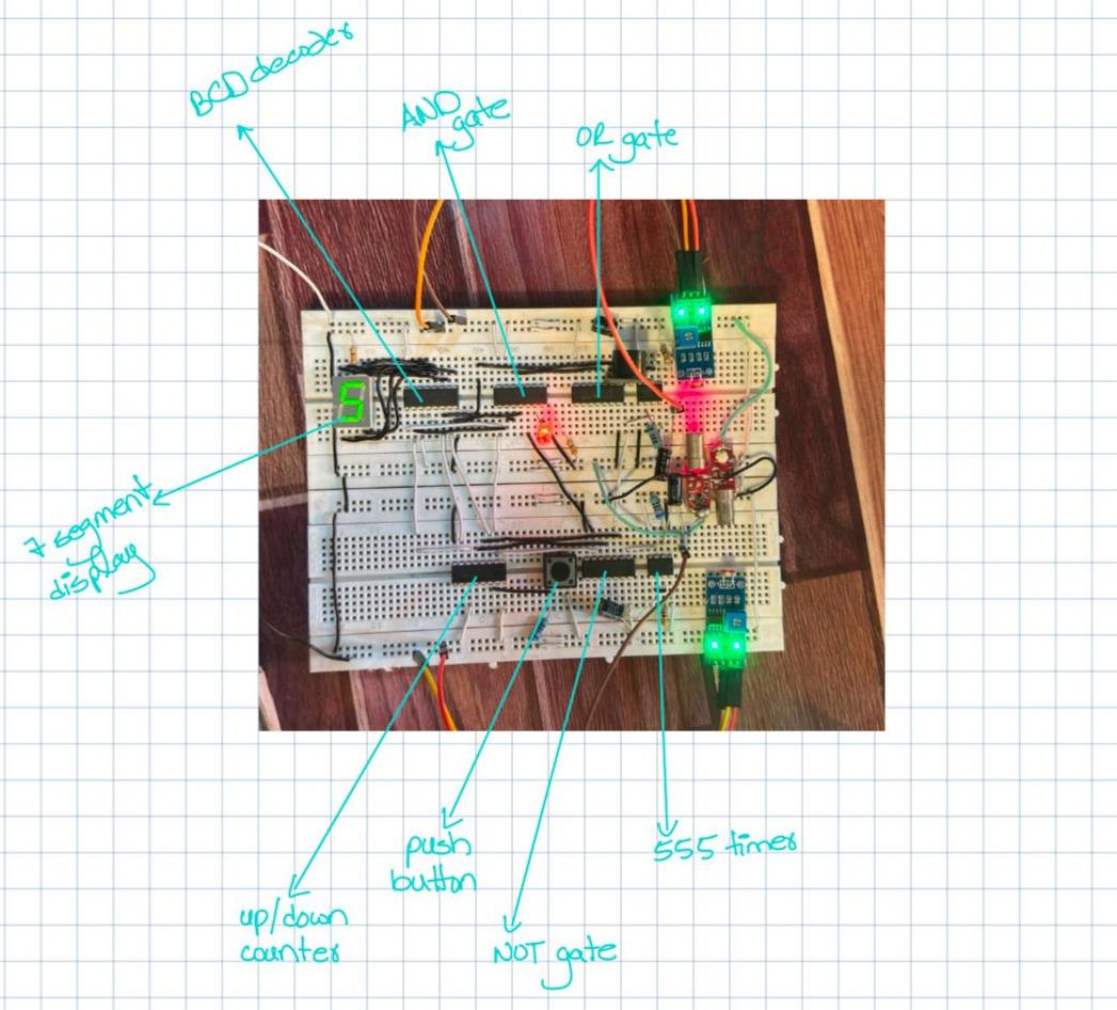
Hardware Implementation:

To implement this design in hardware, we would begin with a breadboard or PCB to assemble all the components. The 74193 IC would serve as the primary up/down counter, connected to two separate 555 timers configured as debounced input triggers for counting up and down. The 7447 BCD-to-7-segment decoder would be used to drive the common anode 7-segment display. Logic gates (AND, OR, NOT) would be connected as per the schematic to handle additional conditions, such as triggering the red LED and buzzer upon specific counts or overflow conditions. For outputs, a red LED with a current-limiting resistor and a piezo buzzer would provide visual and audio feedback. Power would be supplied using a regulated DC source, ensuring stable operation of all ICs and components. Wiring and

connections would be verified using jumper wires, ensuring the up/down counting logic, display, and signaling functionality work seamlessly as per the circuit design.

Summarizing the key points below:

- A 5V DC power supply was used, with pull-up/pull-down resistors to stabilize inputs.
- Logical outputs for LED and buzzer were verified against expected conditions.
- Outputs of the Counter using Light Detection Sensor being fed into the decoder to be properly displayed in the 7-segment display.



RESULTS AND DISCUSSION

Results:

- The counter increments/decrements accurately, displaying output on the 7-segment display.
- The LED and buzzer activate only at the predefined logic states.
- The simulation accurately displayed the count of vehicles on the 7-segment display and triggered alerts when capacity was reached.
- The hardware prototype demonstrated reliable counting and alerting functionality.

Comparison:

- Simulated and practical hardware results were consistent with negligible deviations due to voltage drops or resistor tolerances.

  Expected Results: Theoretical predictions showed accurate counting and seamless alert activation.

  Actual Results: The system aligned with expectations, validating the design and implementation.

Challenges:

During the implementation of the project, several challenges were encountered that required troubleshooting and additional learning:

1. **Counter IC Selection:** Initially, the 74LS192 asynchronous counter was considered. However, it failed to meet the project requirements due to its asynchronous behavior. Transitioning to the 74193 synchronous counters required understanding the IC's detailed documentation, which was a steep learning curve.
2. **Voltage Regulation:** Some components were incompatible with direct low or high voltage levels. To ensure proper functionality and prevent damage, additional components like resistors were integrated into the circuit, demanding careful voltage calculations.

3. **Circuit Organization:** Given the complexity of the project, maintaining a neat and logical structure was a significant challenge. Managing multiple connections, components, and wiring required meticulous planning and constant adjustments to avoid errors and ensure reliability.
4. **Uncoherent Results:** Proteus usually puts many input states pre-defined as either High or Low without enquiring the user about these minor details, which eventually go un-noticed and thus the user may not be able to implement the whole project just by replicating the simulation, therefore it was important to read out the description of the particular ICs like the counter IC to avoid such errors in hardware implementations.
5. **Using 555 timer IC instead of Basic Logic states:**

   In our project, using the 555 timer was essential to ensure seamless transitions in our counter ICs. The input signal from the laser could be unstable or fluctuate rapidly, which risked causing the counter to miscount or skip numbers. The 555-timer addressed this by converting the potentially noisy input into a clean, stable signal, effectively eliminating any fast, unwanted changes. It also introduced a debounce effect, ensuring that even if the laser was quickly blocked or unblocked, only one clean pulse was sent to the counter for each event. This not only prevented miscounting but also maintained the accuracy and reliability of the counting process, making it a critical component for the success of our project.

These challenges provided valuable learning experiences and contributed to the overall success of the project by strengthening problem-solving skills and deepening the understanding of digital systems.