

Characteristic table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

The next state always mirrors the D-flipflop.

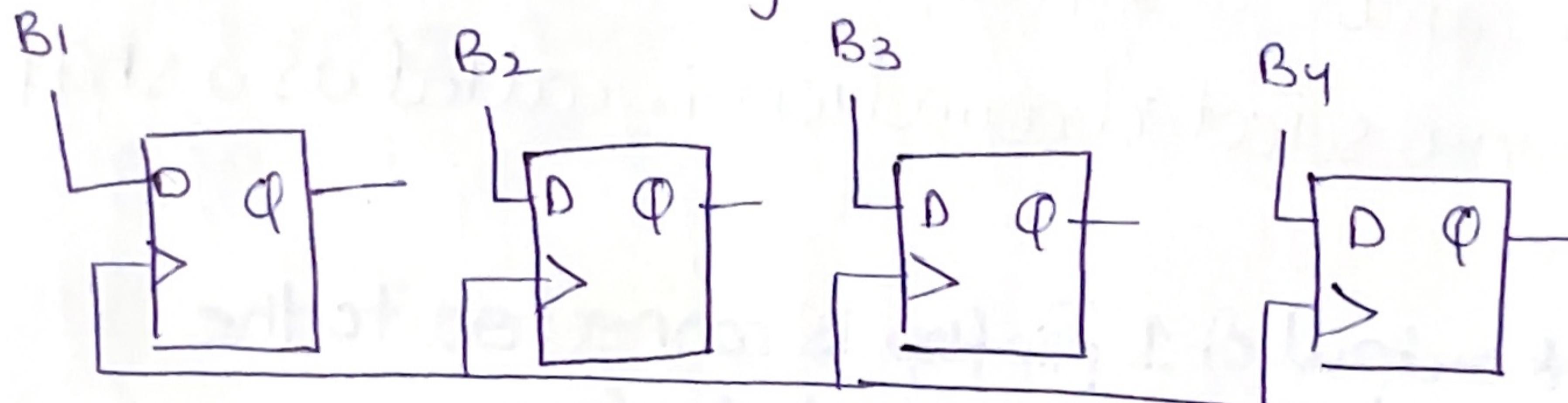
Chapter no.8.

flipflops can store only 1 Bit, in order to store multiple bits of data we use registers (combination of flipflops).

In register usually D-flipflops are used because whatever the input is given to a D-flip flop it is stored in it in the clock transition.

Registers:-

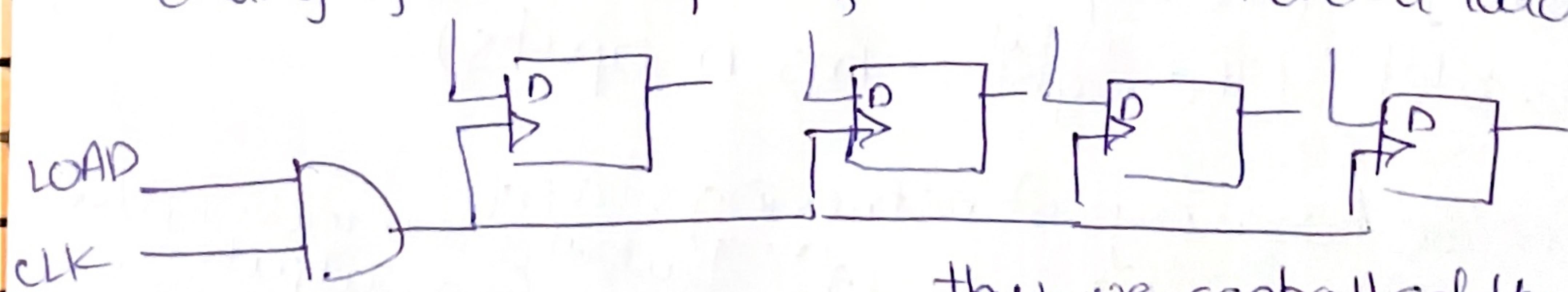
Consider a 4-Bit Register.



Limitations:-

solution 1

Sometimes we would want to load data into the register for a particular amount of time, rather than changing at clock pulse; thus we can add a load.

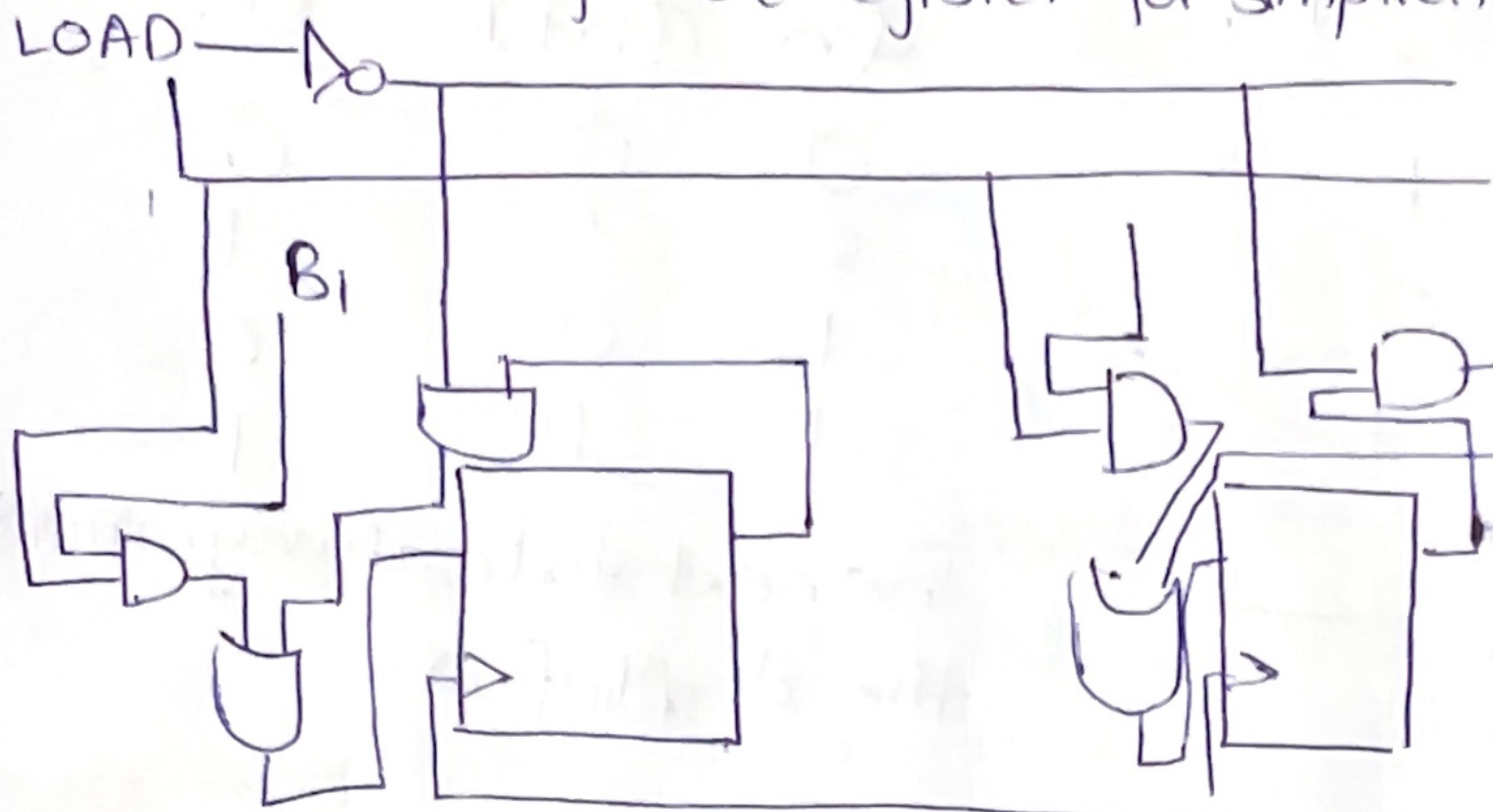


thus we controlled the clock pulse.

however this approach is not preferred in sync systems.

Rather than controlling the clock we will control them

(Now considering 2 Bit Register for simplicity)



and soon for
n-bits of Registers.

if new load

AND load with input (B_1/B_2)
to give new

if no load

AND not load with
previous to maintain.

(Give both of them into OR).

Shift Register :-

A register capable of shifting the data b/w the neighbouring flipflops in a selected direction is called as a shift register.

* output of 1 flipflop is connected to the input of the next flipflop.

There are two ways of loading data.
(i) Serially (the register has 1 input).
(ii) Parallel. (the register has n inputs).

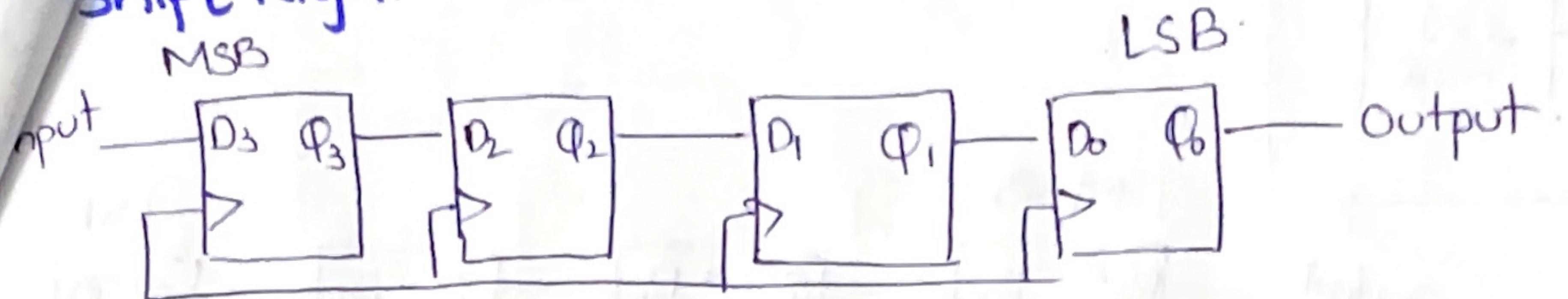
There is/are two ways of retrieving data

(i) serially (1 output) → 1 output access in every clock from outputs.
(ii) parallel (the all output can be achieved through 1 CLK)

3 4 types of Shift Registers.

Serial In Serial Out Register.

Shift Right SISO:-



Suppose we want to input 1010 into the shift right reg.
↓
start from here.

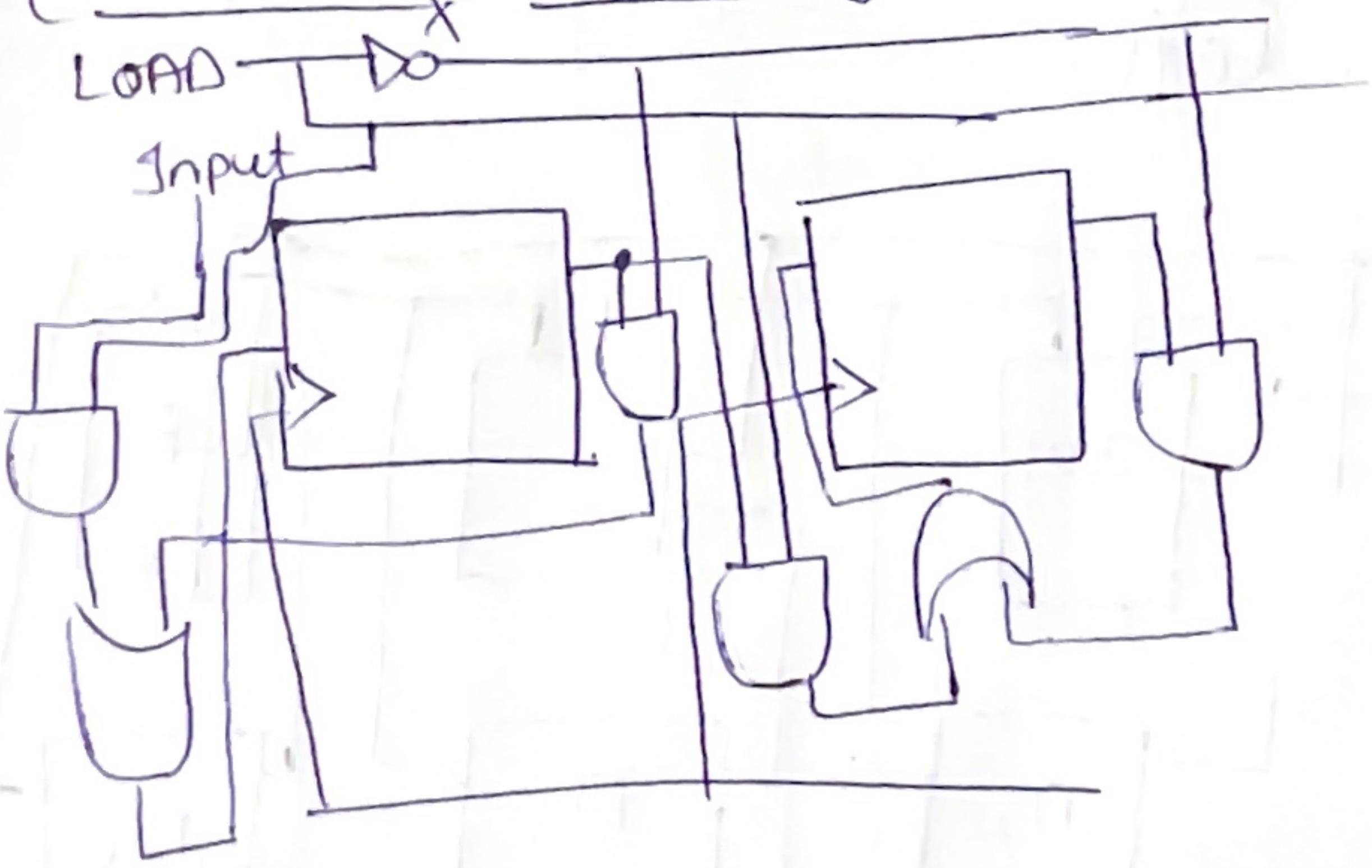
CLK	INPUT	D ₃	D ₂	D ₁	D ₀	
0	X	0	0	0	0	
↑	0	0	0	0	0	1st clock
↑	1	1	0	0	0	2nd clock
↑	0	0	1	0	0	3rd clock
↑	1	1	0	1	0	4th clock

Similarly 4 clk required to move the data outside.

LIMITATION

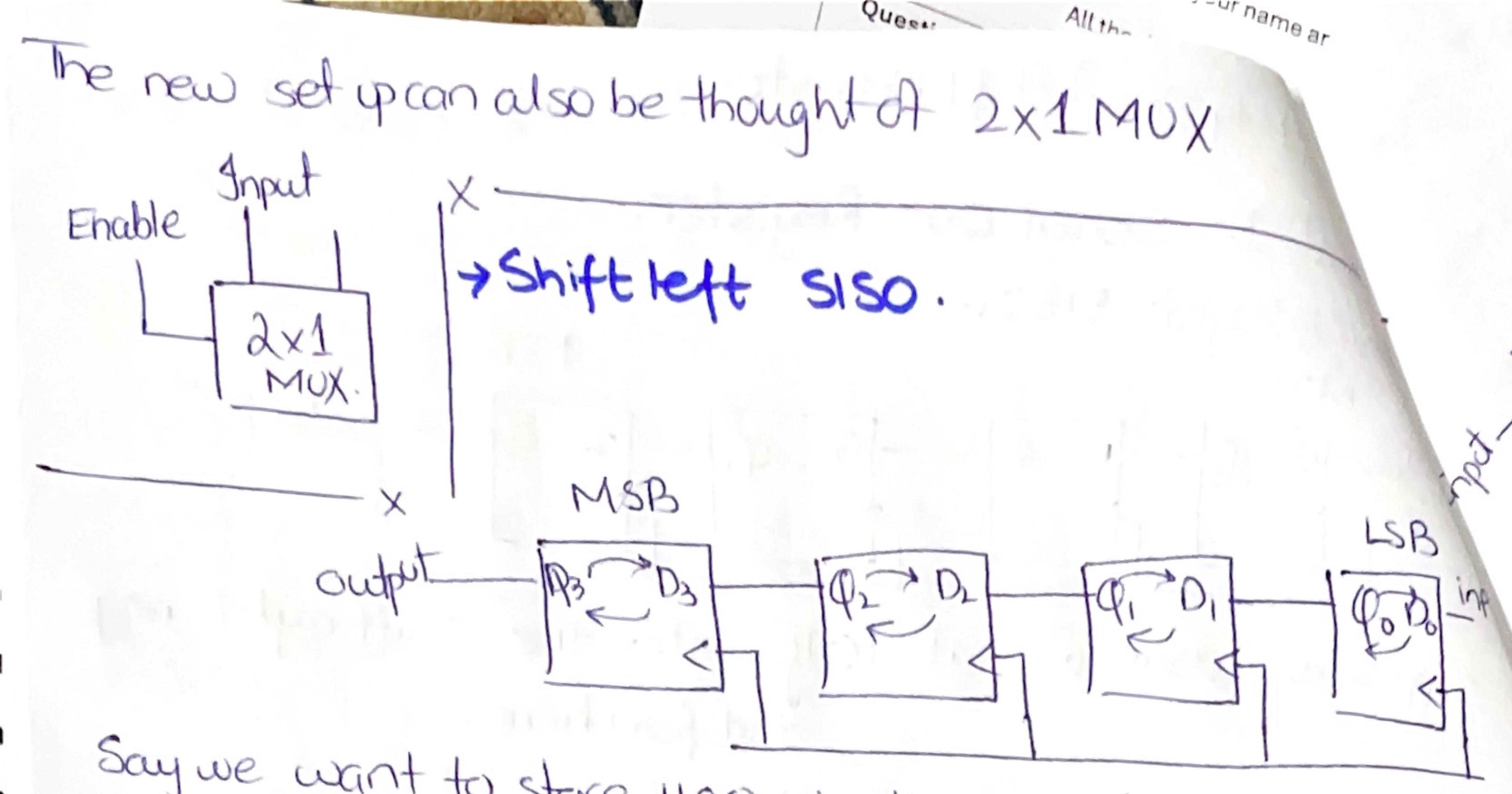
After all the data is input into the SISO we need to block the input line, thus we make adjustments.

(Consider 2 Bit Register)



Basic idea
you connect
D of load with previous
(using AND)

and Direct load with
input (using AND) for
first and output of prev
for 2nd and so on
flip flop



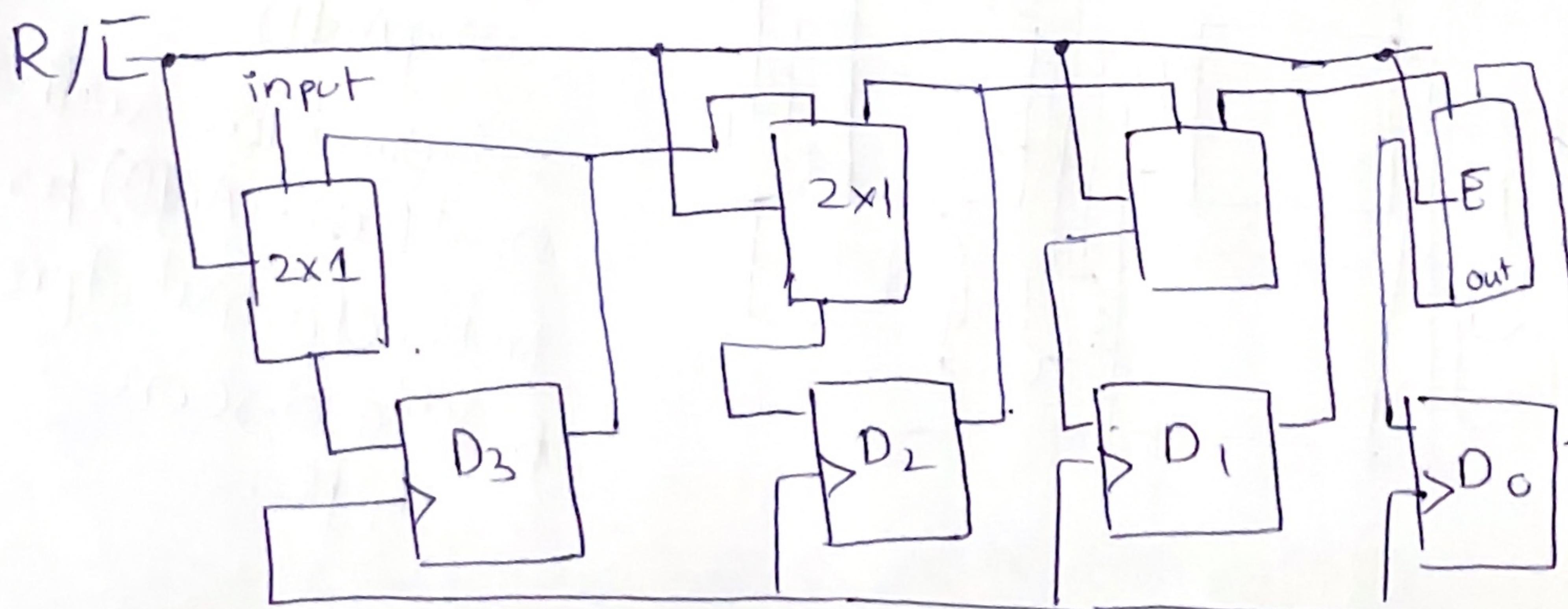
Say we want to store 1100 in this register.
We start from left. \rightarrow

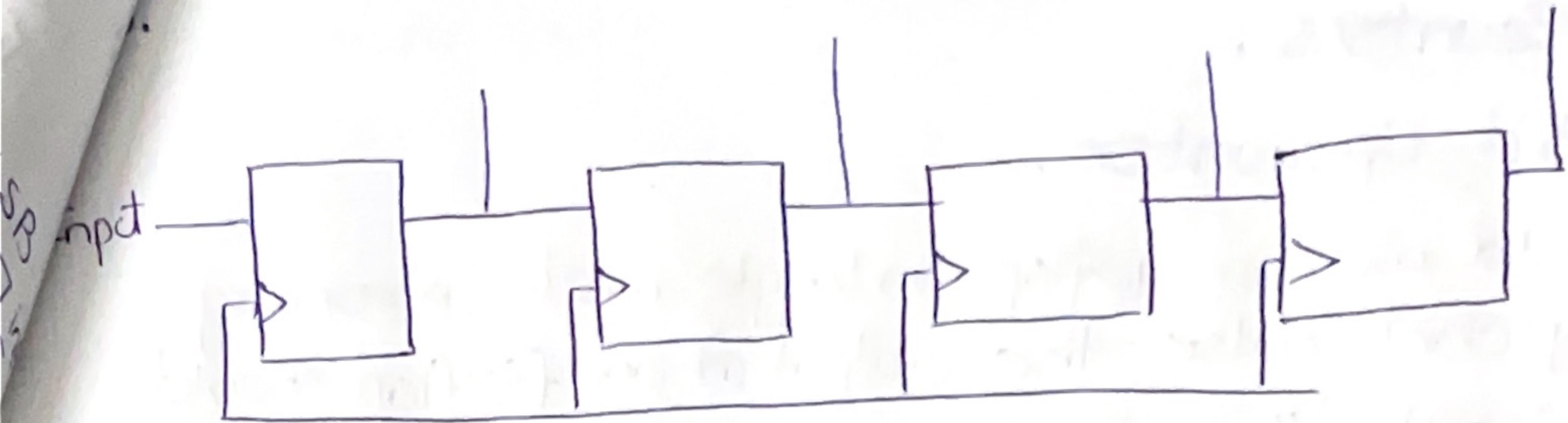
CLK	INPUT	D ₀	Q ₁	Q ₂	Q ₃
0	X	0	0	0	0
\uparrow	1	1	0	0	0
\uparrow	1	1	1	0	0
\uparrow	0	0	1	1	0
0	0	0	0	1	1

This portrays the idea of time delay let for an n bit shift register, after n clock pulse the input Bit is equal to output Bit.

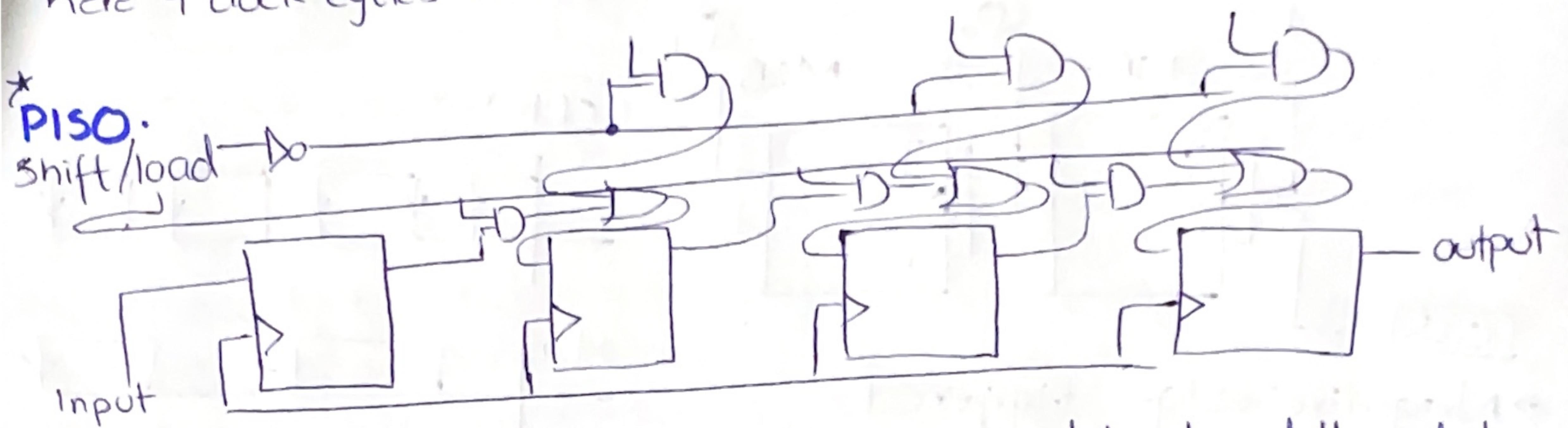
* BIDIRECTIONAL SHIFT REGISTERS

For Arithmetic operations we may require to shift the data to the right or left.



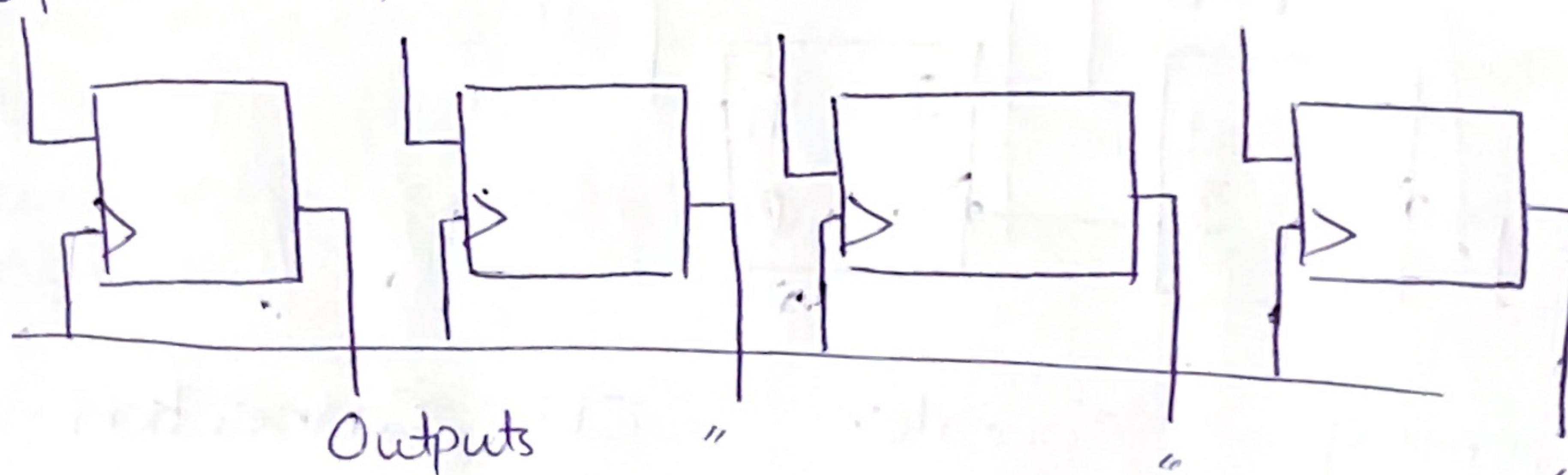


here 4 clock cycles would be needed to store a 4 Bit input.



here only 1 clock cycle would be required to load the data.
and $(n-1)$ more clock cycles to move loaded data out.

PIPO: Inputs

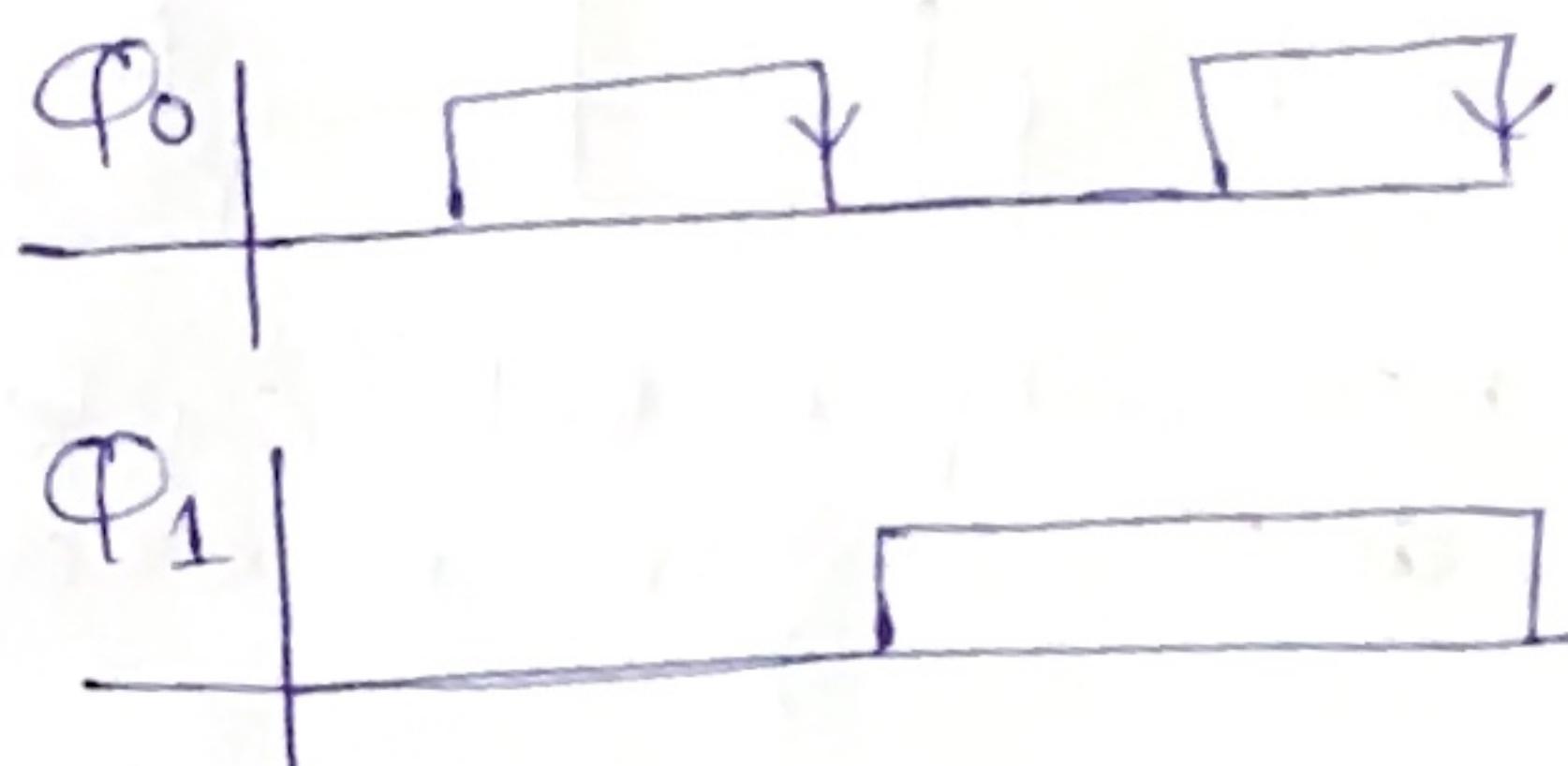
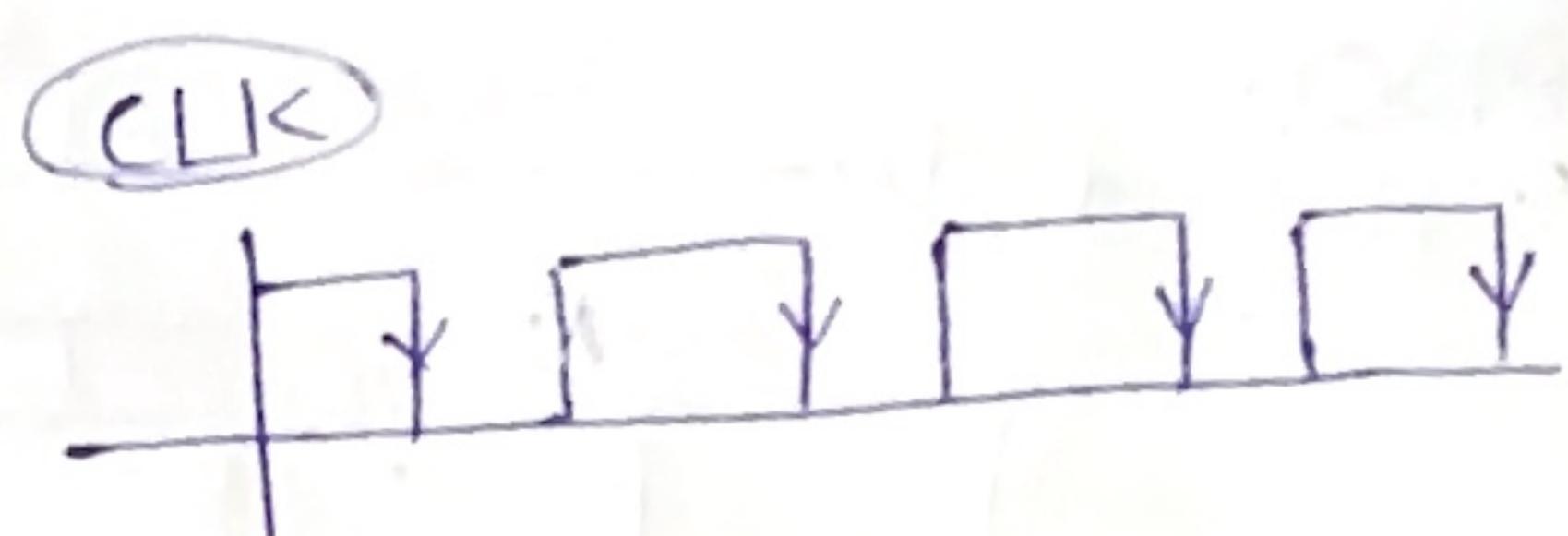
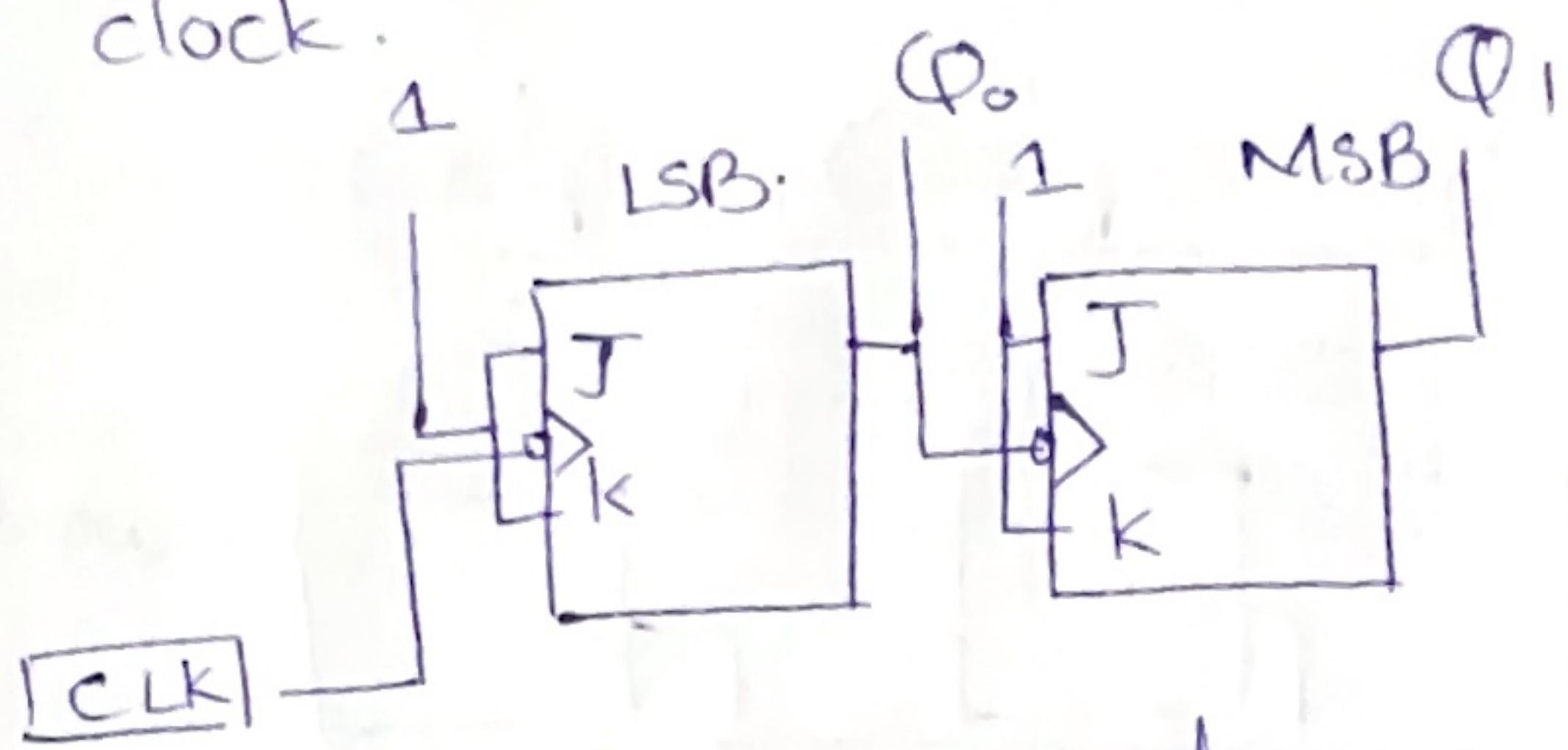


Counters.

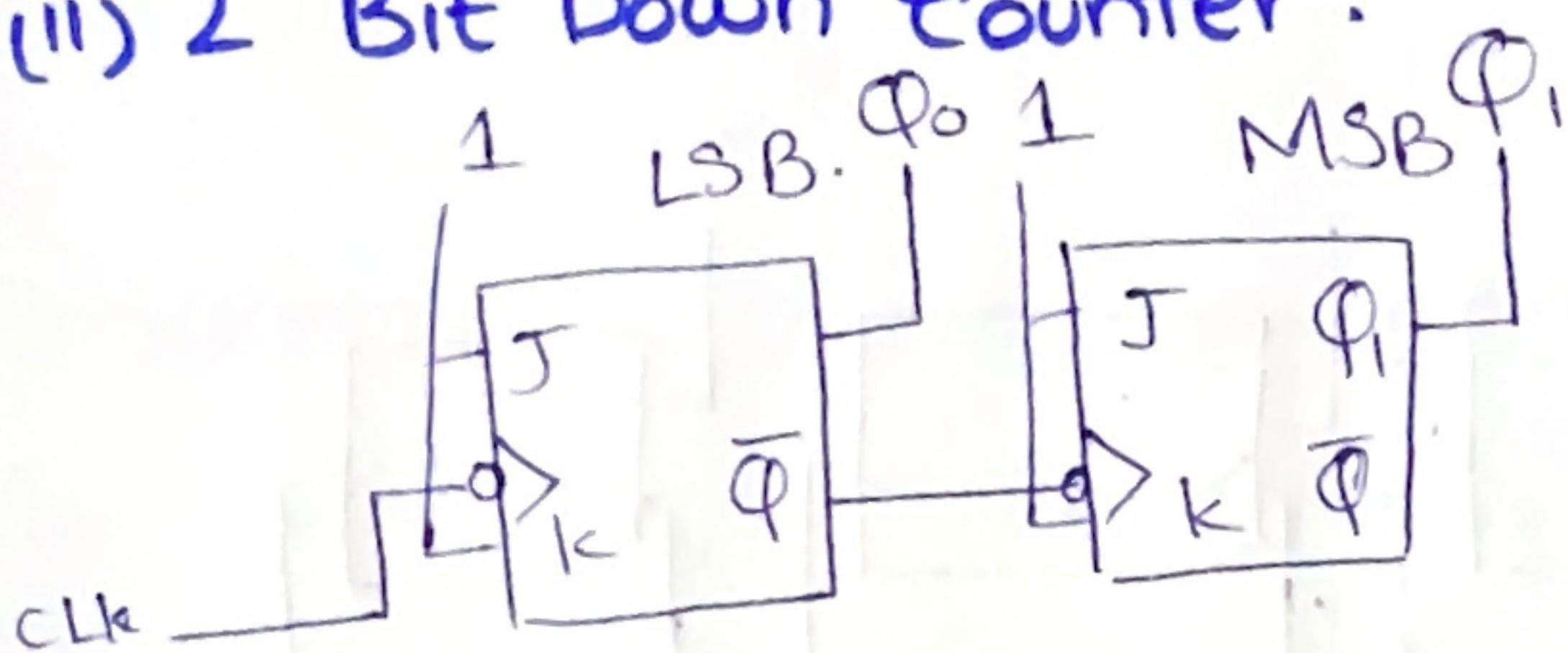
Async counters.

(i) 2 Bit Upcounter.

We should use our flipflops in toggle mode, meaning at every clock pulse the output of our flipflop should toggle; only then the next flipflop should receive the clock.



(ii) 2 Bit Down Counter.



Triggering
✓ Negative
Negative

Counter

Up

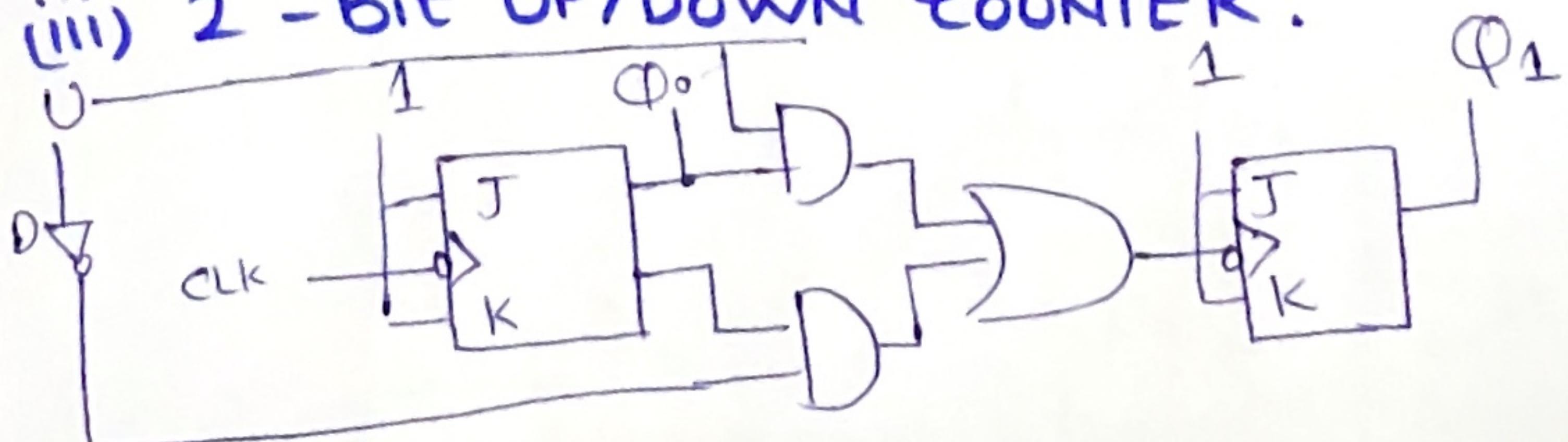
down

CLK Connection

$\frac{Q}{\bar{Q}}$

Q_1

(iii) 2 - Bit UP/DOWN COUNTER.

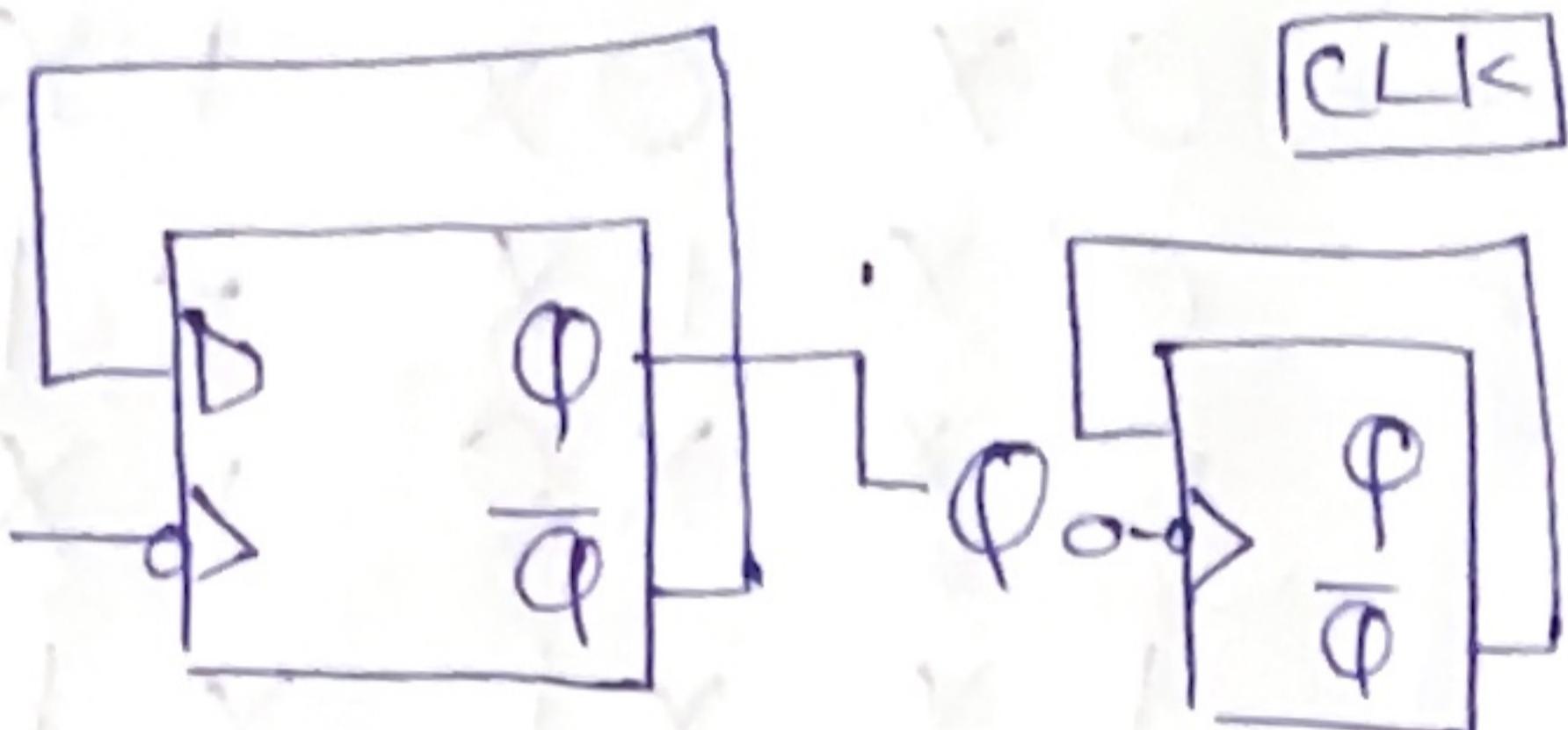


JSII
Toggle mode

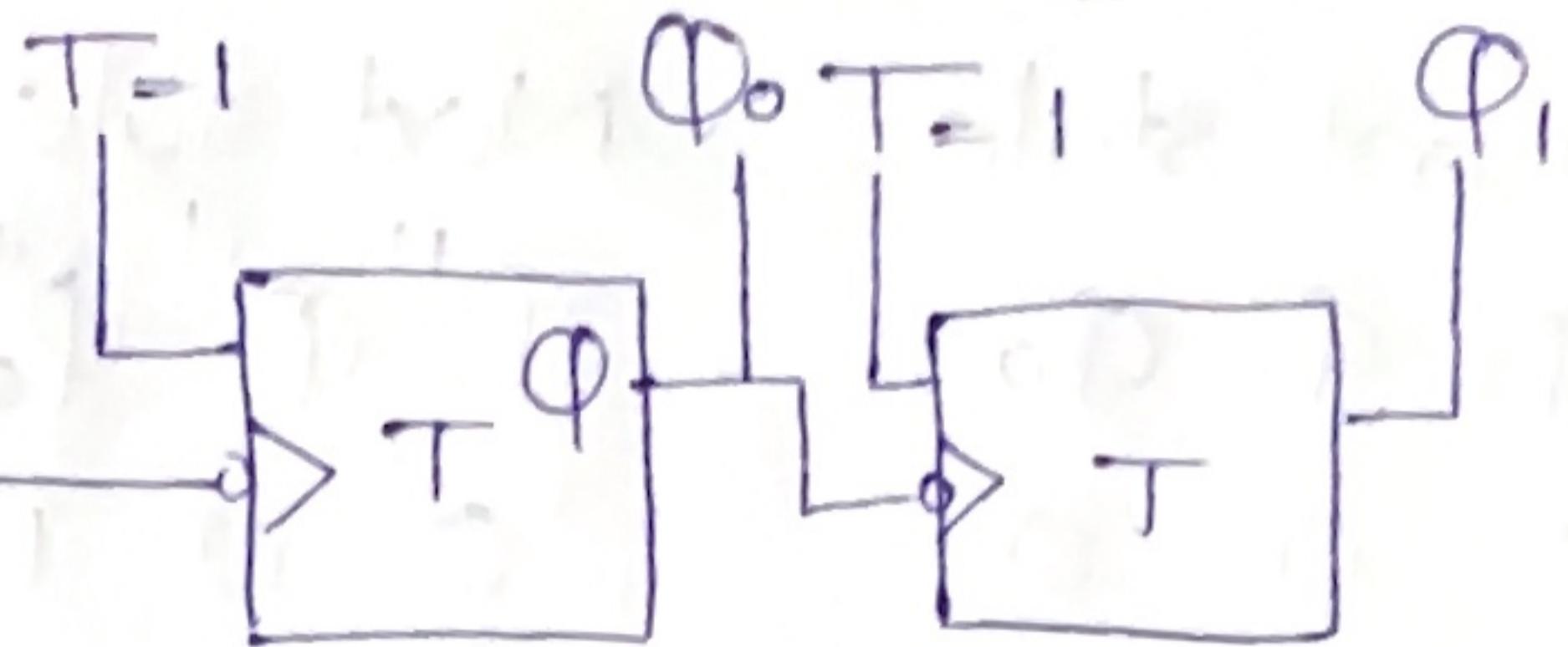
c Using D and T flipflops.

\leftarrow toggle mode wiring.

\rightarrow toggle mode $T=1$.



2 Bit Up counter.



2 Bit Up Counter.

In a sync counter the ripple effect occurs i.e. accumulation of time/propagation delay due to the attachment of CLks b/w flip flops. . sync counter.

Thus the main idea of UP/down counters

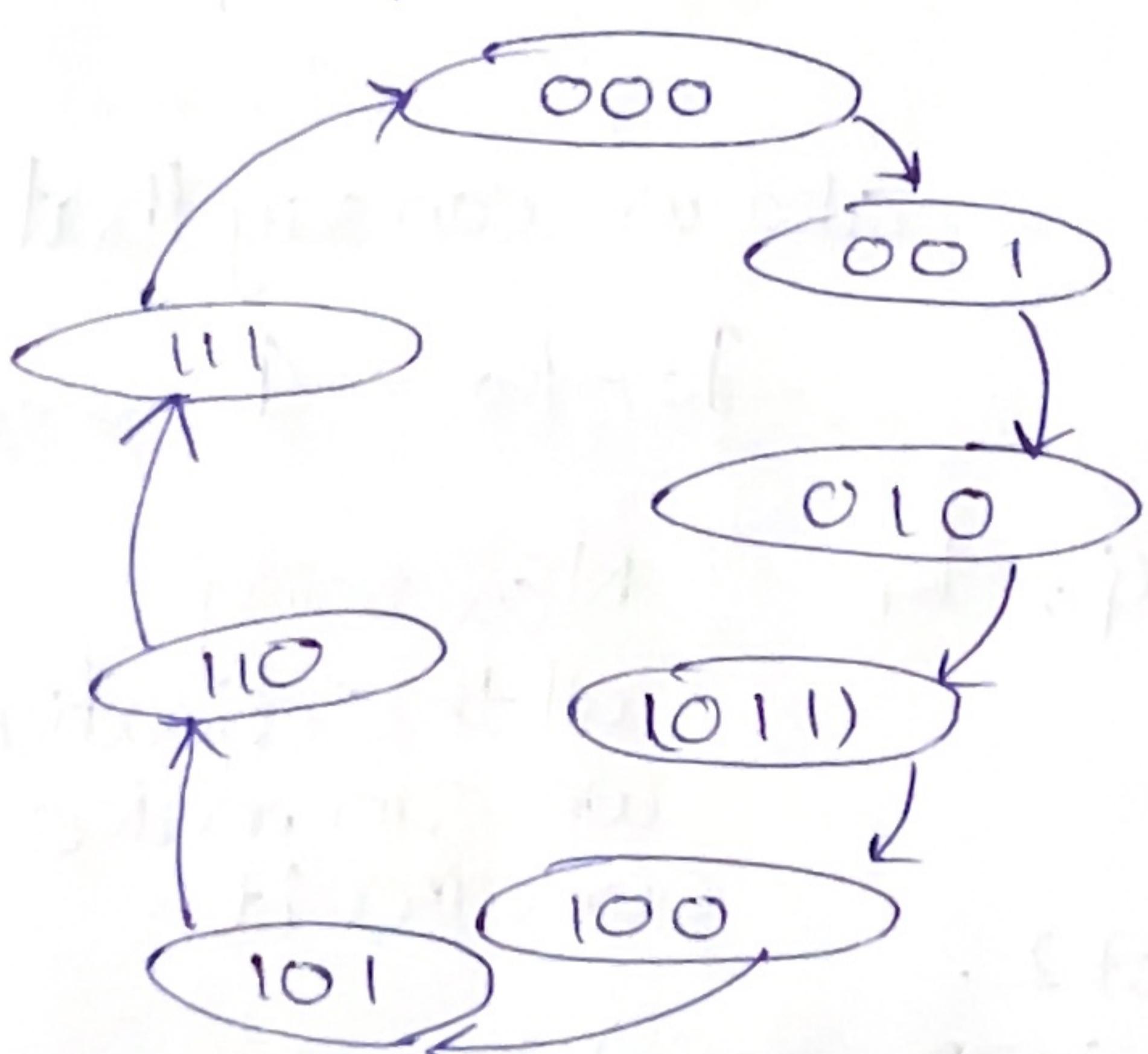
- (i) knowing of toggle mode.
- (ii) and CLK attached b/w flipflops.

Synchronous Counters

Steps to design.

(i) find required no. of flip flops.
3 bit = 3 flip flop.

(ii) Draw the state machine diagram.



3 bit Up Counter.

(iii) Select the type of the flip flop.

JK flip flop.

$Q_n \quad JK \quad Q_{n+1}$

0	0 0	0
0	0 1	0
0	1 0	1
0	1 1	1
1	0 0	1
1	0 1	0
1	1 0	1
1	1 1	0

Q_n	Q_{n+1}	J	K
0	0	X	X
1	0	X	X

(iv) Draw the present state, next state & required excitation table.

Present state	Next state	Required	Excitation
$Q_2\ Q_1\ Q_0$	$Q_2^{+1}\ Q_1^{+1}\ Q_0^{+1}$	$J_2\ K_2\ J_1\ K_1\ J_0\ K_0$	
0 0 0	0 0 1	0 X	0 X
0 0 1	0 1 0	0 X	1 X
0 1 0	0 1 1	0 X	X 1
0 1 1	1 0 0	0 X	0 1 X
1 0 0	1 0 1	X 0	0 X 1 X
1 0 1	1 1 0	X 0	1 X X 1
1 1 0	1 1 1	X 0	X 0 1 X
1 1 1	0 0 0	X 1	X 1 X 1

(v) Kmaps.

J_2	$Q_1\ Q_0$
Q_2	00 01 11 10
0	0 1 0 1
1	X X X X

$$J_2 = Q_1 Q_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$

$$J_1 = ? \quad K_1 = ?$$

Q_2	$Q_1\ Q_0$
0	0 1 X X
1	0 1 X X

K_2	$Q_1\ Q_0$
Q_2	00 01 11 10
0	X X (X) X

also we can say that

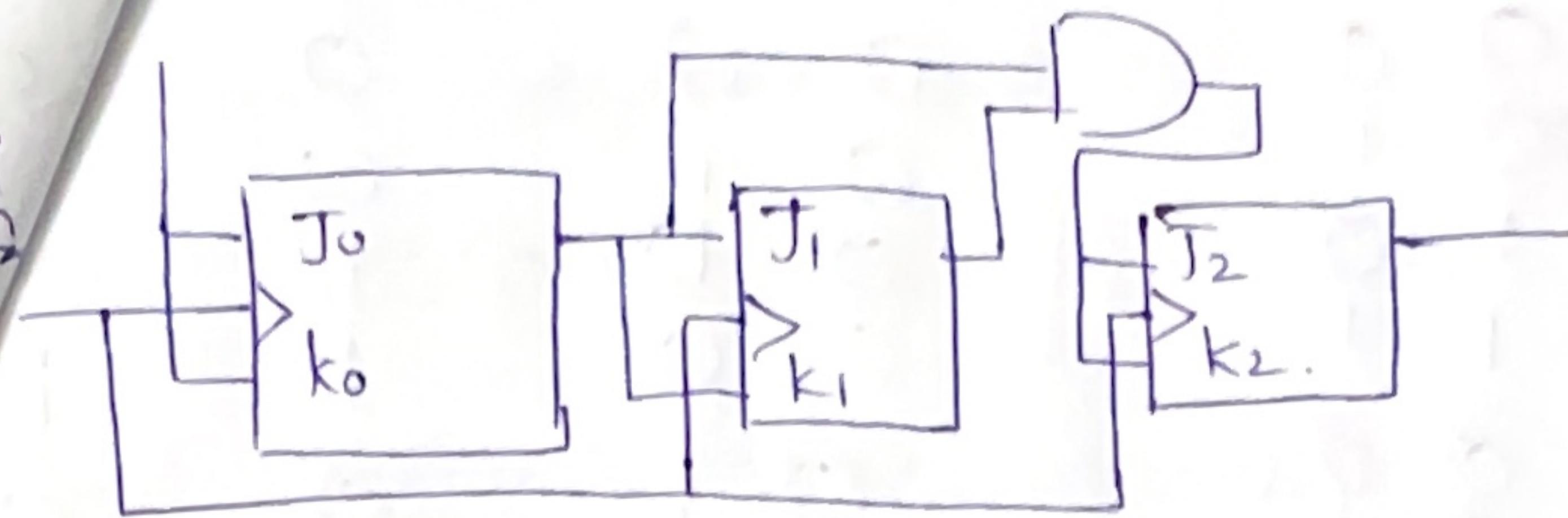
$$J_0 = K_0 = 1$$

$$J_1 = Q_0 = K_1$$

Now using all the equations we can make our circuit.

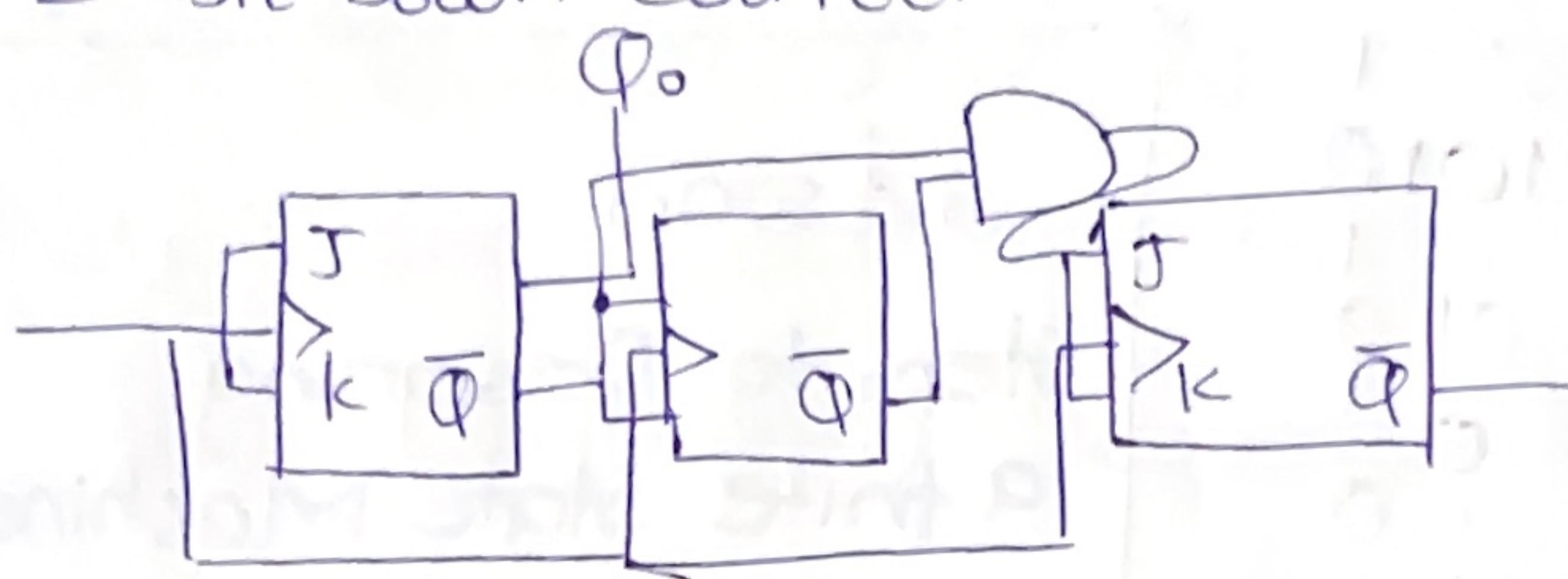
groups can be made in power of 2.

maximize size of group minimize no. of group

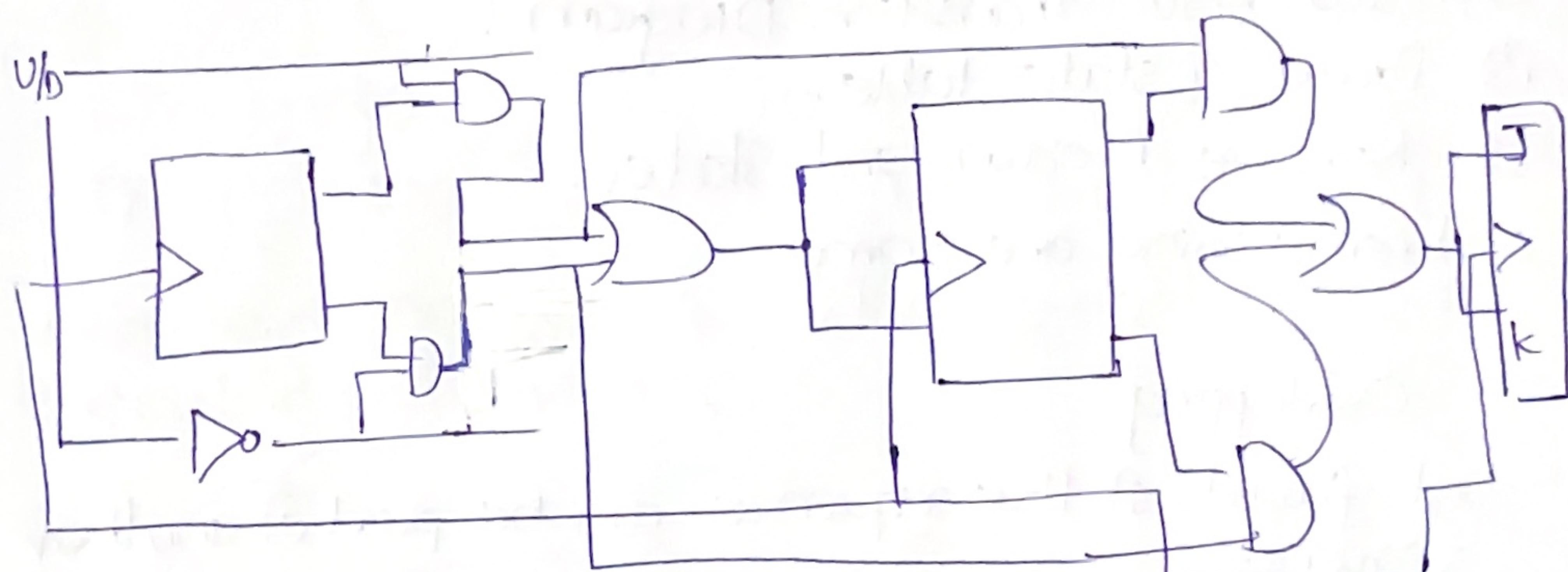


Similarly

2-Bit Down Counter.



3 Bit UP/DOWN SYNC COUNTER.



VENDING MACHINE:-

N = nickels

D = Dimes

