Async
Sync.

↔ circuits whose outputs depends upon
(i) present state/input
(ii) previous outputs.
sequential Circuits.

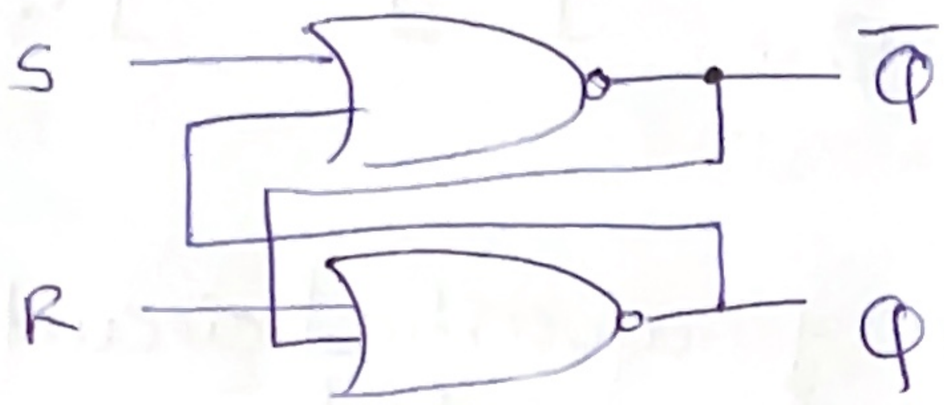
Chapter no. 7
latches.

They are level triggering memory storage devices

Flipflops are edge triggering memory storage sequential Circuits.

↗ made up of logic gates.
SR-latch: ↳ they do store info from the feedback from the outputs.

Using NOR gate.

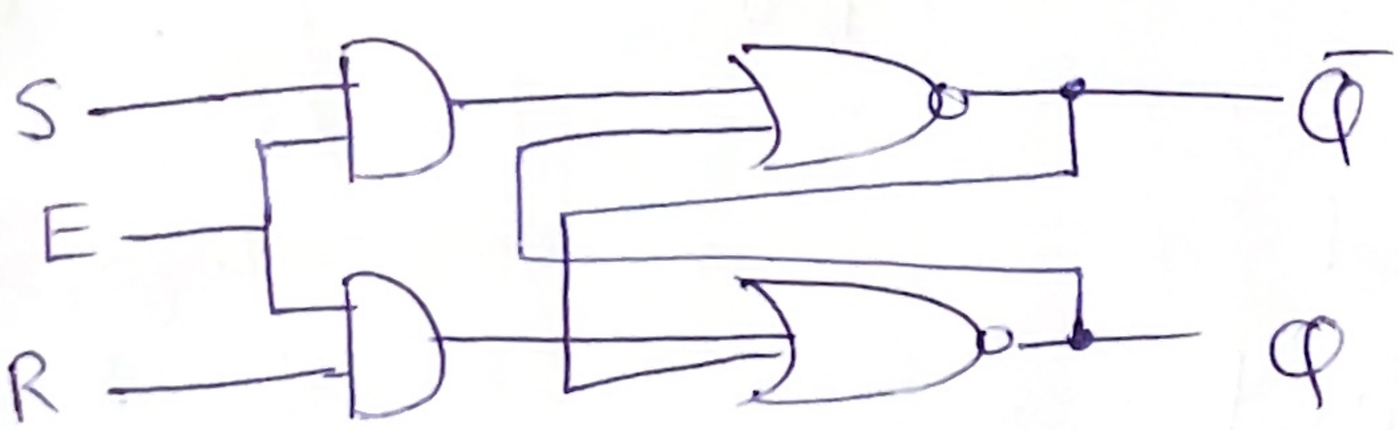


S will mirror Q.

S	R	Q	$\bar{Q}$	
0	0			hold.
0	1			Reset
1	0			set.
1	1			Invalid state.

SR-Gated Latch.

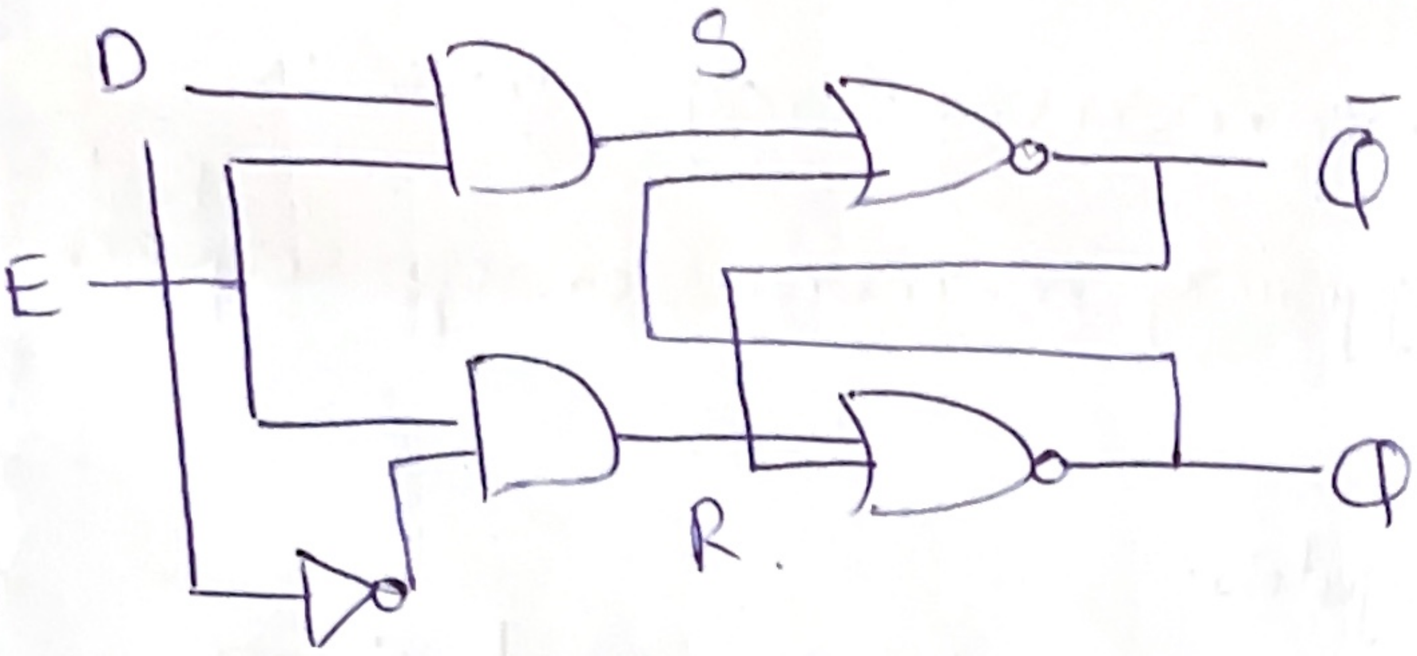
An enable bit is installed to prevent any fluctuations in the inpot of S and R.



E	S	R	Q	$\bar{Q}$	
0	0	0			latched
0	0	1			"
0	1	0			"
0	1	1			"
1	0	0			latched
1	0	1			Reset
1	1	0			set
1	1	1			Invalid state.

D-latch :-

In was made to tackle the problem of invalid state.



E	D	
0	0	latched
0	1	latched.
1	0	Reset → $\varphi=0$, $\bar{\varphi}=1$.
1	1	Set → $\varphi=1$, $\bar{\varphi}=0$.

map to SR.

non
next state table.
excitation table.

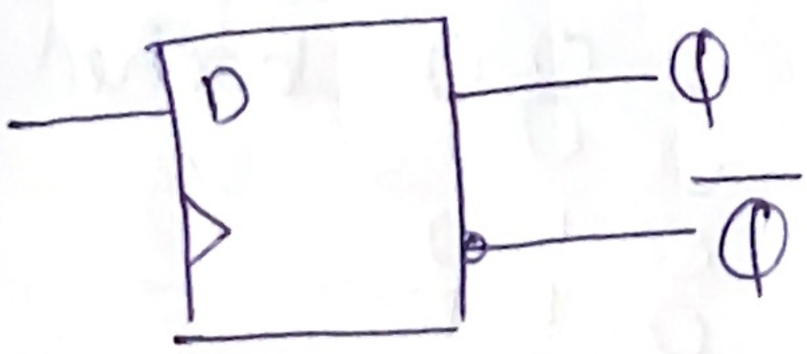
D maps the output φ.

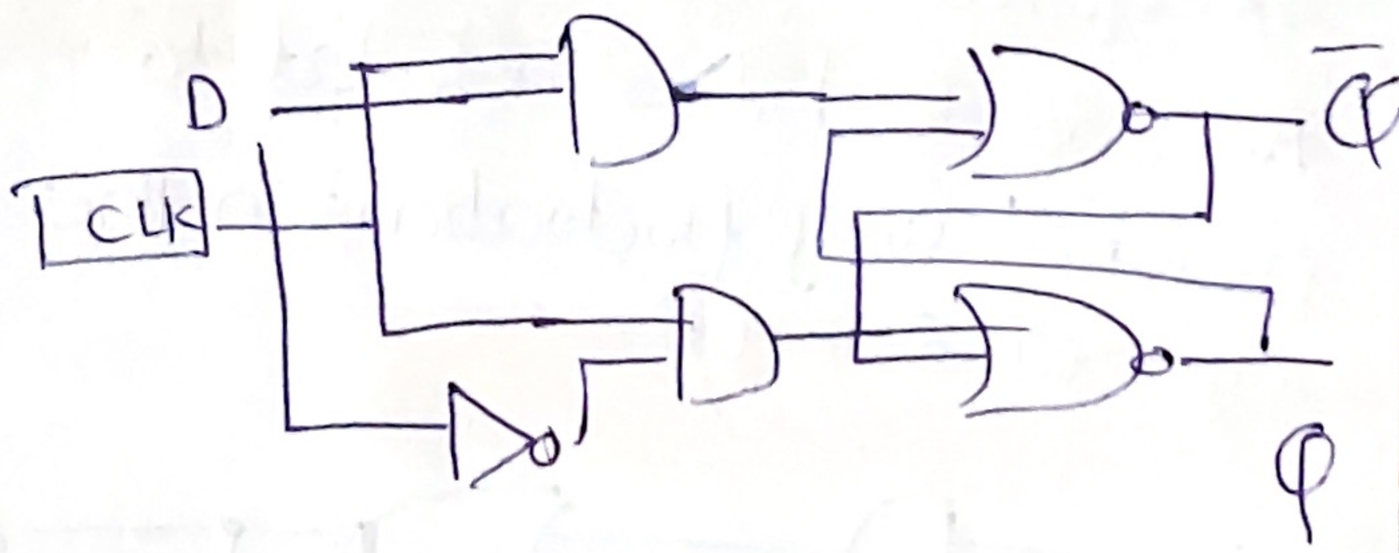
E	D	φ
0	X	memory
1	0	0
1	1	1.

Flipflop.

These are edge triggered memory sequential circuit.
They thus require a clock pulse to be operated.

D Flipflop.





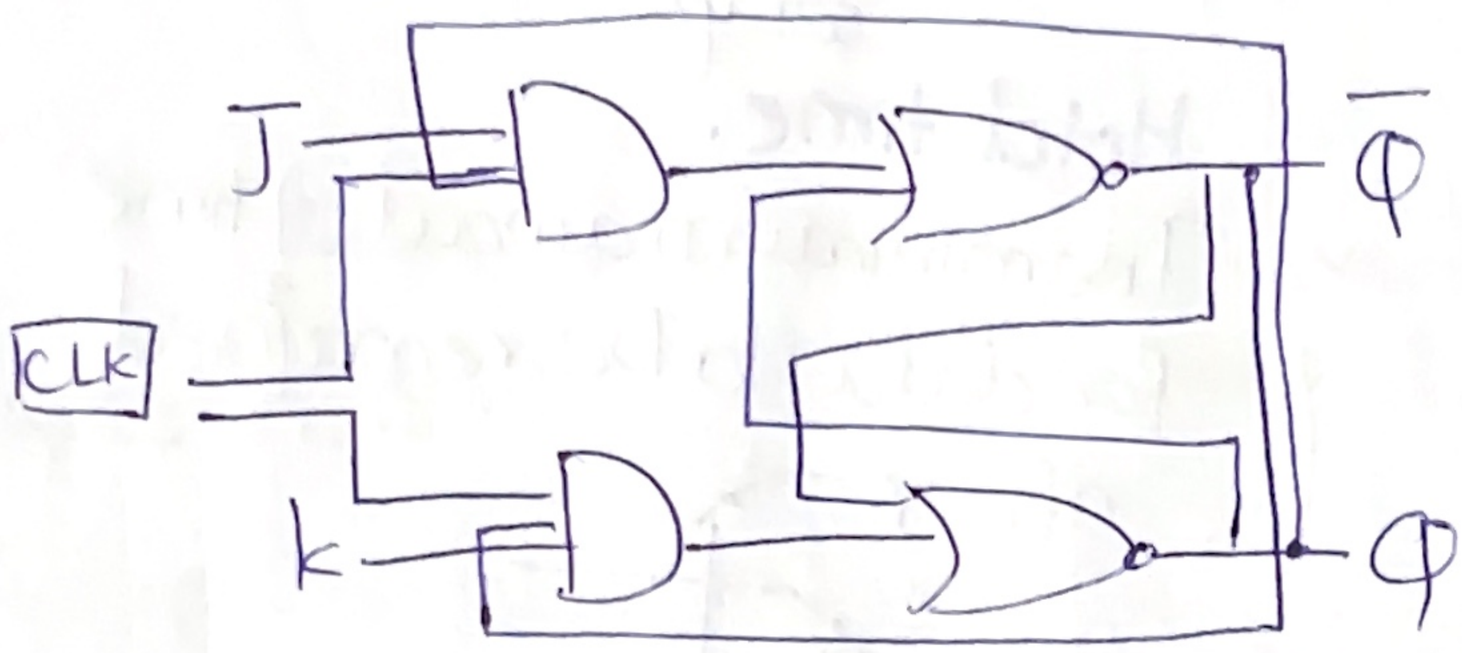
CLk.	D	φ	$\bar{\varphi}$	
↑	1	1	0	set
↑	0	0	1	Reset.

D	Q_n	Q_{n+1}
0	0	0
0	1	0.
1	0	1
1	1	1

so the next state in a D flipflop mirrors D as it is directly being transferred into the output.

...k flipflop.

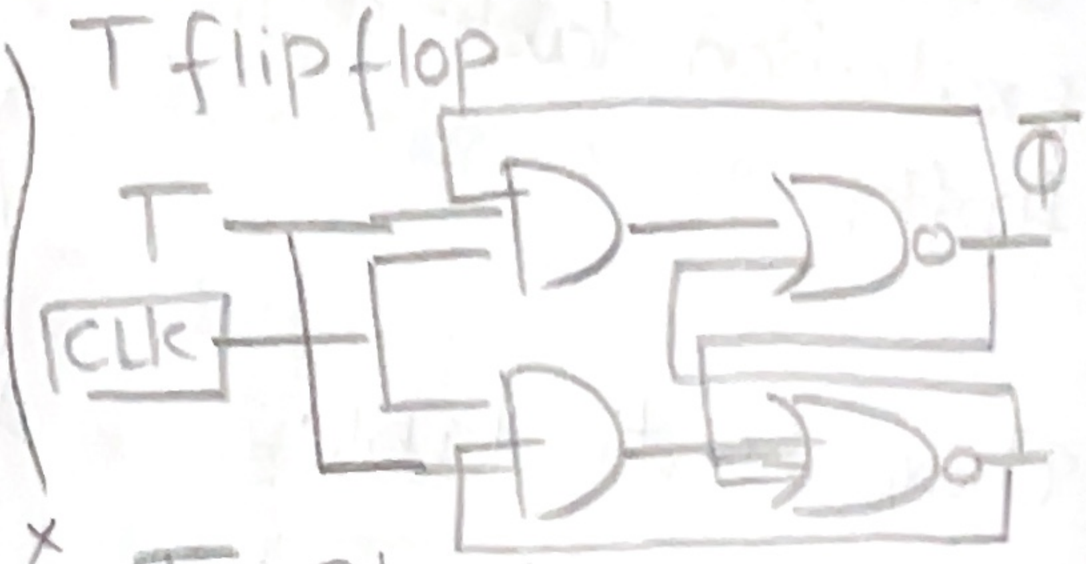
has an additional feature at the rising edge's toggle.



CLK	J	K	Q $\overline{Q}$
↑	0	0	latched
↑	0	1	Reset
↑	1	0	set.
↑	1	1	toggle.

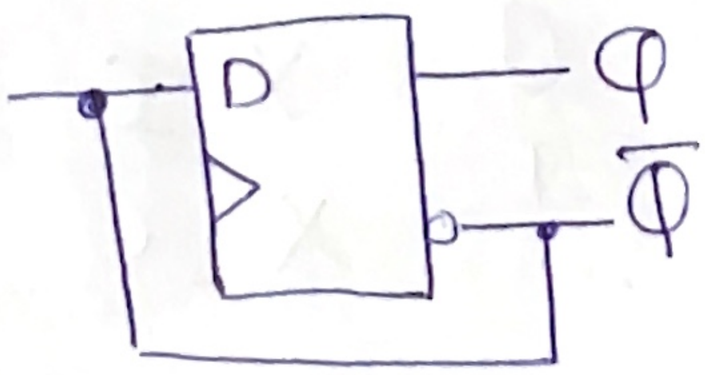
∀↓ it is latched.

T flipflop

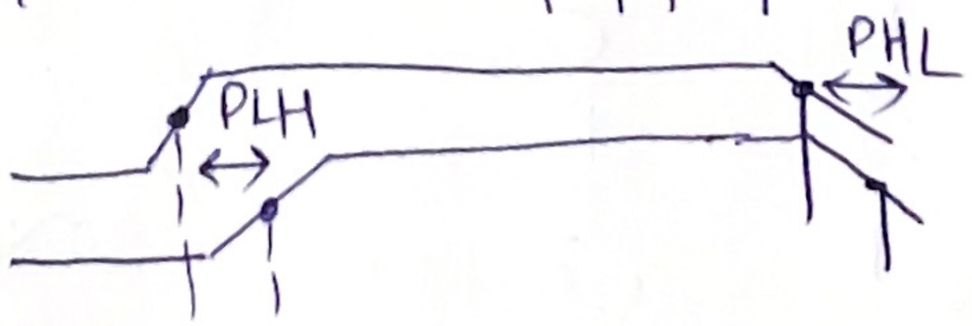


T	Qt	Q(t+1)	
0	0	0	} hold
0	1	1	
1	0	0	} toggle.
1	1	0	

How to convert a D-flipflop to toggle.



=> Now the D flipflop will toggle.



Propogation Delay:-

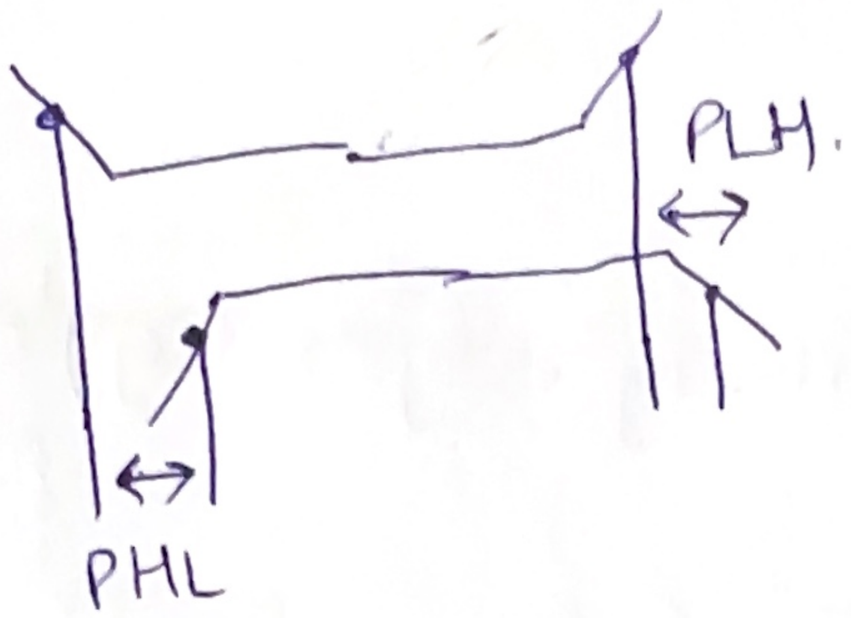
The time it takes for a signal to travel in a circuit and produce a change is called as propogation Delay.

in ~~ut~~ input after the input is applied.

It is specified for the rising and falling edge outputs.

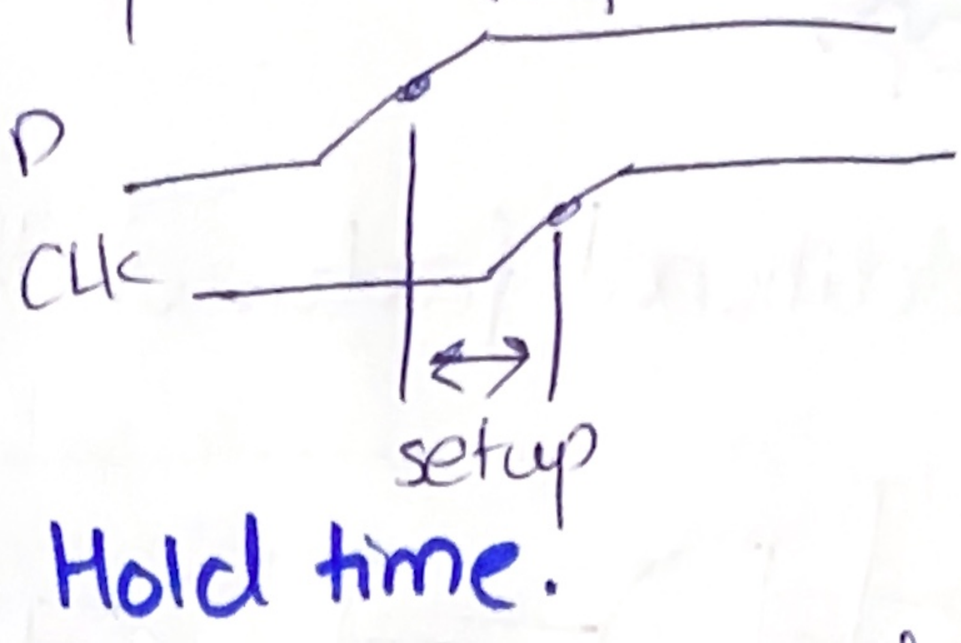
It is measured b/w 50% level of the clock and 50% level of the output transition.

also for async. inputs.



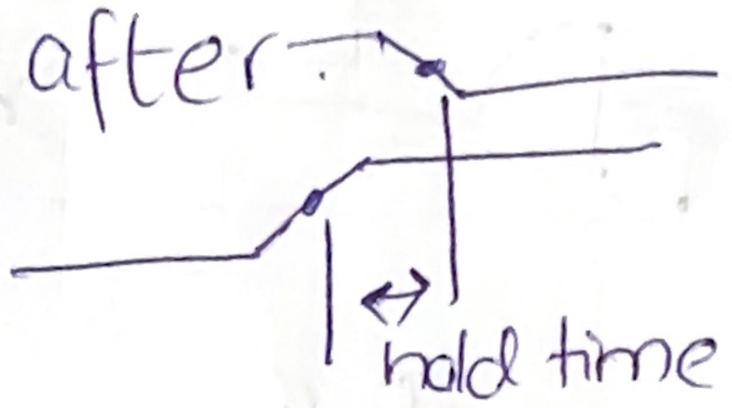
Setup time.

minimum amount of time required for a data to be present before clock.



Hold time.

The minimum amount of time for data to be remained after.



Characteristic table and equation + Excitation table of JK flipflop.

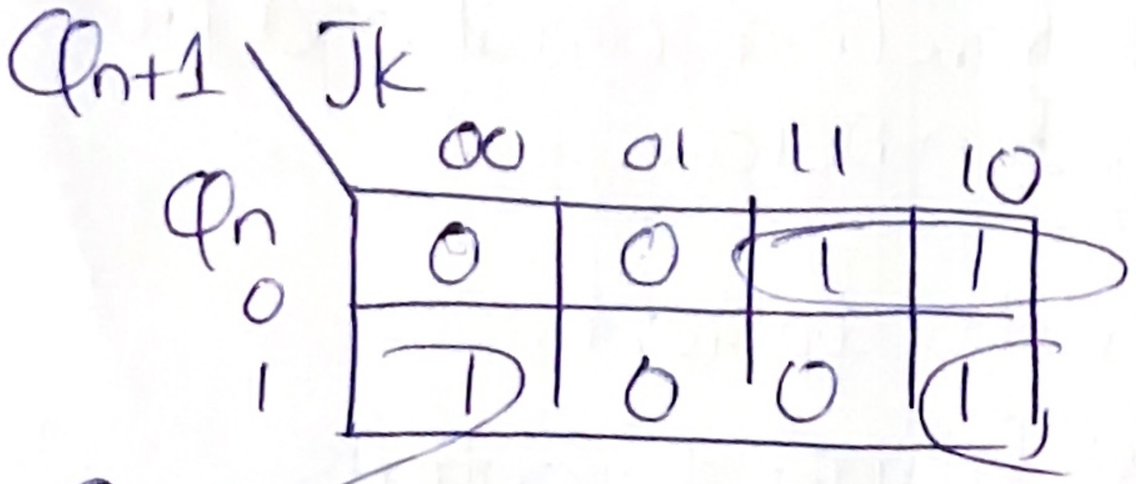
Characteristic table

Qn	(J)	k	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

excitation table alway depends upon the characteristic table.



$Q_{n+1} \Rightarrow Q_n'J + Q_n K'$

ock.

characteristic table

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

excitation table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

The next state always mirrors the d-flipflop.