



Mid-Term Exam Fall-2024

Section (A)

Course Code: CE-221L

Vetted Faculty Name:

Dr. Salman

Course Title: Digital Logic Design

Vetted Faculty Signature:

SM

Program: BS (CS Sec1)

Vetted Faculty Designation

Name of Course Instructor: Engr. Ahsan Shah

Signature of Course Instructor: Ahsan Shah

Date: 04-12-2024

Course Instructor Designation: Assistant Professor

Approved By: Dr. Salman

Lab Instructor: Jazia Sajid

Signature: Dr. Salman

Signature:

Maximum time allowed: 180 minutes.

Instructions:

- Mobile phones, any storage device, and the internet are not allowed in the exam hall.
- If caught cheating by any means, an F grade will be awarded.
- Comment your name and Registration number on top of each code.
- All the detailed calculations and rough work should be done on paper.

Question # 01	Question # 01	Question # 01	Total Marks#
10	10	10	30
Obt Marks:	Obt Marks:	Obt Marks:	Obt Marks:

Question # 01:

Scenario:

You are tasked with developing a smart classroom lighting system. The system should operate based on the following conditions:

Input Signals:

- **S (Student Sensor):** HIGH (1) when students are present in the classroom, LOW (0) when the classroom is empty.
- **P (Presentation Mode):** HIGH (1) when the presentation mode is activated, LOW (0) otherwise.

Lighting Outputs:

- **L1 (Main Lights):** The main lights should be ON when students are present ($S = 1$) and presentation mode is not activated ($P = 0$).
- **L2 (Dim Lights):** Dim lights should be ON during presentation mode, overriding the main lights ($P = 1$).
- **L3 (No Lights):** All lights should be OFF when the classroom is empty ($S = 0$).

Tasks:

1. Create a truth table for the inputs and outputs.
2. Write Boolean equations for the outputs (L1, L2, L3).
3. Draw the circuit diagram based on the equations.
4. Implement on trainer board.

Truth table:

Circuit Diagram:

Equation:

$$\frac{d\theta}{dt} = \frac{1}{2} \left(\frac{\partial \theta}{\partial t} + \frac{\partial \theta}{\partial x} u \right) - \frac{1}{2} \frac{\partial}{\partial x} \left(\frac{\partial \theta}{\partial t} + \frac{\partial \theta}{\partial x} u \right)$$
$$= \frac{1}{2} \frac{\partial \theta}{\partial t} + \frac{1}{2} \frac{\partial \theta}{\partial x} u - \frac{1}{2} \frac{\partial^2 \theta}{\partial x^2} - \frac{1}{2} u \frac{\partial^2 \theta}{\partial x^2}$$
$$= \frac{1}{2} \frac{\partial \theta}{\partial t} + \frac{1}{2} \frac{\partial \theta}{\partial x} u - \frac{1}{2} u_{xx} \theta$$
$$= \frac{1}{2} \frac{\partial \theta}{\partial t} + \frac{1}{2} u \frac{\partial \theta}{\partial x} - \frac{1}{2} u_{xx} \theta$$

(continues)

Implement it on the trainer board:

Question # 02:

You are a computer science engineer working on a data transmission system. You need to design a system that triggers a warning signal (B) when one of the following conditions happens:

1. The data checksum (signal C) fails (C is LOW).
2. The data length is too long (signal D is HIGH) and the data is encrypted (signal E is HIGH).

Design a logic circuit that generates the warning signal (B) when either of these conditions occurs. Use only NAND gates to create the circuit and explain how this setup helps in detecting problems with data transmission.

Truth table:

Equation:

Circuit Diagram:



Implement it on the trainer board:

Question # 03:

Design and implement a full subtractor circuit that handles borrowing.

1. **Create a Truth Table:** Start by making a truth table for a half subtractor, and then expand it to a full subtractor with inputs A, B, and Bin. The outputs will be the difference (D) and borrow (Bout).
2. **Write the Expression:** Simplify the Boolean expressions for the difference (D) and borrow (Bout) using Karnaugh Maps (K-Maps).
3. **Design the Circuit:** Draw the circuit diagram for the full subtractor using basic logic gates.
4. **Simulation:** Simulate the full subtractor to check if it works correctly for all possible input combinations.

Cheat sheet.
Name, Number, and Pin configuration of different ICs.

